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MEMORY: MRAM DESIGN

Cell Shape and Patterning Considerations for Magnetic Random Access Memory (MRAM) Fabrication

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INTRODUCTION

Industrial and academic development laboratories worldwide are working to perfect the circuit designs, fabrication methods and integration schemes required for successful commercial production of Magnetic Random Access Memory (MRAM) devices, a new kind of nonvolatile memory technology that some forecast to be a "universal" memory replacement for DRAM, SRAM and flash. Among the more important issues for MRAM cell design and fabrication are the basic configuration of the magnetic memory element (pseudospin-valve or magnetic tunneling junction, for example), the material set used to fabricate the magnetic memory element, the shape of the magnetic memory element and the patterning techniques used to fabricate the cell. Two important attributes of the MRAM cell may be unfamiliar to those with experience in other IC fabrication processes. These are the special considerations that must be taken when designing the physical shape of the magnetic memory storage element and the specific fabrication techniques that need to be applied to pattern the many layers of alloys (NiFe, for example) and metals (ruthenium, cobalt) found in the MRAM stack. Ion milling has been the historically-important method of record for fabricating low-density MRAM products for applications with limited production volumes. Now that large IDMs like IBM and Infineon, Motorola, Philips, STMicroelectronics and NEC are approaching MRAM processing in earnest, the perceived manufacturing limitations of ion milling have motivated development teams to consider other methods, including wet etch, plasma etch and damascene for patterning MRAM stacks. We review here the theory of MRAM operation, discuss the interaction between the physical shape of the MRAM cell and its ability to store binary information, present the various options for patterning MRAM stacks as championed by the major IDMs with public MRAM programs, and summarize some of our own work on plasma etching MRAM devices.

Each MRAM memory element is connected to a transistor that performs the function of read addressing for an array of memory elements.

MAGNETIC TUNNEL JUNCTION MRAM DESIGN AND OPERATION

The most commonly adopted MRAM design is known as the MTJ design in which a memory element is a magnetic tunnel junction (MTJ), as shown in Figure 1 [1, 2, 3, 4].

The MTJ memory element consists of two electrodes separated by a thin tunnel barrier, usually Al_2O_3. The two electrodes are ferromagnetic thin film layers with an elliptical shape. The magnetic moments of the two ferromagnetic layers are always along the long axis. When the magnetic moments of the two layers are parallel, the resistance of the tunnel junction is lower than that when they are antiparallel, corresponding to the two memory states with two distinctive resistance levels and defining the binary memory states. The resistance difference between the parallel and the antiparallel states can be as high as 40 percent of the parallel state resistance, and this ratio is often referred to as the tunneling magnetoresistance (TMR). The product of the barrier resistance and the barrier surface area, referred to as RA, is on the order of $1k\Omega \cdot micron^2$. The thicknesses of the ferromagnetic layers range from 20 Å to 50 Å. The SAF is usually a Co/Ru/Co or $Co_{90}Fe_{10}/Ru/Co_{90}Fe_{10}$ with ruthenium layer thickness around 6 Å to 8 Å.

A practical MTJ memory element is more complicated with a few more magnetic layers added, as shown in Figure 2.

The top magnetic layer whose magnetic moment can be reversed along the long axis is referred to as the storage layer.

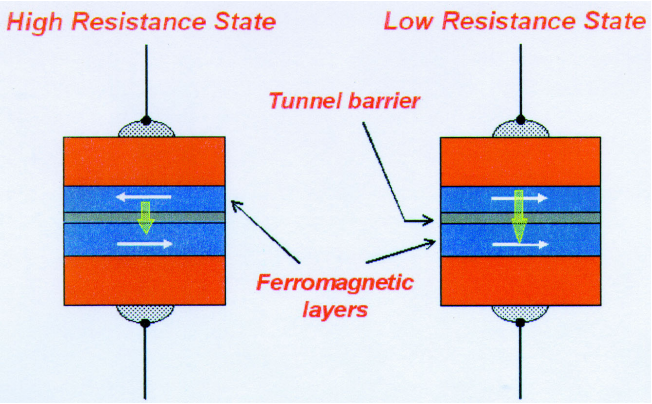
The single-layer bottom electrode in Figure 1 is replaced by a structure that consists of a pair of ferromagnetic layers sandwiching a thin metal layer, referred to as a synthetic antiferromagnet (SAF) and an antiferromagnetic (AF) layer. The two magnetic layers in the SAF are always antiparallel due to a strong antiparallel coupling between the two layers, and the magnetic moment orientation is "pinned" via the exchange field arising at the interface between the magnetic layer in the SAF and the AF layer. The SAF forms a closure of the magnetic flux within, yielding no stray field on the free layer. The magnetic moment orientation in the top layer of the SAF acts as a fixed reference to that of the storage layer.

Each MRAM memory element is connected to a transistor that performs the function of read addressing for an array of memory elements. To write a memory state, i.e. to reverse the magnetic moment direction in the storage layer, in a two dimensional array of memory elements, an x-y grid of conducting wires are laid over and under the memory elements, as shown in Figure 3. For writing a selected element, the two corresponding conducting wires are activated with current pulses, generating a magnetic field along the long-axis (x-component of the field) and a magnetic field along the short-axis (y-component) simultaneously.

If the current amplitudes are adequately chosen, the memory state of the addressed element will be changed while the states of the elements along only one of the two activated wires will not, since they experience only one of the field components. This mechanism is illustrated in Figure 4 where the reversing threshold of the storage layer magnetic moment is graphed for the two write field components.

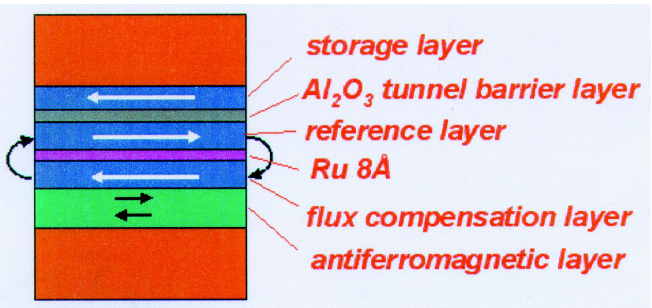
The red dot indicates an ideal operating point where the co-application of both field components yields a desired switching while either one of the field components alone is significantly below the switching threshold.

FIGURE 1



Schematic drawing of magnetic tunnel junction (MTJ) memory element and the two memory states.

FIGURE 2



A practical MRAM memory element with virtually a stray-field-free reference layer. The magnetic moments of the reference layer and the flux compensation layer are always antiparallel to each other through a strong interlayer coupling and the sandwich is know as a synthetic antiferromagnet (SAF). The bottom antiferromagnetic layer provides a pinning field to the moment orientation in the SAF.

MEMORY ELEMENT SHAPE EFFECTS

For the MRAM design described above, a memory element is always an elongated shape so that a magnetic anisotropy, referred to as shape anisotropy, is induced to keep the magnetic moment in the element always along the long axis. The linearly-oriented magnetic moment generates magnetic poles at the ends of the element. Magnetic moment switching varies significantly for elements with different end shapes. For a rectangular shape element where the ends are flat, the poles at the end surfaces can be so strong to rotate the local magnetic moment at the ends of the storage layer to orient parallel to the end edges, resulting in magnetic domains at the ends, as illustrated in Figure 5 [5, 6, 7].

The existence of the end domains causes the field threshold to vary from time to time. Tapering the ends into relatively sharp tips allows the poles to distribute along the slanted edges and eliminates any possible end domains and enforces switching repeatability. In practice, the fabricated elements usually have relatively rounded ends instead of sharp tips and become naturally elliptical shapes.

The end shape of an MRAM element strongly affects the distribution of the magnetic poles and consequently affects the switching field threshold. As the element shape varies from a rectangle with flat ends to an eye-shape with sharp curved ends, the switching field threshold varies by more than 120 percent as a computer simulation showed in Figure 6.

Variations of the shape of the MRAM element's ends resulting from fabrication inconsistencies yields a corresponding variation of the switching field thresholds of both the half-select elements and the full-select element, as illustrated in Figure 7. The dispersion of the switching field thresholds can significantly reduce the operation margin of the device. Controlling the variation of the ends over an array of memory elements presents one of the main challenges for MRAM device manufacturing. ➡

To enhance the switching field threshold difference between a full-select element and a half-select element, memory elements with alternative shapes, such as the asymmetric ellipse shown in Figure 5, have been suggested. Again, shape control precision remains as a key factor in successfully manufacturing these devices.

Since the strong sensitivity of the switching field threshold on the ends of a memory element originates from the magnetic poles at the ends, annular shaped magnetic elements, also shown in Figure 5, have also been proposed [8, 9] The magnetic flux closure configuration in an annular shape element eliminates the magnetic poles in the two memory states determined by the helicity of the flux rotation. However, since the magnetic moment is no longer linear, the write field application scheme described in the previous section cannot be used. Instead, alternate schemes for annular shaped memory element design have been invented [10, 11].

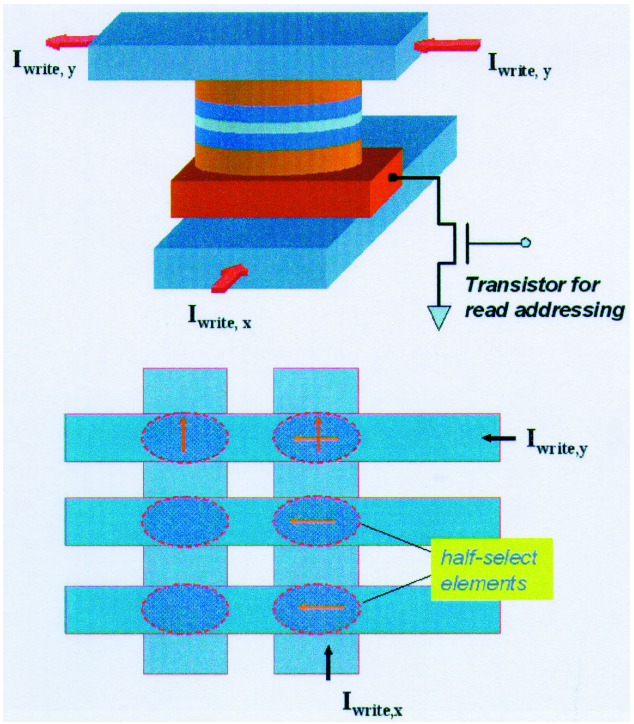
PATTERNING OPTIONS FOR MRAM STACKS

The patterning options available to MRAM device manufacturers for creating MRAM storage cells have evolved from a single basic technique, ion milling, employed during the historical phase of MRAM development, to the several significantly different methods documented today by the commercial IDMs with active MRAM development programs. In at least one case, using CMP to create MRAM cells, the patterning strategy is highly dependent on porting advances made in IC fabrication processes and processing tools for other applications, like multi-level metal interconnect formation; other MRAM patterning methods rely on tried-and-true concepts, like metal lift-off, albeit with a need for especially precise control for the thin metal layers of which the MRAM cell is composed.

Ion milling is a versatile technique that has been used in laboratory applications for patterning almost any known material. An ion beam can be made to be sufficiently energetic so as to remove thin film atoms from surfaces on which the beam impinges, under temperature and pressure conditions where the vapor pressure of the material(s) to be removed is negligibly small. Ion milling lends itself perfectly to laboratory demonstrations of MRAM cell formation, where the problems of patterning the magnetic, metallic and insulating films in the MRAM stack don't warrant extensive exploration of other patterning techniques when the work is being performed at the feasibility stage of device fabrication (corresponding to the historical phase of MRAM development).

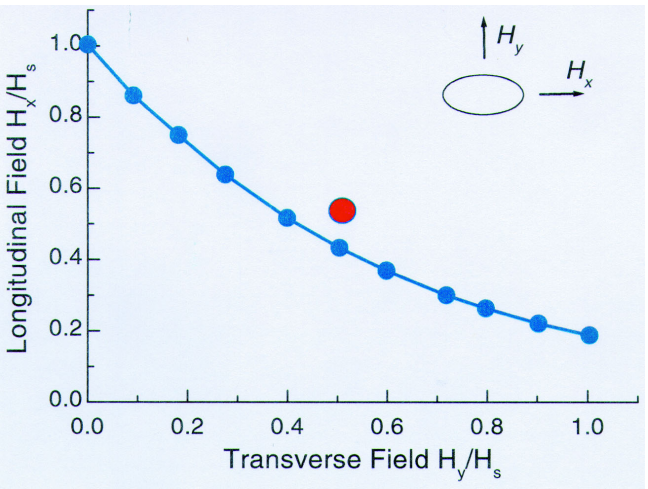
Researchers have noted several drawbacks to ion milling MRAM devices, the most troubling of which is the tendency of the milled material to redeposit on the side of the patterned feature (or on the patterning mask), causing yield-limiting electrical defects in finished devices. There are methods (overmilling, for example) that allow for removal of deposited sidewalls on widely-spaced features, but for the small, dense geometries characteristic of first-wave commercial MRAM devices, both Motorola and NEC are on record stating that the serious drawbacks to patterning MRAM stacks with ion milling preclude

FIGURE 3



Schematic view of MTJ memory architecture. A x-y grid of the write lines perform the write of a selected element. The read addressing is performed with an addressing transistor, one per memory element. The elements on either one of the two activated lines during a write operation are referred to as half-select elements.

FIGURE 4



Switching field threshold as a function of the two field components and the operating point.

milling from being considered a manufacturable process compatible with high-volume and low-maintenance semiconductor production practices [12, 13].

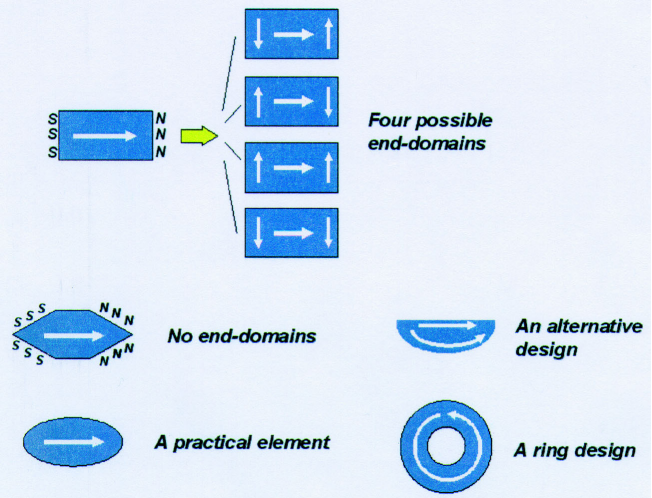
Damascene formation of metal structures has been universally adopted for copper-based multi-level electrical interconnects in advanced IC fabrication, owing primarily to the difficulty of reliably patterning relatively thick (hundreds of nanometers) copper using traditional wet or dry processing. Motorola has documented a method for fabricating MRAM elements whereby a blanket deposition of the multiple films forming the magnetic memory layer is performed over trenches previously cut into a dielectric isolation structure [14]. The magnetic and electrically conductive films are then removed via chemical mechanical polishing, producing discrete MRAM memory elements in the dielectric trench (Figure 8).

Motorola has also developed a method for MRAM cell formation that looks something like the metal lift-off processes that have been successfully used over the years to pattern fine metal structures [15]. Here, poor step coverage is deliberately induced in deposited magnetic and metallic films to create complete discontinuities in the films as the deposited metals ride up and over topographic features. An advantage touted by Motorola is that this undercut gap tapered-deposition process produces an MRAM memory element with a taper, which decreases the chances of inadvertently creating electrical shorts across the MRAM device and thereby increases potential device yield. Motorola also says that, by eliminating reactive etching steps utilizing corrosive components like chlorine, this method avoids corrosion-related degradation of the thin magnetic layers used in the MRAM device.

The MRAM patterning techniques described above, along with other techniques, including wet etch, must all satisfy the multiple competing demands incumbent upon commercial microelectronic fabrication. The patterning technique chosen for commercial fabrication of MRAM devices must not have deleterious effects on the electrical properties of the MRAM memory element; for example, the MRAM cell must be patterned without creating electrical shorts across the sides of the MRAM stack. The magnetic properties of the MRAM memory element must remain unaffected regardless of how the memory element is patterned. Excessive heat applied during the patterning process (as little as 200°C) can adversely affect the magnetoresistive ratio, hence the performance, of the MRAM cell. The patterning technique shall introduce no uncertainties into device reliability. Incipient or latent corrosion of the metal films in the MRAM stack may be revealed by excessive device failures in the field, with reputation-robbing consequences for the commercial MRAM maker. And the overall manufacturability of the patterning module must be rigorously considered, as overly complex methods with an inherently high cost of ownership will create economic barriers to widespread adoption of MRAM devices.

Finally, the future extendibility of the MRAM cell patterning technique must be taken into consideration. The optimal patterning method should flexibly accommodate the adoption

FIGURE 5



Magnetic poles at the ends of a rectangular element will yield the formation of transverse domains at both ends, causing non-repeatable magnetic switching. Tapering the ends into sharp tips eliminates the end domains. A practical element is typically elliptical shape. An asymmetrical ellipse yields a better control of the ends domains in an ellipse. A ring shape element enables a magnetic flux closure, eliminates the magnetic poles, but the write lines need to be re-designed since the magnetic moment is no longer linear.

of new or alternative materials into the MRAM stack. The optimal patterning technique should ideally be able to continue to perform effectively as device geometries shrink, as they surely will under the dual pressures of expectations for continually decreasing chip costs and expectations for continually increasing device performance exerted by the commercial market. And, due to the unique interactions between the performance of MRAM memory elements and their shapes (the effects of shape anisotropy), the optimal MRAM patterning technique must be able to work for any of the various MRAM cell shapes being produced now or being considered for future generations of MRAM devices.

PLASMA ETCH FOR MRAM STACKS

Reactive ion etching has been used extensively for microelectronic device fabrication over the past 30 years and dry etch reactor technology has continued to develop to keep up with the stringent requirements for the fabrication of advanced integrated circuits. With the recent advances in IC design have come an unprecedented increase in the rate of introduction and use of new materials in IC fabrication. Many of these new materials have halogen-based etch products which are significantly less volatile than the etch products of conventional materials such as aluminum and silicon, which have long enjoyed the many benefits inherent in plasma etch patterning. In typical MRAM cells under investigation today, alloys containing iron, cobalt, nickel, platinum, iridium and manganese, among others, have been described in the literature [16]. In the plasma etch-based patterning of magnetic stacks containing these

metallic elements, consideration must be given to a combination of issues that present an as-yet unseen engineering challenge to the etch process engineer. This combination of issues includes the following:

- The etch products are considerably less volatile (have a lower vapor pressure) than the etch products of conventional materials used in IC fabrication.
- Individual metallic layers can be quite thin, on the order of 10Å.
- Many of the metals in the stack are prone to corrosion after exposure to halogen chemistries.
- The top and bottom magnet layers (free and pinned layers) in the device must remain electrically isolated (no shorting across the dielectric tunneling layer).
- Process temperatures must not exceed the temperatures at which degradation to the magnetic properties of the layers is observed (<200°C typical).

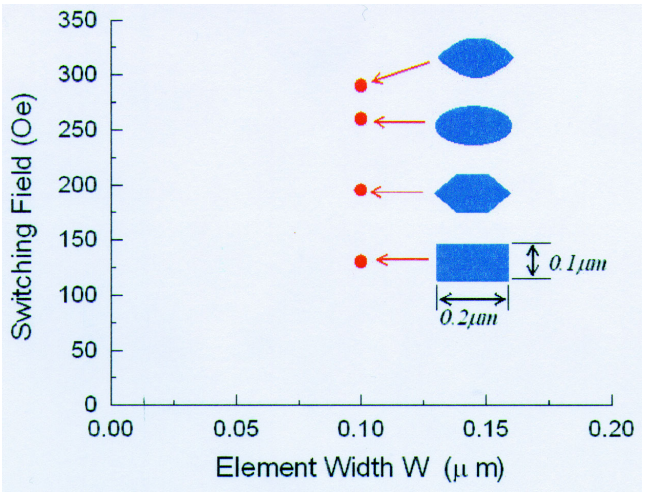
Although some of these obstacles have been encountered and effectively overcome in other applications, this specific combination of requirements is unique to MRAM.

The introduction of metals with low-volatility etch products is not unique to MRAM fabrication. In FeRAM (ferroelectric random access memory) structures, for example, patterning the platinum and iridium contact layers and PZT, BST, SBT ferroelectric layers posed a formidable challenge to the industry in the early 1990s. The introduction of these metallic and ferroelectric materials initiated a significant effort to improve the general understanding of the etching of materials with low volatility etch products. For the FeRAM applications, solutions were found at higher temperature process regimes than those that had been used for conventional materials with high volatility etch products. Currently, FeRAM materials are etched at temperatures as high as 500°C [17]. In MRAM structures, the overall volume of material requiring removal for a given stack can be considerably less than in FeRAM, but an alternative method to higher temperature is required to overcome the constraint in temperature to maintain the magnetic properties of the materials in the MRAM stack.

Gas chemistry selection plays an important role in reactive plasma etching particularly in cases such as TMR stacks where film structures containing 5 to 10 individual layers are commonly used. The volatility of etch products can vary significantly from layer to layer depending on the elemental constituents of the films and the reactive gases that are used. Halogen-based etch chemistries containing chlorine, bromine and fluorine are most common and can be used to effectively pattern MRAM stacks, although the implications of the selection on post etch corrosion treatments must be taken into consideration. Mixtures of carbon monoxide and ammonia have been investigated as alternatives to the halogen-based etch chemistries which ease the requirement for a post-etch corrosion treatment. These mixtures, however, tend to be less reactive than halogens and their use in patterning MRAM stacks can result in thick veil formation [18].

From the design side, it is important for the MRAM storage element designer to correctly specify the materials used in the complex stack that composes the MRAM cell.

FIGURE 6



Calculated switching field threshold for various element shapes.

In manufacturing methods for both GMR and TMR structures in which ion milling is used with noble gases, veils and residues can form on the sidewalls of patterned features that can interfere with subsequent steps in the fabrication sequence. Incomplete removal of these sidewall layers after milling can adversely affect device performance if the residue layer results in an electrical short across the TMR junction or if the residue interferes with subsequent deposition and repatterning steps. In contrast to non-reactive ion milling techniques, the use of reactive chemistries in the case of plasma etching helps to eliminate sidewall residue formation through the creation of etch products that can be removed more readily from the wafer surface.

One of the tradeoffs with plasma etching that is particularly relevant when chlorine and bromine chemistries are used is the requirement for a post-etch treatment to eliminate the potential for the materials in the MRAM stack to corrode upon re-exposure of the etched wafers to ambient conditions. An integrated post-etch rinse treatment is one method that has been used at Tegal for addressing this issue, as shown in Figure 9.

Immediately after etching, wafers are exposed to a post-etch rinse to remove residual halogens from the wafer surface. This post-etch rinse treatment, either alone or in combination

with other integrated plasma processing techniques, has been used for effectively eliminating the potential for corrosion in halogen-exposed magnetic films. Special consideration must be given to the materials in the stack and the selection of etch chemistry in determining the proper combination of process steps for ensuring that the potential for corrosion is eliminated.

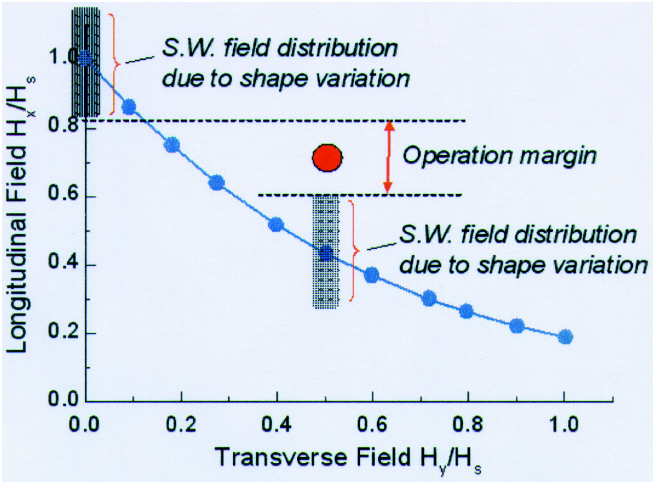
In patterning MRAM structures, the multilayer stack has in some cases been treated as a single layer. In this situation, a highly reactive process gas such as chlorine is used to indiscriminately etch through the entire structure. The advantage of this approach is its simplicity in that the full stack is etched in a single pass without the need to repattern. However, the main disadvantage of this approach is that microscopic residue can remain on the sidewall that can lead to shorting of the thin dielectric tunneling junction. This junction is typically on the order of a few atomic layers and is difficult to remove reliably with post-etch treatments.

The alternative to a single indiscriminate multilayer etch process is a process in which individual process steps are introduced for each layer in the stack or for specific groupings of layers. NiFe and CoFe, for example, tend to behave similarly from a plasma etch perspective and can often be etched with the same process conditions. The etch characteristics for tantalum, however, which is often used for top and bottom contact layers, tend to differ significantly from the magnetic layers in the stack and the introduction of a more appropriate etch process that is specifically tailored to tantalum can yield a more favorable etch profile in these contact layers.

A notable advantage of reactive plasma etching over ion milling is the ability to obtain appreciable selectivity between individual layers films in the MRAM stack structure. The ability to tailor the etch chemistry for each layer in the TMR structure provides a means for introducing an optimized process step for each layer. Coupled with advanced optical endpointing capabilities, selective processes help to ensure that the etch can be stopped at intermediate layers in the film stack. The ability to stop the etch process at specific interfaces within the structure provides a means for compensating for any non-uniformity that might inherently exist in either the reactor or the process. High selectivity processes, coupled with the ability to control ion energies to very low levels, prevent the premature removal of materials below the targeted layer for a specific step in the process with a non-optimal chemistry.

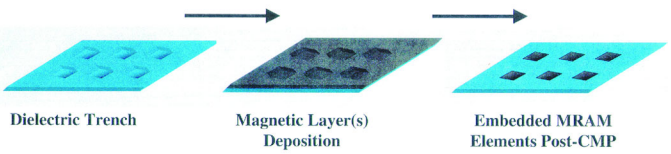
Regardless of the dry etch sequence that is used for the patterning of the TMR structures, and whether the stack is etched in its entirety in a single process or in multiple steps, measures must be taken to ensure that the integrity of the tunneling junction is not compromised at the completion of the patterning sequence. Adverse effects from etching residue or from other unintended modifications to the sidewall surface can lead to electrical shorting across the tunneling junction, for example, that can sacrifice device performance and device yield. An integrated approach that incorporates a patterning sequence which minimizes the potential for the formation of electrical shorts, coupled with a compatible post etch treatment strategy that eliminates residual byproducts from the etch process, will help to ensure peak device performance.

FIGURE 7



Effect of switching field distribution due to fabrication variations from element to element.

FIGURE 8



MRAM memory elements created by damascene processing.

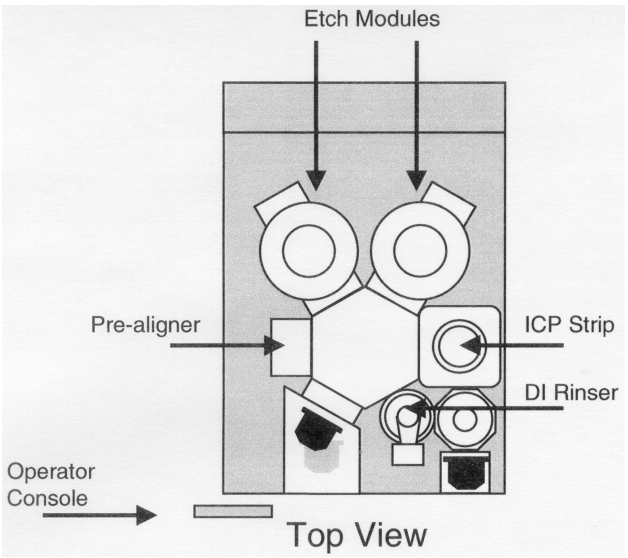
We have been working on effective MRAM patterning sequences that incorporate dry etching because we are convinced of the suitability and merits of plasma processing for these applications. One of the approaches we have taken at Tegal incorporates an etch-stop on the thin alumina junction layer to provide the necessary isolation between the top and bottom magnet layers. In this approach, individually optimized etch steps are combined to pattern each layer in the MRAM structure above the alumina junction without etching the alumina layer. This unique dry etch technique ensures that the junction integrity remains intact and that the potential for residual sidewall deposits to short the top and bottom magnet layers is eliminated. This approach is shown schematically in Figure 10. It has been proven effective in laboratory demonstrations and in etch systems installed in MRAM development lines at customer sites.

CONCLUSION

Designing and patterning of MRAM stack structures presents a unique set of challenges whose solutions are bounded by several important constraints. From the design side, it is important for the MRAM storage element designer to correctly specify the materials used in the complex stack that composes the MRAM

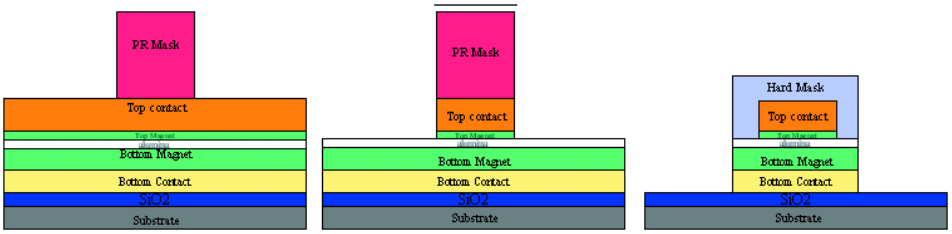
cell. It is equally important for the design engineer to specify the shape of the MRAM element, understanding that the storage properties of the MRAM cell are a strong function of the interaction between the physical shape of the cell and the magnetic moments it generates. Next, the fabrication engineer must choose between the several possible methods available for patterning MRAM stacks. Now that commercial efforts to introduce large-scale MRAM fabrication programs are passing from the development phase to pilot production, the relative merits of the various patterning schemes are being even more closely examined. The plasma etch engineer choosing to develop effective plasma etch processes for MRAM fabrication must understand that the MRAM cell is a multi-layer stack with very thin layers of materials that, in general, possess low volatility etch products and have a tendency to corrode upon exposure to atmosphere after etching. Added to these characteristics are the requirements that the dielectric tunneling layer that is part of the MRAM stack, and that is only 3-5 atomic layers in thickness, must not be compromised by the etch, and that process temperatures must be limited to below 200°C. Recent announcements by NEC, IBM and Motorola, however, suggest that significant progress has been made to fabricate MRAM devices using dry-etch techniques. We think the long history of successfully employing dry etching in IC fabrication, along with the relatively low cost of ownership and ease of use of plasma etch, make it the preferred choice over techniques like ion milling, damascene or others for commercial MRAM device fabrication.

FIGURE 9



MRAM etch tool platform with integrated post-etch rinse.

FIGURE 10



MRAM etch sequence incorporating stop on alumina.

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