

Digital Logic Using Molecular Electronics

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In this paper we introduce a reconfigurable architecture based on chemically assembled electronic nanotechnology (CAEN). CAEN is a promising alternative to CMOS that takes advantage of chemical synthesis techniques to combine molecular-scale circuit elements (such as resistors, diodes, and reconfigurable switches) using directed self-assembly. A serious drawback to CAEN is the inability (in the near-term) to include three-terminal devices (e.g., transistors) in circuits. Here, we present a molecular latch, based on molecular resonant tunneling diodes (RTDs) [6], which provides the most important benefits of the lithographically fabricated transistor: voltage restoration, fan-out, tolerance to manufacturing variability, and I/O isolation.

To make CAEN circuits economically viable they must be manufactured through thermodynamic self-assembly and self-alignment. For example, devices will be incorporated into the circuit out of topological necessity, i.e., devices are included only at the intersection of two wires coated with the appropriate molecular device. Because self-assembly will be an imprecise, thermodynamically controlled process, we can no longer expect to produce working devices in specified locations with high reliability. This implies that the devices must be testable and that defects must be tolerated. Moreover, self-assembly can produce only a limited range of circuit complexity while remaining manageable. Thus the manufacturing process must be decoupled from the production of the final circuit. Any deterministic aperiodic circuit will have to be created through configuration after the device is fabricated.

A plausible hybrid architecture combines molecular self-assembly and lithographically produced aperiodic structure. At the nanoscale, all subprocesses are self-directed; only at the micron scale do we allow deterministic operations. Functionalized wires are aligned into parallel rafts using flow techniques. These rafts are then combined into 2-D grids. Active devices are created, without the requirement of precise alignment, wherever two appropriately functionalized wires intersect. The rafts are then aligned with a lithographically produced CMOS die which provides support circuitry. Note that this manufacturing technique rules out 3-terminal devices.

Figure 1 shows a schematic for a proposed nanoBlock that can be constructed using the above techniques. The MLA is a 2-D grid of reconfigurable diodes [2] that can be configured into circuits based on diode/resistor threshold logic. Figure 2 shows how a nanoBlock can be configured

into an AND gate. The reconfigurable nature of the circuit also allows defects to be tolerated [3].

The architecture described above satisfies the key constraints of nanoscale technology: it requires no deterministic manufacturing steps at the nanoscale, it uses only two-terminal nanoscale devices, and it is reconfigurable. To build an operational circuit, however, requires signal restoration between nanoscale wire grids. Figure 3 shows a molecular scale latch that provides signal restoration through the interaction of a pair of molecular RTDs. This latch is constructed using a nanowire that includes the RTD molecules within the wire. Such inline wires have been constructed and characterized [5]. Our simulations

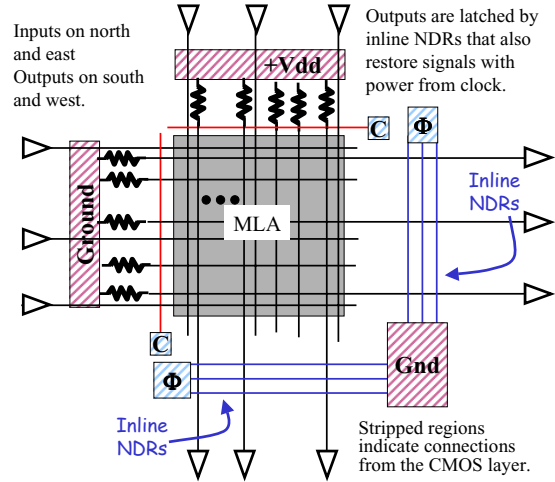


Figure 1: A schematic of a nanoBlock.

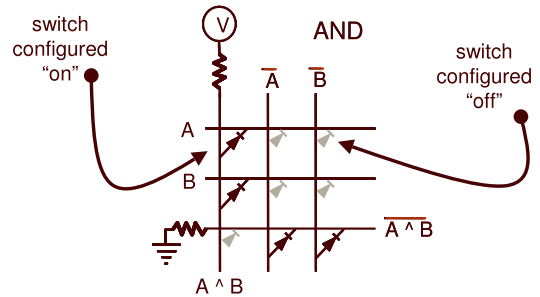


Figure 2: A two-input AND gate implemented in a reconfigurable CAEN grid.

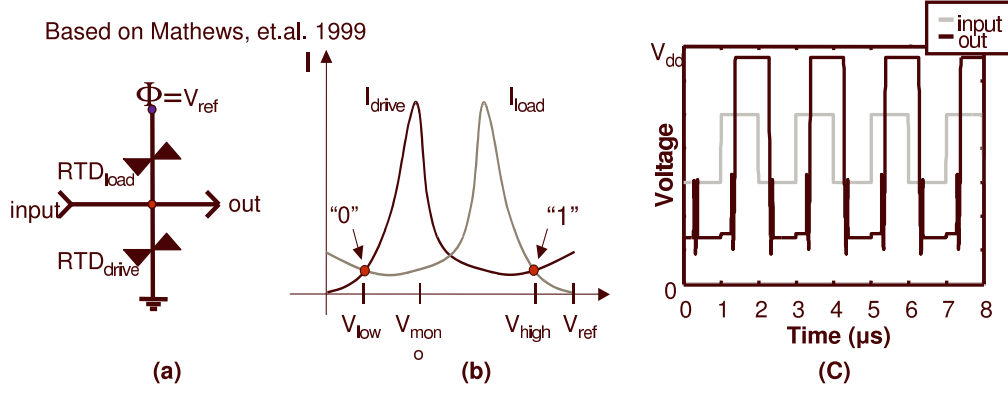


Figure 3: (a) Simple molecular latch circuit. (b) Load-line diagram (c) Simulation results showing latching and voltage restoration.

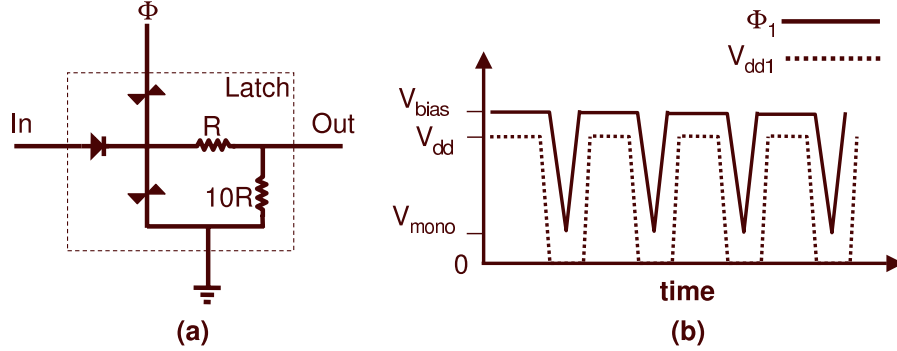


Figure 4: (a) The complete molecular latch and (b) the clocking methodology

are based on RTD molecules characterized by Chen and Reed [1].

While RTD latch technology has been exploited in constructing a GaAsFET logic family [4], in CAEN the RTD latches are used for a different purpose: they are used primarily for signal restoration. All computation is performed by diode-resistor logic and the latch restores the signal for a later stage. Work in the 1960s with tunnel diodes and threshold logic was hampered for two reasons. The first, high inter-device manufacturing variability, is solved due to the characteristics of the molecular RTDs (they have a much higher peak-to-valley ratio). The second was a lack of I/O-isolation.

To provide I/O isolation, we incorporate additional devices into the latch and we clock V_{dd} , as shown in Figure 4. The molecular-scale diode is added to prevent current from a downstream latch from flowing to set an upstream latch. The resistor immediately following the RTD-pair forces enough current into RTD_{drive} to allow it to switch high, while allowing enough current into the next latch to determine its value. The resistor to ground allows a latch to go low when the downstream circuit is

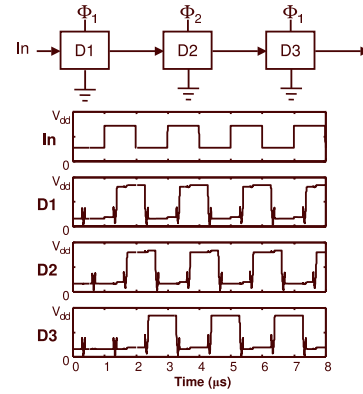


Figure 5: Simple 3-stage delay circuit using molecular latch from Figure 4.

high. The value of this resistor must be large to prevent current loss that would cause latch-setting failure. However, the resistor should also be as small as possible in order to minimize the latch reset time.

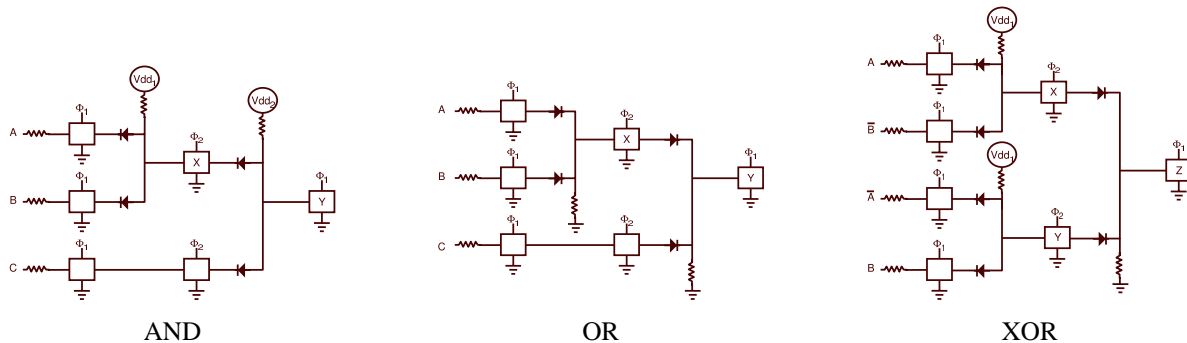


Figure 6: AND, OR, XOR circuits using diode-resistor logic and intermediate molecular latches.

Finally, we introduce a clocking scheme for the pull-up voltage, as shown in Figure 4b. The pull-up voltage is temporarily brought to ground during the setting of the preceding latch. This removes the forward influence and allows the latches to be set properly.

Using SPICE we simulated several simple circuits using the above latch configuration, including the delay circuit in Figure 5 and the AND, OR, and XOR circuits shown in Figure 6. Circuits with more logic levels were also successfully simulated. The latch appears to be stable against the expected variability brought about by manufacture. Because of the relatively low current required to switch states, one molecular latch can drive several other latches, i.e., latches can have moderate fan-out. In combination with the clocking scheme described above, the latch also provides the necessary I/O isolation to ensure scalability of these circuits.

Some caveats are necessary, however. While not intrinsically slow, the RTD devices discovered thus far are extremely resistive, thus, the RC constant for circuits incorporating them is very large (on the order of hundreds of nanoseconds). Also, the relative sizes of the various resistors must be controlled during manufacture to ensure that they are properly matched. Lastly, the use of a clocked pull-up voltage may result in increased power consumption.

Acknowledgments

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