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Current-Driven Magnetic Devices

For Non-Volatile Logic and Memory

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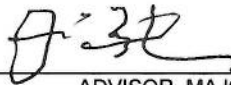
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Abstract

Magnetic logic has entered the spotlight as an intriguing candidate for future electronic systems. Recently we proposed a magnetic logic technology (“mLogic”) based on a current-driven four terminal device (“mCell”) with isolated read- and write- paths. The first step with this nascent technology is to understand the device limitations and performance in response to input stimuli and material properties. In this thesis we explore the design, micromagnetic modeling, and experimental verification of mCell devices.

The concept of an mCell is best described as a “black box” device with four terminals. Two terminals constitute a write-path, wherein the direction of input current flows to program the digital state of the device. The other two terminals constitute a read-path that is electrically-isolated from the write-path. The state of the device is read out as a high or low resistance through the read-path terminals. Because multiple nanomagnetic phenomena (including spin-transfer torque and the spin Hall effect) can be used to program a magnetization (logic) state based on a current direction, we introduce several mCell designs that all satisfy the conceptual 4-terminal mCell model. For each design we describe the operating principles and key features, followed by a presentation of modeling results that indicate performance trends. Of particular focus is the influence of material properties and device geometry on the current density required to instigate state switching. It is found that with appropriate design choices in scaled devices, sub-10 μA switching currents are achievable. Furthermore, we explore other mCell designs that can accommodate switching times below 1 ns.

As part of this device exploration work, we experimentally demonstrate successful domain wall motion, tunnel magnetoresistance, and coupling through a magnetic oxide to validate write-path, read-path, and interlayer components. These components are then integrated into a prototype device. We show this prototype can be reliably switched into one of two (binary) states by pulsing current through the write-path, thereby demonstrating the fundamental mCell concept. We conclude this thesis by proposing future research directions in device design and fabrication to improve this device to enable logic circuits and all-magnetic MRAM bitcells.

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First, I thank my advisors Professor Larry Pileggi and Professor Jimmy Zhu for their support and guidance over the course of my graduate student career. Both Larry and Jimmy served as constant sources of intuition, innovation, and wisdom on how to proceed with this interdisciplinary research. I could write an appendix the size of this thesis itself and I still wouldn't be able to list everything I have learned working with them. It is a rare opportunity to be able to work with two giants of their respective fields, and I am very grateful for the experience.

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1 Introduction

The enormous growth of the integrated circuit (IC) industry over the last forty years has been fueled by Moore’s observation that doubling the number of transistors on a chip every year minimizes cost [1]. As we approach the physical scaling limits for CMOS devices, however, this aggressive density scaling slows down and the cost benefits are no longer evident. Continued growth of the electronics industry, and hence a large portion of world economic growth, relies on the discovery and application of new technologies and devices. A number of post-CMOS technology candidates have been proposed [2], and it is likely that future integrated systems will be composed of an amalgam of such technologies.

Certain applications, however, may benefit from the characteristics of specific devices and/or circuit schemes. Consider an IC that could operate with a voltage supply an order of magnitude smaller than that required for a CMOS chip. Furthermore, allow that voltage to vary almost wildly, without any regulation, or perhaps even shut off from time to time without affecting the functionality of the chip. Now suppose that IC could be fabricated considerably cheaper than its CMOS counterpart in a more environmentally-friendly process. Such a technology would certainly be an attractive candidate to replace or augment CMOS for portable applications, particularly those designed to operate with only a limited supply of energy scavenged from the environment.

1.1 Magnetic Logic Devices and Circuits

Spintronics, where the spin polarization of electrons is exploited in computation, has been studied in recent years as a potential platform for logic circuit design. Generally speaking, spintronic devices represent digital state as the orientation of magnetization in a ferromagnetic material with uniaxial anisotropy, which allows only two (e.g., “up” or “down”) states. Because this information is stored as a magnetization direction, and not inherently dependent on an electrical power supply, it is non-volatile by nature. Recent research has shown that magnetic state can be programmed by electrical currents [3]-[10], eliminating the need for externally-

applied clocking fields only attainable in a lab setting. With modern fabrication techniques, the current densities required to drive magnetization switching may even be provided by voltages well below the 0.9 V required for CMOS operation. Together, these characteristics make spintronics an attractive candidate for portable applications and sensor networks that would benefit from low-energy, non-volatile operation.

Many spintronics concepts have been spawned or inspired by the research on magnetoresistive random access memory (MRAM) that has progressed over the past decade. Combinations of CMOS with magnetoresistive devices have produced the first current-driven products being sampled today [11]. Research groups have further proposed using MRAM-like devices to combine with CMOS that create non-volatile latches for persistence of logic state [12]-[14]. However, this approach requires the tight integration of two heterogeneous technologies, which could increase routing complexity, fabrication cost, and density.

In this thesis we explore the design, modeling, and testing of a particular class of magnetic devices, mCells, for an approach to spintronic circuit design known as mLogic [15]-[17] that does not require tight integration with CMOS. An mCell is a four terminal device with isolated read- and write- paths. An input current pulse through the write-path switches the magnetic state of the write-path by spin-transfer torque or the spin Hall effect; the magnetic state is then coupled through an electrically insulating magnetic material to a free-layer that is sandwiched by two magnetic tunnel junctions (MTJs) to form a read-path. These devices can be configured into circuits based on current steering and can operate on low, noisy supply voltages. The goal of this work is to study the operation and performance of mCell devices in order to understand how to better design them for use in logic and memory applications. Micromagnetic simulation is used to verify device designs and explore switching current requirements and switching speed as a function of material properties and device geometry. Experiments on prototyped structures are used to verify the simulation results and device concepts.

1.2 Overview of Document

This document is arranged as follows:

- Chapter 2 provides a brief survey of magnetic logic device and circuit approaches,

followed by a description of mLogic circuit design concepts and applications;

- Chapter 3 describes the design and micromagnetic modeling of (a) a perpendicularly-magnetized, domain wall-based mCell switched by spin-transfer torque, and (b) a perpendicularly-magnetized, domain wall-based mCell switched by the spin Hall effect;
- Chapter 4 describes the design and micromagnetic modeling of an in-plane magnetized, single domain mCell switched by the spin Hall effect;
- Chapter 5 covers the experimental efforts in developing the constituent components (write-path, read-path, interlayer coupling material) of a domain wall-based mCell from Chapter 3;
- Chapter 6 discusses the development and testing of a device prototype based on the work presented in Chapter 5;
- Chapter 7 concludes this thesis by summarizing the contributions of this research and proposing future work to further advance mLogic.

2 Magnetic Logic Devices and Concepts

There has been a great deal of interest in magnetic logic technologies over the past decade. A number of approaches have been put forth that differ in design and implementation, but all tend to share the common thread that electron spin – not charge – is used to represent and/or transfer data. The magnetization direction of a bistable element generally stores the logic value, making the circuits non-volatile. In this chapter we will introduce a small sampling of these approaches before describing mLogic, the circuit and system application of the devices examined in this thesis.

2.1 Three-Terminal Domain Wall Device Memory and Logic

An MRAM device based on current-driven domain wall motion (DWM) is shown in Figure 2.1 [19]-[21]. It is a three-terminal cell, with write terminals (w^+ , w^-), and a read-path between the R terminal and either of the write terminals. The write-path electrodes are magnetic, with the moments at the two opposite ends permanently oriented in opposite directions. This leaves a domain wall in the write-path. When a current is passed into a write terminal, its constituent electron spins become polarized in the direction of the terminal's magnetic moment, and as a result can move the wall in the direction of the electron flow by spin-transfer torque [3]-[5]. The resulting magnetization state is read out through a magnetic tunnel junction (MTJ) [22] between R , another permanent magnetic electrode, and a write terminal. The resistance of the MTJ is lowest when the moments of the write path and the R electrode are parallel and highest when antiparallel. A closer look at the operating principles behind this device will be presented in the following chapter.

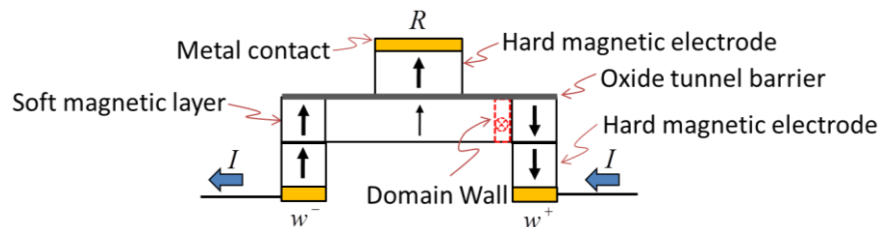


Figure 2.1 – Cross-sectional illustration of three-terminal domain wall motion-based MRAM device.

Although this device has been demonstrated as part of a memory bitcell, the lack of isolated

read- and write- paths makes driving fanout in logic circuits difficult, as current sneak paths within the devices or between devices may exist. One group has devised a scheme in an attempt to avoid this problem by using dummy devices that are intentionally overwritten [23]; this approach, however, requires at least three phases of clocking because a single gate evaluation sends currents through three stages of logic to isolate sneak path currents. Other groups have proposed using this device as resistive pull-down element, with a pull-up consisting of a standard (fixed resistance) MTJ; this structure then acts as a voltage divider that triggers a CMOS inverter in an adjacent stage [24].

There has been more recent research in this area, with modified three-terminal devices being prototyped [25]. These devices are still based on a domain wall-based write and MTJ-based read, but tweaked to exploit better materials combinations for both. Consider Figure 2.1, where the free layer of the MTJ constitutes the same material as the domain wall-driven write-path. There is no material that exists that is optimal for MTJ properties in addition to domain wall motion; FeCoB could be used to yield low resistance-area (RA) product, high tunnel magnetoresistance (TMR) ratio tunnel junctions, but the domain wall mobility would be low, making the write inefficient [26]. Alternatively, Co/Ni multilayers could be used to give good DWM, but at the expense of MTJ properties. The new devices being studied physically separate these materials, relying on magnetostatic coupling between a perpendicular Co/Ni wire (for the write operation) and an in-plane CoFeB free layer (for the MTJ-based read); in newer iterations, the free layer is made to be perpendicular as well for scalability reasons [27]. Note that although the two materials are separate and magnetically coupled, the write- and read-paths are still shared electrically. This still complicates circuit design despite the fact that the read and write operations are individually more efficient due to the use of better materials.

2.2 All-Spin Logic

The device described in section 2.1 uses an electric current to drive switching. The itinerant electrons become spin-polarized by the input terminals and then exert a spin-transfer torque on the domain wall. This is essentially a conversion of charge to spin in the sense that the input is not by itself a magnetic signal, but must be acted on (spin-polarized) to become one. In some approaches to magnetic logic, however, the signaling is not performed with charge current directions but is instead based upon a pure flow of spin. Traditionally, the word “current” is

associated with the flow of charge, but it is possible to have a net flow of spin with no charge flow. This is the basis for all-spin logic [28]-[30]. In this approach, a voltage is applied across a ferromagnetic material deposited on top of a non-magnetic channel such as copper. This results in a current flow to ground. However, the current becomes spin-polarized as it flows through the ferromagnetic material. This leads to an accumulation of minority spin in the channel that can diffuse and act on a second ferromagnetic element (output magnet) down the channel. This is sometimes described as a non-local spin torque. The process is then repeated so that the output magnet can drive other devices (fanout). Insulating regions must be embedded within the channel to prevent back current flow from an output magnet to an input magnet. Multiple spin currents may be superimposed to perform elementary logic operations.

There are significant challenges in the generation and transport of the spin currents [31] which must be addressed for this device and circuit scheme to become a reality. In particular, the channel in the device, as well as the device-to-device routing material, must have a long spin coherence length such that the constituent spins in the signal do not relax to random orientations. Any impurities or defects, which are difficult to avoid in practice, will lead to spin scattering as well. Embedding insulating regions in the channel also complicates the fabrication process.

2.3 Nanomagnetic Logic

Nanomagnetic logic (NML) [32]-[35] is founded on the principle of using coupled nanomagnets to perform logic functions. The placement of these nanomagnets relative to one another defines the logic function; there is no physical wiring between elements or gates, making this approach radically different from those in sections 2.1 and 2.2. Dipole coupling between these magnets induces the magnetization in neighboring structures to align parallel or antiparallel with the magnetization of the “input” magnet, depending on whether these “output” magnets are vertically- or horizontally-collinear (Figure 2.2).

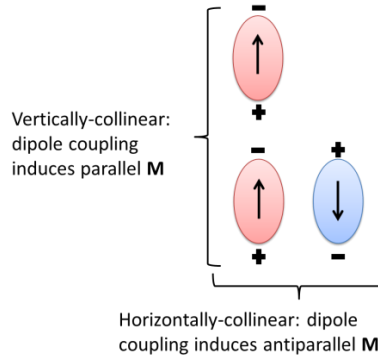


Figure 2.2 – Illustration of nanomagnetic logic coupling preferences. A top-down view is shown, with in-plane magnetization assumed.

Porod et al. have developed a variety of structures based on this approach. An early fabricated three-input majority logic gate [32] of these coupled nanomagnets demonstrated correct logic operation roughly 25% of the time, with an external field used to write the initial state to a set of input magnets. This result highlights one of the key challenges of the NML approach. For the coupling mechanism to work reliably, the nanomagnets must be nominally identical in shape, magnetic characteristics, and relative separation to one another. This is no easy task, and the authors of [32] acknowledged the lack of reliability was most likely a result of variation due to fabrication and field application. The lack of physical wiring is also a challenge for cross-chip signal propagation. More recent work in this area has incorporated perpendicular materials for high thermal stability, explored schemes to ensure a directed signal flow from an input to an output magnet, and studied using current-based clocking to eliminate the need for an external field [33]-[37]. However, there are still many reliability issues that are being addressed as of the time of this writing, with high error rates (i.e., greater than 50%) continuing to be observed due to the unreliability of dipolar coupling.

2.4 mLogic

Consider again the device in section 2.1. Unless true switches are integrated into every stage of a logic design, circuits built from these devices would have current sneak paths. This is because when logic state is evaluated by applying a voltage to the MTJ, current flows directly into the write layer, which can sink to ground or enter other devices unintentionally depending on how the circuit is wired. When read- and write-signals become mixed, making sure devices do not unintentionally switch, or that the write current to a device actually gets there, becomes a

challenge.

In a MOSFET, signals are voltage-based. When a high voltage is applied to the gate of an ideal NMOS transistor, for example, this allows conduction from source to drain, both of which are electrically isolated from the gate terminal. What this describes can be represented as a higher level process: a control signal is applied to a “write-path,” which then affects the current conduction in a “read-path.” The two paths are “coupled,” by an electric field in the case of a MOSFET, but distinct and electrically isolated. In the three-terminal device, distinct read- and write-paths do not exist. This makes designing circuits a challenge when one stage of devices has to drive another stage, as there are multiple paths for the output signals (currents) to flow.

2.4.1 Four-Terminal Device Concept

Imagine a device with the black box model shown in Figure 2.3. In this structure, a current is passed between the (w^+, w^-) terminals, flowing through some (small) resistance r_{wp} . Like in the domain wall device in section 2.1, this input current causes the magnetization state of the device to switch between two stable states. Unlike that device, however, the magnetic state of this device is coupled to a distinct, electrically isolated read-path, with switchable resistance r_{rp} between terminals (r, r') . In this model, the input current through the write path (w^+, w^-) causes the resistance of the read-path (r, r') to switch between two stable states, with complete isolation. Such a device follows the concept described earlier, where a control signal to a write-path affects the current conduction of a read-path. We can condense this black box to a schematic symbol more ideal for constructing circuit diagrams with, shown in Figure 2.4. The contents of the black box will be discussed in great detail in the following chapters; for now, we will consider how a device with this basic model – which we will call an “mCell” – can be used to design circuits.

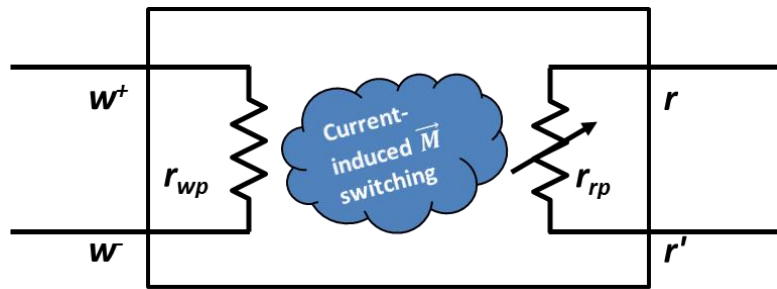


Figure 2.3 – “Black box” model of a four-terminal magnetic device where a controlling current through the write-path terminals (w^+, w^-) switches the resistance between (r, r') between two stable states. The write- and read-paths are electrically-insulated from one another.

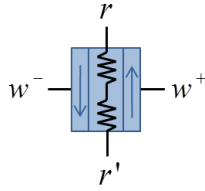


Figure 2.4 – Schematic symbol of four-terminal magnetic element with electrical isolation between the read-path (r, r') and write-paths (w^+, w^-).

2.4.2 Magnetic Logic Circuits with No Integrated CMOS

Based on current technology it is unreasonable to assume the device described in the previous section acts as a perfect switch. Magnetic tunnel junctions are the most commonly-used elements today that convert a magnetization state to an electrical resistance. At best (to date), an MTJ with a reasonably low RA product has a switching ratio of 2-3x. In this section, we will assume the mCell has a 2x switching ratio (100% TMR) and a low resistance of 1.25 k Ω , which can be achieved with appropriate sizing of a low-RA junction. We will also assume the current required to switch the resistance state of the device is 10 μ A and the write-path resistance is 100 Ω .

Because the impedance switching ratio of the mCell is limited by the tunnel magnetoresistance ratio and is small compared to CMOS, a new approach to circuit design is required. In “mLogic” [15]-[18], this approach is based on current steering, where currents are used as signals instead of voltages. Resistor divider networks of the mCell read-paths steer current into or out of a low impedance fanout path in an adjacent logic stage. This is demonstrated by Figure 2.5, where the ratio of the pull-up to pull-down mCell read-path resistances causes a current to flow into or out of an mCell write-path in the next stage. The direction of this current programs the fanout mCell resistance to be either high or low, and so it is the direction (sign) of the current, not its magnitude, that represents the logical sense of the signal. The current leads to state switching, as our black box model assumes. All fanout mCells are connected in series through their write-paths so that each receives the full programming current, with no shunting through unbalanced parallel loads. It is worth noting that all mCells connected in a fanout chain are written simultaneously. In other words, the programming of mCells is not sequential or domino-like; since each write-path in the chain receives the same

programming current at the same time, they all switch together. Adding more mCells to the chain does not impact the switching period, though it does increase the resistive load.

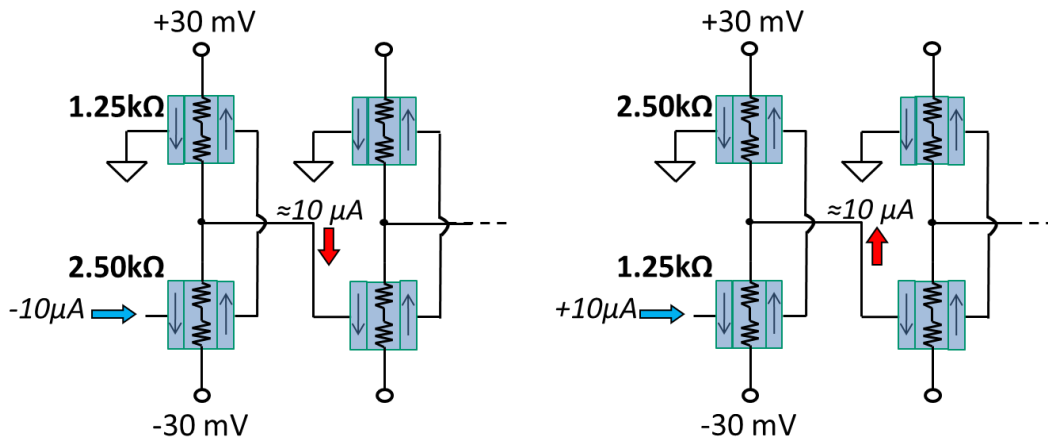


Figure 2.5 – Pull-up and pull-down networks of STT-mCell read paths (MTJ resistances) steer current into or out of fanout STT-mCell write paths. The direction of the output current is the logical sense of the signal.

Because the current through the fanout is small ($10\ \mu\text{A}$ in this example), the required power supply voltage is correspondingly small. Matched positive and negative voltage rails on the order of $100\ \text{mV}$ are sufficient to power mLogic circuits by providing the write currents (e.g., $\pm 30\ \text{mV}$ in Figure 2.5). Improved MTJ properties (low RA , high TMR) and low critical current density in the write-path further reduce the supply requirements (this is discussed in more detail in section 7.2.2). These power rails are pulsed in a scheme referred to as pClocking, where alternating stages of logic use non-overlapping phases of power clock (Figure 2.6). By clocking the power, a gate is only on when its output is to be evaluated, providing for energy savings and avoiding timing errors.

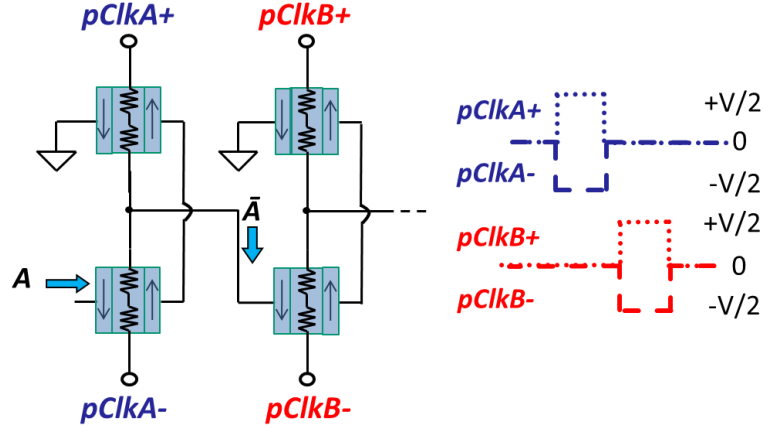


Figure 2.6. A driving inverter powered on one phase of pClk, and a fanout inverter powered on a second, non-overlapping phase. Note the mCells constituting the fanout inverter are wired in series through their write paths.

More advanced principles behind mLogic circuit design can be found in [15]-[17]. The focus of this thesis is on device characterization and experimental verification. However, it is still important to recognize that the primary motivation for studying this device is its suitability as a circuit element. The design of the mCell is intimately tied to the circuit design principles of mLogic, which is what sets it apart from other bistable storage magnetic devices that are not appropriate for creating electrical logic circuits (e.g., driving fanout).

2.4.3 All Magnetic “3M”-MRAM

In the past ten years, research on magnetoresistive random access memory (MRAM) [22] has intensified in the hopes of developing a fast, non-volatile, dense memory technology. A common approach places a magnetic tunnel junction (MTJ) in series with a CMOS access transistor. The state is written when the control signal (wordline) to the transistor is high, which passes a large current through the MTJ that switches its logic state from a high resistance to a low resistance by spin-transfer torque. To read, a smaller voltage is applied to the transistor, which passes a sensing current through the MTJ to evaluate its resistance. Another approach is based on the three-terminal MRAM element that is switched by current-driven domain wall motion (section 2.1). This device provides the benefit of not having to supply write current through a high resistance MTJ. This approach, however, requires two CMOS access transistors, increasing the cell size, and typically uses non-optimal materials due to shared read- and write-paths.

Due to the electrical isolation between the read- and write-paths, the mCell can be used in a

memory bitcell with no access transistors, allowing for the first design of an all-magnetic MRAM (Figure 2.7). Each bitcell consists of three mCells, essentially a buffer (inverter) driving an output device. We will first describe a write operation. The write bitline (WBL) is a current signal (unlike in traditional memories) where the direction of the current programs the states of the buffer devices. For the row(s) that will write the bitline value into the storage cell, the write wordlines WWL+ and WWL- are asserted to V^+ and V^- , respectively. This causes a current to flow through the write-path of the third mCell (the storage element), the directionality of which is determined by the ratio of the buffer's pull-up and pull-down read-path resistances. This programs the bit value of the output mCell, which holds the data value of the bitcell. To read, WWL+ and WWL- are returned to GND, the read wordline (RWL) is asserted to V^+ , and an output current flows through the storage element's read-path on the read bitline (RBL).

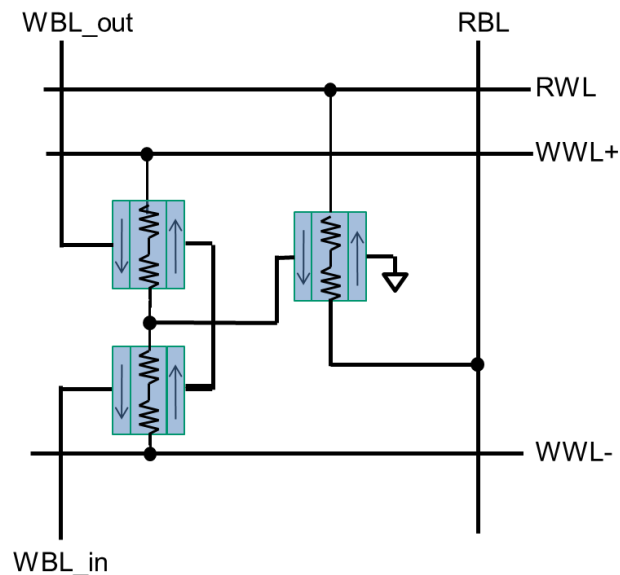


Figure 2.7 – Schematic of an all-magnetic mCell-based bitcell. No CMOS access transistors are required due to the electrical isolation between read- and write-paths.

An exemplary 2x2 memory array based on such a bitcell is shown in Figure 2.8. Like conventional memory technologies such as DRAM and SRAM, the memory is divided into rows and columns. Each row shares the same wordlines, and each column shares the same bitlines, allowing for addressing anywhere in the array. Each wordline is connected to an inverter or buffer that sets the line voltage to the required value (as indicated in the schematic and described in the previous paragraph in the context of one bitcell) when activated by the proper control signal (also indicated in the schematic). Note that because the write bitline signals are currents,

all the buffers are driven in a series connection; the WBL is asserted to a voltage such that the resulting current direction will program all the scratch buffers. During a read operation, a high voltage is applied to the appropriate RWL, causing a current to flow through the mCell read-path it is connected to. The magnitude of this current will depend on the resistance (and therefore, the logic state) of the mCell and can be compared to a reference current by using a transimpedance amplifier (TIA). The output of the TIA indicates if the bit stored in the mCell was a logic-0 or logic-1. The TIA input where the mCell current flows is held at virtual ground to prevent the current from “sneaking” into other devices. A sample simulation of a 4x4 array is shown in Figure 2.9. The bit patterns “1111”, “1010,” “1001”, and “0000” are written from the top row down to the bottom row. When the appropriate RWL signal is asserted, the bitlines will either have a large current or a small current flowing down into the read circuitry, as shown in the figure. Note that a high current signal being read actually represents a logic-0 written to the bitcell, due to the logical inversion that happens in every bitcell.

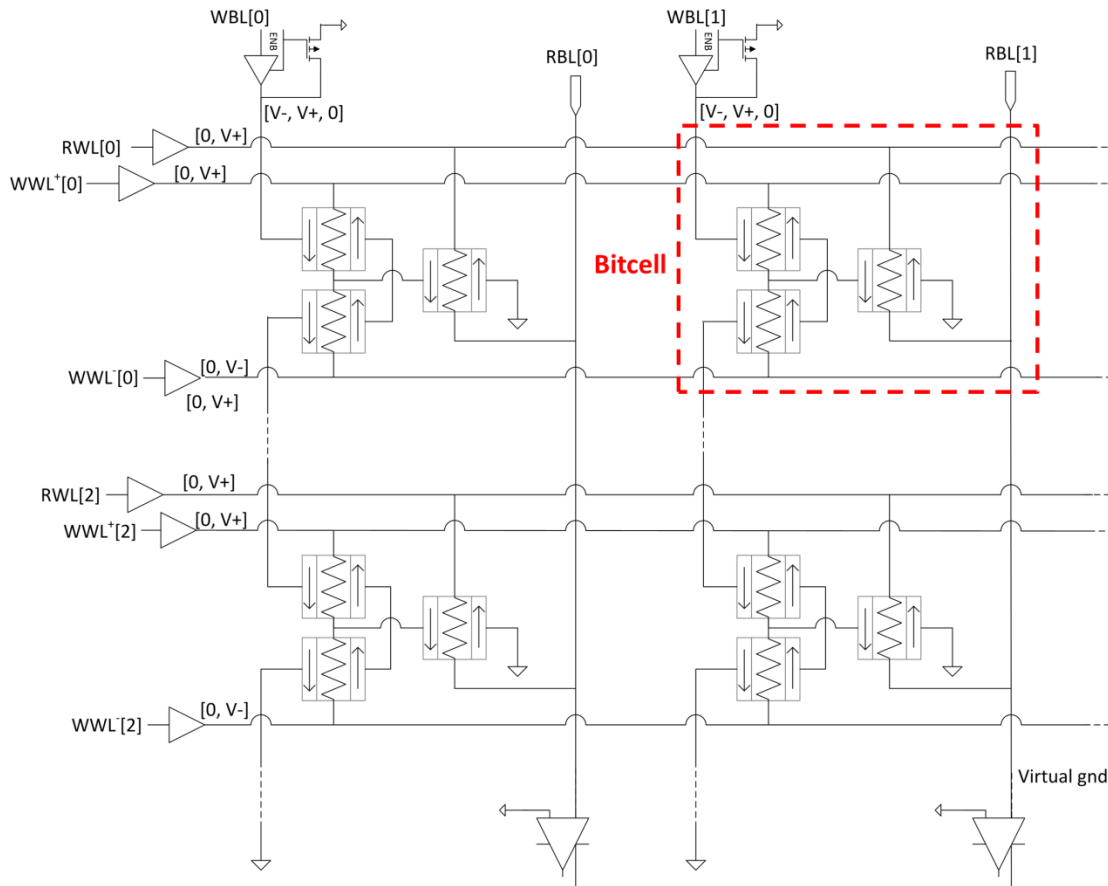


Figure 2.8 – 2x2 memory array of all magnetic devices. Peripheral elements, such as sense amplifiers and PMOS

transistors, are shared between columns and rows.

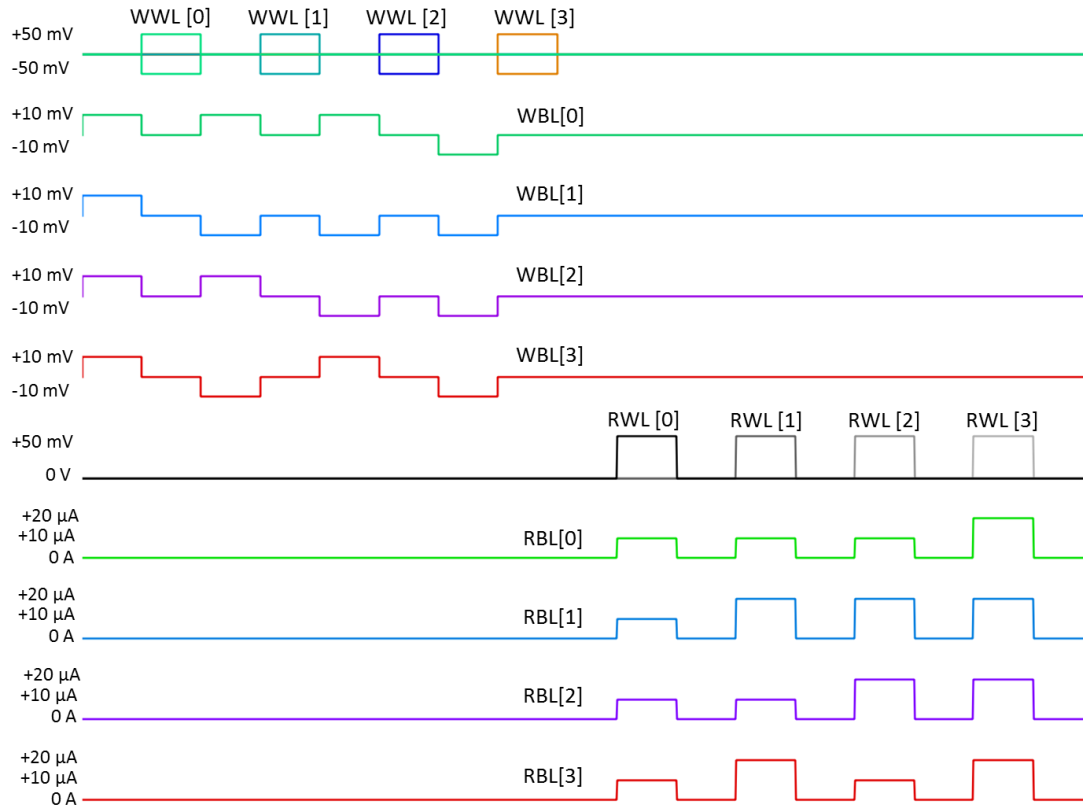


Figure 2.9 – Sample simulation showing a functioning write/read test. Signals being read are logical inversions of input data due to built-in inversion in the bitcell.

The absence of CMOS devices in the bitcells enables the use of ultra-low voltages (< 100 mV), which greatly reduces the energy wasted in charging bitline and wordline capacitances. For a 16×16 array, we estimate the write energy to be 5.1 fJ/bit, a roughly $5 \times$ improvement over traditional STT-MRAM assuming the same MTJ parameters. As the array size scales, we expect this improvement to become even more significant since the voltage levels are lower, thereby reducing the energy burned in charging the line capacitances. Array periphery elements (i.e., anything not in the bitcell array itself) can all be designed using standard CMOS devices. Even though three mCells are required per bitcell, the density can still be very high. First, because no CMOS is actually required in the array itself, the entire CMOS periphery (read and write driver) can be built directly underneath the array. Additionally, the bitcell area is not at all limited by stringent CMOS design rules. Even for an aggressively-scaled 10 nm node FinFET (Figure 2.10),

the transistor could still occupy more total area than three aggressively-scaled (e.g., 10 nm node) mCells. We estimate a 10 nm FinFET would occupy 3x4 metal tracks, whereas our scaled bitcell design would occupy 5.5x2 tracks for a net smaller area.

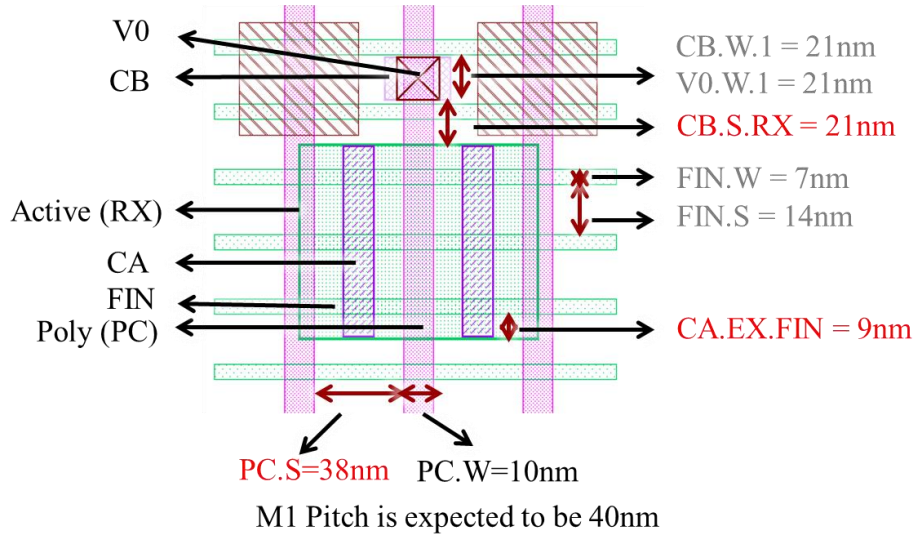


Figure 2.10 – Three-fin device with ITRS projected design rules in 10 nm. Stringent spacing rules increase the area requirement for a transistor. (Courtesy K. Vaidyanathan)

2.5 Conclusions

This chapter has provided a brief overview of proposed magnetic logic technologies, with emphasis on mLogic. These mCell-based circuits can operate at low voltages with noisy or even intermittent power supplies due to the inherent nonvolatility of the devices. The nature of the mCell – a four terminal element with isolated read- and write-paths – makes it possible to design circuits capable of driving fanout without any integration of CMOS transistors. mCells also allow for a dense, low power, all-magnetic MRAM.

In the following chapters, we will explore the design, modeling, and fabrication of the devices that make mLogic possible. Wherever relevant, we will discuss specific device-level findings in the context of mLogic circuit design.

3 Four-Terminal Domain Wall Devices

In this chapter we propose configurations and introduce the concepts for possible mCell logic devices based on moving domain walls. A brief overview of the underlying physics is presented, followed by a discussion on design considerations and constraints. A micromagnetic characterization is shown, illustrating the energy and speed performance that can be expected based on current technology. Particular attention is paid to common material properties and device sizing that would be important to realize the devices in the lab.

3.1 Background

3.1.1 Spin-Transfer Torque (STT) Domain Wall Motion

When an electron passes through a magnetized material (Figure 3.1) its spin becomes polarized in the direction of the magnetization (e.g., “spin-down” or “spin-up”). Once this spin-polarized electron reaches a region of magnetization of different orientation, as in a domain wall, its spin is again polarized to align with the magnetization. The spin re-alignment results in a change in the angular momentum of the electron. To conserve angular momentum, a torque is exerted on the local magnetic moment of the material. This spin-transfer torque [3]-[4] acts on the magnetization to align it with the electron’s initial polarization. For example, if a spin-down electron enters a region of magnetization oriented up, the spin-transfer torque will then act to pull that magnetization downward. This phenomenon can be used to move domain walls in magnetic materials in the direction of electron flow, and has been used to drive switching in various magnetic memories, including the one described in section 2.1 and the first demonstrations of racetrack memory [38]. STT is used for switching single domain pillar MRAM as well [11].

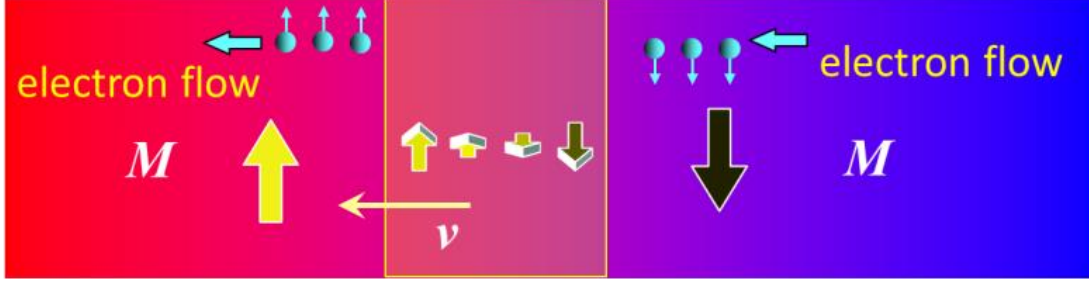


Figure 3.1. Illustration of spin-transfer torque-driven domain wall motion. The domain wall moves in the direction of the electron flow.

If we consider a sample slice of thickness dx in the direction of (a one-dimensional) current flow, the spin torque, or the time rate of change of the spin angular momentum $\vec{S}$, can be determined by equating the time evolution of the local magnetization and the amount of angular momentum deposited by the spin-polarized conduction electrons:

$$\frac{d\vec{S}}{dt} = -\frac{1}{\gamma} \frac{\partial \vec{\mu}}{\partial t} = -\frac{1}{\gamma} \frac{\partial \vec{M}}{\partial t} dx dy dz = P \left(\frac{J}{e} \right) \frac{\hbar}{2} dy dz \left[\frac{\vec{M}(x+dx) - \vec{M}(x)}{M_s} \right] \quad (3.1)$$

Here, $\vec{\mu}$ is the magnetic moment, M_s the saturation magnetization of the material, γ the gyromagnetic ratio (equal to $\frac{g\mu_B}{\hbar}$, where g is the Landé factor and μ_B the Bohr magneton), P the electron spin polarization, J the charge current density, e the electron charge, $\hbar$ the reduced Planck constant, and $\vec{M}$ the magnetization vector. The resulting time rate of change of the magnetization due to the spin current is obtained by solving the above equation for $\frac{\partial \vec{M}}{\partial t}$:

$$\frac{\partial \vec{M}}{\partial t} = -\frac{gJ\mu_B P}{2eM_s} \frac{\partial \vec{M}}{\partial x} \quad (3.2)$$

The coefficient $\frac{gJ\mu_B P}{2eM_s}$ is generally lumped into a single quantity u , often referred to as the spin current velocity or spin current density, with units of m/s. For a three-dimensional current flow and magnetization gradient, we can generalize the above result to:

$$\frac{\partial \vec{M}}{\partial t} = -(\vec{u} \cdot \vec{\nabla}) \vec{M} \quad (3.3)$$

As shown in the above equation, the spin transfer torque behind domain wall motion is proportional to the current density and to the spatial gradient of the magnetization.

3.1.2 Spin Hall Effect

The spin Hall effect (SHE) [9]-[10] occurs in structures where a magnetic layer is adjacent to a select non-magnetic material with strong spin-orbit coupling. When a charge current flows through the non-magnetic material (e.g., Pt, Ta), electrons with different spin orientations are deflected to different surfaces. This essentially generates a spin current, transverse to the direction of the charge current, that can be used to act on the magnetization state of the adjacent magnetic layer (Figure 3.2). The resulting Slonczewski torque can be added to the LLG equation:

$$-\frac{\hbar J_{NM} \theta_{SH}}{2e M_s t_{FM}} \vec{M} \times (\vec{M} \times \hat{\sigma}) \quad (3.4)$$

Here, $\hbar$ is the reduced Planck constant, θ_{SH} is the spin Hall angle (which can be thought of as the fraction of the current deflected toward the nonmagnetic/magnetic interface), t_{FM} the thickness of the ferromagnetic material, and J_{NM} the current density in the nonmagnetic material. This is an important distinction. In STT, the current flow through the magnetic materials drove switching. In this case, it is desirable for the current density to be highest in the nonmagnetic metal under- or capping-layers.

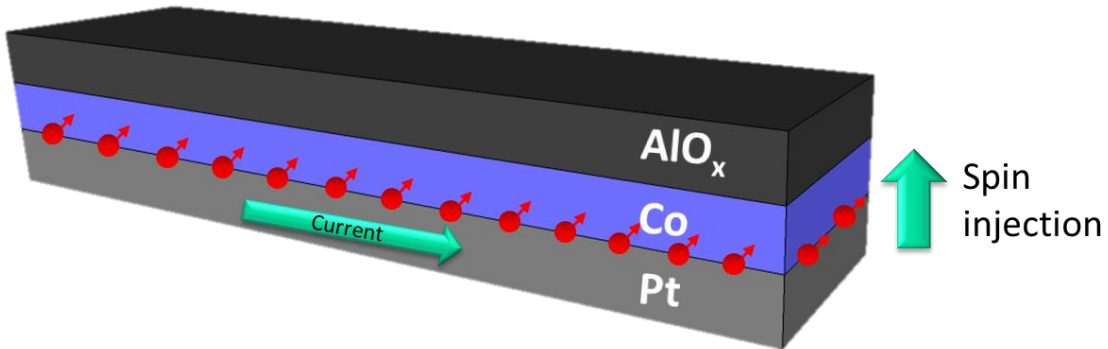


Figure 3.2 – Illustration of spin injection from Pt to Co due to the spin Hall effect in a Pt/Co/AIO_x structure.

One would not initially expect this injection of in-plane spin to be capable of sustaining the motion of a perpendicular domain wall. However, if the domain wall structure is set to be of Néel form, with a wall center along the wire length and orthogonal to the injected spins, the domain wall can be moved. An illustration of this scenario is shown in Figure 3.3, which is representative of the experiments described in Chapter 5. Assume the domain wall has the chirality shown, such that the center moment of the domain wall is in the $-\hat{x}$ -direction. If the electron flow is in the $+\hat{x}$ -direction, spins aligned along $-\hat{y}$ will be injected from the Pt into the magnetic layer. The domain wall then moves along the direction of the current flow.

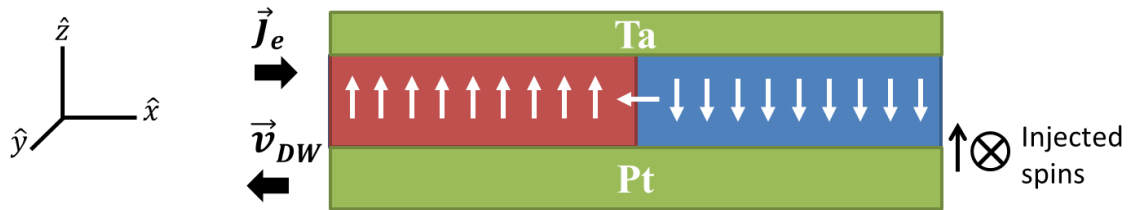


Figure 3.3 – Illustration of scenario in which in-plane spins injected by the SHE move a domain wall with Néel structure opposite the electron flow.

Note that the injected spins only create a torque that drives the domain wall because they are aligned at 90° to the wall center. If the domain wall were Bloch-type, the two moments would be parallel or antiparallel and no torque would result. In scaled perpendicular wires, Bloch walls are usually expected to be found because Néel walls have an associated internal demagnetization energy that makes them unfavorable [39]. However, it has been found that in some cases an additional force, the Dzyaloshinskii-Moriya interaction (DMI) [40]-[43], can dominate. This effect tends to produce stable Néel walls suitable for moving with the SHE. High velocity domain wall motion has been experimentally demonstrated in these systems [40]-[44]. By reversing the chirality, one can actually set which way the domain wall moves in response to the current; in other words, SHE-DWM along the electron flow is possible if the DMI (or an external field) sets the wall chirality in the correct direction.

3.1.3 Magnetic Tunnel Junctions (MTJs)

A magnetic tunnel junction consists of a thin tunnel barrier (an oxide) sandwiched by two magnetic layers (Figure 3.4). One of these magnetic layers, the reference layer, is fabricated to be more difficult to switch, such that its magnetization can be considered fixed. The other magnetic layer is engineered to be softer, such that its magnetization can be more easily switched by field or current. The conductance of the junction is a function of the orientation of this free layer's magnetization relative to the magnetization of the fixed layer. When the two layers have parallel magnetization, the resistance of the MTJ is at its lowest state; when the layers have antiparallel magnetization, the resistance of the MTJ is at its highest state. In general, the conductance G is given by

$$G(\theta) = \frac{1}{2}(G_P + G_{AP}) + \frac{1}{2}(G_P - G_{AP})\cos(\theta) \quad (3.5)$$

where G_P is the conductance in the parallel state (maximum), G_{AP} is the conductance in the antiparallel state (minimum), and θ is the angle of the free layer magnetization relative to the fixed layer magnetization. The tunnel magnetoresistance (TMR) ratio, which measures the change in resistance from low state (R_P) to high state (R_{AP}), is given by

$$TMR = \frac{G_P - G_{AP}}{G_{AP}} = \frac{R_{AP} - R_P}{R_P} \quad (3.6)$$

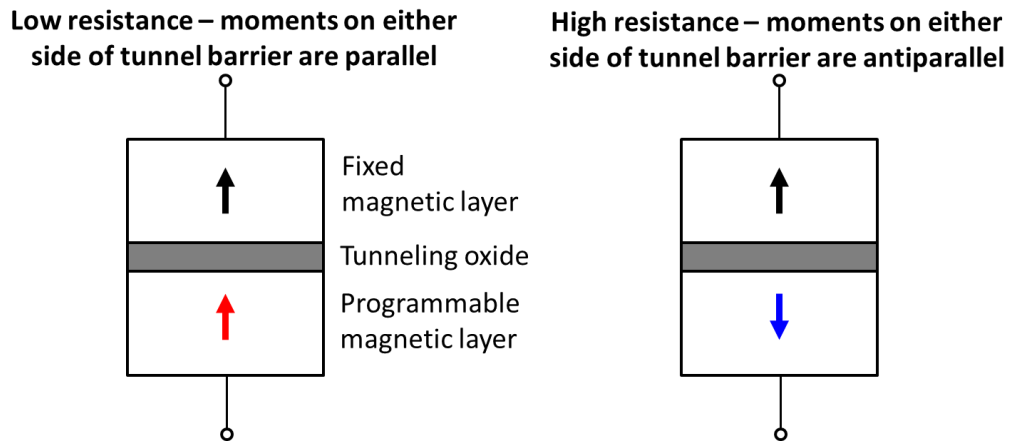


Figure 3.4 – Illustration of MTJ stack and resistance states.

TMR arises from the difference in the electron density of states at the Fermi level between

majority and minority spins. During tunneling, electron spin is conserved, and so the electrons can only tunnel into the sub-band of the same spin orientation. Thus, the tunneling conductance is directly proportional to the product of the Fermi level density of states. If many electrons are available at the Fermi level for tunneling and many states are available on the other side of the barrier, the resistance is low; if many electrons are available for tunneling, but few states are available on the other side of the barrier (when the moments are antiparallel), the resistance is high. More detailed information can be found in [45].

Today, the most common MTJ film stacks with perpendicular magnetization consist of CoFeB (or FeCoB) grown on a tantalum seed layer, followed by a magnesium oxide (MgO) tunnel barrier 0.9-1.8 nm thick, followed by another CoFeB magnetic layer [46].

3.1.4 Micromagnetic Simulation Environment

Fabricating and testing samples to characterize device performance (e.g., domain wall velocity) across a wide array of parameters can be prohibitively expensive and time consuming. To understand how the devices described in this thesis perform as a function of material properties, geometry, and input stimuli, a custom micromagnetic simulation tool based on the finite difference method [47] was utilized. In this method of simulation, an input geometry is discretized into a mesh of cubes (or cuboids), with a magnetic moment of constant magnitude defined in each cell. For every time step, the effective magnetic field acting on a cell is calculated. This calculation includes any applied field, as well as internal fields due to anisotropy (equation (3.7)), exchange ((equation (3.8))), and demagnetization (equation (3.9)). The terms are defined in Table 3-I. To be clear, the calculation of the demagnetization field involves working with fictitious magnetization “charge” representing the magnetization at a given point ($\vec{r}'$) to evaluate the field at another point ($\vec{r}$).

$$\vec{H}_K = \frac{2K_u}{M_S^2} \hat{a}(\vec{M} \cdot \hat{a}) \quad (3.7)$$

$$\vec{H}_{EX} = \frac{2A}{M_S^2} \nabla^2 \vec{M} \quad (3.8)$$

$$\vec{H}_D = \int \frac{\rho(\vec{r}')(\vec{r} - \vec{r}')}{|\vec{r} - \vec{r}'|^3} dV' + \int \frac{\sigma(\vec{r}')(\vec{r} - \vec{r}')}{|\vec{r} - \vec{r}'|^3} dA' \quad (3.9)$$

Table 3-I – Definitions of terms appearing in the equations for effective fields due to anisotropy, exchange, and demagnetization.

Symbol	Definition
K_u	Uniaxial anisotropy strength
$\hat{a}$	Direction in which the anisotropy acts (e.g., $\hat{z}$)
A	Exchange stiffness
$\rho(\vec{r}')$	Volume pole density of magnetization “charge”
$\sigma(\vec{r}')$	Surface pole density of magnetization “charge”
$\vec{r}'$	Source point of magnetization “charge”
$\vec{r}$	Evaluation point of demagnetization field

Torques that depend on current flow, including the STT and SHE terms (equations (3.3) and (3.4)), are evaluated in those cells that have current flowing through them. The underlying phenomenological Landau-Lifshitz-Gilbert equation (equation (3.10), where $\vec{H}_{EFF}$ is the effective magnetic field and α the Gilbert damping constant) is then solved in each cell for each time step:

$$\begin{aligned} \frac{\partial \vec{M}}{\partial t} = & -\gamma(\vec{M} \times \vec{H}_{EFF}) + \frac{\alpha}{M_s} \vec{M} \times \frac{\partial \vec{M}}{\partial t} + \frac{\vec{M}}{M_s^2} \times [\vec{M} \times (\vec{u} \cdot \vec{v}) \vec{M}] + \frac{\beta}{M_s} \vec{M} \times (\vec{u} \cdot \vec{v}) \vec{M} \\ & - \frac{\hbar J_{NM} \theta_{SH}}{2e M_s t_{FM}} \vec{M} \times (\vec{M} \times \hat{\sigma}) \end{aligned} \quad (3.10)$$

Because space is discretized into cubic cells, the original nonlinear partial differential equation becomes a nonlinear ordinary differential equation in each cell. The discrete forms of equations (3.7)-(3.9) become

$$\begin{aligned} \vec{H}_K(i, j, k) = & \frac{2K_u}{M_s^2} \left[\sin\theta_{i,j,k} \cos\varphi_{i,j,k} M_{X_{i,j,k}} + \sin\theta_{i,j,k} \sin\varphi_{i,j,k} M_{Y_{i,j,k}} \right. \\ & \left. + \cos\theta_{i,j,k} M_{Z_{i,j,k}} \right] \left[\sin\theta_{i,j,k} \cos\varphi_{i,j,k} \hat{x} + \sin\theta_{i,j,k} \sin\varphi_{i,j,k} \hat{y} + \cos\theta_{i,j,k} \hat{z} \right] \end{aligned} \quad (3.11)$$

$$\begin{aligned}
\vec{H}_{EX}(i, j, k) = \frac{2A}{M_S^2} & \left[\frac{1}{\Delta x^2} \sum_{i'}^{nnx} M_{X_{i+i'}} \hat{x} + M_{Y_{i+i'}} \hat{y} + M_{Z_{i+i'}} \hat{z} \right. \\
& + \frac{1}{\Delta y^2} \sum_{j'}^{nny} M_{X_{j+j'}} \hat{x} + M_{Y_{j+j'}} \hat{y} + M_{Z_{j+j'}} \hat{z} \\
& \left. + \frac{1}{\Delta z^2} \sum_{k'}^{nnz} M_{X_{k+k'}} \hat{x} + M_{Y_{k+k'}} \hat{y} + M_{Z_{k+k'}} \hat{z} \right]
\end{aligned} \tag{3.12}$$

$$\vec{H}_D(i, j, k) = \sum_{i'=1}^{N_X} \sum_{j'=1}^{N_Y} \sum_{k'=1}^{N_Z} \begin{bmatrix} D_{XX} & D_{XY} & D_{XZ} \\ D_{YX} & D_{YY} & D_{YZ} \\ D_{ZX} & D_{ZY} & D_{ZZ} \end{bmatrix}_{(i'-i), (j'-j), (k'-k)} \begin{bmatrix} M_X \\ M_Y \\ M_Z \end{bmatrix}_{i', j', k'} \tag{3.13}$$

In the above equations, N_X , N_Y , and N_Z are the number of mesh cells in the $\hat{x}$, $\hat{y}$, and $\hat{z}$ directions, and nnx , nny , and nnz are the nearest neighbors of a cell in the $\hat{x}$, $\hat{y}$, and $\hat{z}$ directions. $\vec{M}$ is the magnetization vector, with components $[M_X, M_Y, M_Z]$. The orientation of the easy axes of cell (i, j, k) are given by the angles $(\theta_{i,j,k}, \phi_{i,j,k})$ in spherical coordinates. For a perfect perpendicular material, θ and ϕ would be 0 in every cell. In the demagnetizing field calculation, the magnetization components are convolved with a matrix of demagnetizing factors, $\vec{D}$, a tensor which represents the coupling between cells as a function of geometrical position. Importantly, any given cell in the mesh is coupled to every other cell, which makes the calculation of this field tedious. The tensor component expressions may be found in the literature [48]. A fast Fourier transform (FFT) is used to reduce the problem complexity from $O(N^2)$ to $O(N \log N)$ [49]. Various standard problems proposed by NIST [50] were successfully tested on the simulator. Figure 3.5 gives the desired sample results for standard problem 4a [51], in which a 25 mT field at 170° to the $+\hat{x}$ axis is applied to a permalloy bar 500 nm long, 125 nm wide, and 3 nm thick. These results are in good agreement with those from other simulation tools and research groups, including NIST's own OOMMF [52].

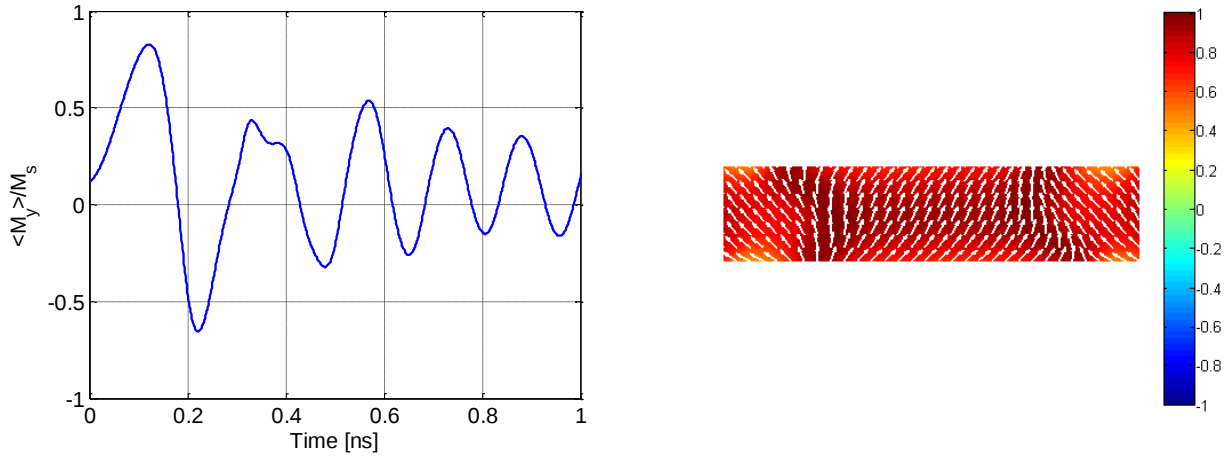


Figure 3.5 – (left) Average y-component of magnetization as a function of time for NIST standard micromagnetics problem 4a; (right) snapshot of magnetization as average x-component crosses 0 in the same problem. These results agree well with other groups’ data.

In addition to internal fields and external stimuli, thermal energy can directly influence magnetization. At any non-zero temperature, thermal fluctuations can act on the magnetic moment in a material and alter its orientation. To model this effect we add a “thermal field” [53] to each cell. Two randomly oriented but mutually orthogonal vectors are generated; by symmetry, each vector has the same RMS value. Each vector is then scaled by a factor from a standard normal distribution such that the thermal field can be expressed as

$$\vec{H}_{th} = \eta_1 H_{th,RMS} \hat{\theta} + \eta_2 H_{th,RMS} \hat{\phi} \quad (3.14)$$

$$H_{th,RMS} = \sqrt{\frac{2\alpha k_B T}{\gamma M_S V \Delta t}} \quad (3.15)$$

Even if the devices are built perfectly, with absolutely no variation across the chip or defects of any kind, thermal agitation still makes switching stochastic.

It is important to recognize the limitations of micromagnetic modeling. Generally speaking, micromagnetics can be useful to observe trends; for example, simulations in this thesis are used to understand how the switching current density varies with material properties. The resulting trends contain more information than the precise values of current density found in the simulations, because they help shed light on dependencies that may not be immediately or intuitively apparent. These trends can then guide sample design for experimental evaluation. The precise current densities, however, may vary from simulation to experiment, largely due to all the

effects and non-idealities the micromagnetic framework described in this section does not include (e.g., imperfect film interfaces, edge roughness, defects, etc.). Additionally, the current-driven switching effects studied in this thesis are truly an abstraction level below micromagnetics, and the torque terms added to the LLG equation are an attempt at treating them semi-classically. Other groups have approached the problem differently and have developed “self-consistent” simulation tools, where some effects are treated at a lower, spin-transport level, before being plugged into a micromagnetic simulator. Finding the most accurate way to simulate these nanomagnetic devices, particularly those driven by current, is still an ongoing research effort. Additional information on lower-level modeling of spin transport mixed with micromagnetics can be found in [54]-[55].

3.2 STT-mCell Device Design and Modeling

In the previous chapter, a black box model for the 4-terminal mCell abstraction was presented. Here, we introduce one possible device that implements that black box model. This device, the STT-mCell, is shown in Figure 3.6. It is a four-terminal device that consists of a write-path (w^+, w^-) and electrically-isolated read-path (R, R'). The write-path is composed of a low-impedance, ferromagnetic metal with perpendicular anisotropy connecting the (w^+, w^-) electrodes. These electrodes are magnetic, with the moments at the two ends permanently oriented in opposite directions. This leaves a domain wall in the write-path, much like in the three-terminal domain wall memory device described in section 2.1. Spin-transfer torque (section 3.1.1) is the mechanism that causes domain wall motion.

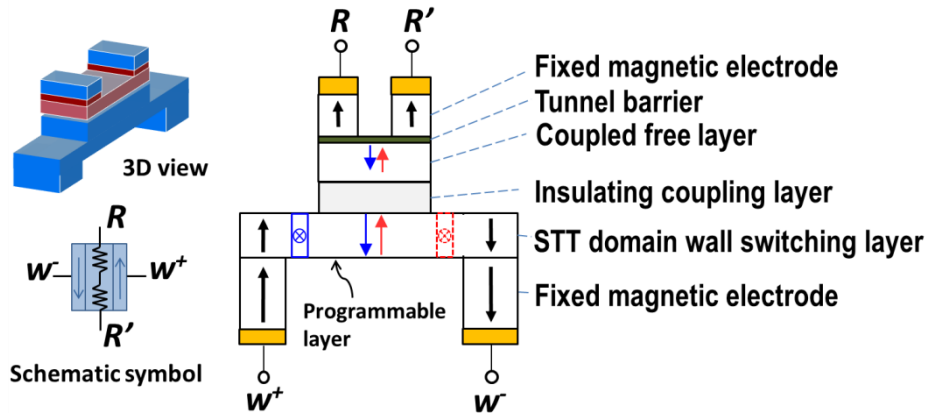


Figure 3.6 – mCell cross section, 3D view, and schematic symbol. The read-path of the device is through the (R, R') terminals and the write-path is through the (w^+, w^-) terminals.

The write-path, though electrically-insulated from the read-path, is exchange-coupled to a switchable free layer in the read-path through an insulating magnetic material. As a result, the programming of the write-path also programs the magnetization of this free layer. Depending on the domain wall position, the resistance between the terminals R and R', fixed magnetic electrodes which sandwich a tunnel barrier (hence forming two MTJs with a shared free layer in series), is changed from its lowest stable value (R_L) to its highest stable value (R_H), and vice versa. It is possible to short out the tunnel barrier under one of the read-path electrodes to lower the overall read-path resistance, which is beneficial for the circuits [15]. This can be done by applying a large voltage (e.g., 1-2 V) between a read-path terminal and write-path terminal (for example, R' and w⁻).

The result is that by sending a small electron current pulse from w⁻ to w⁺ or w⁺ to w⁻, the mCell read-path resistance between R and R' is programmed to be high or low, respectively. The two resulting stable resistance states are non-volatile, as removing power has no effect on the orientation of any layer's magnetization, and an energy barrier is inherently built in to the device. The energy density (in ergs/cm²) of a 180° Bloch wall is given by

$$E_{DW} = 4\sqrt{AK_u} \quad (3.16)$$

where A is the exchange stiffness of the material and K_u the uniaxial anisotropy strength. Since the actual energy is proportional to the cross-sectional area of the domain wall, an energy barrier can be established if the wall changes size as it moves:

$$E_B \approx 4W\sqrt{AK_u}(\Delta h) \quad (3.17)$$

Here, W is the width of the wire supporting the domain wall and Δh the change in wall height as the wall moves past the position of the barrier. The deposition of the insulating magnetic material and read-path free layer over the STT layer effectively creates a step in the write-path of the mCell, such that the domain wall is taller during travel. When no current is applied, the wall naturally rests in either of the thin necking regions between a write-path electrode and the step. As a result, it is not out in the middle of the write-path and changing the resistance state of the device.

To characterize the switching behavior of an mCell, the micromagnetic simulation framework described in section 3.1.4 was utilized.

3.2.1 State Switching Process

Simulation of current-driven domain wall motion in the STT-mCell is shown in Figure 3.7. At $t=0$, the magnetization of the write-path is initialized antiparallel to the read-path electrodes (high resistance state). An electron current is then applied from left to right. The domain wall is freed from its initial position and swept across the write-path by STT; note that as the domain wall moves, the free layer in the read-path switches in tandem. At the end of the simulation, the domain wall is on the other side of the device, with the magnetization now oriented parallel to the read-path electrodes (low resistance state).

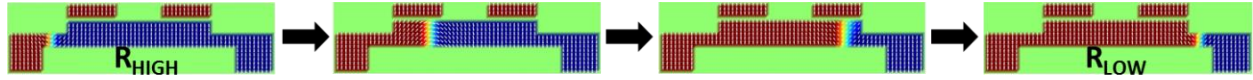


Figure 3.7 – Micromagnetic simulation of STT-mCell state switching. The device begins in a high resistance state and ends in a low resistance state for an electron current flowing from the left terminal to the right terminal.

Figure 3.8 shows the energy of the system as a function of time over the course of 100 simulations, each modeling a different set of random thermal fluctuations. The behavior is essentially the same; the device begins at a low energy state, and when the domain wall is pushed into the write-path, the energy increases due to the difference in wall height. When switching is complete, the device enters a second low energy state (the simulations were programmed to end at a certain value of the average magnetization of the free layer, and because this is not the true final state of the system, the energy curves end prematurely and do not reach their true minima). The mean energy barrier in this example was $73.8 k_B T$ with a standard deviation of $1.22 k_B T$. The mean switching time was 1.00 ns with a standard deviation of 0.34 ns .

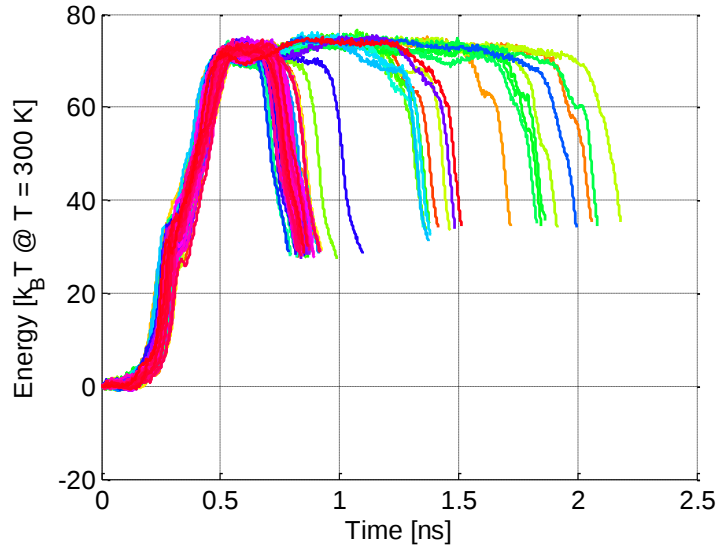


Figure 3.8 – Energy as a function of time during switching. Note that while the domain wall is in the middle of the device, the energy is considerably larger than at its stable endpoints.

3.2.2 Switching Probability

Referring to Equations (3.2) and (3.3), we see that the magnitude of the spin-transfer torque is linear with the current density. Because thermal fluctuations make domain wall depinning and subsequent motion a stochastic process, we expect that there is a critical current density required to overcome wall pinning and thermal agitation with high probability. Figure 3.9 shows that increasing the current density increases the probability of switching (out of 100 total cases per current density), and that lower currents can be used for longer pulses (because the probability of overcoming an energy barrier for a given J is time-dependent). In this thesis, we will define a switching probability of 95% as the critical current density. This is not sufficient for real logic circuits, where the devices are expected to switch correctly on every cycle, but it will still enable us to understand the relevant trends as device parameters and properties are varied. A more detailed look at how the threshold current, defined as the current required to switch the device at a given probability for a fixed pulse width, varies as a function of sample size (number of simulated cases) is shown in Figure 3.10. From the figure, we see the critical current density tends to increase (or remain constant) as we consider an increasing number of cases and increasing success threshold. This result implies that current pulses in actual logic circuits would need to be margined in order to overcome this error rate, particularly when we consider the lifetime of the chip and how many cycles each device would experience. In the concluding

chapter of this thesis we briefly introduce alternative uses of the mCell where this challenge is no longer important to meet, and where the inherent randomness of the devices may be exploited.

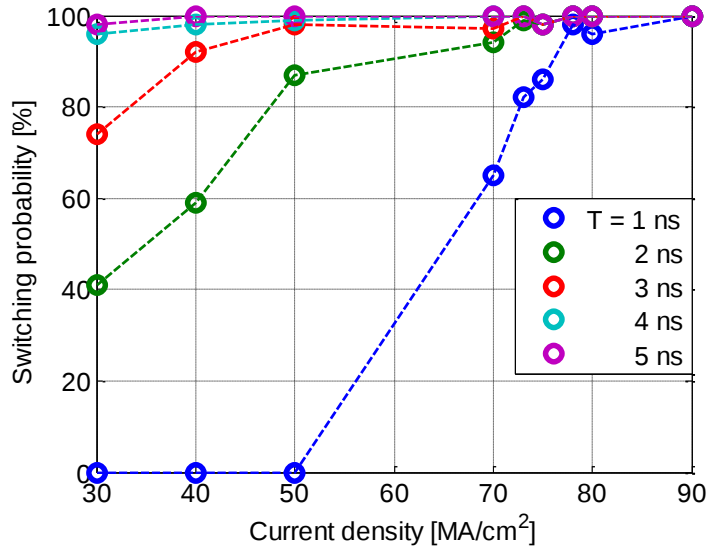


Figure 3.9 – Switching probability increases with current density and pulse width.

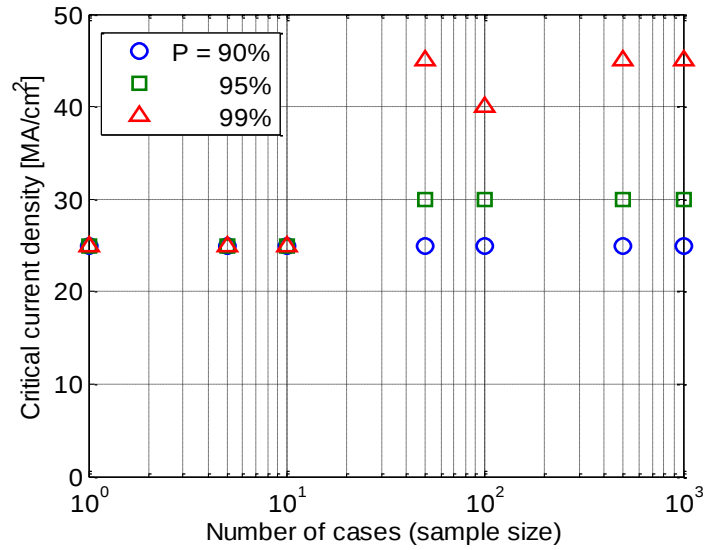


Figure 3.10 – Critical current density for 90%, 95%, and 99% probability tends to increase (or remain constant) as an increasing number of samples are considered.

3.2.3 Current Density, Domain Wall Velocity, and Switching Time

Since the magnitude of the spin-transfer torque is linear with current density, with increasing J we can expect that STT will be more efficient in moving the domain wall and the velocity of

the wall will increase. In a one-dimensional model of domain wall motion driven by STT, the velocity for large current density can be expressed as [56]

$$v = \left(\frac{1}{1 + \alpha^2} \right) \frac{g\mu_B PJ}{2eM_S} \quad (3.18)$$

where all terms were previously defined in section 3.1.1 and the direction of motion is along the direction of the electron flow. Based on this model, we can approximate the velocity of the domain wall as linear with the current density. Higher velocities equate to faster device switching, and so as with traditional logic technologies we see there is a tradeoff between energy (current density) and speed (domain wall velocity).

Figure 3.11 shows a micromagnetic simulation of the average domain wall velocity as a function of current density. We can see the linear relationship is roughly demonstrated, with a slight deviation from the 1D model. The depinning time and overall switching time of the device is shown in Figure 3.12. Both exhibit a roughly $1/J$ dependence in the simulated range of current density. The important result to take away from this is that the mCell can be expected to switch in the nanosecond regime for current densities on the order of 10^7 A/cm^2 , and not much faster. As such, the STT-mCell is not intended to be a high-performance computing device; it is too slow and cannot be made significantly faster in any energy efficient manner.

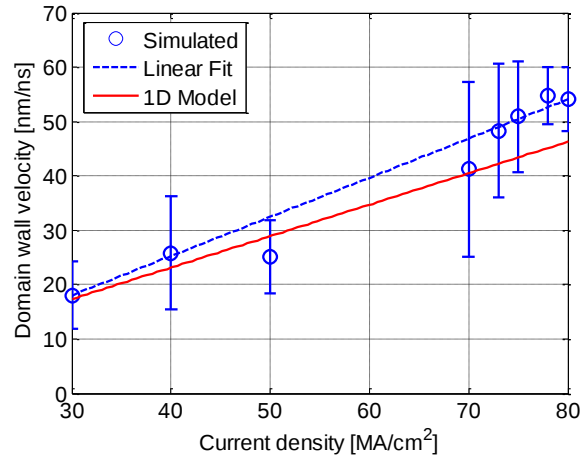


Figure 3.11 – Domain wall velocity is roughly linear with current density.

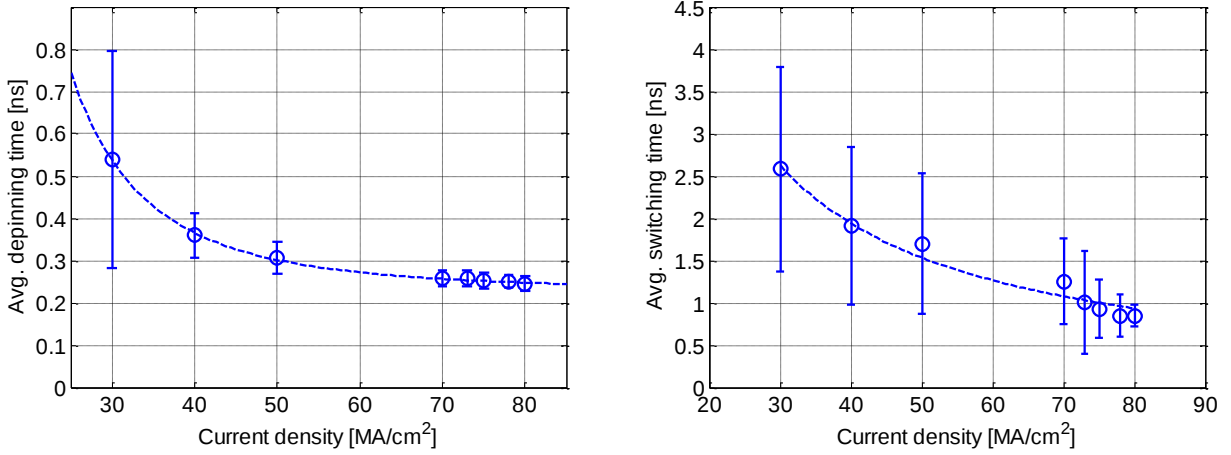


Figure 3.12 – Both the domain wall depinning time and the overall switching time of the device decrease with increasing current density according to an approximate $1/J$ dependence.

3.2.4 Write-Path Anisotropy Strength

An important parameter in the design of the mCell is the perpendicular anisotropy strength of the write-path. Referring again to equation (3.3), we see that the magnitude of the spin-transfer torque for any current density J (embedded within the velocity term $\vec{u}$) is proportional to the spatial gradient of the magnetization. With no magnetization gradient, the spin-transfer torque is zero; this is the case when the magnetized material has no domain wall present, indicating the magnetization is uniform. The presence of a domain wall implies the existence of a magnetization gradient, but it is the width of the domain wall that determines whether the magnetization gradient is small or large. Narrow walls, where the transition between up- and down- magnetization states is rapid, represent a larger magnetization gradient than wide walls where the transition takes place over a longer length. With a larger magnetization gradient, we can see that the magnitude of the spin-transfer torque for a given current density is greater than for a smaller gradient.

The width of a 180° Bloch wall, which is common for nanoscale elements with perpendicular magnetization [39] and no DMI [40]-[43] is given by

$$W_{DW} = \pi \sqrt{\frac{A}{K_u}} \quad (3.19)$$

Here again, A is the exchange stiffness of the material and K_u the uniaxial anisotropy strength. The exchange stiffness in a ferromagnetic material is a measure of the energy keeping adjacent magnetic moments parallel; large A favors domain walls that are very wide such that the difference in orientation between adjacent moments is small. The anisotropy strength, however, is a measure of the energy keeping the magnetization aligned with the easy axis. Large K_u favors narrow domain walls, such that the transition of the moments in the wall off the easy axis is kept short. We can see, then, that having a material with a large K_u will yield a narrow domain wall and as a result, a large magnetization gradient (Figure 3.13).

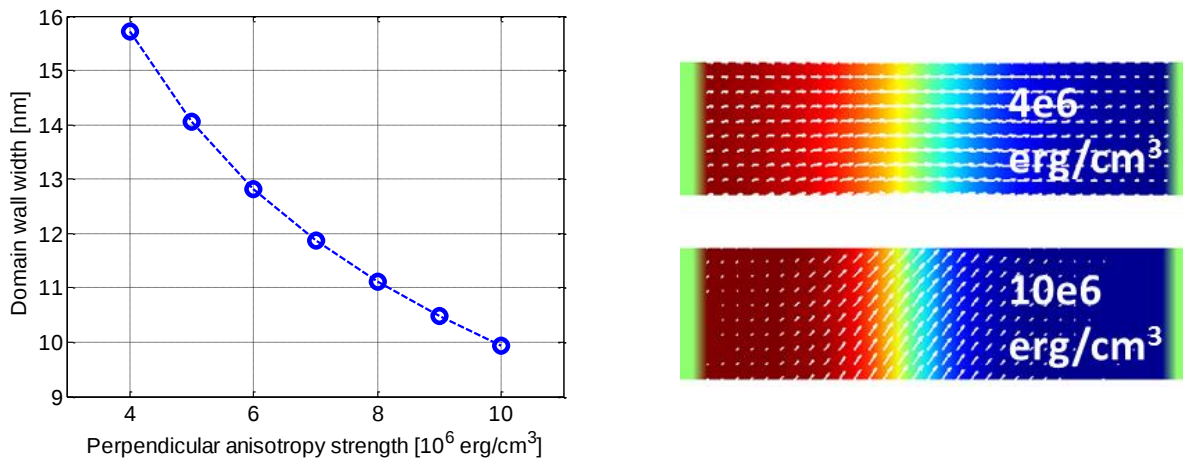


Figure 3.13 – (left) Domain wall width decreases with increasing anisotropy strength, leading to increasing magnetization gradients; (right) micromagnetic simulation showing narrowing of domain wall for higher K_u .

Figure 3.14 shows how the critical current density varies as a function of anisotropy strength. We see that as K_u increases, the current density required to free the domain wall decreases on average. This decrease can be attributed to a proportional increase in magnetization gradient for the higher anisotropy materials. The reduction in current density appears to level off as the anisotropy strength becomes very large; this may indicate a balance between efficient STT and a larger energy barrier, which is also proportional to the write-path anisotropy. In any case, it appears to be preferable to build an STT-mCell write-path from a material with a strong perpendicular anisotropy.

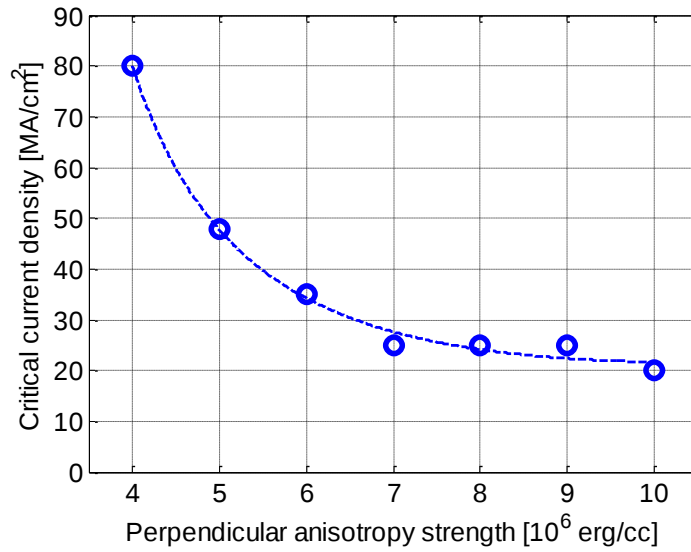


Figure 3.14 – Critical current density decreases with increasing anisotropy strength.

3.2.5 Write-Path Thickness

Because the energy barrier to domain wall motion is determined by the step height formed by the coupling layer and the read-path, the thickness of the write-path does not affect it. Increasing the thickness of the write-path, however, does increase the cross-section and overall volume of magnetization that must be switched. Even if the critical current density remains the same, then, higher currents would be required to maintain that current density.

Making the write-path thicker, however, could lead to reduced threshold current densities. The way the write operation works in an mCell is by driving a domain wall in the write-path and relying on coupling to switch the read-path. If the write-path, coupling layer, and read-path are each 1 nm thick, that means only 1/3 of the total domain wall height is actually being driven by current; the rest is moving just due to coupling. If the write-path is made to be 2 nm thick, then that brings the fraction of driven material up to 1/2. This effect may serve to reduce the required current densities, because it effectively reduces the coupled load on the write-path.

The simulation results in Figure 3.15(a) show that as write-path thickness increases in a range of 1-3 nm, the critical current density tends to decrease. When the write-path thickness is further increased, the critical current density is observed to be larger. It is possible that additional simulations are necessary to smooth out the curve, or that thicker write-paths introduce other behavior that makes switching more difficult (such as changes in wall structure due to a

difference in demagnetization energies).

That said, Figure 3.15(b) shows that on average the critical current actually increases with increasing write-path thickness. Thinner write-paths, therefore, may be preferable despite having decreased coupling to the read-path (assuming the resistance of the write-path, which also includes under-/capping-layers and contacts, remains about the same or increases slower than the thickness decreases). In reality, however, additional concerns on device stability set a limit on the minimum thickness of the write-path. These issues are addressed in the following sections on the coupling layer and in the following chapters detailing experimental efforts to realize this device.

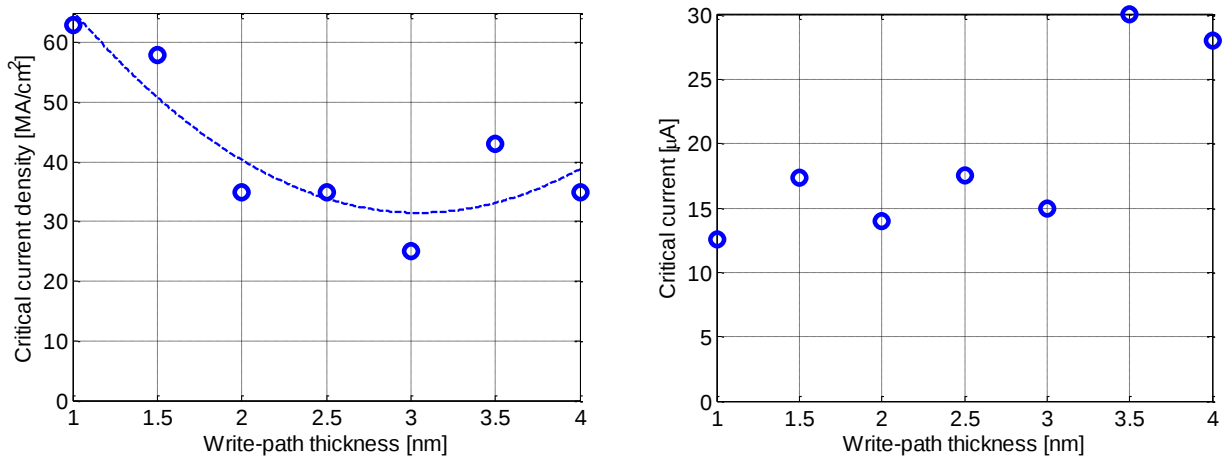


Figure 3.15 – (left) Critical current density is a non-monotonic function of write-path thickness, decreasing with increasing write-path thickness before taking a turn as the write-path goes thicker than 3 nm; (right) Absolute current requirement increases with write-path thickness on average.

3.2.6 Write/Read-Path Coupling Layer Thickness

Unlike the thickness of the write-path, increasing the thickness of the coupling layer does not serve to reduce the required current density. By making this material thicker, we are in effect increasing the “load” on the write-path, as the domain wall has to be pushed through a greater volume despite only being driven by current in the write-path itself. The thickness of the step that helps set the energy barrier also increases. Figure 3.16 shows a micromagnetic simulation of this, where the thickness of the coupling material is increased as the write-path thickness is held constant at 3 nm and the coupling strength at 10^{-6} erg/cm.

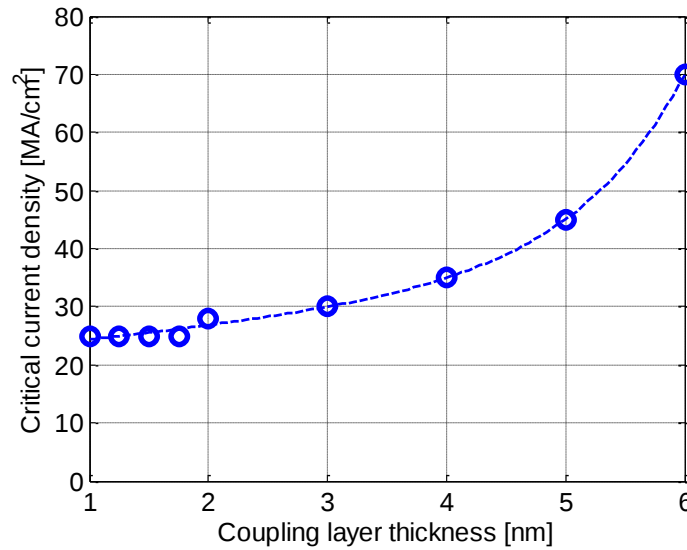


Figure 3.16 – Threshold current density is immune to changes in coupling layer thickness as long as the layer is kept relatively thin, and then increases exponentially as the layer becomes thick (assuming a constant exchange strength).

The design of the mCell does not require the coupling layer to be overly thick. Magnetically, it is preferable to have as thin a layer as possible to maintain strong coupling between the write- and read-paths. Alone, the coupling material (e.g., some magnetic oxide) is not perpendicular, and so if it is too thick it will not adequately couple the perpendicular materials on either side. The anisotropy strength of the write- and read-paths was set to be large for the simulations captured in Figure 3.16 ($K_u = 8e6 \text{ erg/cm}^3$); for slightly smaller values of K_u ($5e6 \text{ erg/cm}^3$), the bulk of the magnetization goes in-plane for thick (e.g., $> 2.5 \text{ nm}$) coupling layers (Figure 3.17). Electrically, however, it is desirable to have a thick coupling layer, which will yield a greater resistance (particularly if the conduction mechanism is tunneling). As such, a compromise must be set between good magnetic properties and good electrical properties, which will most likely lie between 1 and 2 nm. As shown in Figure 3.16, the critical current density does not fluctuate much in this thickness region, and therefore not much is lost from that standpoint.

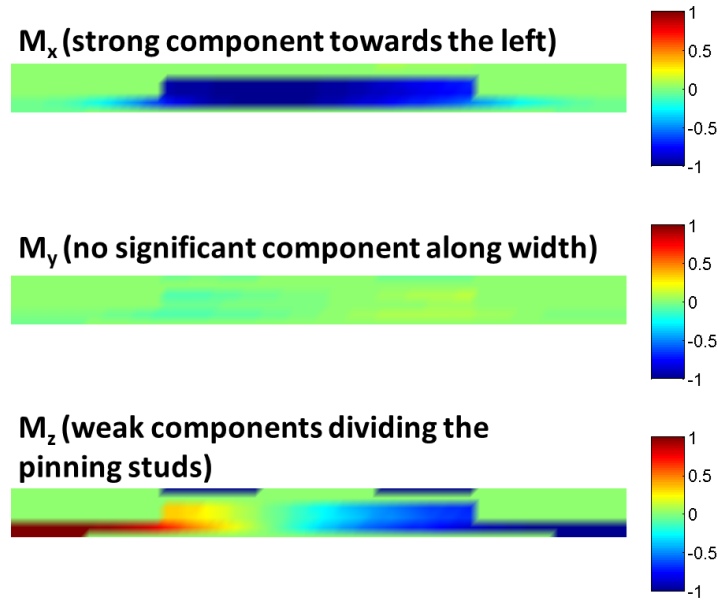


Figure 3.17 – Magnetization components of mCell for a thick coupling layer when the write-path anisotropy is $5e6$ erg/cm³. The magnetization tends to be forced in-plane due to the coupling layer’s demagnetization outweighing the perpendicular anisotropy.

3.2.7 Write/Read-Path Coupling Layer Interlayer Exchange Strength

In the previous section, the importance of coupling strength was discussed in the context of keeping the coupling interlayer thin. In Figure 3.16, the coupling strength was held constant at 10^{-6} erg/cm; Figure 3.18 shows that the coupling strength does not have an effect on the required switching current density, so long as the material is kept thin (1 nm in this simulation). Any exchange coupling, even if small, helps stabilize the magnetization state of the device and allow for smooth wall motion and switching. This is a good result from a materials standpoint, as it relaxes the coupling strength requirements on the coupling material. With only small coupling required, more materials (that are perhaps good insulators but not strong couplers) can be considered.

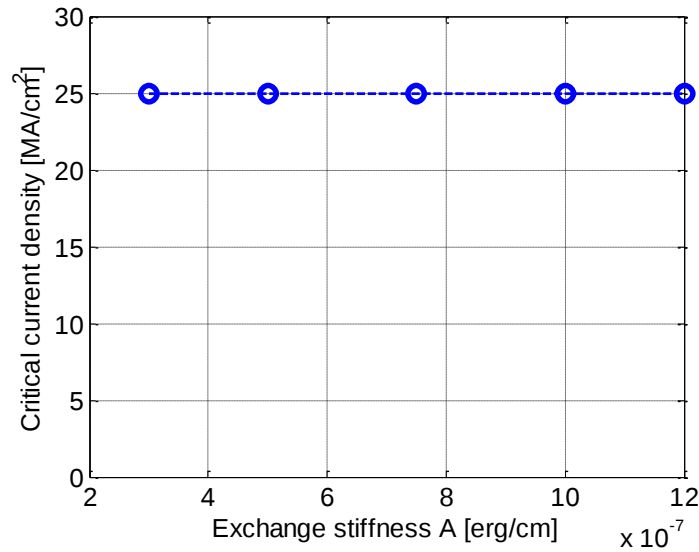


Figure 3.18 – Critical current density is not strongly dependent upon exchange stiffness.

An interesting question to consider is whether the exchange coupling is required at all, given that it does not have to be very strong. Pure dipolar coupling through a non-magnetic insulating material would yield the same result, with the read-path free layer magnetization aligning parallel to that of the write-path to maximize flux closure and minimize magnetostatic energy. However, micromagnetic simulation indicates dipolar coupling alone is not strong enough to reliably switch the mCell. With exchange coupling, the domain wall moves through the write-path and read-path in tandem (Figure 3.19 top), but without exchange the read-path magnetization does not switch with the write-path (Figure 3.19 middle). If the anisotropy strength of the read-path free layer is decreased, the material becomes easier to switch and dipolar coupling can in fact couple it to the write-path, but at the sacrifice of stability (Figure 3.19 bottom).

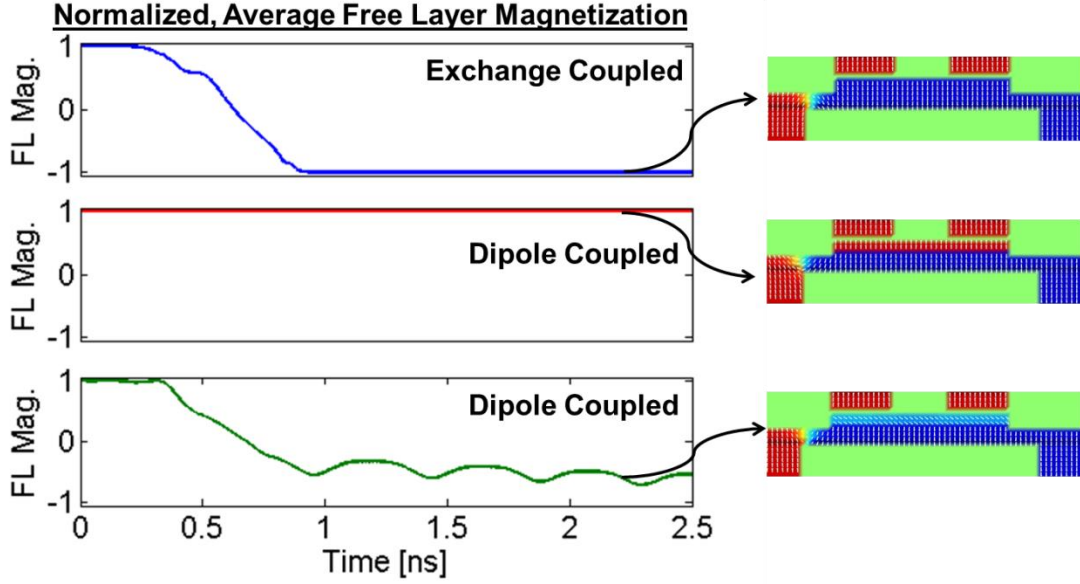


Figure 3.19 – Exchange coupling allows for reliable switching of the read-path along with the write-path (top); dipolar coupling fails to couple the read-path magnetization to the write-path’s during switching (middle); reducing the anisotropy strength of the read-path allows dipolar coupling to suffice, but greatly reduces the stability of the state.

3.2.8 Non-adiabaticity Factor β

The basic principle of STT-based domain wall motion was described in section 3.1.1. Theoretical and experimental work in the area [26],[57]-[61] led to an expanded theory on spin-transfer torque in domain walls, namely a “non-adiabatic” torque that can be added to the LLG equation (Eqn. (3.10)):

$$\frac{\partial \vec{M}}{\partial t} = \frac{\beta}{M_s} \hat{M} \times (\vec{u} \cdot \vec{\nabla}) \vec{M} \quad (3.20)$$

Physically, this term represents a “mis-alignment” in the spin of a conduction electron in the magnetic material. The essence of STT is the alignment of conduction spin with local spin, which generates a torque used to rotate the local spin. When the magnetization gradient is high, as can occur in perpendicular materials with a strong anisotropy, a fraction of the conduction spins are not re-oriented instantaneously, an effect that can be thought of classically as a lag. The magnitude of that fraction is represented by β in equation (3.20), and can affect both threshold current density and wall velocity. Incorporating the non-adiabatic torque into the one-dimensional model of wall velocity scales equation (3.18) by $(1 + \alpha\beta)$.

The effect of varying β is shown in Figure 3.20. The critical current density tends to increase with increasing non-adiabatic torque strength as the wall speed slightly increases for a fixed current density. Since the β term is scaled by $\alpha = 0.015$ in the 1D model of velocity, the velocity appears flat but is actually increasing very slightly; this occurs when the domain wall moves by precessional propagation [26]. We can interpret these results to mean that the presence of a non-adiabatic torque in the mCell is not a major factor in device performance (energy or speed) when relevant current densities are used to switch the device.

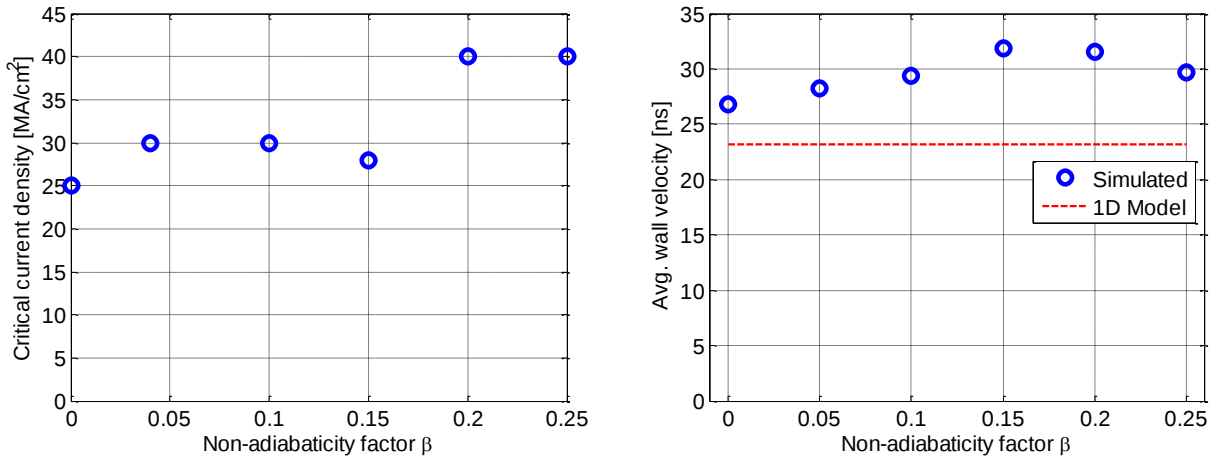


Figure 3.20 – (left) Threshold current density as a function of non-adiabatic torque strength; (right) average wall velocity as a function of non-adiabatic torque strength for a fixed current density of 40 MA/cm².

3.2.9 Device Size and Scaling

An important question to consider regarding mCells is their ability to scale, physically and in terms of energy and speed. Theoretically, an mCell can be made quite small; the energy barrier issues that affect MRAM are less of a problem here because the energy barrier is set by the domain wall “step” inherent to the design.

The primary concern with fabricating scaled mCells is being able to define two MTJs in the read-path without significant damage or sidewall residue that could destroy the TMR and/or RA. Additionally, there must be enough space outside the MTJs, between an MTJ and the write-path pinning electrode, to contain a domain wall. Luckily, materials with strong perpendicular anisotropy promote narrow domain walls, and so this space can be as small as 8-10 nm on either side. Assuming an MTJ can eventually be patterned to be 10 nm in length with 15 nm pitch, the overall length of an mCell may be as small as 65 nm. Although the length of the device does not impact the energy barrier, it does have some impact on the critical current, depending on the

definition of critical current being used. The switching speed of the device is determined by the domain wall velocity; the further the domain wall has to travel, the longer the switching time. As a result, a level of current that yields complete switching in 2 ns may not allow for complete switching in 1 ns. The domain wall may be left somewhere in the middle of the device. As the device scales in length, of course, the required current to switch in a given amount of time decreases; if the length is scaled by α ($\alpha < 1$), the switching time is scaled by α for the same current. A smaller current may also yield the same switching time if the increase in depinning time does not offset the decrease in wall travel time. A shorter device length also reduces the resistance of the write-path by α , which is helpful in reducing fanout load.

Changing the width of the device directly impacts the energy barrier, as well as the current density. Micromagnetic simulation indicates the critical current density does not vary appreciably as a function of width (Figure 3.21, left) for narrow devices. Of course, to maintain the same current density as the width gets larger, additional current needs to be applied (Figure 3.21, right). The trend is approximately linear, with a slope of one. A device with a current requirement of I scaled in width by β ($\beta < 1$) therefore requires βI of current to switch in the same time period. Assuming fabrication techniques improve to allow patterning of magnetic tracks at extremely narrow widths with low edge roughness, mCells can be made to be 10 nm wide, or even narrower, and still maintain a sufficient energy barrier due to the “step” and use of high K_u materials.

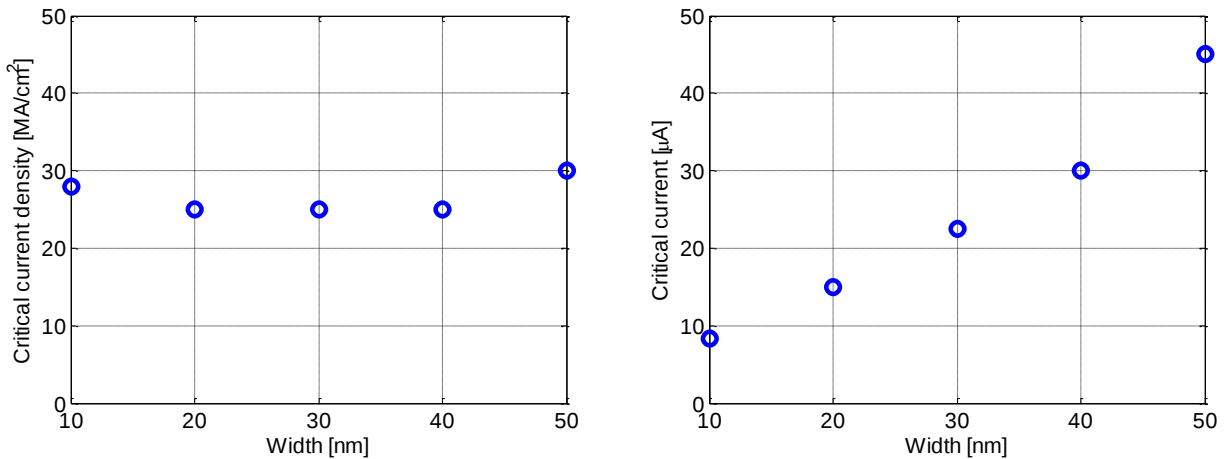


Figure 3.21 – (left) Threshold current density does not vary substantially as a function of device width; (right) absolute threshold current, however, decreases as the device is scaled in width.

3.3 SHEDW-mCell Device Design and Modeling

The SHEDW-mCell (Figure 3.22) device structure is essentially identical to the STT-mCell design. The write-path consists of a magnetic layer switched by current-driven domain wall motion. This can be a Co/Ni multilayer with a Pt underlayer, such as that used in Chapters 5-6. The write-path is magnetically coupled to a read-path free layer through an electrically insulating magnetic material. The read-path free layer forms two MTJs in series.

The only major difference in this device is that the write current ideally flows through the non-magnetic underlayer (not shown specifically) and not the write-path magnetic layer. This allows for maximum switching efficiency; current flow in the magnetic layer is essentially shunted and wasted. Additionally, the domain wall in this device must be of a chiral Néel type, as mentioned in section 3.1.2. Materials engineered to have a sizable Dzyaloshinskii-Moriya interaction are preferable to ensure a chiral Néel wall exists. Although the domain wall energy takes a different mathematical form compared to equation (3.16), it is still proportional to the cross-sectional area and so the “step” in the write-path still establishes an energy barrier that defines stable states.

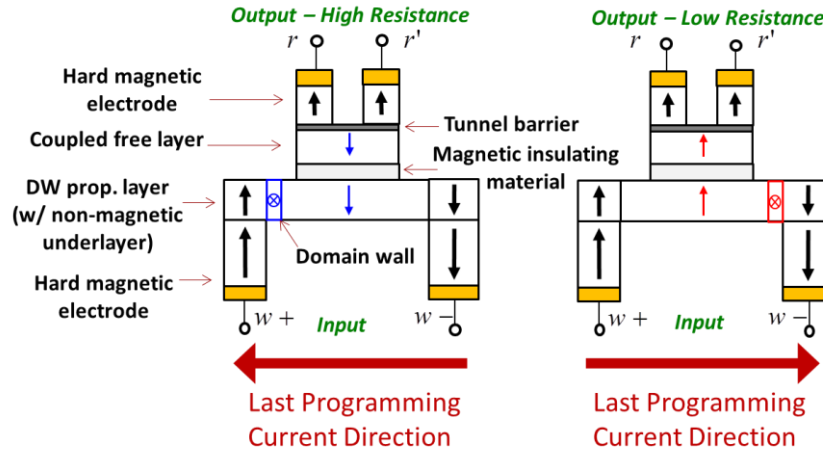


Figure 3.22 – Cross-section of DW-mCell driven by the SHE.

3.3.1 State Switching Process

Micromagnetic simulation of current-driven state switching is shown in Figure 3.23. At $t=0$, the magnetization of the write-path is initialized parallel to the read-path electrodes (low

resistance state). A conventional current is then applied along the $+\hat{x}$ -direction, from left to right in the figure. The domain wall is freed from its initial position and swept across the write-path by the SHE; note that as the domain wall moves, the free layer in the read-path switches in tandem. At the end of the simulation, the domain wall is on the other side of the device, with the magnetization now oriented antiparallel to the read-path electrodes (high resistance state).

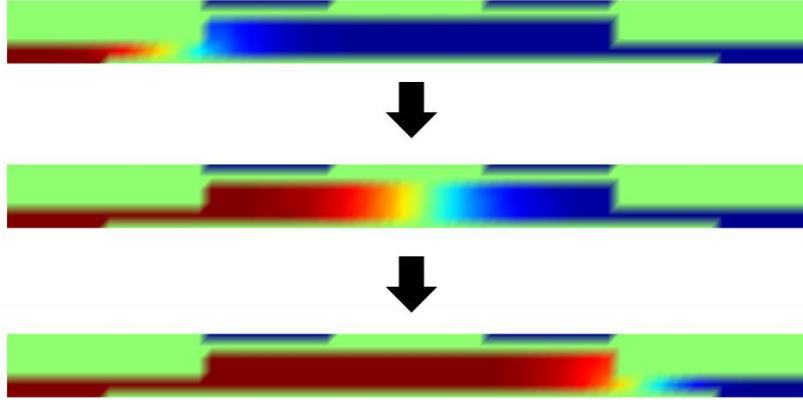


Figure 3.23 – Micromagnetic simulation of SHE-DWM-based state switching.

Similar to the case in Figure 3.8 for the STT-mCell, the step in the write-path that increases domain wall height establishes an energy barrier to switching (Figure 3.24). The energy barrier can be tuned by the same parameters as before, namely the perpendicular anisotropy strength, step height, and device width. As discussed in section 3.3.4, the domain wall velocity in this device can be quite high. This explains why the high energy state in Figure 3.24 is so narrow compared to that in Figure 3.8.

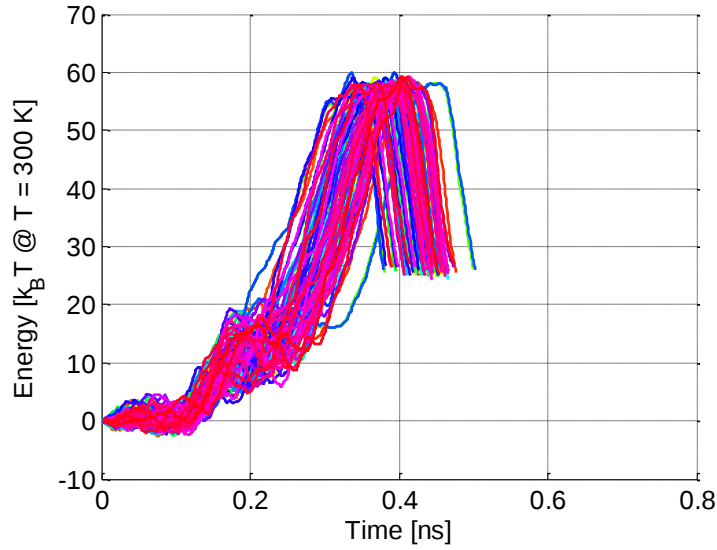


Figure 3.24 – An energy barrier must be overcome for the domain wall to travel across the write-path and switch the device due to the increase in wall height.

3.3.2 Domain Wall Motion Direction

The domain wall structure and chirality is determined by the DMI in the micromagnetic simulations. In turn, this determines the direction of domain wall motion in combination with the current direction and spin Hall angle (θ_{SH}). Table 3-II gives the direction of domain wall motion for different current and effective DMI field directions and the sign of θ_{SH} . The simulations presented in later sections all incorporate a positive spin Hall angle and effective DMI field in the $+\hat{x}$ -direction. This most closely matches the physical reality of the experiments we conducted with Pt/[Co/Ni]₂/Co/Ta structures detailed in later chapters.

Table 3-II – Direction of domain wall motion for different combinations of current direction, spin Hall angle, and wall chirality.

Current Direction	Spin Hall Angle	DMI Direction	DWM Direction
$+\hat{x}$	+	$+\hat{x}$	$+\hat{x}$
$+\hat{x}$	+	$-\hat{x}$	$-\hat{x}$
$+\hat{x}$	-	$+\hat{x}$	$-\hat{x}$
$+\hat{x}$	-	$-\hat{x}$	$+\hat{x}$
$-\hat{x}$	+	$+\hat{x}$	$-\hat{x}$

$-\hat{x}$	+	$-\hat{x}$	$+\hat{x}$
$-\hat{x}$	-	$+\hat{x}$	$+\hat{x}$
$-\hat{x}$	-	$-\hat{x}$	$-\hat{x}$

3.3.3 Switching Probability

Domain wall depinning is stochastic regardless of what phenomenon is used to instigate the process. It is therefore not surprising that switching is probabilistic in a SHE-based domain wall device as well. Figure 3.25 shows a trend much like that for the STT-mCell in Figure 3.9, where increasing the current density and/or pulse width increases the probability that a device will switch successfully. It is worth noting that the probability of correct switching for smaller current densities in this SHE-based device is lower than the corresponding probability in the STT-based device. As we will see in the following section, the SHEDW-mCell does not appear to have as low a threshold current density as the STT-mCell, but it does switch faster.

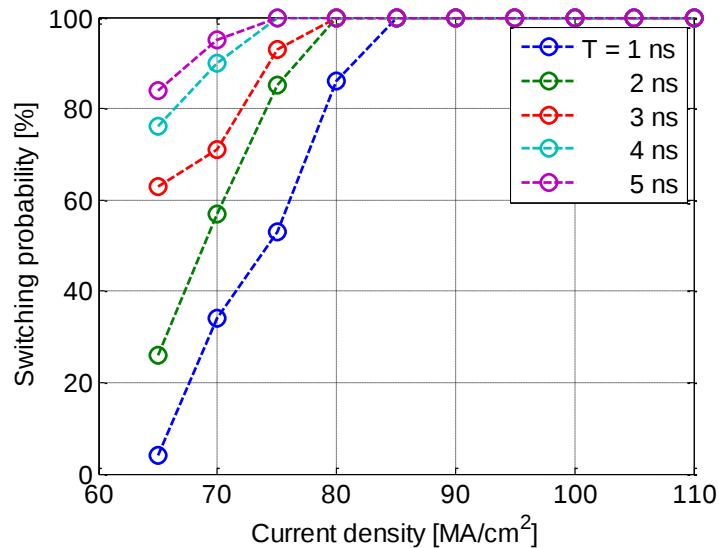


Figure 3.25 – Switching probability increases with current density and pulse width.

3.3.4 Current Density, Domain Wall Velocity, and Switching Time

Because the SHE torque term (equation (3.4)) is linear with current density, it is reasonable to assume the domain velocity is as well. This was the case in the STT-based device. From Figure 3.26, we see that the velocity does fit a line fairly well (up to a saturating limit), but with a slope greater than one. This fast increase allows the device to switch at higher speeds than the

STT-mCell, even though it starts out with a lower velocity (the velocity at 70 MA/cm² is twice as large in the STT device, but by 80 MA/cm² the velocities are the same and then higher in the SHEDW-mCell). Aside from the velocity, there is also a decrease in domain wall depinning time (Figure 3.27, left) compared to the STT-mCell. The higher velocity and faster depinning lead to overall faster switching (Figure 3.27, right). These sub-ns switching times are difficult to achieve in the STT-mCell. This SHE-based device may be better suited for applications that require higher performance at the expense of increased energy.

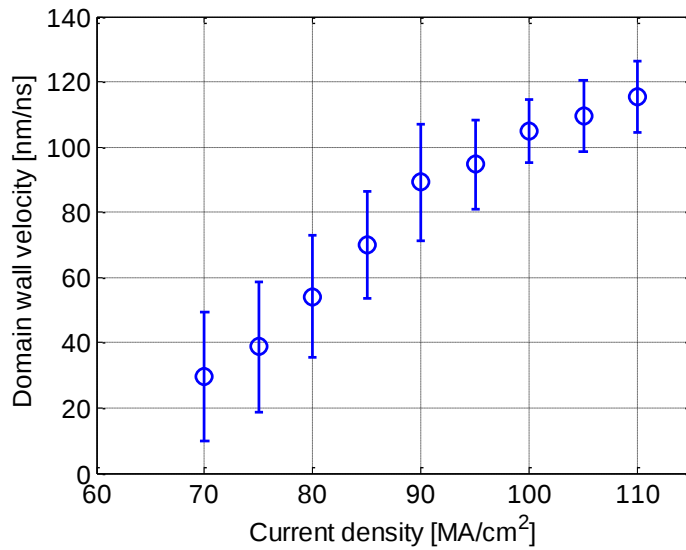


Figure 3.26 – Velocity of domain wall driven by the SHE is approximately linear with current density before leveling off.

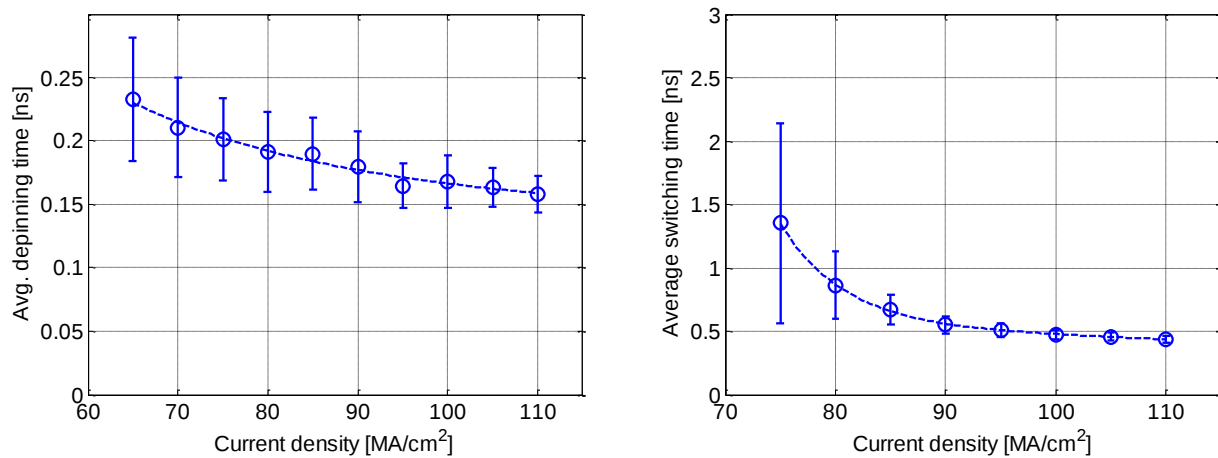


Figure 3.27 – (left) Domain wall depinning time decreases with increasing current density according to an approximate 1/J dependence; (right) overall switching time of the device decreases with increasing current density, but tends to saturate at high currents.

3.3.5 Write-Path Thickness

For the STT-mCell we observed in simulation that as the write-path becomes thicker the required current density decreases but the required current itself increases (Figure 3.15). As shown in Figure 3.28, this trend is also observed in the SHE-DWM mCell. Having a thin write-path is preferable for another reason as well. The SHE arises due to current flow in the non-magnetic under-layer, and so by having a thinner magnetic layer we can ensure not too much current is shunted away from the underlayer. And given that the SHE is really an interface effect, where spin accumulates at the interface between the under-layer and magnetic layer, we want the thickness of the magnetic layer to be thin so what happens at the interface is still a major factor in controlling the magnetization dynamics. Of course, the considerations in section 3.2.6 regarding magnetic insulator thickness must be kept in mind here as well. A write-path that is too thin may not be adequately coupled to the read-path due to the instability of the perpendicular magnetization of the magnetic insulator.

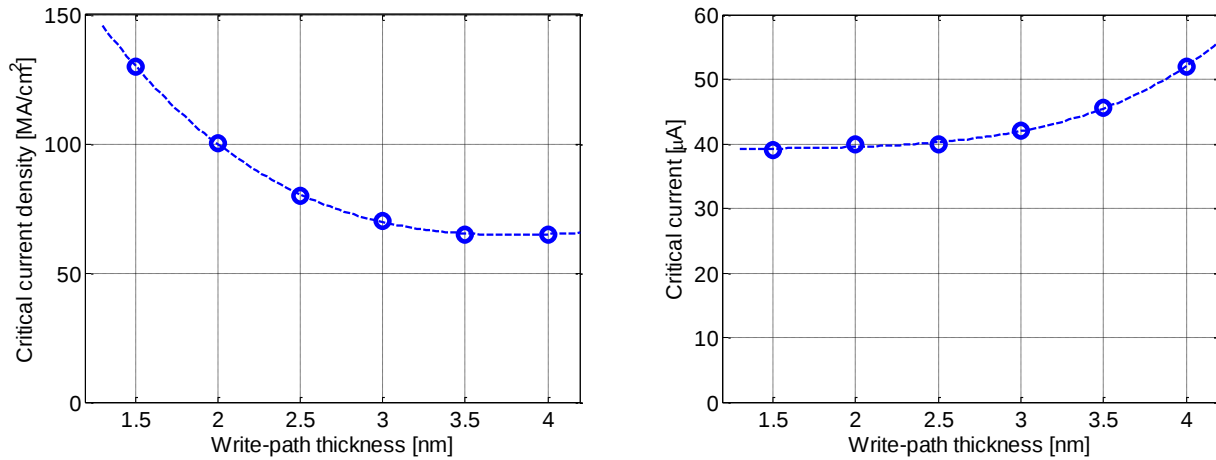


Figure 3.28– (left) Threshold current density decreases as the write-path becomes thicker; (right) Absolute critical current tends to increase as the write-path becomes thicker.

3.3.6 Write-Path Saturation Magnetization

Another factor to consider is that the SHE torque is in effect “weaker” when acting on materials with large M_s , as described by equation (3.4). Figure 3.29 shows a micromagnetic simulation indicating that for a sufficient perpendicular anisotropy ($K_u = 8\text{e}6 \text{ erg/cm}^3$, which places the average energy barrier at about $80 \text{ k}_B\text{T}$ at room temperature for a device 20 nm wide),

the critical current density does not vary appreciably with M_s in a reasonable range. A value of 800 emu/cm³ is roughly the same as that for saturation magnetization in the Co/Ni nanowires that will be discussed in Chapters 5 and 6.

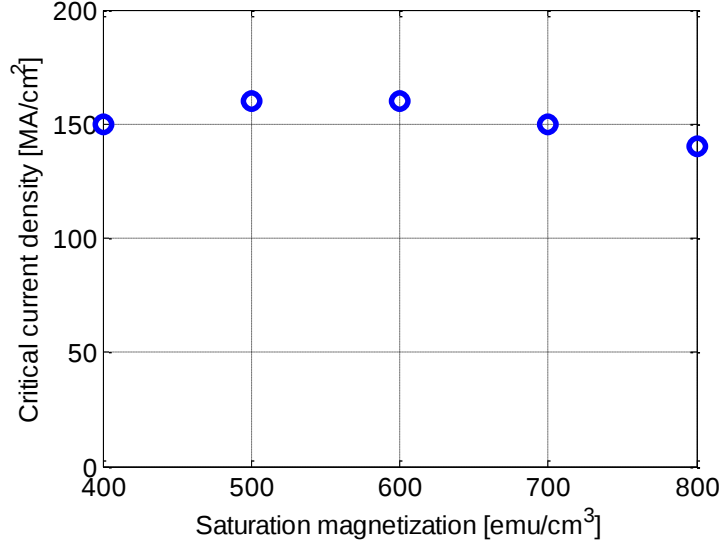


Figure 3.29 – Critical current density is not a strong function of write-path saturation magnetization in the simulated range.

3.3.7 Write-Path Perpendicular Anisotropy Strength

As discussed in Section 3.2.4 the anisotropy strength plays an important role in the STT-driven device. This is because STT-DWM is based on the presence and magnitude of a magnetization gradient, and the domain wall width is proportional to the anisotropy. The SHE torque, however, is not proportional to a gradient in magnetization. It is a Slonczewski-type injection torque that arises from current flow in the non-magnetic underlayer. Increasing the anisotropy strength of the write-path does nothing to the torque itself, but it does increase the energy barrier. It is therefore expected that unlike in the STT-mCell, a lower anisotropy write-path is preferred for the SHE-based DW-mCell. This is confirmed by micromagnetic simulation (Figure 3.30), which shows the critical current density is smaller for lower values of K_u . Of course, K_u must be kept large enough such that a sufficient energy barrier is present to ensure state stability.

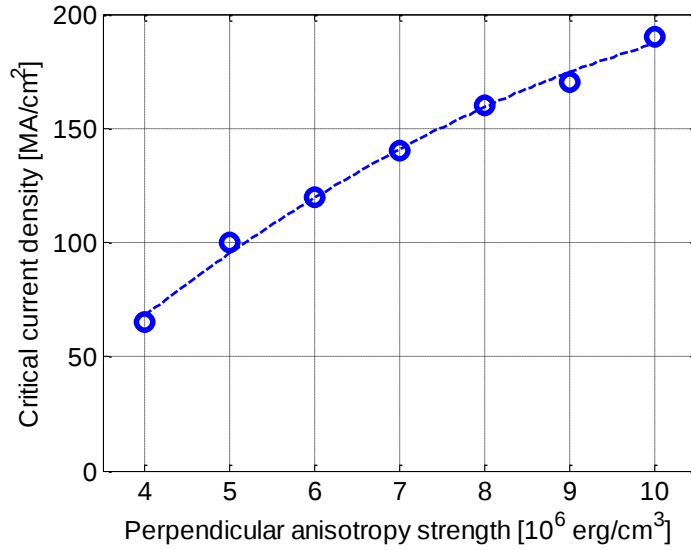


Figure 3.30 – Threshold current density increases as a function of write-path anisotropy.

3.3.8 Device Size and Scaling

Because this device is the same as the STT-mCell in all respects except for the driving force, it faces the same scaling challenges in virtually the same fabrication process. The domain wall pinning studs must be fabricated, and there must be a region between a write-path stud and the read-path step long enough to contain a domain wall. Additionally, the edge roughness along the sides of the device must be minimized to eliminate domain wall pinning everywhere along the write-path. Minimizing the length of the device has the same benefits of reducing write-path resistance (the fanout load on a driving gate) and shortening domain wall travel distance.

Desirable scaling behavior would show critical current density remaining constant or decreasing as a function of width. Either of these would lead to a reduction in required current (and therefore, pClock voltage) as devices get smaller. Figure 3.31 shows that like in the STT-mCell, the critical current density in this device is roughly constant with device width. As a result, the critical current scales linearly with device width. An important thing to notice in Figure 3.31 as compared to Figure 3.21 (the STT-mCell scaling results) is that the current density is considerably larger. As discussed in section 3.3.4, this device does not seem to offer the low current operation of the STT-mCell; it does, however, offer faster switching.

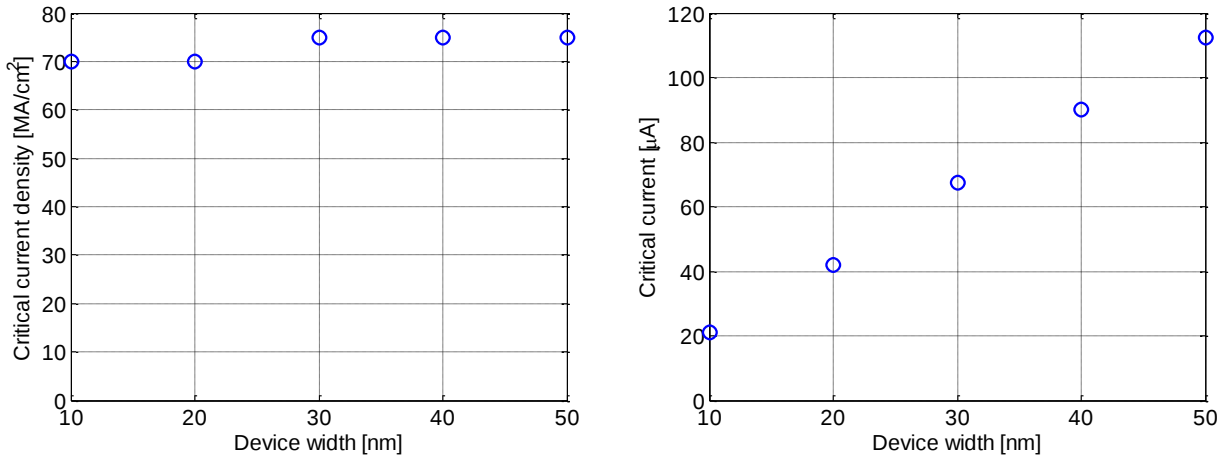


Figure 3.31 – (left) Threshold current density is approximately constant for device widths of 10-50 nm; (right) Absolute critical current scales linearly with device width.

3.4 Conclusions

In this chapter we explored the design and modeling of two magnetic logic devices with the same 4-terminal black box model. In one device, an input current moves a magnetic domain wall by spin-transfer torque to switch the perpendicular magnetization state of a write-path that is magnetically coupled to a free layer in an MTJ-based read-path, yielding high or low resistance states. The other device works much the same way, but the input current moves the domain wall by the spin Hall effect. Micromagnetic modeling demonstrated both devices can be switched reliably and can be designed to have a sufficient energy barrier. Although the specific simulation results presented in this chapter are dependent on the parameters and simulation techniques used, they are meant to indicate performance trends as material properties and device geometry vary. The modeling results of this chapter leave us with the following lessons:

- Switching currents below 50 μA are easily achievable in scaled devices. Sub-10-20 μA switching currents are also achievable for specific design choices, especially in the STT-mCell (see following points).
- Switching times of 1-5 ns are easily achievable in scaled devices, even at the critical current. There is an unsurprising trade-off between energy and performance, and so applying higher currents (i.e., larger pClock signals) increases the switching speed of the devices with a roughly $1/J$ relationship.
- The SHE-based device is capable of achieving sub-1 ns switching times at lower current

density than the STT device, but the critical current density tends to be larger. The STT-mCell may be a better choice for low power applications and the SHEDW-mCell a better choice for higher performance applications.

- If the insulating coupling layer is kept thin (e.g., 1-2 nm), its exchange coupling strength does not need to be large (i.e., full ferromagnetic coupling). However, dipolar coupling alone is not enough to ensure reliable state switching. Making the insulating layer too thick overcomes the required perpendicular anisotropy.
- It is possible to margin the current pulse (magnitude and width) to ensure a high probability of switching. Additional simulations are necessary to see how the distributions change from the ones in this chapter (e.g., upwards of $1e5$ trials instead of 100 per set of inputs). The absolute pClock requirements for mLogic can only be determined by the application. Some applications in which probabilistic switching can be exploited rather than avoided are discussed in the final chapter of this thesis.

These trends will ideally guide physical experiments to converge on functional, efficient devices. These experimental efforts will be discussed in detail in later chapters.

4 Four-Terminal Single Domain Device

In this chapter we introduce the concept and structure of a possible mCell logic device that does not include a domain wall. The conceptual mCell model introduced in Chapter 2 requires a direction of current through a write-path to switch the resistance state in a separate read-path; it does not fundamentally require a domain wall to be present. A single domain device may provide several advantages over a domain wall-based device. No write-path spinning studs would be required, which would greatly reduce fabrication complexity. It is also possible that a single domain device may switch faster since it is not limited by the domain wall travel time. Here we explore micromagnetic simulation of a single domain to evaluate its performance. The switching mechanism is the spin Hall effect described in the previous chapter, but in this device the magnetization lies in the plane of the film.

4.1 In-Plane Single Domain mCell (SHE-mCell)

Figure 4.1 shows a 3D representation of an mCell with a spin Hall effect-based switching mechanism. Like the mCells in the previous chapter, a read-path consisting of two magnetic tunnel junctions (MTJs) is formed between (r, r') and a write-path between (w^+, w^-) . In this device, however, the write-path is comprised of a magnetic layer with in-plane magnetization sandwiched between normal metal or oxide interfaces (e.g., Pt/Co/AlO_x, Ta/CoFeB/MgO); note that only one of these interfaces is shown specifically, between a non-magnetic underlayer and the magnetic material. The other interfaces, which may include under-, seed-, and/or capping-layers, are implied. The write-path magnetization couples to a free magnetic layer in the read-path through an electrically-insulating magnetic material, the same material that is required for the STT-mCell. The orientation of this layer's magnetization determines the resistance between (r, r') . A synthetic antiferromagnetic (SAF) layer is used to pin the reference layers of the MTJs. The device is non-volatile and retains its resistance (or logic) state even when no power is applied. Note that in the drawing the non-magnetic underlayer “expands” under the device, patterned to match the magnetic write-path in the figure, but can just as easily be designed to always be as wide as the ellipse major axis.

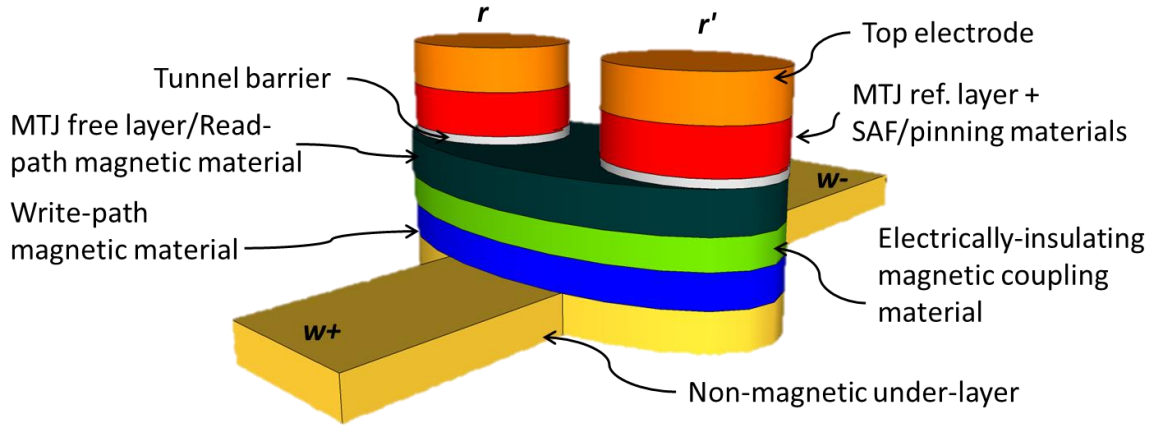


Figure 4.1 -- 3D view of four-terminal SHE-mCell logic device. (r , r') form a read-path, while (w^+ , w^-) form an electrically-insulated but magnetically-coupled write-path.s

Because the direction of the current determines the sign of the SHE torque (equation (3.4)), this device has the same “black box” representation as the domain wall-based mCells: the current direction through the write-path will switch the magnetization of the device one way or the other, yielding a low- or high-resistance state. The elliptical shape of the magnetic layers in Figure 4.1 is required to induce a shape anisotropy that helps keep the magnetization direction stable in steady state, orthogonal to the direction of the current flow in the write-path (rectangular shapes are also possible, but not necessarily preferable due to edge effects at corners). The MTJs in the read-path are also patterned into ellipses, but the SAF is the key in keeping the reference layers stable. The aspect ratio of the ellipse, in addition to the overall volume and other material properties, determines the switching energy barrier that keeps the device non-volatile and stable. In the previous chapter on the domain wall devices, the issue of the energy barrier was largely ignored, because the device design (perpendicular anisotropy plus the write-path “step”) makes it simple to establish a sufficiently large barrier. Establishing a suitable energy barrier in this device is less straightforward.

As we have discussed, thermal energy acts on the magnetic moment of a material at any non-zero temperature. This thermal energy can potentially cause instability in the stored state of a magnetic device, such as (any variant of) the mCell. In the hard disk drive industry, it is generally accepted that the minimum energy barrier to magnetization reversal is 40-50 $k_B T$ to maintain state storage over a period of ten years [62]. This is shown in Figure 4.2, which plots the exponential rise in thermal stability as a function of energy barrier [63].

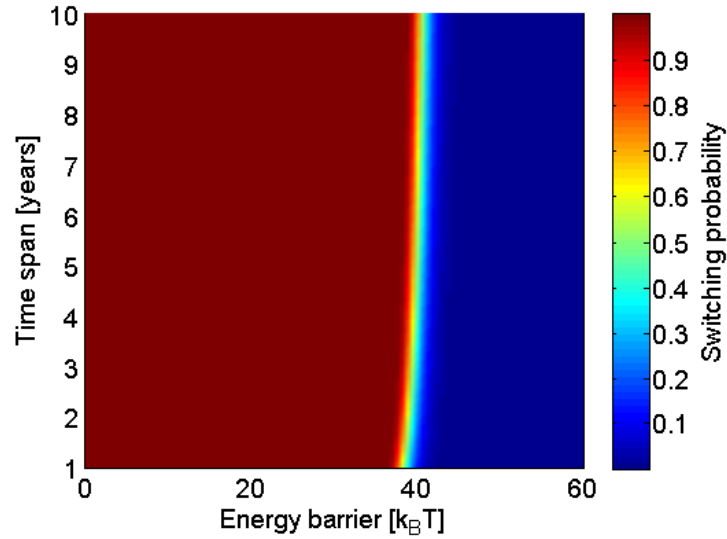


Figure 4.2 – Thermal switching probability at room temperature sharply reduces when the energy barrier of a magnetic element reaches roughly $40 k_B T$.

However, what works for hard drives does not necessarily work for mLogic. The data bits stored on a hard drive consist of a number of magnetic grains; if some of them erroneously switch due to thermal agitation, the data is not lost. Additionally, bits are sensed only when transitions in magnetization along the track are detected. As such, lower energy barriers may be used without causing data corruption. For mLogic (and MRAM), the logic state of a device is stored within one magnetic element, but millions of devices may exist on a chip. If the overall product is to be truly non-volatile over a specified time, the thermal switching probability of a given device must be sufficiently small that the aggregate probability of all the devices staying stable remains high. This typically raises the energy barrier to at least $60 k_B T$ depending on the array size (e.g., one million versus one billion devices) and desired retention time (e.g., one year versus ten years) [63]. For the purposes of this thesis, we will generally consider an energy barrier of $55 k_B T$ to be suitable. The actual energy barrier requirement is likely to be determined by the application, as it is not necessary that the devices maintain their states for years in most logic (and some memory) applications.

4.1.1 State Switching Process

The same simulation tool introduced in the previous chapter is utilized here to characterize

the SHE-mCell. Much like the previous simulation experiments, a default set of device parameters are used with the exception of a given parameter being swept. The results here and in following sections are meant to show trends, and in order to show those trends the device was required to remain stable (as defined above) across all values of the parameters being swept. As such, highly-scaled devices that could ordinarily return the smallest switching currents and fastest switching times could not be used here, since they are only stable under limited ranges of free layer thickness, major axis length, etc. The following results, therefore, do not represent the most optimal current and speed levels possible with the SHE-mCell. Different sizing schemes that could yield better performance numbers are discussed in Section 4.1.9.

Simulation of current-driven switching in the SHE-mCell is shown in Figure 4.3. At $t=0$, the magnetization of the write-path is initialized parallel to the read-path electrodes (low resistance state). A current is then applied to the write-path, with a Pt underlayer (positive spin Hall angle) assumed. The write-path and read-path free layer magnetization begin to switch together, due to the coupling between the paths. The switching begins at the center of the elliptical shape and “spreads” outward; at the end of the simulation, the magnetization is now oriented antiparallel to the read-path electrodes (high resistance state).

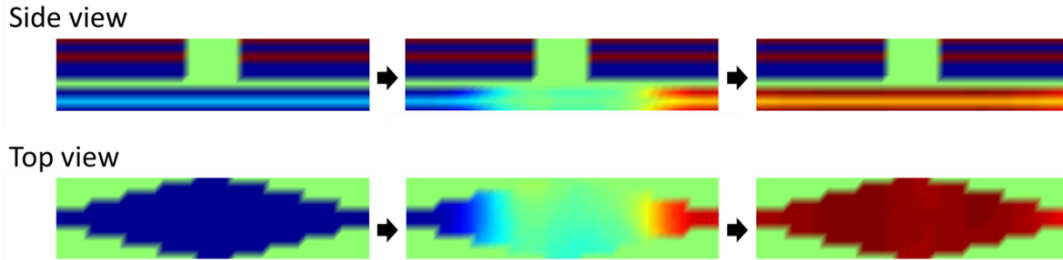


Figure 4.3 – Micromagnetic simulation of SHE-mCell state switching. The device begins in a low resistance state and ends in a high resistance state due to polarized spin-injection from a bottom layer. Side view showing cross-section (top) and top view showing free layer only (bottom) are shown.

Figure 4.4 shows the distribution in the energy profile over 100 simulations. The mean energy barrier is 71.2 $k_B T$ with a standard deviation of about 7.9 $k_B T$. The mean switching time (where the energy profiles cut off) is 3.72 ns, with a standard deviation of 0.56 ns; switching time as a function of current density is discussed further in section 4.1.3. In these simulations, the energy profile never flattens out at a peak value as in Figure 3.8; in that device, the energy was

dictated by the domain wall, whereas in this device the energy reaches a peak and decays as the bulk of the magnetization crosses the hard axis.

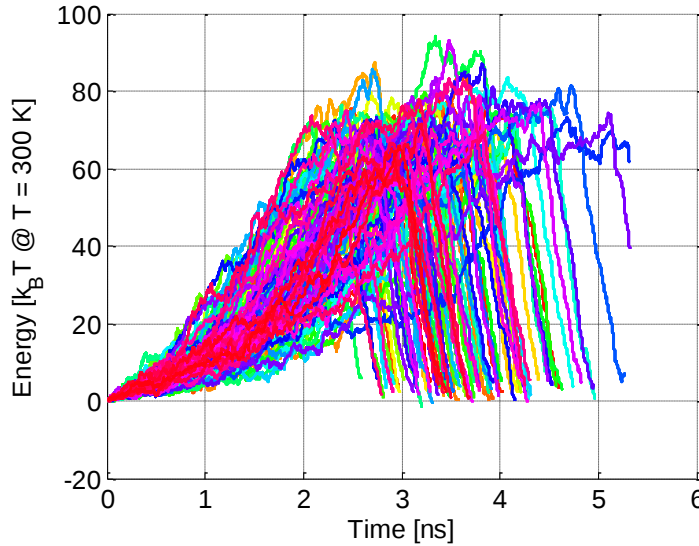


Figure 4.4 – Energy as a function of time for 100 cases of random thermal fluctuations. An energy barrier must be overcome to fully switch the device.

4.1.2 Switching Probability

Referring to equation (3.4), we see that the magnitude of the SHE is linear with the current density. Previously, we considered the probability of depinning a domain wall; in this case, we must consider the switching of a single-domain, in-plane magnetic device through an energy barrier due to the shape anisotropy. Regardless of the difference, the expectation that higher currents will increase the switching probability due to a larger total driving force is the same. Figure 4.5 demonstrates this assertion, where switching probability out of 100 total cases per current density increases with rising current density. Additionally, increasing the pulse width accommodates the use of lower switching currents because the switching is time-dependent. We will again define a switching probability of 95% as the critical current density.

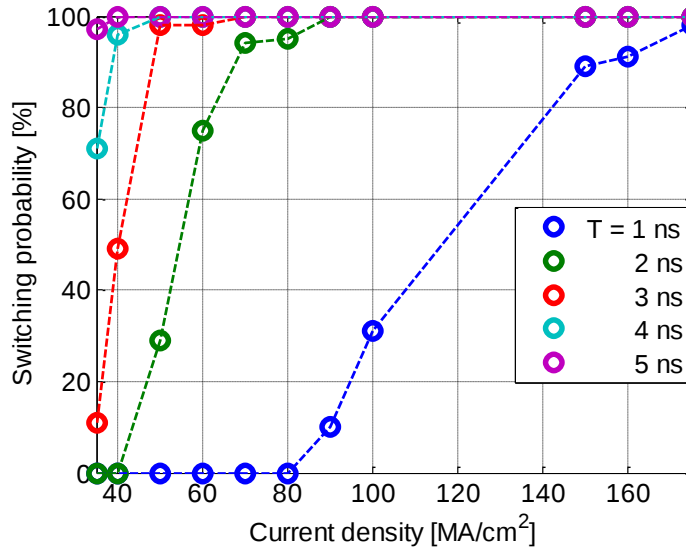


Figure 4.5 – Switching probability increases with increasing current density and pulse width.

4.1.3 Current Density and Switching Time

Since the magnitude of the SHE is linear with current density, we can expect that increasing current density reduces the overall switching time of the device (this is partially captured in Figure 4.5). Figure 4.6 shows a micromagnetic simulation of the average switching time of the SHE-mCell as a function of current density (simulated with 100 cases of random thermal fluctuations for each value of current density). Note the approximate $1/J$ dependence of the switching time, the same relationship observed in the domain wall devices (Figure 3.12, Figure 3.27). The performance is also quite similar; this device can be expected to switch in the nanosecond regime for current densities on the order of 10^7 A/cm², and trying to push it faster requires very large current densities (more so than what is required to make the STT-mCell or SHE-mCell equivalently fast).

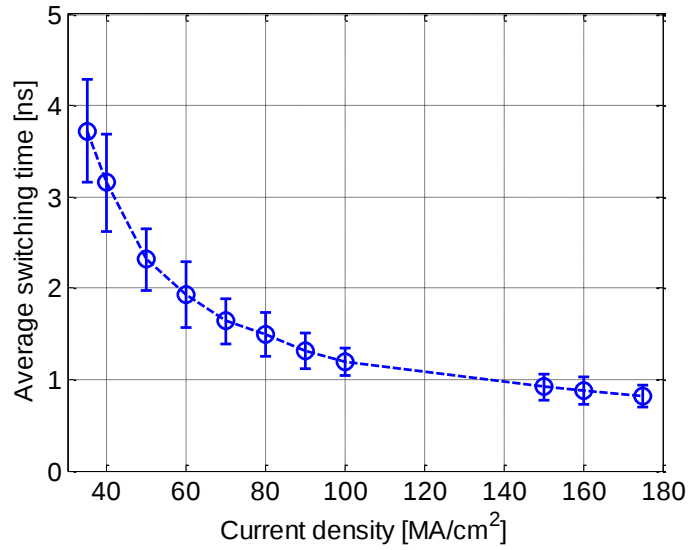


Figure 4.6 – Switching time decreases with increasing current density.

4.1.4 Write-Path Thickness

Based on Equation (3.4) a thinner ferromagnetic layer may enhance the SHE, perhaps indicating a thicker write-path necessitates additional current density to allow switching. And although in the domain wall-based devices the energy barrier is not affected by the write-path thickness, in this device the energy barrier is determined by the overall volume of magnetization being switched. A thinner write-path implies a decreased energy barrier, and so smaller currents or current densities may be required. However, a similar “load” effect is possible, where decreasing the ratio of $t_{WP}:(t_{FL} + t_{OX})$ makes the switching process more difficult.

As we saw with the STT-mCell and SHEDW-mCell, the critical current density tends to decrease with increasing write-path thickness, perhaps due to better coupling with more of the overall magnetization volume being driven by the current, but the absolute current increases (Figure 4.7). The thickness (or really, the thinness) of the write-path is limited in the perpendicular variants because of the presence of the insulating coupling layer, which is not inherently perpendicular; making the write-path in perpendicular devices thin is detrimental to the overall coupling and state stability. With an in-plane device, however, this is no longer an issue and the write-path can be made thin (e.g., 1-2 nm) to minimize the write current (assuming the coupling strength through the interlayer is strong enough).

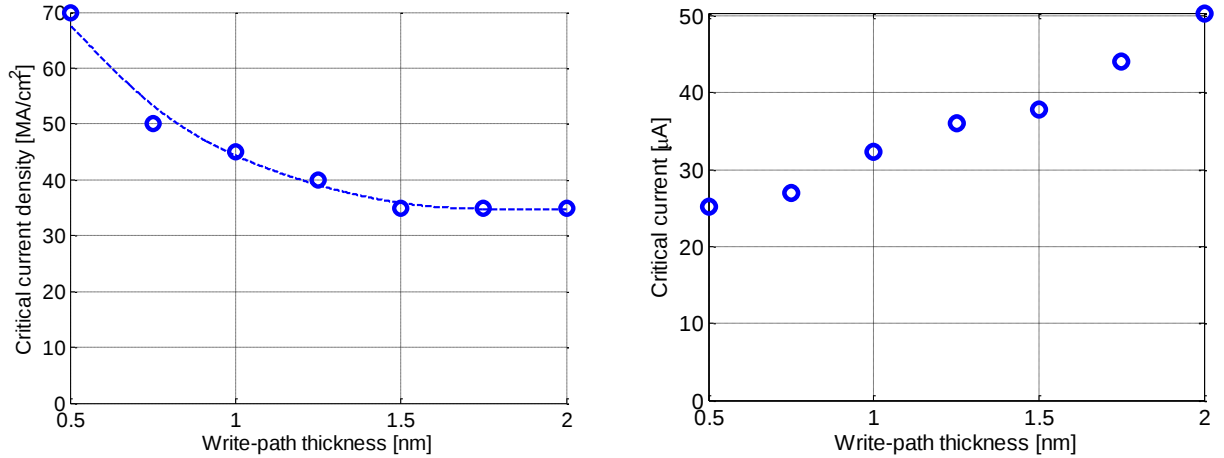


Figure 4.7 – (left) Critical current density decreases with increasing write-path thickness; (right) Absolute current decreases with increasing write-path thickness.

4.1.5 Coupling Interlayer Thickness

As in the domain wall devices, increasing the thickness of the electrically-insulating magnetic material that separates the write- and read-paths plays a significant role in device performance. Again, from an electrical standpoint it is preferable to have a thick coupling material to maximize the resistance. Previously, however, increasing the thickness of the coupling layer had a detrimental effect on the magnetic stability of the device, because the two perpendicular layers on either side of this default in-plane material could not be adequately coupled. With an in-plane SHE-mCell this effect is no longer observed; increasing the thickness of the coupling interlayer improves the electrical performance as well as enhances the state stability by raising the energy barrier, which is important for a highly-scaled device. However, as the effective switching load on the write-path is increased, the critical current density required to drive switching increases as well (Figure 4.8). The increase is not large in the relevant range of thickness, however. This implies the interlayer can be made thicker than that in the perpendicular mCells with only a small effect on switching performance.

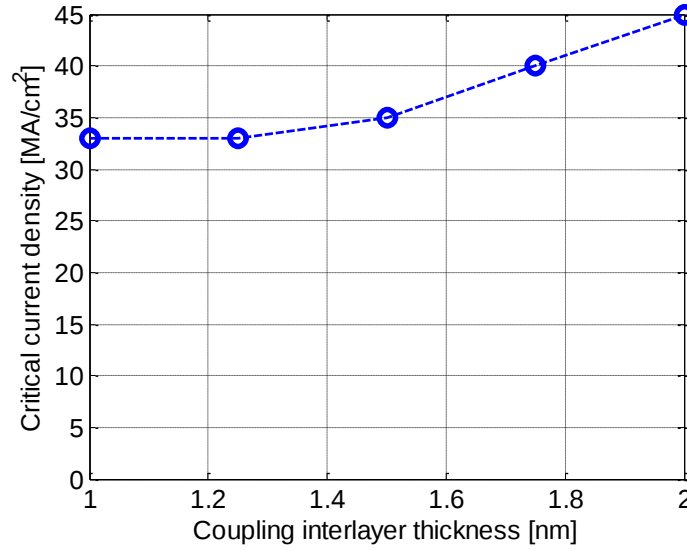


Figure 4.8 – Critical current density increases with coupling interlayer thickness, as the switching energy barriers increases.

4.1.6 Free Layer Thickness

Unlike in the perpendicularly-magnetized mCells, the thickness of the free layer in the read-path is a tunable variable. This is because the typical free layer material, FeCoB, is only perpendicular when extremely thin ($< \approx 1.2$ nm) and cannot be made much thicker [46]. By increasing the thickness of this layer we can tune the energy barrier by increasing the overall switching volume. This should have a similar effect to increasing the coupling layer thickness. This is supported by Figure 4.9, which shows nearly identical behavior to Figure 4.8. The magnitude of the critical current density increase here, however, is larger because we are enhancing the influence of a material with a greater saturation magnetization (1000 emu/cm^3 free layer vs. 500 emu/cm^3 coupling layer, both of which are reasonable estimates based on measured values).

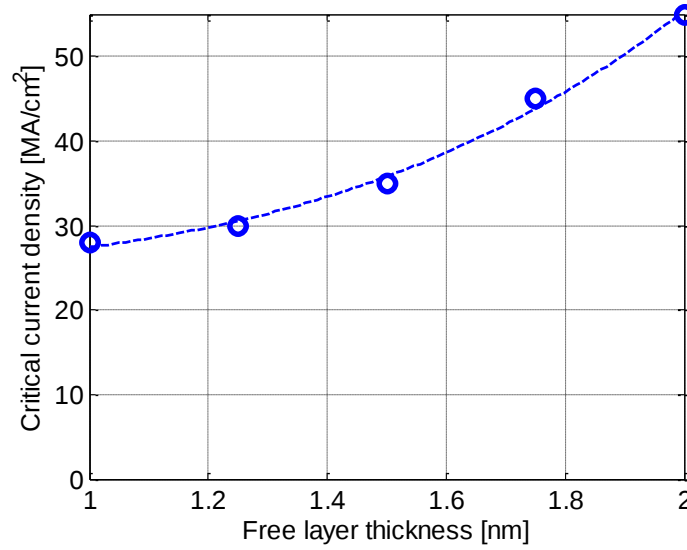


Figure 4.9 – Critical current density increases with free layer thickness, as the switching energy barriers increases.

4.1.7 Write-Path Saturation Magnetization

The saturation magnetization of the write-path also plays an important role in device stability and performance. The energy barrier is proportional to M_s , and so we can expect that larger M_s will increase the required switching current. Additionally, the magnitude of the SHE is inversely proportional to M_s , as shown in Equation (3.4). However, an increased saturation magnetization of the write-path implies a larger moment to couple up to the free-layer, which as we saw can reduce the switching current density when we considered the write-path thickness (Figure 4.7). The net effect of increasing the write-path M_s is shown in Figure 4.10. The critical current density is roughly linear with M_s in a range spanning such materials as Ni ($\approx 500 \text{ emu/cm}^3$), permalloy ($\approx 800 \text{ emu/cm}^3$), and CoFeB ($\approx 1000 \text{ emu/cm}^3$).

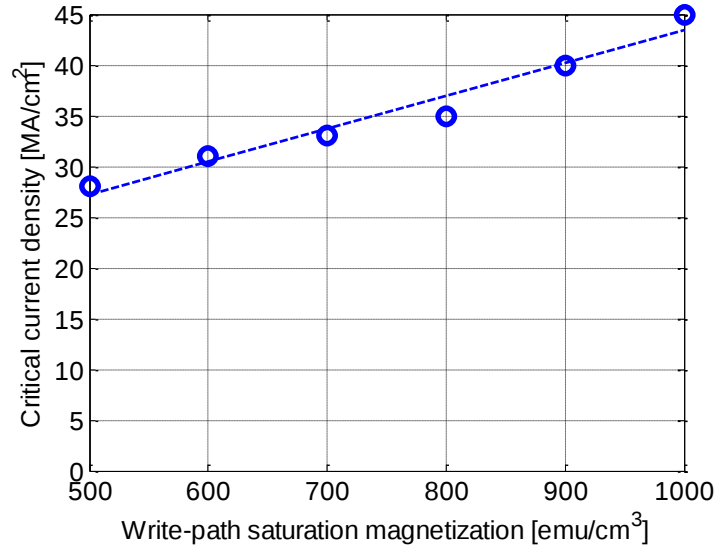


Figure 4.10 – Critical current density increases with write-path saturation magnetization in a linear fashion.

4.1.8 Spin Hall Angle

Referring again to Equation (3.4), the spin Hall angle θ_{SH} plays an important role in SHE efficiency. This quantity effectively represents the fraction of polarized spin being deflected to the non-magnetic/magnetic material interface, and just like the spin polarization factor can vary for magnetic materials, θ_{SH} can vary for non-magnetic materials. The three most commonly used non-magnetic materials for generating SHE torque are Pt ($|\theta_{SH}| \approx 0.05$), Ta ($|\theta_{SH}| \approx 0.15$), and W ($|\theta_{SH}| \approx 0.30$), although only certain phases of the latter two yield such high SHE efficiency [10],[64]. Given the linear dependence of the SHE torque with θ_{SH} , it is reasonable to expect the critical current density has an inverse relationship with θ_{SH} . Figure 4.11 confirms this.

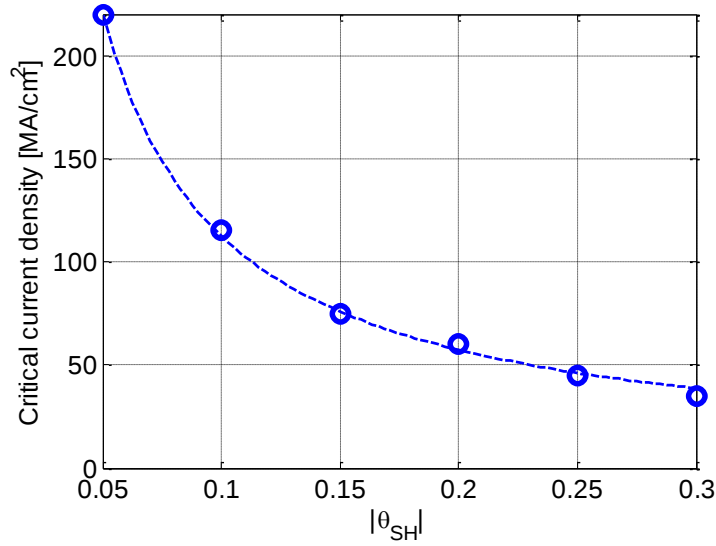


Figure 4.11 – Critical current density follows $1/\theta_{SH}$ dependence.

One may wonder why the critical current density varies exactly with θ_{SH} , given that there are other torques that contain J , namely the spin-transfer torques discussed in the previous chapter. It is important to remember that such torques only exist when domain walls are present, as they are dependent on a magnetization gradient. During the switching process of the SHE-mCell, a domain wall may indeed form; however, to minimize energy the domain wall “height” is across the width of the SHE-mCell (Figure 4.12), as this gives the smallest cross-sectional area possible. The magnetization gradient is then in the y -direction, orthogonal to the current flow in the x -direction, and so the spin-transfer torque on the wall is effectively zero. Therefore, the SHE is the only current-based torque acting on the magnetization. In the ideal case most of the current would flow through the non-magnetic underlayer anyway, in which case there could be no gradient-based STT in the magnetic material.

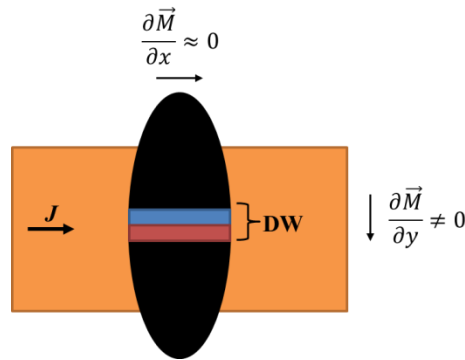


Figure 4.12 – A domain wall that forms to switch the magnetization state of the SHE-mCell tends to have its width

(gradient) orthogonal to the current flow, minimizing the STT effect.

4.1.9 Aspect Ratio and Device Volume for Sizing Switching Energy Barrier

In section 4.1 we described the requirements on the energy barrier of the SHE-mCell. Material properties, especially the saturation magnetization, play an important role in determining the energy barrier, as does device size. The best SHE-mCell design should include a sizable energy barrier to guarantee stability while minimizing the switching current. Because some parameters lead to more efficient current-based switching, increasing the energy barrier does not necessarily increase the switching energy.

Table 4-I presents a sampling of different device sizes and their resulting energy barriers and critical currents. When the device becomes very small (and in reality extremely difficult to fabricate), the energy barrier becomes correspondingly small. From this data, we observe that it is unlikely the in-plane SHE-mCell can switch at currents as low as the STT-mCell. This is not limited by the efficiency of the SHE – the current densities required to switch the devices are similar – but is instead a result of the wider cross-section required to establish a strong shape anisotropy. This is an unfortunate result, because the in-plane SHE-mCell provides a number of benefits over its domain wall-based counterpart (better MTJs, no pinning studs, and more flexibility in the use of the coupling interlayer, for example).

Table 4-I – Energy barrier and switching current for various size devices. M_s is assumed to be 800, 500, and 1000 emu/cm³ of the write-path, coupling layer, and free layer, respectively.

Major Axis [nm]	Minor Axis [nm]	t_{WP} [nm]	t_{MagOx} [nm]	t_{FL} [nm]	E_B [k _B T @ 300K]	I_c [μA]
36	10	2.0	2.0	2.0	43.4	32.4
45	10	2.0	2.0	2.0	54.3	45.0
45	10	2.0	2.0	1.5	50.1	36.0
45	10	2.0	1.5	2.0	56.9	40.5
45	10	2.0	1.5	1.5	46.6	31.5
45	10	1.5	2.0	2.0	46.1	37.0
54	10	2.0	2.0	2.0	63.3	54.0

54	10	2.0	2.0	1.5	55.5	43.2
54	10	2.0	2.0	1.0	47.7	32.4
54	10	2.0	1.5	2.0	57.6	48.6
54	10	2.0	1.5	1.5	50.9	37.8
54	10	1.5	2.0	2.0	53.4	44.6
54	10	1.5	2.0	1.5	48.7	40.5
54	10	1.5	2.0	1.0	40.6	24.3
54	10	1.5	1.5	2.0	51.8	40.5
54	10	1.5	1.5	1.5	43.1	28.4

4.2 Conclusions

In this chapter we explored the design and modeling of a magnetic logic device where a single domain in-plane magnetic layer is switched by the spin Hall effect. Although the specific simulation results presented in this chapter are dependent on the parameters and simulation techniques used, they are meant to indicate performance trends as material properties and device geometry vary. The modeling results of this chapter leave us with the following lessons:

- Switching currents below 50 μA are easily achievable in scaled devices. Sub-10-20 μA switching currents are difficult, if not impossible, to achieve. This makes it unlikely that this device would be useful in implementing low voltage, non-volatile circuits.
- Switching times of 1-5 ns are easily achievable in scaled devices, even at the critical current. There is an unsurprising trade-off between energy and performance, and so applying higher currents (i.e., larger pClock signals) increases the switching speed of the devices with a roughly $1/J$ relationship.
- Minimizing the thickness of the “load” layers (insulating coupling layer and read-path free layer) in both devices is important to ensure reliable coupling with low critical current density, assuming the energy barrier is still above 55 $k_B T$. This is one of the best ways to reduce the critical current, because the dependence is clear and no changes to the write-path itself need to be made.
- Using a material with the largest spin Hall angle accommodates the lowest critical current density, as it allows for maximum spin injection into the write-path magnetic layers.

(This, however, is a result best left for testing in experiment, as the increased resistance of the materials with large θ_{SH} may outweigh any benefit in increased SHE efficiency.)

- It is possible to margin the current pulse (magnitude and width) to ensure a high probability of switching. Additional simulations are necessary to see how the distributions change from the ones in this chapter (e.g., upwards of $1e5$ trials instead of 100 per set of inputs). The absolute pClock requirements can only be determined by the application. Some applications in which probabilistic switching can be exploited rather than avoided are discussed in the final chapter of this thesis.

5 Read- and Write-Path Development

In this chapter we introduce the experimental studies used to validate the simulation results and explore read- and write-path tests structures. We first describe the measurement techniques, and then present data on test structures. Kerr microscopy, magnetometry, and electrical probe measurements are all utilized to understand the magnetic and electrical behavior of the structures. The primary goal of this work was to determine what materials yield the necessary properties for making the building blocks of an mCell. Only a domain wall based mCell is addressed in this chapter.

5.1 Write-Path Development

5.1.1 Experimental Techniques

5.1.1.1 Kerr Microscopy

A Kerr microscope was the primary tool used to investigate domain wall motion in perpendicular thin films in this thesis. This type of microscope uses the magneto-optical Kerr effect to image magnetic domains, which appear as a change in contrast.

The Kerr effect works as follows [39]. Light is passed through a plane polarizer before reaching the magnetic material. Depending on the domain orientation, the reflected light will have a polarization rotated by a certain angle. For example, in Figure 5.1 beam 1 strikes a domain magnetized “up” and rotates by $+\theta$, while beam 2 strikes a domain magnetized in the opposite direction and rotates by $-\theta$. The reflected light passes through an analyzer, which is rotated until it is crossed with respect to beam 2. This extinguishes the beam 2 signal; however, beam 1 is not extinguished. As a result, the domain orientation represented by beam 1 appears light and the domain orientation represented by beam 2 appears dark. This change in contrast makes domains and domain walls visible.

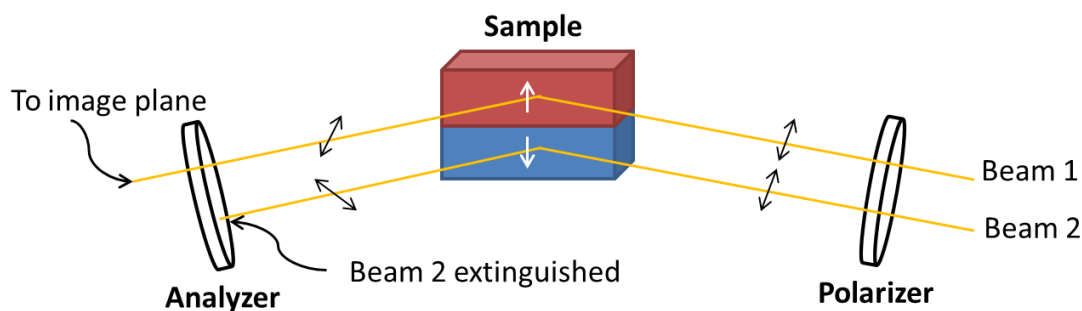


Figure 5.1 – Illustration of magneto-optical Kerr effect.

All Kerr images presented in this document will use a subtraction mode to clearly highlight portions of the nanowires that have switched in a particular direction. In this mode, a background magnetic image is subtracted from the real time magnetic image to present only the regions of the image in which the domain structure has changed. If a region has not been remagnetized, it will appear gray; if it has been switched up, it will appear black; and if it has switched down, it will appear white (Figure 5.2).

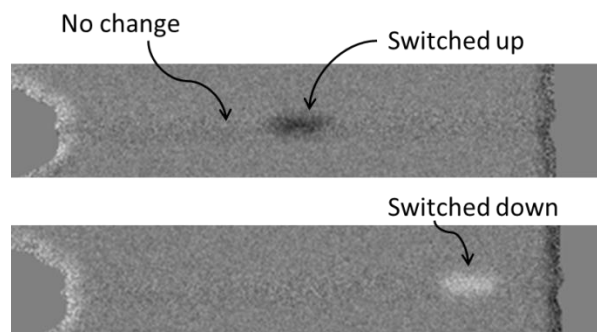


Figure 5.2 – Example Kerr microscopy images demonstrating subtraction mode. Regions with contrast represent areas in which the domain structure has changed since the background image was taken.

5.1.2 Co/Ni Multilayers

Films were prepared by DC magnetron sputtering on 3" float zone Si substrates by CMU collaborator V. Sokalski, with the following stack structure (all values listed in nm): TaN(3)/Pt(t_{Pt})/[Co(0.2)/Ni(t_{Ni})]₂/Co(0.2)/ Ta(t_{Ta})/TaN(6). The working pressure was fixed at 2.5 mTorr argon with a base pressure less than 2×10^{-7} Torr. Thickness variations were achieved using a wedge growth technique (Figure 5.3), where the substrate slowly enters the deposition path of the sputtering target before exiting out the same side. Therefore, the portion of the substrate that enters the deposition path first (last) will be thicker (thinner) with a linear thickness

profile across the surface. A cross-sectional TEM micrograph of a sample with $t_{\text{Pt}} = 2.5$ nm, $t_{\text{Ni}} = 0.6$ nm, and $t_{\text{Ta}} = 1$ nm is shown in Figure 5.4.

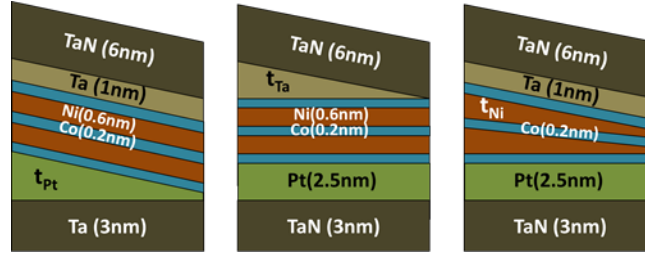


Figure 5.3 – Illustration of a Pt wedge (left), Ta wedge (middle), and Ni wedge (right) sample. Thickness varies approximately linearly as a function of spatial position on the wafer.

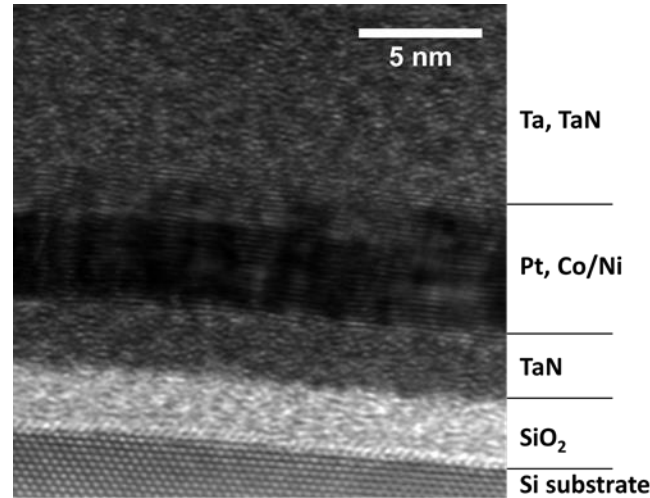


Figure 5.4 – Cross-sectional TEM of one section of the Ni wedge. [Courtesy V. Sundar]

Wires 20 μm in length and 2-4 μm in width were photolithographically patterned by CMU collaborator M. Moneck. Copper leads were patterned to connect to the nanowire test structures and form a coplanar waveguide to minimize reflections of the high-frequency injected current pulses (Figure 5.5(a)). Before CIDWM tests, the nanowire is first exposed to a large DC perpendicular magnetic field from an external electromagnet, which saturates the magnetization of the wire in the direction of the field. To form a domain wall in the wire, a current pulse is injected through the ground leads of the waveguide, which generates a circulating Oersted field that switches the magnetization of the nanowire in the locality of the waveguide (Figure 5.5 (b)).

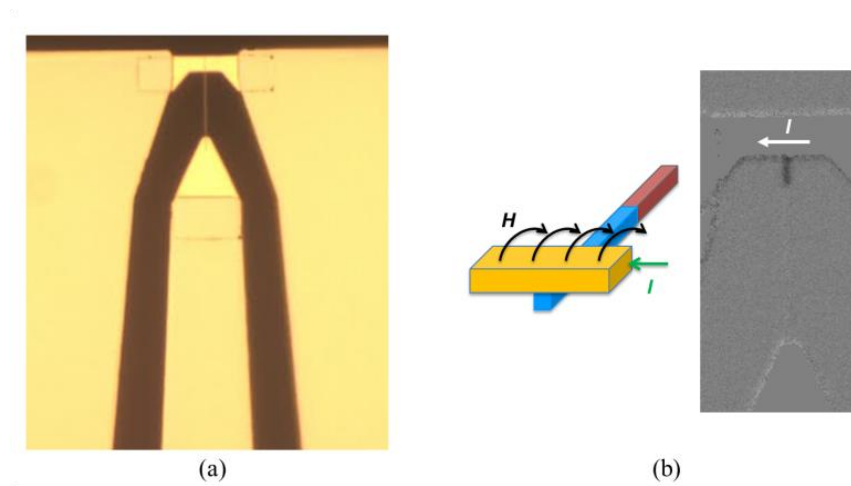


Figure 5.5 – (a) Optical image of patterned nanowire and waveguide structure; (b) illustration of domain wall nucleation procedure and Kerr image of nucleated domain wall.

Polar Kerr microscopy was used to directly image the domain wall movement, allowing one to separate true CIDWM from other effects, such as demagnetization due to Joule heating that may be hidden in a purely electrical device test. Difference imaging was used, where the background image is subtracted from the live image (as described in section 5.1.1.1) to clearly depict any changes in the magnetization state of the wire. Once a domain wall is formed using the previously described injection process, current pulses of programmable pulse width and 2 ns rise time are injected in the nanowires to observe any changes in the magnetic state. Figure 5.6 depicts the switching sequence of a Co/Ni wire. Each image was taken after applying a 50 ns current pulse with the net wall displacement being given by the width of the dark (left) or light (right) segments of the wire. The CIDWM is opposite the electron flow in Figure 5.6, indicating the motion is driven by the spin Hall effect rather than conventional STT. No applied field (in any direction) was used, indicating the Dzyaloshinskii-Moriya interaction (DMI) is likely at play in the structures.

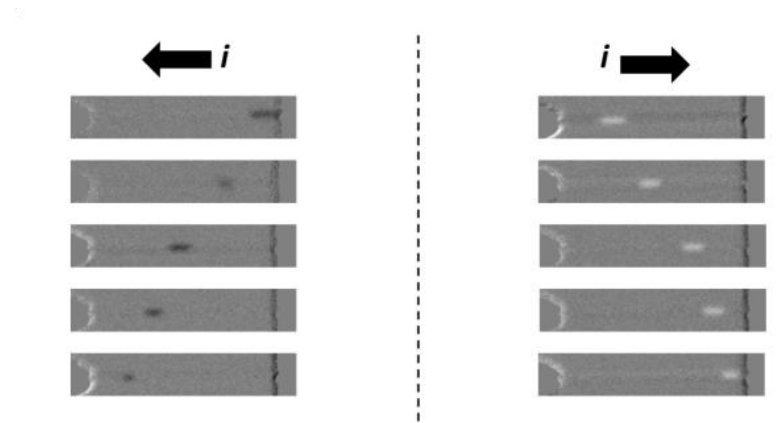


Figure 5.6 – Kerr microscopy images showing domain wall motion along the direction of current.

The general characteristics of domain wall motion as a function of current density and pulse width are shown in Figure 5.7. Example Kerr images depicting the domain wall motion in a TaN(3nm)/Pt(2.5)/[Co(0.2)/Ni(0.3)]₂/Co(0.2)/Ta(0.32)/TaN(6) wire are provided in Figure 5.7(a), demonstrating that increasing the current density and/or the pulse width yields a greater wall displacement. Figure 5.7(b) shows the average displacement for a combination of pulse widths and amplitudes. Each point represents the average of five injected pulses, with error bars denoting the standard deviation. As shown in Figure 5.7(b), the increase in displacement with current density is roughly linear, with a y-intercept below the origin. This is a reasonable result, as lower current densities may fall below a critical current density required to initially de-pin a domain wall. Displacement is also found to be linear with pulse width in the time range studied here indicating that dynamic heating effects are not significant. As a result, the domain wall velocity (approximated as displacement over pulse width) is not a function of pulse width (Figure 5.8).

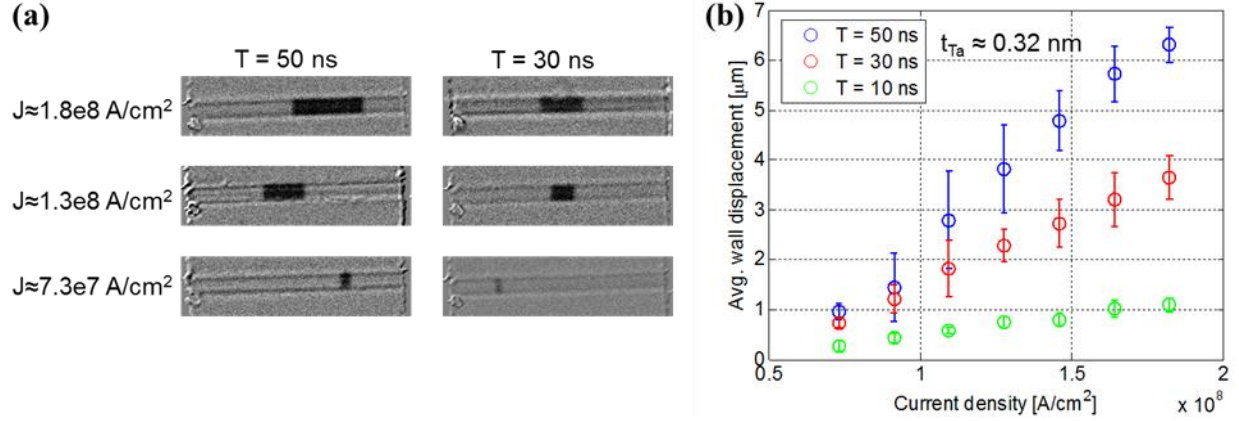


Figure 5.7 – (a) Example Kerr images depicting domain wall displacement for various current densities for 50 and 30 ns pulses; (b) mean wall displacement as a function of current density and pulse width in a TaN(3nm) / Pt(2.5) / [Co(0.2) / Ni(0.3)]₂ / Co(0.2) / Ta(0.32) / TaN(6) wire.

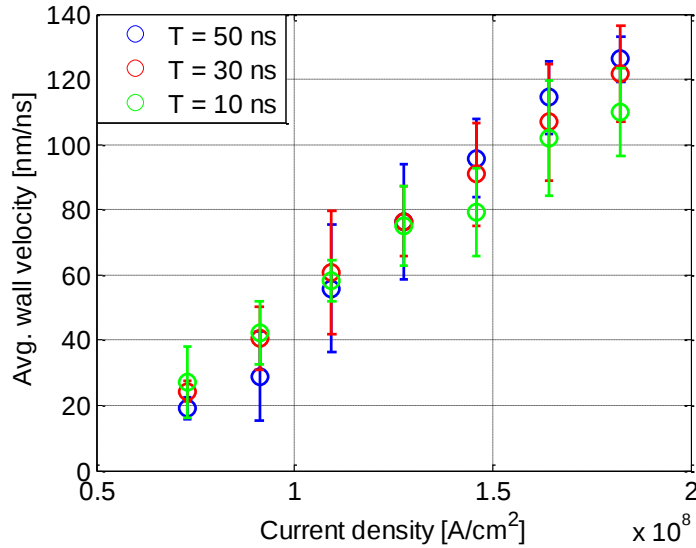


Figure 5.8 – Mean wall velocity increases linearly with current density and is not a function of pulse width.

With the wedge films patterned into wires we were quickly able to consider how variations in film thicknesses affect the DWM. Figure 5.9 and Figure 5.10 show that the thicknesses of Ni and Pt, respectively, do not play a major role in increasing the domain wall displacement for a given applied voltage. Reducing the thickness of the Ta capping layer, however, does impact displacement quite significantly (Figure 5.11). A number of recent studies have shown that the presence of Néel walls, with chirality believed to be dictated by the DMI, is crucial to accommodate domain wall motion driven by the spin Hall effect with no external fields [41]-[42]. While Ta and Pt have spin Hall angles of opposite sign and therefore contribute additive

Slonczewski-like torque when on opposite sides of the Co/Ni multilayers, there is strong evidence to suggest that the DMI associated with Ta and Pt interfaces are the same sign and set the same wall chirality [41]. Consequently, in the films studied here, Ta and Pt have subtractive effects with regard to setting a chiral Néel wall as they are on opposite sides of the Co/Ni multilayers. If the Ta cap's contribution to the DMI is reduced when it is made thinner, then it is possible the domain wall would become more Néel-like, which would explain the observed increase in wall displacement for thin Ta. This effect may outweigh the difference in spin torque generated by current flow in the Ta, which adds onto the torque generated by the Pt under-layer. The trend becomes evident when the thickness data is normalized to a constant current density (Figure 5.12). Thin Ta yields the greatest displacement for a given current density.

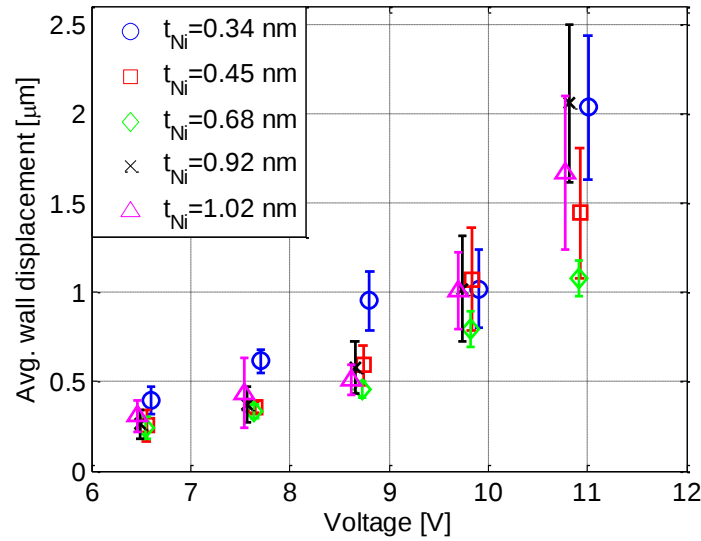


Figure 5.9 – Wall displacement increases with applied voltage (current) but is not strongly dependent on Ni thickness in TaN(3nm) / Pt(2.5) / [Co(0.2) / Ni(t_{Ni})]₂ / Co(0.2) / Ta(1) / TaN(6) stack.

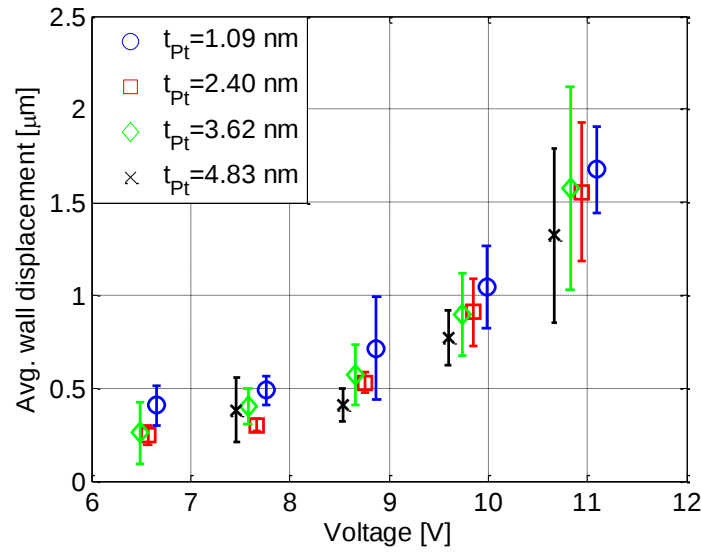


Figure 5.10 – Wall displacement increases with applied voltage (current) but is not strongly dependent on Pt thickness in TaN(3nm) / Pt(t_{Pt}) / [Co(0.2) / Ni(0.6)]₂ / Co(0.2) / Ta(1) / TaN(6) stack.

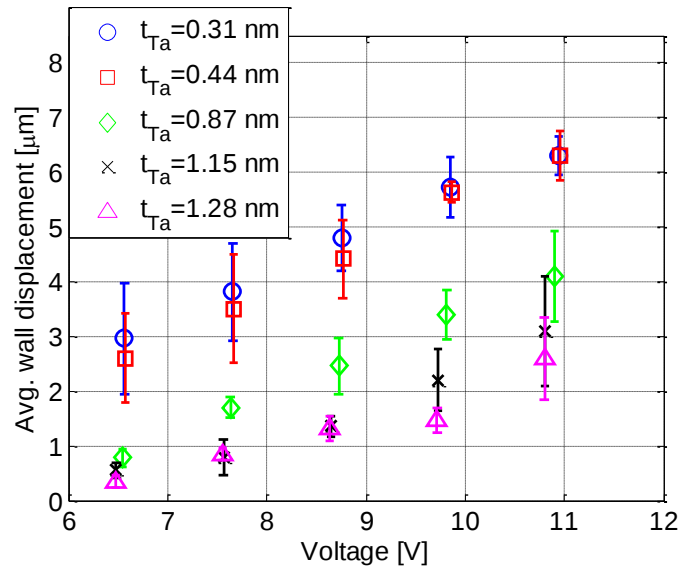


Figure 5.11 – Wall displacement increases with applied voltage (current) and is largest when the Ta capping layer is kept thin in a TaN(3nm) / Pt(2.5) / [Co(0.2) / Ni(0.3)]₂ / Co(0.2) / Ta(t_{Ta}) / TaN(6) stack.

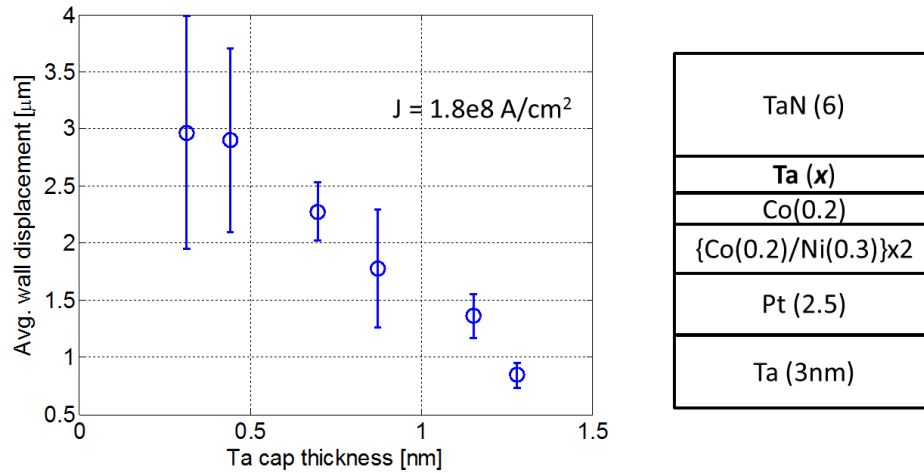


Figure 5.12 – A thin Ta cap yields the greatest displacement for a fixed current density.

Based on these results it is likely that integrated device prototypes will consist of a 2-3 nm Pt under-layer, and 0.2 nm Co and 0.3-0.6 nm Ni in a Co/Ni stack. Ultimately, the write-path will be capped by a magnetic oxide and not Ta; if our understanding of why thin Ta yields better DWM (smaller contribution in determining wall chirality), then integrating the magnetic oxide will likely have the same effect. This study did not address varying the number of repeats of Co/Ni. [Co/Ni]_{x2}/Co represents a good choice, however, because it makes the write-path thick enough that coupling to the read-path is possible, but not so thick that the SHE is too weak to drive the motion.

5.2 Read-Path Development

5.2.1 Experimental Techniques

5.2.1.1 TMR Electromagnet Probe Tester

As described in Chapter 3, an MTJ is in its lowest resistance state when the magnetization on either side of the tunnel barrier is parallel and it is in its highest resistance state when the magnetization on either side of the barrier is antiparallel. Using an external applied magnetic field, the magnetization of the free layer can be switched to align parallel or antiparallel to the fixed layer magnetization. An electromagnet can be used to apply the field, with the MTJ sitting in between the pole tips where the field is uniform. An ohmmeter can then be used to probe leads

that contact to the MTJ to measure the resistance. The TMR can be extracted from the high and low resistance values measured.

The first step in the measurement is to saturate the MTJ with a strong field, which causes the magnetization in the fixed and free layers to align parallel. The field strength is then decreased, crosses zero, and reverses direction. Because the free layer switches more easily than the fixed layer, at a certain negative field strength the free layer will align with the field, which is antiparallel to the fixed layer magnetization. This leads to a high resistance state. If the field is further increased in magnitude, at some point the fixed layer magnetization will also align with the field, causing a parallel or low resistance state. The process is then reversed; the field is increased back up to zero and becomes positive. The free layer magnetization will become antiparallel to the fixed layer magnetization, until a strong field once again brings it all into alignment. The resistance can be plotted as a function of field, giving what is known as an R-H loop (Figure 5.13). This technique was the primary tool used to evaluate patterned MTJs in the lab.

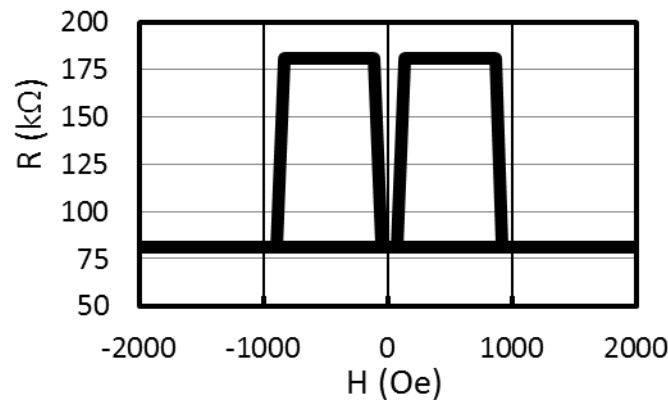


Figure 5.13 – R-H loop for an MTJ. A TMR of 124% is shown.

5.2.1.2 Current-In-Plane Tunneling (CIPT)

Patterning MTJs using electron-beam lithography is a low throughput process, making it difficult to quickly evaluate properties when materials and layer thicknesses are varied. Current-in-plane tunneling (CIPT) is a measurement technique that allows one to extract the TMR and RA of a magnetic tunnel junction from the sheet film level, obviating the need to pattern distinct pillars and analyze them in the probe tester [65]. The CIPT method involves a series of four-point probe tests, where a current is injected between two probes through a set of films

consisting of a top electrode, tunnel barrier, and bottom electrode, and the resulting voltage drop measured between the other two probes. The sheet resistance is then extracted using Ohm's law. The key to CIPT is using a variety of probe spacings and then fitting the sheet resistance measurements to extract the true MTJ properties. When the probe spacing is small, practically all the current flows through the top electrode because that is the lowest resistance path; however, if the spacing is made to be large, the current has the opportunity to tunnel through the barrier, dividing the flow between the top and bottom electrodes. Between these two limits exist a variety of probe spacings in which the current flow through the bottom electrode will depend on the tunnel barrier resistance.

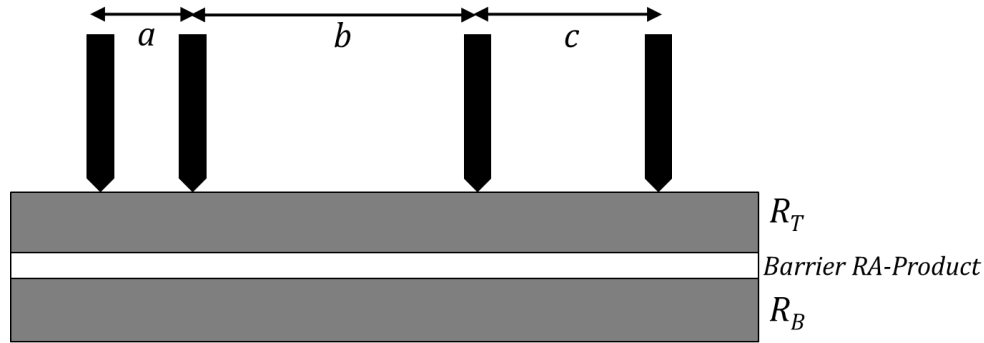


Figure 5.14 – Illustration of CIPT measurement. R_T is the sheet resistance of the top electrode, R_B the sheet resistance of the bottom electrode, and a , b , and c represent the probe spacings.

In our experimental setup, a probe with twelve available tips is used. At any given time, the current is injected through two probes and the voltage measured between another two. Eight to ten of these four-point probe measurements are generally taken, with different combinations of probes for injecting and measuring. The sheet resistance measurements are then fit according to the model defined in [65] and replicated in Equation (5.1), where $\lambda = \sqrt{\frac{RA}{R_T + R_B}}$ and K_0 is the modified Bessel function of the second kind, order zero. Current-in-plane MR (MR_{cip}) is measured by performing the experiment when the magnetizations of the top and bottom films are parallel (R_{LOW}) and antiparallel (R_{HIGH}) and taking the ratio $MR_{cip} = \frac{R_{HIGH} - R_{LOW}}{R_{LOW}}$. An integrated electromagnet is included to put the films in a parallel or antiparallel state. The actual TMR can be determined from the best fit curve.

$$R_{meas} = f(R_T, R_B, RA, a, b, c) \quad (5.1)$$

$$= \frac{1}{2\pi} \frac{R_T R_B}{R_T + R_B} \left\{ \frac{R_T}{R_B} \left[K_0 \left(\frac{a}{\lambda} \right) + K_0 \left(\frac{c}{\lambda} \right) - K_0 \left(\frac{a+b}{\lambda} \right) - K_0 \left(\frac{b+c}{\lambda} \right) \right] \right. \\ \left. + \ln \left[\frac{(a+b)(b+c)}{ac} \right] \right\}$$

The resulting data is usually plotted in terms of $R_{\square}$ and MR_{CIPT} as a function of mean probe spacing, where $R_{\square}$ begins at a value of R_T (for small probe spacing) and eventually transitions to the parallel combination of R_T and R_B , when the probe spacing is large and the current divides proportionally between the top and bottom electrodes. An example MTJ stack structure, R-H loop, measured, and fitted results are shown in Figure 5.15. Based on what model parameters give the best fit, we estimate the actual TMR and RA. We evaluated a number of films this way prior to choosing candidates to pattern. Results on patterned devices are discussed in the following section.

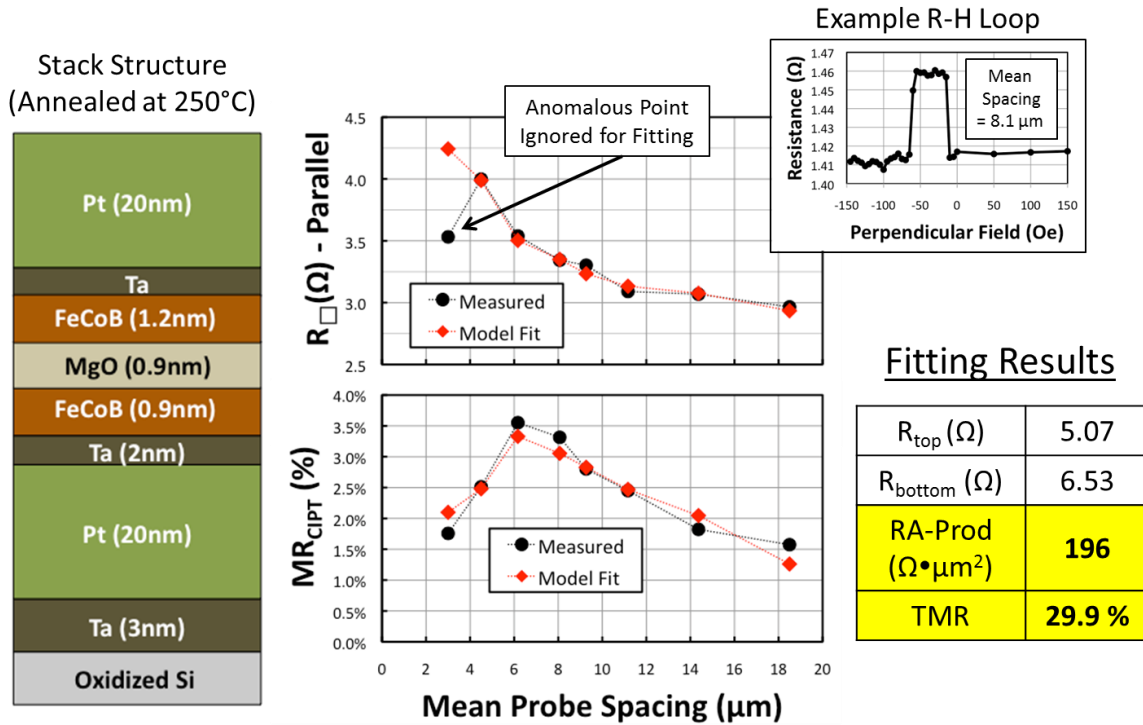


Figure 5.15 – Stack structure, R-H loop, and measured and fitted CIPT results. [In conjunction with Z. Dai, M. Moneck, V. Sokalski]

5.2.2 FeCoB/MgO/FeCoB MTJ System

The standard material system used to fabricate perpendicular MTJs is FeCoB/MgO/FeCoB, with $t_{\text{FeCoB}} < \approx 1$ nm. Research has shown that these materials yield, to date, the highest TMR and lowest RA. Annealing the films is a crucial part of the MTJ fabrication process, due to the well-studied crystallization of the FeCo to a BCC (001) texture (naturally occurring in the MgO) during heating. Without annealing the structure, the MTJ properties (TMR and RA) are not favorable; however, annealing for too long or at too high of a temperature kills the perpendicular anisotropy of the FeCoB layers. Annealing studies performed by V. Sokalski indicate a perpendicular easy axis is difficult to obtain in a standard Ta/Fe₆₀Co₂₀B₂₀/MgO/Fe₆₀Co₂₀B₂₀ structure beyond 350 °C (Figure 5.16) [66]. Tuning the deposition rate of Ta in Ta/Ru/Ta underlayers was found to improve the annealing stability to 350 °C; the MgO texture, and resulting TMR in optically patterned devices, improved with increasing annealing temperature [67]. The highest TMR recorded in our experiments was 138%, well within the range necessary for mLogic fanout (Figure 5.17). The voltage bias dependence of the MTJs is plotted in Figure 5.18. As expected from theory [45],[68], the TMR degrades as the bias increases. The degradation in the range of voltage levels expected for mLogic (≈ 100 mV) is slight enough to not have an impact on the feasibility of driving fanout based on biasing and passing current through MTJs. A cross-sectional TEM micrograph of the film from which these MTJs were fabricated is shown in Figure 5.19; the MgO is uniform and smooth, which helped contribute to the high TMR.

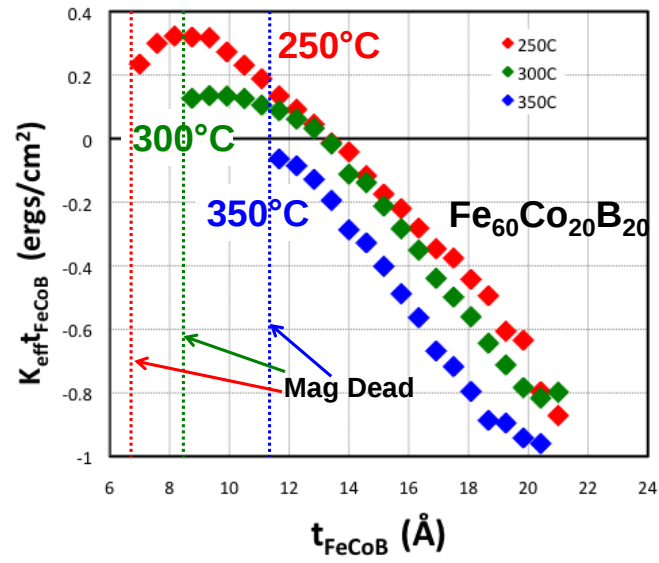


Figure 5.16 – Perpendicular anisotropy decreases as the FeCoB thickness in a Ta/FeCoB/MgO sample increases, and as annealing temperature increases. [Courtesy V. Sokalski]

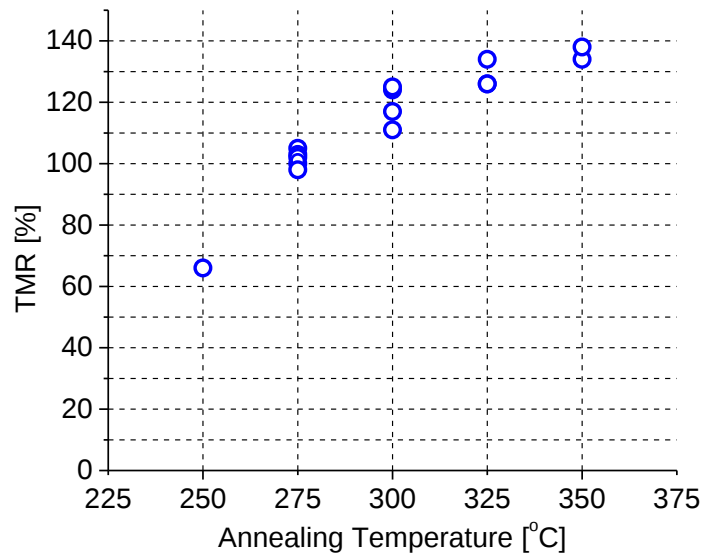


Figure 5.17 – TMR as a function of annealing temperature. TMR as high as 138% is achieved for a 1.8 nm tunnel barrier.

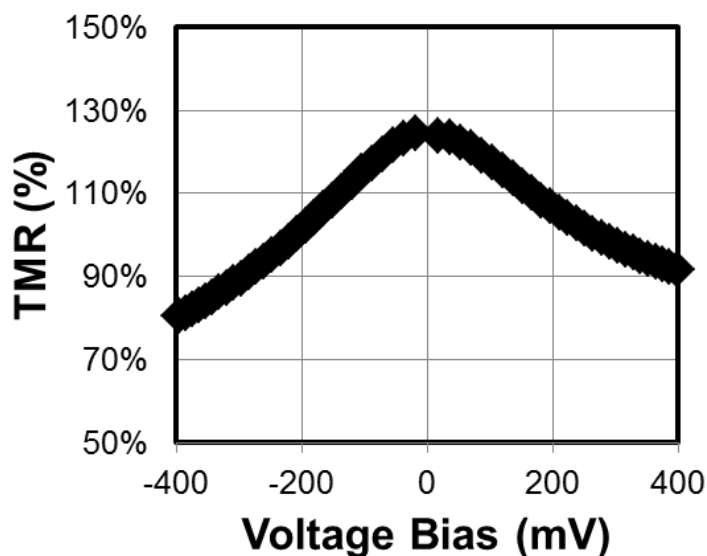


Figure 5.18 – Exemplary voltage bias dependence of TMR for the 1.8 nm MTJs.

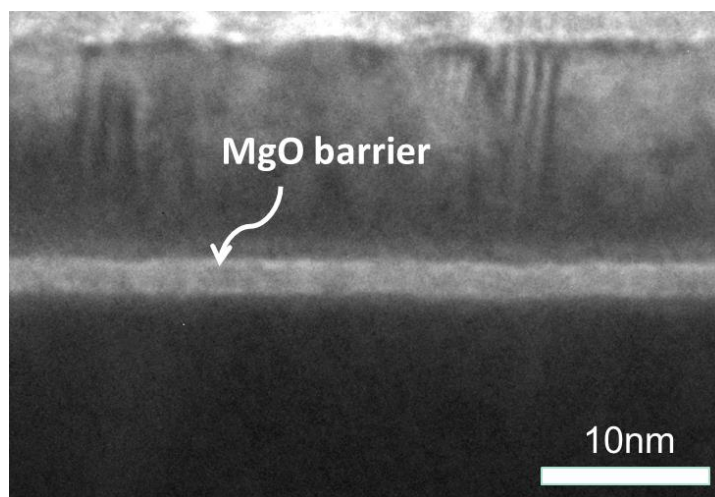


Figure 5.19 – Cross-sectional TEM micrograph of Ta/FeCoB/MgO/FeCoB film indicating smooth, uniform MgO. [Courtesy V. Sokalski, E. Yang]

Using thick (> 1 nm) MgO negatively impacts the RA product. mLogic circuits are not designed to operate for read-path resistances in the $M\Omega$ range. For a first generation device prototype designed to demonstrate the basic concept of an mCell (current through a write-path can switch the resistance state of a separate read-path), thick MgO can be used. This eases the fabrication challenges because it allows for more time to stop the etch that defines the separate MTJs in the read-path before blowing through the tunnel barrier and damaging the read-path free layer (FeCoB). It should be noted, however, that to demonstrate mLogic – actual logic circuits built from mCells – thinner MgO that yields lower RA product (and ideally the same or better

TMR) is a requirement.

5.3 Interlayer Coupling Layer Development

5.3.1 Experimental Techniques

No special techniques were applied to evaluate the magnetic oxide samples. Experiments were based on film-level four point probe measurements and electrical measurements on patterned pillar test structures.

5.3.2 FeCo-Oxide and FeCoB-Oxide

The first material we explored to electrically isolate but magnetically couple the write- and read-paths was FeCo-oxide. Equiatomic FeCo was sputter deposited by V. Sokalski to a thickness of 30 nm with periodic breaks in deposition where the film was exposed to 0.1 mTorr O_2 for 60 seconds, allowing natural oxidation to occur. Approximately 1.1 nm of oxide formed during each oxidation step. AGFM measurements (Figure 5.20) indicate the saturation magnetization of a pure oxide (volume fraction approaches 1) is approximately 500 emu/cm³, which is the exact value assumed in the micromagnetic simulations. This value is similar to the expected M_s for $(FeCo)_3O_4$ [69].

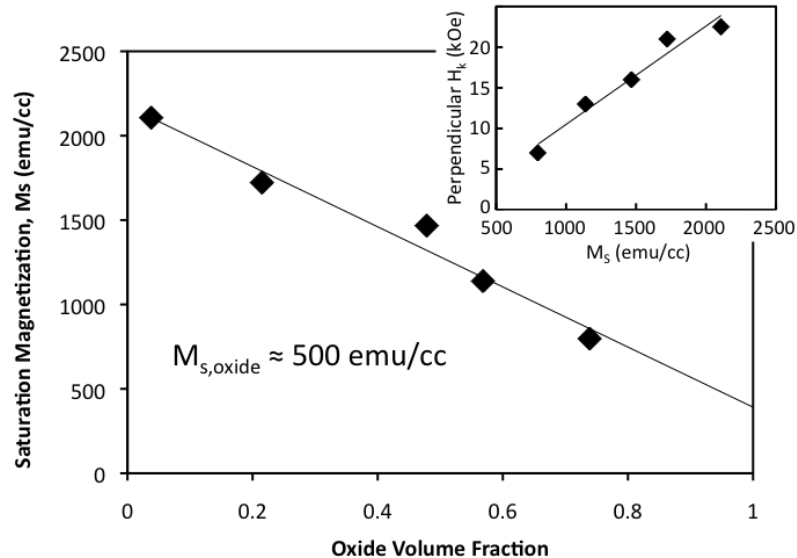


Figure 5.20 – Saturation magnetization vs. estimated oxide volume fraction. Extrapolation to 100% indicates the FeCo-oxide has M_s of ≈ 500 emu/cc. Inset shows linear dependence of perpendicular saturation field on M_s , which extrapolates to 0 at $M_s=0$. This indicates anisotropy is due primarily to shape. [Courtesy V. Sokalski]

Four-point probe tests were utilized to measure the sheet resistance of the films. The measured resistivity increases exponentially as the FeCo repeat thickness decreases (Figure 5.21); this suggests the oxide is intrinsically insulating, as decreasing FeCo repeat thickness effectively increases the oxide volume fraction.

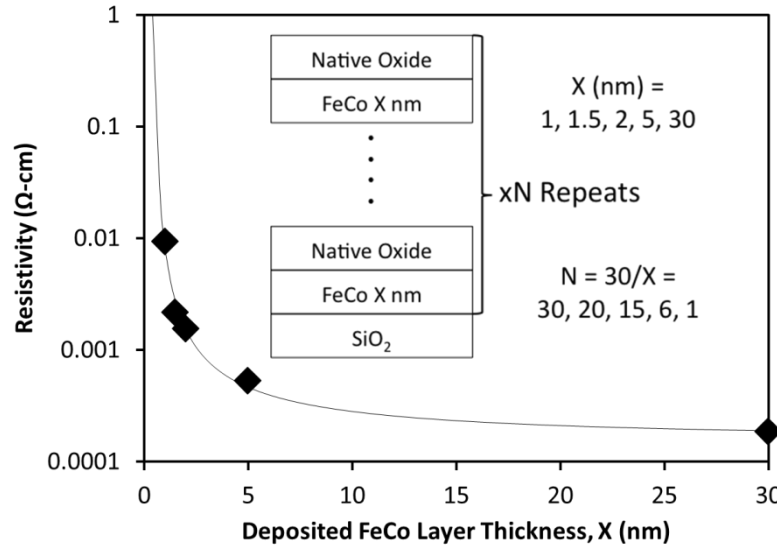


Figure 5.21 – Sheet resistivity of naturally-oxidized FeCo film as a function of FeCo layer thickness.

To test magnetic coupling, the naturally oxidized FeCo was deposited between two perpendicular FeCoB layers, with a very thin layer of Ta deposited at both FeCo-oxide/FeCoB interfaces. The Ta is necessary to accommodate a strong perpendicular anisotropy in the FeCoB magnetic layers. If the Ta is made too thick, however, it breaks the exchange that facilitates the coupling. The thickness of the Ta was varied to determine an optimal point at which both the perpendicular anisotropy and the coupling are strong, with the oxide thickness fixed at 1.1 nm. The results are shown in Figure 5.22. First, Figure 5.22(a) is shown as a reference, where the two magnetic layers are fully decoupled with thick Ta between them and no magnetic oxide. When the Ta is thin (0.3 nm, Figure 5.22(b)) the coupling is strong, but the perpendicular anisotropy is not as the Ta was not thick enough to support a perpendicular easy axis. This is indicated by the 100% in-plane remanence and zero perpendicular remanence. If the Ta is too thick (0.9 nm, Figure 5.22(c)) the perpendicular anisotropy is strong, but the coupling is weak, with less than 100% perpendicular remanence. However, if the Ta thickness is just right (0.7 nm, Figure 5.22(d)) the perpendicular remanence is 100% and the in-plane remanence is zero, indicating

strong coupling and strong anisotropy. The minimum coupling field is 6 kOe, corresponding to a coupling strength of about 0.3 erg/cm².

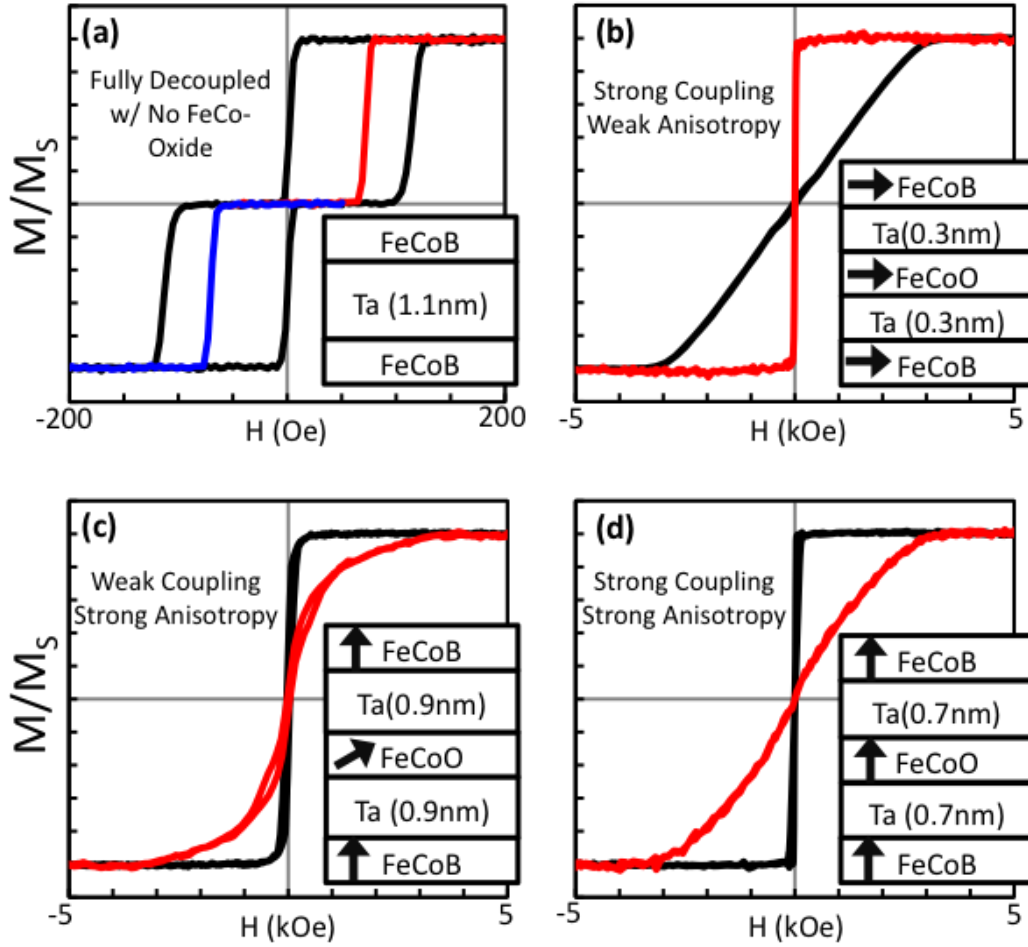


Figure 5.22 – MH loops for two perpendicular FeCoB layers separated by (a) Ta(1.1nm); (b) Ta(0.3nm)/FeCo-Oxide(1.1nm)/ Ta(0.3nm); (c) Ta(0.9nm) / FeCo-Oxide(1.1nm) / Ta(0.9nm); (d) Ta(0.7nm) / FeCo-Oxide(1.1nm) / Ta(0.7nm). [Courtesy V. Sokalski]

This study was also performed using oxidized FeCoB, which is easier for our group to work with due to the limited number of targets that can be placed in our sputtering system. Figure 5.23 shows that the oxide has a saturation magnetization of about 400 emu/cm³ (left) and its sheet film resistance increases by roughly three orders of magnitude as the oxide volume fraction approaches 1. These are similar to the FeCo-oxide trends shown in Figure 5.20 and Figure 5.21. Coupling measurements between a Co/Ni “write-path” and FeCoB “read-path” are shown in Figure 5.24. This was another wedge film, where the FeCoB that is allowed to oxidize (to 1 nm)

is varied in thickness. When the deposited FeCoB is too thin, it cannot adequately couple the Co/Ni to the top FeCoB (Figure 5.24(a)); when it is too thick, the switching is combined but the remanence is less than 100% (Figure 5.24(c)). At an intermediate thickness (Figure 5.24(b)), the top FeCoB and the Co/Ni switch together and the remanence is roughly 100%.

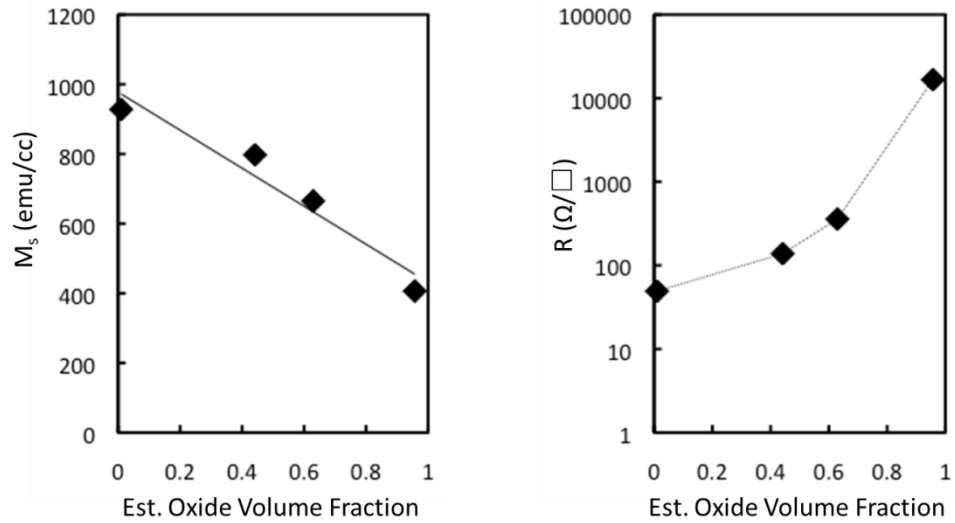


Figure 5.23 – (left) Saturation magnetization of oxidized FeCoB decays linearly to 400 emu/cm³ as the oxide volume fraction approaches 100%; (right) sheet film resistance increases by orders of magnitude as oxide volume fraction approaches 100%. [Courtesy V. Sokalski]

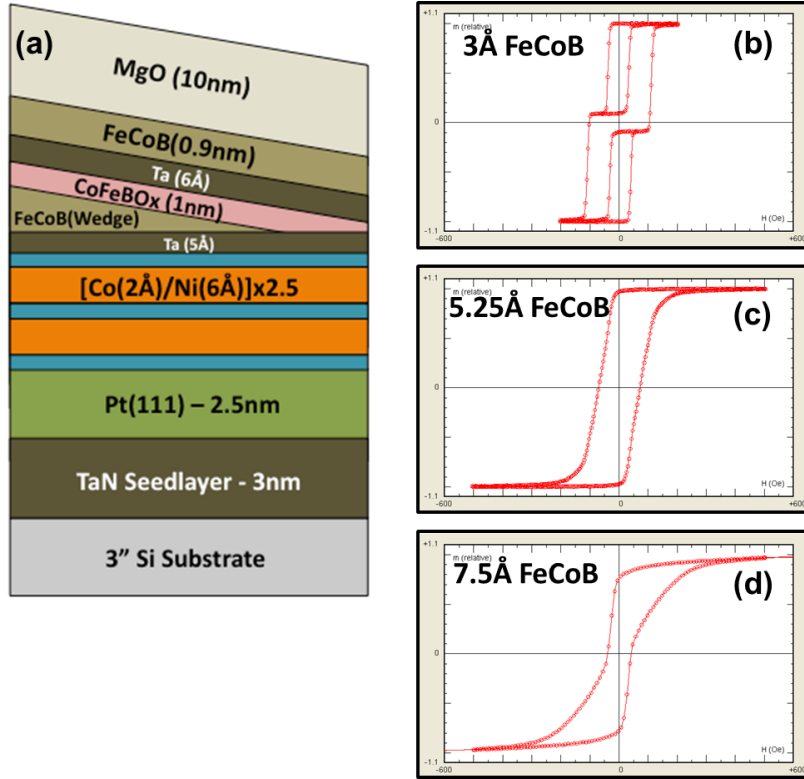


Figure 5.24 – (a) Stack structure of wedge film with variable FeCoB thickness to couple to another FeCoB layer through 1 nm of oxide; (b) M-H loop for 0.3 nm FeCoB that demonstrates insufficient coupling (separate switching); (c) M-H loop for 0.525 nm FeCoB that demonstrates good coupling (combined switching, $\approx 100\%$ remanence); (d) M-H loop for 0.75 nm FeCoB that demonstrates combined switching, but with less than 100% remanence. [Courtesy V. Sokalski]

These results help establish a thickness range for the deposited FeCoB, which can be used to design an integrated prototype device.

5.4 Conclusions

In this chapter we have detailed our experimental efforts in developing the write- and read-paths of mCells. We performed a study to determine how the thicknesses of Pt, Ni, and Ta affect the DW displacement in a Pt/[Co/Ni]₂/Co/Ta stack. It was observed that only the Ta thickness had a significant influence on the motion, which we attribute to its role in setting the domain wall chirality. Importantly, the effect behind the DWM was not STT, but the SHE. These physics have been, and continue to be, investigated in the magnetism community. From the “black box” perspective of the mCell, it makes no difference whether the domain wall is driven by STT or the SHE. Regardless, the experiments performed here provide a guide in choosing a write-path

structure for a prototype device.

Perpendicular tunnel junctions were also examined, from a sheet film level using CIPT and also in patterned pillars. We achieved a TMR of 138% for high-RA MTJs that exhibit a slight enough voltage bias dependence perfect for operation in mLogic circuits. Although these results are not up to par with industry's top-of-the-line devices, our MTJs suffice for demonstrating the concept of an mCell. It is not difficult to foresee integration of high quality MTJs with improvements in fabrication equipment and facilities. The materials, thicknesses, and deposition conditions used in this read-path development study will be applied directly to a device prototype.

The utility of the FeCo- and FeCoB-based oxides remains a question. Although sufficient magnetic coupling was observed, it is as of yet unknown whether these materials are sufficiently resistive (RA roughly 10x that of the MTJs) at the small thicknesses required. Further work in this area must be undertaken, as discussed in the last chapter of this thesis.

6 Logic Device Prototype

In this chapter we discuss the results of experiments in which the read- and write-paths described in the previous chapter were integrated into a device prototype. We demonstrate that pulsed current in a device's write-path yields a change in the resistance state of its read-path, the fundamental concept behind the mCell that was first introduced in Chapter 2.

6.1 SHE-Domain Wall Motion mCell (SHEDW-mCell)

Building an mCell involves the integration of the DWM write-path, the MTJ read-path, and the oxide that magnetically couples but electrically insulates the two. This is no easy task, as the best properties or films for one do not necessarily mesh well with those for the other; for example, a thick oxide is preferable for maximum electrical isolation, but this would break the coupling between read- and write-paths. There are film and growth issues as well. The FeCoB in the read-path needs to be grown on Ta for optimal properties, and so a layer of Ta must be deposited on top of the magnetic oxide. The presence of this non-magnetic metal may break the coupling through the oxide if it is too thick, as shown in Chapter 5.

To begin the integration process we first designed the structure shown in Figure 6.1. This prototype mCell includes a DWM-based write-path and MTJ read-path, with a thin layer of Ta between the two. The thin Ta (≈ 0.5 nm) layer still allows for coupling between the two paths, but it does not isolate them electrically. With such a structure we can demonstrate that current through the write-path can switch the resistance of the read-path by domain wall motion. Terminals can be left floating to simulate isolation between the paths. Of course, some current will diffuse into the read-path during the write operation because the FeCoB free layer is not isolated from the Co/Ni write-path. The FeCoB and Ta are thin compared to the write-path and its Pt under-layer, however, and so the “leakage” current is not anticipated to be large.

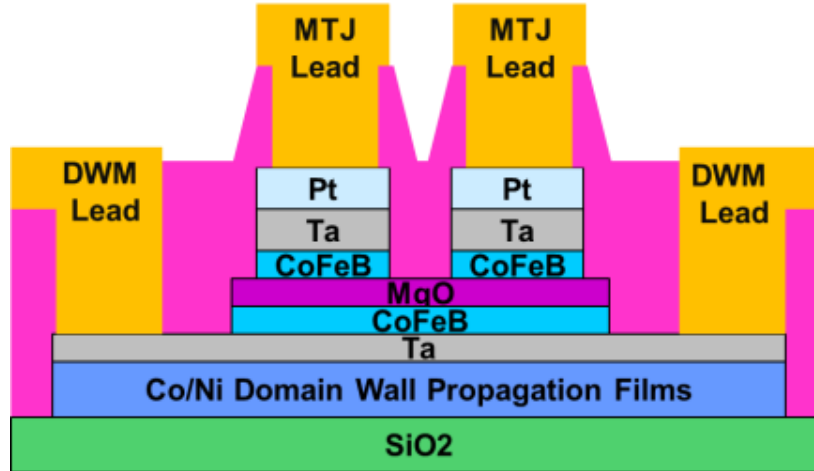


Figure 6.1 – Film stack/cross-section of first generation mCell prototype.

Optical images of a fabricated mCell prototype are shown in Figure 6.2. The device is 10 μm long and 1 μm wide; 500 nm wide devices were also fabricated on the same chip. A plan-view SEM of one such device is shown in Figure 6.3(a), with MTJ and write-path labels added for clarity. A cross-sectional TEM micrograph is shown in Figure 6.3(b), clearly depicting the roughly 275 nm separation between the two read-path MTJs on top of a continuous write-path. The high resolution TEM micrograph in Figure 6.3(c) shows the individual constituent materials are continuous and are of good quality.

Referring again to Figure 6.2, a domain wall injection wire is placed over the end of one side of the write-path. A large burst of current through the wire (resulting in a circulating Oersted field) can nucleate a domain wall in the Co/Ni (Figure 6.4). This is the same procedure used in Chapter 5 to nucleate domain walls in the test structures. A current pulse can then be injected in the write-path and the MTJ terminals probed to measure a resistance change.

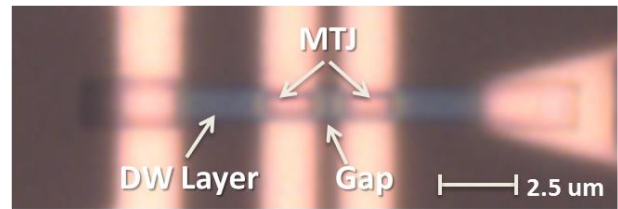
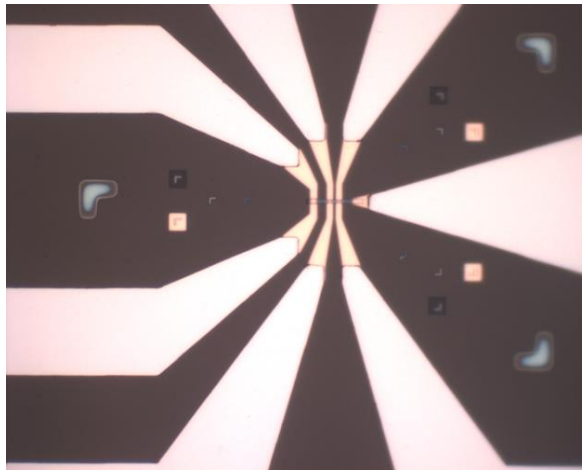


Figure 6.2 – Optical microscope image of completed mCell prototype with leads shown (left); close-up view of mCell prototype showing MTJ separation in the read-path (right). [Courtesy M. Moneck]

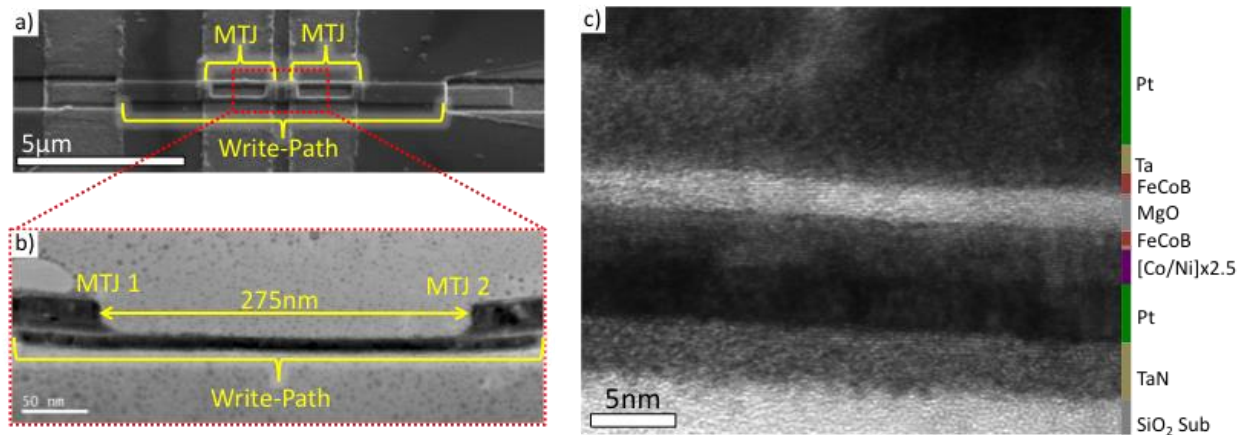


Figure 6.3 – (a) Plan view SEM image of prototype; (b) cross-sectional TEM image of prototype; (c) high resolution TEM image of the MTJ region of the prototype. [Courtesy J. Wu]

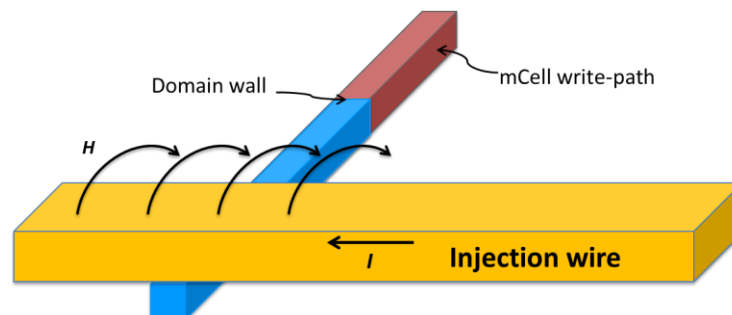


Figure 6.4 – The circulating field due to a current in the injection wire can nucleate a domain wall in the Co/Ni mCell write-path underneath.

Prior to testing the write- and read-paths simultaneously, individual tests were carried out similar to those described in Chapter 5. Figure 6.5 shows an R-H loop of an mCell read-path. Two switching events are observed, the first of which (at a field of approximately 300 Oe) represents the reference layer(s) aligning with the applied field. On one half, it appears that one reference layer switched just before the other, leading to a midpoint in the resistance where one MTJ in the read-path is in a parallel state and the other an antiparallel state. Once both MTJs are in an antiparallel state the resistance reaches a maximum. At a field of about 950 Oe, the free layer in the read-path (as well as the Co/Ni write-path it is coupled to) then switches, causing the MTJs to then enter a parallel, low resistance state; Kerr microscopy was used to confirm the 950 Oe switching event represented the free-layer and Co/Ni aligning with the field. Note that in these structures, the reference layer(s) actually switch at a lower field than the free layer, because the free layer is now coupled to the Co/Ni write-path. The TMR of these MTJs is only about 40%, in part because the annealing temperature was only 250 °C. The RA is quite large due to the thick tunnel barrier. Decreasing the thickness of the MgO barrier to approximately 1 nm brings down the resistance by orders of magnitude.

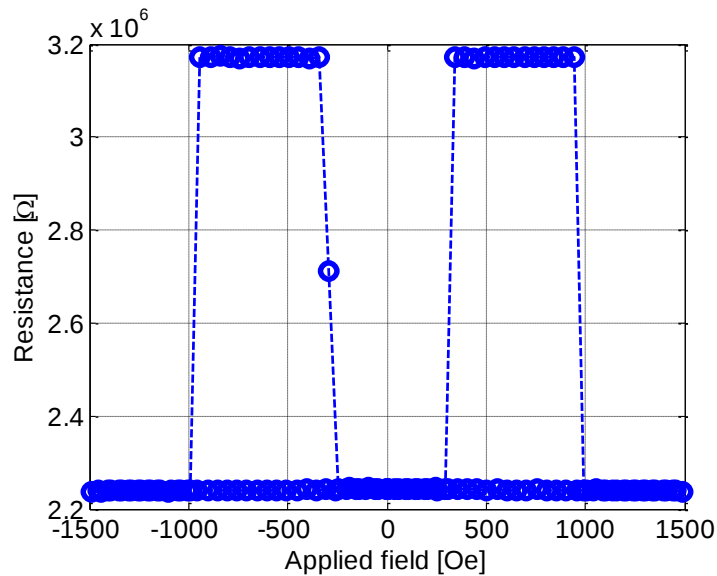


Figure 6.5 – R-H loop of mCell prototype read-path, demonstrating coercivity difference in reference layer (low coercivity switch) and free layer (high coercivity switch). The midpoint caught on the left half likely represents one MTJ reference layer switching earlier than the other.

Figure 6.6 shows the bias voltage dependence of the tunnel magnetoresistance ratio. The drop in TMR is not sharp, and given the low voltages required for mLogic, is not expected to be a

problem.

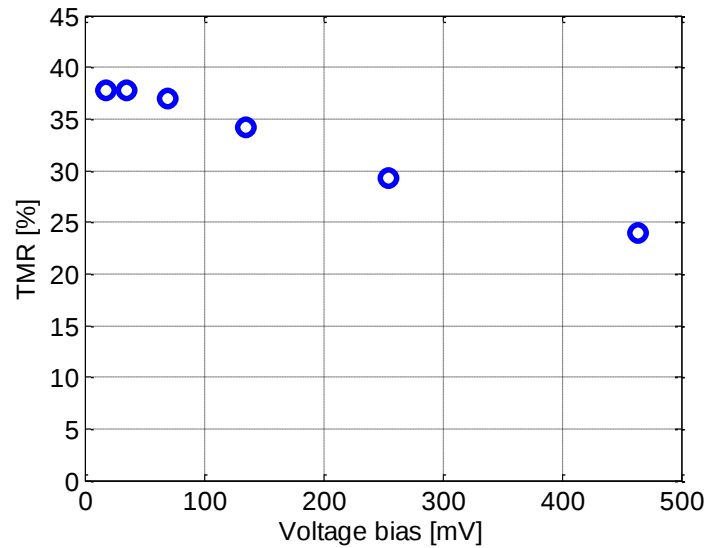


Figure 6.6 – TMR decreases as a function of bias voltage.

Additionally, we tested current-driven domain wall motion on a test structure fabricated on the same chip. The test structure is exactly the same as the mCell shown in Figure 6.2 but without the MTJ leads. Current pulses 50 ns long and on the order of 50 MA/cm² were applied after a domain wall was nucleated. Figure 6.7 shows a sequence of Kerr images of the domain wall motion; the first frame shows the initial location of the wall, the second shows the wall moving to/under the first MTJ, the third shows the wall appearing in between the two MTJs, and the fourth shows the domain wall reaching the end of the wire. A bias field of 50 Oe was applied to aid the domain wall motion under the MTJs; the motion could be purely current-driven in the parts of the wire that just include Co/Ni and/or FeCoB, but a field was required to assist motion under the MTJs themselves. It is likely that this is because of stronger-than-anticipated magnetostatic coupling between the reference layer and the free layer, which creates an energy barrier to domain wall motion when entering an antiparallel state. This can be fixed in future designs by adding a synthetic antiferromagnet (SAF) to eliminate the stray field of the reference layer.

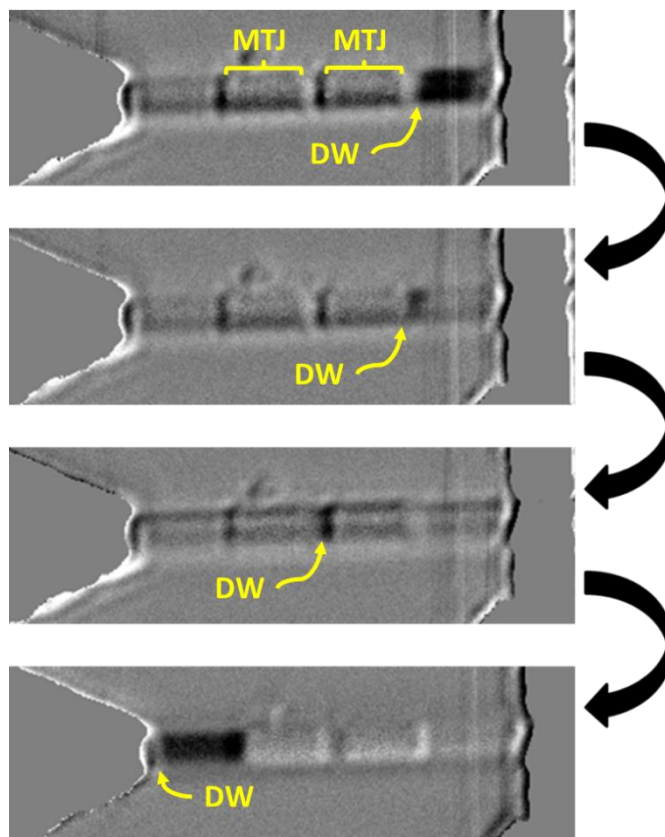


Figure 6.7 – Injected current pulses move a domain wall along the direction of the current flow in an mCell write-path.

The domain wall motion in Figure 6.7 is with the current flow, not the electron flow. As discussed in the previous chapters, if the motion were based on spin-transfer torque this would not be the case. The driving force of the domain wall motion in the test structures discussed in the previous chapter was most likely the spin Hall effect. The write-path design in this prototype is structurally similar, and as the DWM is again with the current flow we suspect the SHE is the dominant effect.

With confirmation that the read- and write-paths work individually, combined testing was undertaken. A domain wall was nucleated with a $1\ \mu\text{s}$, $\approx 100\ \text{mA}$ current pulse through the injection leads. An ohmmeter sourcing $10\ \text{nA}$ of current was then connected to the two MTJs in the read-path to measure the resistance while $50\ \text{ns}$, $1\text{--}5\ \text{mA}$ pulses (equivalent current density on the order of $10^8\ \text{A}/\text{cm}^2$) were injected through the write-path. During a pulse injection, the read-path was made floating, and likewise during a read-path resistance measurement the write-path was made floating. This prevents current from shunting away.

Figure 6.8 shows the resistance as a function of (an arbitrary amount of) time as the domain

wall in the write-path is driven through the device. Initially, the domain wall is in the state labeled “1”, where the domain wall is on the left of the device “outside” of the MTJs (low resistance). A current pulse is injected, bringing the device to the state labeled “2” where the domain wall is in the middle of the write-path, between the MTJs (midpoint resistance). A bias field of roughly 50 Oe was required here as well. A subsequent current pulse brings the device to state “3,” with the domain wall now at the other end of the device (high resistance). The test demonstrates the basic concept of an mCell: current pulsed into the write-path effects a resistance change in the read-path.

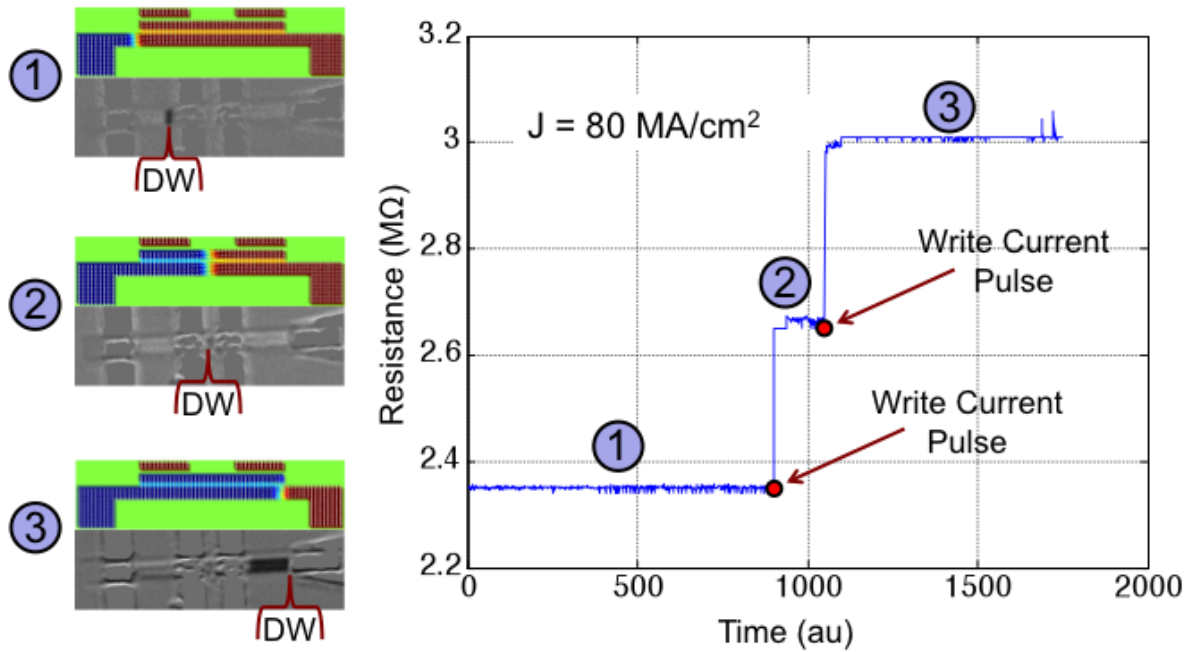


Figure 6.8 – Read-path resistance changes as the domain wall in the write-path is moved along with current. The resistance hits a midpoint when the wall is between the MTJs and increases to its maximum value when the wall moves under the second MTJ. Micromagnetic and Kerr images shown for domain wall location reference. The read-path resistance is large because of the thick (1.8 nm) tunnel barrier used in the prototype.

In some cases the switching was not as clean as that shown in Figure 6.8. For example, Figure 6.9 shows the same type of test on a different device, but this time current is injected in the opposite direction once the wall reaches the end to return it to its initial position (putting the device back in a low resistance state). No field is applied during the return, because the field was only required to help the domain wall switch the free layer antiparallel to the reference layers, and now the free layer is returning to a parallel state. Interestingly, many intermediate resistance values are observed, particularly during the wall’s journey back to its initial position. This seems

to indicate there are many pinning sites under the MTJs where the domain wall can get stuck, leaving an MTJ partially switched and causing intermediate values of resistance. The pinning would also have to be strong in order to overcome the magnetostatic coupling between the MTJ free layer and reference layer, which prefers a parallel orientation. The combination of applied field and current likely helped the domain wall skip past most of these pinning sites during the first part of the test. This characteristic was not observed in many devices.

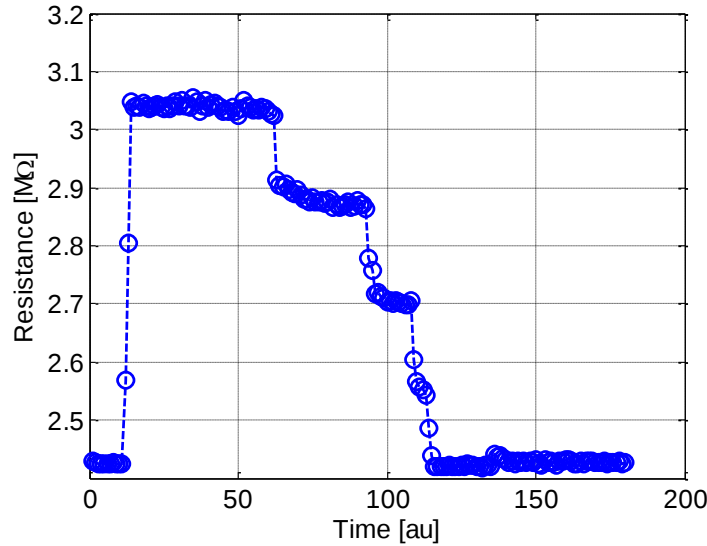


Figure 6.9 – Read-path resistance changes as the domain wall in the write-path is moved along with current. The resistance has many intermediate values between high and low points, likely due to wall pinning under the MTJs between current pulses.

The pinning sites under the read-path can also play a role in switching the device into an antiparallel state if the current density is too small. Figure 6.10 shows many more current pulses are required to switch the device for smaller current densities. This is likely due to the presence of pinning sites in the wire that also cause the behavior in Figure 6.9. A sufficiently large current pulse is able to overcome these pinning sites, such that a single pulse is all that is required to fully switch the device. In these experiments this current density is roughly 10^8 A/cm^2 .

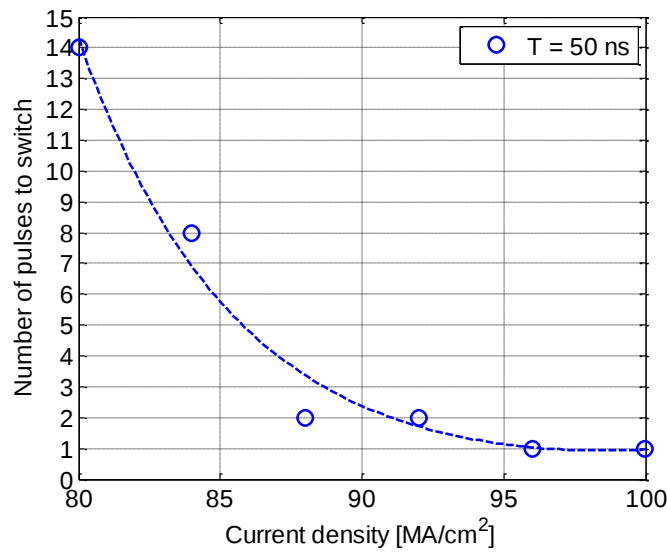


Figure 6.10 – Current densities of sufficient magnitude can overcome pinning under the read-path to fully switch the device with a single pulse.

With the ability to switch the device using a single current pulse, it becomes possible to test back-and-forth digital switching. Figure 6.11 demonstrates the device switching between high and low resistance states when negative and positive current pulses are applied, respectively. The switching is observed to be highly repeatable, with only a small fluctuation in read-path resistance between measurements. This result indicates that provided the current pulse is large enough, mCell switching can be very reliable.

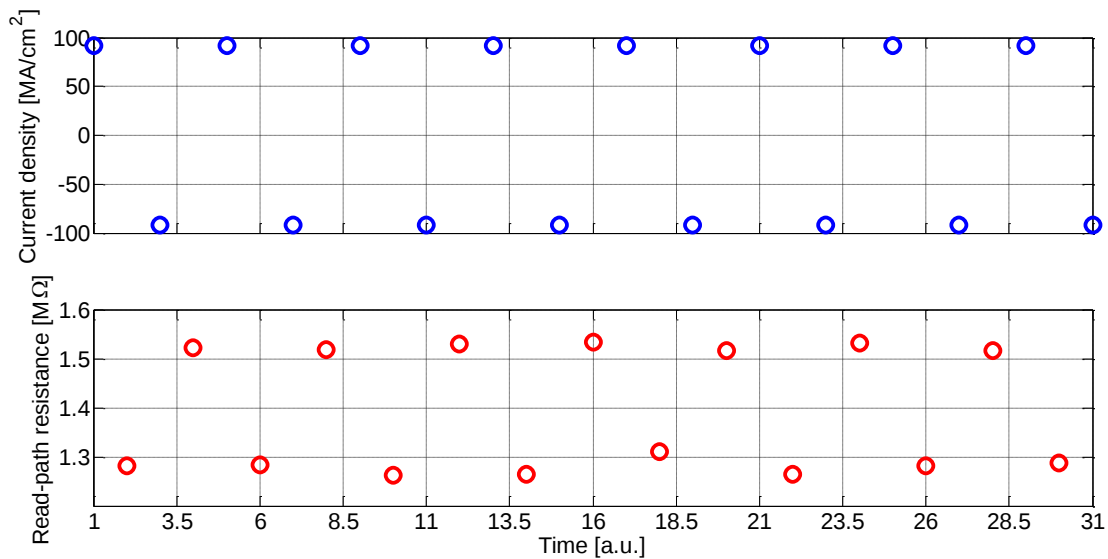


Figure 6.11 – Reliable digital switching of device is achieved, with a positive current pulse bringing the device into a low resistance state and a negative current pulse returning the device to a high resistance state.

Note that in Figure 6.11, the read-path resistance is roughly half the value of that in Figure 6.8. It is preferable that the devices have as low a read-path resistance as possible from an mLogic circuit standpoint. This allows for lower pClock voltages. Although the read-path of the mCell consists of two MTJs in series with a shared free layer, only one of the tunnel junctions is necessary; the same dynamic range is observed if one of the MTJs is replaced by an ohmic contact, and the overall resistance would be lower. To enable this, we purposely damaged one MTJ by applying 3 V between a read-path electrode and a write-path electrode (Figure 6.12(a)). The large voltage shorted out the tunnel barrier, creating a low resistance contact between that read-path electrode and the free layer (essentially creating the read-path in Figure 6.12(b)).

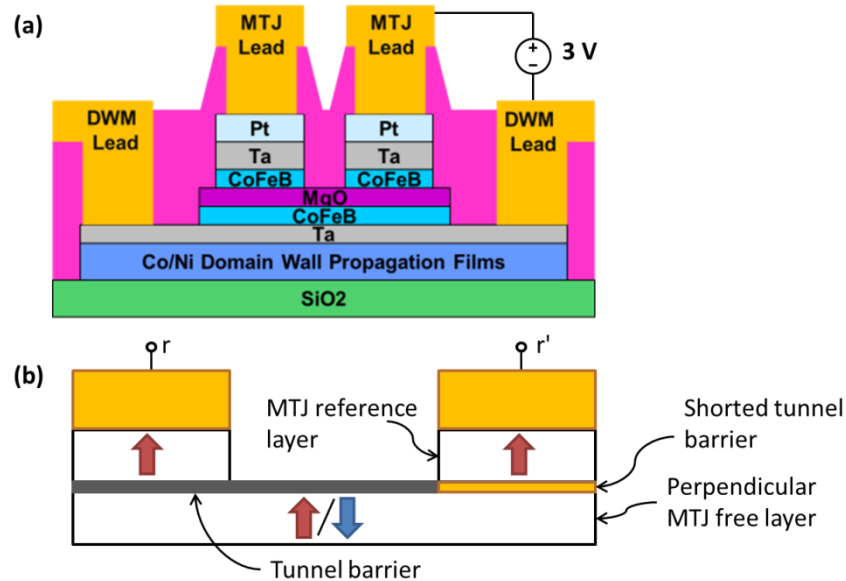


Figure 6.12 – A large voltage applied between an MTJ electrode and neighboring write-path electrode, as shown in (a), creates a read-path like that shown in (b), where the tunnel barrier under the blown MTJ becomes a short.

6.2 Conclusions

In this chapter we have detailed our experimental work in realizing the first generation mCell prototypes. We intended to demonstrate the basic concepts of mCells and successfully observed that current-induced domain wall motion in a write-path could switch the resistance state of a separate MTJ-based read-path via magnetic coupling. Although representing a good start, this device is lacking in terms of being a useful circuit element. First, it does not have electrically isolated read- and write-paths, the key feature of the mCell black box that makes it appropriate

for circuit design. The read-path resistances are also enormous, roughly four orders of magnitude higher than desired. A bias field is required to initiate state switching, and the magnetostatic coupling between the MTJ reference and free layers is problematic. In short, this is not a demonstration of a complete device suitable for mLogic fanout or memory. Additional development to improve these issues is necessary. This work is ongoing as summarized in the following chapter.

7 Conclusions and Future Work

With the cost benefits of CMOS scaling coming to an end and the lack of a single device to replace transistors, it is likely that future electronics will be made from a variety of technologies targeted toward specific applications. In this thesis we have explored a class of magnetic logic devices, “mCells,” in an attempt to understand how well these devices could perform in order to establish whether or not they could fill a niche for non-volatile electronics designed to operate at low voltages. We now provide some concluding remarks to summarize our work and discuss the viability of mCell technology for the aforementioned logic and memory applications. We will also discuss future work plans for this project.

7.1 Summary

7.1.1 STT-mCell

Through micromagnetic simulation we have observed that it is possible to reliably switch a domain wall-based device by pulsing $2\text{-}5 \times 10^7$ A/cm² current pulses for 2-4 ns. This critical current density remains roughly constant as the device width decreases, implying the absolute current requirement scales linearly with device width. For highly-scaled devices (e.g., 10-20 nm wide), these currents can be as low as 10 μ A. Although lower critical currents are always desirable, a 10 μ A target still leaves mCells as a viable candidate for use in logic and memory. For example, STT-MRAM is expected to reach a write energy of 20 fJ/bit by 2017 (at the 16 nm node) when perpendicular MTJ technology matures, assuming 250% TMR and 16 μ A write current [63]; the mCell-based MRAM introduced in Chapter 2 requires about 5 fJ/bit for 10 μ A (roughly 25 MA/cm² current density), 2 ns current pulses through 130 Ω write-paths with just 100% TMR (but at a lower RA product, 2.5 $\Omega \cdot \mu\text{m}^2$ for STT-MRAM compared to about 1 $\Omega \cdot \mu\text{m}^2$ for mCell-MRAM).

Experimental work to date has shown existing materials have properties and performance compatible with mCell design requirements. Oxidized FeCoB accommodates strong coupling and was found to be resistive enough to be integrated with the mCell. FeCoB/MgO/FeCoB MTJs are also easily integrated in an STT-mCell structure. We have not, however, prototyped a structure based on STT domain wall motion. This is certainly possible, and could be an important

step moving forward given the promising modeling results based on spin-transfer torque.

7.1.2 SHEDW-mCell

The SHEDW-mCell seems to require larger switching currents to operate compared to the STT device based on micromagnetic simulation. However, efficient SHE-based motion leads to velocities far greater than what is achievable with STT at similar current density. These devices can be switched in sub-ns time, implying they may be useful for applications in which non-volatility and performance are critical. Like the STT-mCell, this device can theoretically be scaled to very small sizes and maintain thermally stable.

SHE-driven write-path structures based on Co/Ni multilayers were designed to test this device. We found that with a thin Ta cap and a Pt under-layer, domain walls in multilayer Co/Ni films could move with velocity above 100 m/s. Using this structure and the perpendicular MTJ work, we fabricated prototype SHEDW-mCells for proof of concept demonstration purposes. We showed that these devices can be reliably digitally switched between high and low resistance states by injecting current back and forth through the write-path.

7.1.3 Single Domain, In-Plane mCell

Micromagnetic simulation indicates that the single domain, in-plane mCell device performs at a similar level to the DW-based device in terms of current density and switching time. $5\text{-}10\text{e}7$ A/cm² current pulses allowed for switching in 1-3 ns, even for devices designed to maintain a large energy barrier (above 55 k_BT). Desirable values for write-path thickness and saturation magnetization, oxide thickness and coupling strength, and free layer thickness are all in range with what is achievable based on current materials.

A problem with this device, however, is the write current needs to be applied across an inherently wide area. The device cannot be scaled to very small widths (e.g., anything below 40-50 nm) without sacrificing stability. Although the required current density is similar to what is observed in the DW-based device, this unfortunate characteristic implies higher currents are required to operate. The output current of one gate with pull-up resistance R_{PU} and pull-down resistance R_{PD} driving a gate with series write-path resistance R_L can be expressed as

(7.1)

$$I_{out} = V_{pclk,\pm} \left(\frac{\frac{1}{R_{PU}} - \frac{1}{R_{PD}}}{1 + R_L \left(\frac{1}{R_{PU}} + \frac{1}{R_{PD}} \right)} \right)$$

Increasing the magnitude of the output current of a gate, which is used to switch fanout devices, implies the pClk voltage must be increased. One fortunate aspect of having a wider device is that the write-path resistance will be smaller, which does help lower the voltage requirement when trying to maintain a certain current density. For example, assuming $R_{PU} = 1.25 \text{ k}\Omega$ and $R_{PD} = 2.50 \text{ k}\Omega$, it takes $\pm 28 \text{ mV}$ to drive $10 \text{ }\mu\text{A}$ of output current through a $100 \text{ }\Omega$ load versus $\pm 128 \text{ mV}$ to drive $50 \text{ }\mu\text{A}$ through a $20 \text{ }\Omega$ load, slightly less than a 5x increase in pClock voltage in response to the 5x increase in required current. Clearly, though, this is still not enough to make the use of a bigger device preferable for logic.

7.2 Future Work

7.2.1 Second Generation DW-mCell

A second device prototype was designed to address the issues with the first generation prototype in the previous chapter. The tunnel barrier thickness was reduced to 1 nm , and 1 nm of FeCoB-Ox was inserted between the read- and write-paths. Additionally, the tunnel junction reference layers were patterned to taper off towards the end of the devices (Figure 7.1) in order to reduce the fringing field on the domain wall when it attempts to enter the read-path. This modification could help obviate the need for a bias field in moving the domain wall underneath the read-path. Unfortunately, equipment limitations prevented us from incorporating a SAF, which would have helped a great deal in reducing the reference layer stray field.

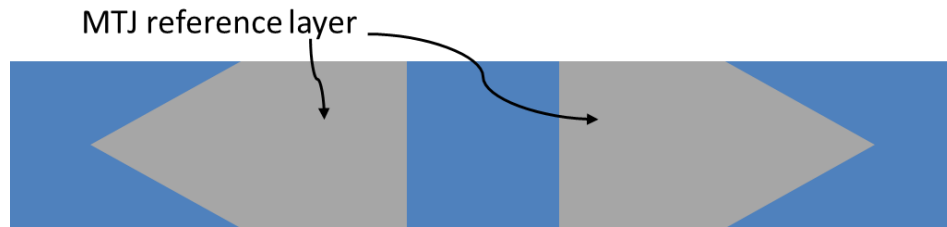


Figure 7.1 – Illustration of reference layer tapered patterning to help reduce the stray field on the domain wall.

The purpose of this round of devices is to demonstrate the concept of the memory bitcell

introduced in Chapter 2, but perhaps more fundamentally, to show that mLogic-style current steering through tunnel junctions and write-paths is feasible. The circuit is shown below in Figure 7.2, where m1 and m2 comprise an inverter (scratch buffer in the context of a full memory array) and m3 is a storage cell. An input current I_{IN} programs the state of the inverter. pClkA is then asserted, causing a direction of current flow through m3's write-path based on the relative read-path resistances of m1 and m2. Once programming of m3 is complete, pClkA is shut off and pClkB, a sense voltage, is applied to m3's read-path. This causes an output current, the magnitude of which represents m3's read-path resistance and therefore, its logic state.

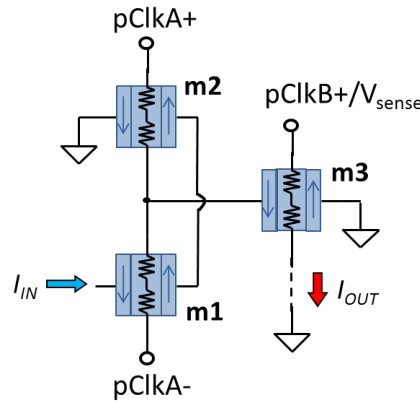


Figure 7.2 – Memory bitcell proof of concept circuit fabricated for second round device testing.

In order for the current steering to work efficiently, the MTJs must be optimized for low resistance and high switching ratio. A 1 nm tunnel barrier was chosen to enable greater yield, and as a result the driving devices (m1 and m2 in Figure 7.2) must be upsized to compensate for the expected RA of about $1 \text{ k}\Omega \cdot \mu\text{m}^2$. The precise size needed depends on the TMR of the MTJs and the required current level. Figure 7.3 shows that increasing the driver width yields diminishing returns (i.e., small increases in steered output current) beyond $5 \mu\text{m}$ for the anticipated TMR (40-60%). From the figure we also observe the steered output current density (10^6 - 10^7 A/cm^2) is not as large as that sourced from the pulse generator (10^8 A/cm^2) in the domain wall motion and previous device prototype experiments. This essentially brings the probability that nano- or micro-second pulses of current (from pulsing pClkA in Figure 7.2) will correctly switch the output device's state to 0. To compensate for this, pClkA in Figure 7.2 will be applied for very long times, most likely on the order of 1-10 seconds. Applying a smaller current for a longer time can help demonstrate the bitcell/current steering concept.

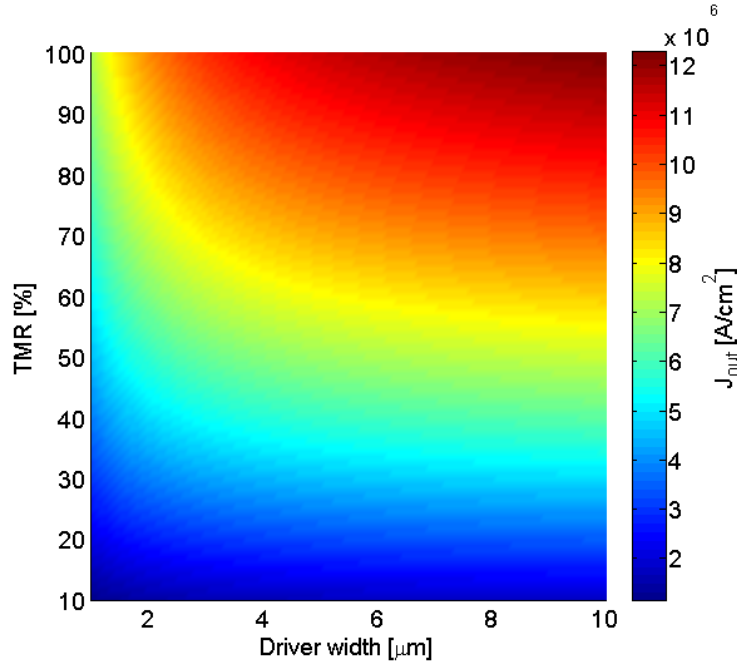


Figure 7.3 – Increasing driver size and MTJ TMR leads to increased output current steered through the fanout mCell write-path.

Testing results for this round of devices is pending fabrication.

7.2.2 Improving Magnetic Tunnel Junction Properties

The most difficult challenge we faced when fabricating the device prototypes was integrating a high TMR, low RA MTJ. In fabricating the read-path, an etch step is required to separate and define the two MTJs that share the same free layer. An ion mill equipped with an endpoint detector was used to determine when to stop the etch, which is (ideally) when the FeCoB forming the reference layers has been etched away and the MgO tunnel barrier is exposed. In practice, it is difficult to control the etch precisely. Using a thicker tunnel barrier helps ensure that if the etch is performed for too long, the underlying FeCoB that constitutes the free layer will remain undamaged. Although making the fabrication process more reliable, this drastically limits any practical use of the mCell. A 1.8 nm tunnel barrier yields resistances in the MΩ range, four orders of magnitude too large to accommodate the current steering required for mLogic. Future work must be devoted to studying the etch process and ensuring a thinner (e.g., 0.8-1.0 nm) tunnel barrier can be integrated.

Aside from reducing the RA, the TMR of the devices needs to be improved. We have already begun to address this issue, and are currently working on lowering the base pressure used in the

deposition and increasing the annealing temperature of the structures. Whatever methods are applied, improving the MTJs is one of the most critical tasks in making mLogic a reality. Figure 7.4 illustrates this point for the simple case of an inverter driving 10 μA of current through a 1000 Ω load. The pClock voltages can be well under 100 mV if the MTJs have a low enough RA and/or high enough TMR. Similar analysis on more complex gates (with the same conclusions) can be found in Chapter 4 of [15]. It is worth noting that industry values for TMR and RA are significantly better than those achieved here at CMU, implying that more advanced fabrication facilities and processes could yield substantially better results.

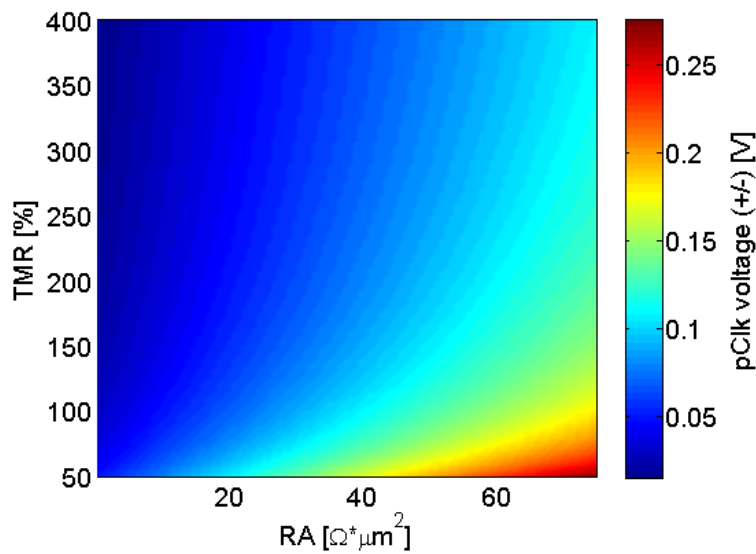


Figure 7.4 – pClk requirement decreases for high TMR and low RA. A critical current of 10 μA driven through a 1000 Ω load by an inverter was assumed in this calculation.

7.2.3 Exploring Perpendicular Insulators

As discussed in Chapters 3-5, the insulating materials used to separate the read-path from the write-path are generally in-plane by default. If we make the interlayer too thick or the write-path too thin, the interlayer will not reliably couple the two perpendicular materials on either side. Finding a material that exhibits a strong perpendicular anisotropy and is also highly resistive (e.g., RA at least 10x higher than the RA of the MTJs) would play an important role in expanding the material and size choices to enable more efficient devices. It would enable us to use a thicker interlayer for better electrical isolation in addition to a thinner write-path for lower current operation.

7.2.4 Incorporation of Magnetic Studs

For the domain-wall based devices the write-path terminals are supposed to be magnetic studs polarized in opposite directions to establish the domain wall. All fabricated test structures and devices based on domain walls in this thesis used a current-carrying wire to nucleate walls instead. This was done primarily because it is not feasible for the studs to be integrated into a device with our fabrication equipment. Ultimately, it will be necessary to determine how to properly size the studs such that when subjected to fields of different strengths one will go “up” and the other “down” in each device (with 100% probability). Industry experiments on the three-terminal MRAM device (section 2.1) indicate this is achievable [19]. A significant advantage of the single-domain SHE devices is that they do not require these magnetic write-path terminals.

7.2.5 Single-Domain Device Scalability – In-Plane vs. Perpendicular

Both the hard drive and the MRAM communities have established that highly-scaled magnetic technologies are more easily achievable with perpendicular films. In this thesis we presented a single-domain device with in-plane magnetization. Perpendicular films were not initially considered because the spins injected into the write-path (based on the device geometry) via the SHE are polarized in the plane of the film. However, it is possible to integrate perpendicular films instead that are still digitally switched by the SHE, provided a bias magnetic field is applied [70],[71]. The field must be aligned along the direction of the current flow. Reversing the direction of the field changes how the device switches in response to the current direction, but from a circuits perspective the field never needs to be reversed. This makes perpendicular single-domain devices switched by the SHE not an impractical option to consider. Perhaps a chip could be housed in a magnetic package, or bias magnets integrated into every device, as shown in Figure 7.5 where the fringing field of an embedded thick permanent magnet biases the write-path longitudinally (the direction in which the write current flows between w^+ and w^-).

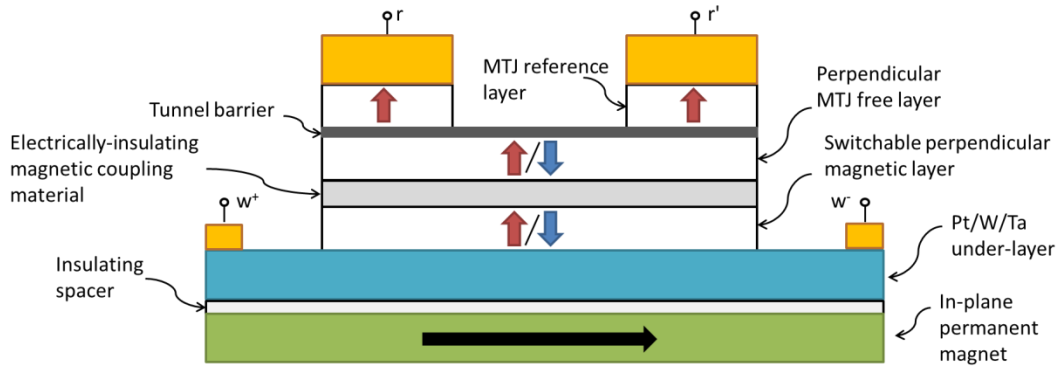


Figure 7.5 – Illustration of single-domain perpendicular device driven by the SHE. A permanent magnet is embedded underneath the device to bias the write-path longitudinally.

7.2.6 Exploring New Applications

In Chapter 3 it was noted that the switching probability could be increased by margining the input current and pulse width. The simulations in this thesis were intended to help extract important design factors (e.g., how thick to make the write-path, what coupling strength does the oxide need to have, etc.), but the critical current densities given were for a switching probability of 95% of only 100 trials. More simulations must be carried out to better capture the switching distributions due to thermal fluctuations. As of this writing it is unclear if switching can be made to have a very low (e.g., 10^{-9}) error rate. Increasing the pClock magnitude and pulse width, in addition to applying the same pulse more than once, can all help to increase the switching probability at the expense of increased energy. However, there are some applications where this stochastic switching can be tolerated, or even exploited, that are worth considering for mLogic.

Some groups have proposed to use the stochastic behavior of deep submicron CMOS transistors to implement probabilistic logic and algorithms [72]-[74]. They demonstrate that these algorithms can be implemented with excellent energy efficiency, provided the probability of error in the devices is well-characterized. One example is a probabilistic neural network, which can be implemented much more efficiently with truly random switches (bits) than with software-implemented pseudo-random bits [75]. Bayesian inferencing and encryption have also been targeted as applications that could benefit from probabilistic devices [72]-[74]. mCells may be an excellent choice to implement these algorithms because the switching probability can be well-controlled by varying the write current and pulse width. This is doubly beneficial from an energy standpoint, since using smaller currents (to bring the probability of switching down from

$\approx 100\%$) cuts the pClock voltage requirements.

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