Design Techniques for Frequency Reconfigurability in Multi-Standard RF Transceivers

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Rahul Singh

B.Tech., Electronics Engineering, Indian Institute of Technology (BHU), Varanasi
M.Sc., Electrical Engineering, Seoul National University, Seoul

Carnegie Mellon University
Pittsburgh, PA

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Abstract

Compared to current single-standard radio solutions, multi-standard radio transceivers enable higher integration, backward compatibility and save power, area and cost. The primary bottleneck in their realization is the development of high-performance frequency-reconfigurable RF circuits. To that end, this research introduces several CMOS-integrated, transformer-based reconfigurable circuit techniques whose effectiveness is validated through measurements of designed transceiver front-end low-noise (LNA) and power amplifier (PA) prototypes.

In the first part, the use of high figure-of-merit phase-change (PC) based RF switches in the reconfiguration of CMOS LNAs in the receiver front-end is proposed. The first reported demonstration of an integrated, PC-switch based, dual-band (3/5 GHz) reconfigurable CMOS LNA with transformer source degeneration and designed in a 0.13 µm process is presented.

In the second part, a frequency-reconfigurable CMOS transformer combiner is introduced that can be reconfigured to have similar efficiencies at widely separated frequency bands. A 65-nm CMOS triple-band (2.5/3/3.5 GHz) PA employing the reconfigurable combiner was designed.

In the final part of this work, the use of transformer coupled-resonators in mm-wave LNA designs for 28 GHz bands was investigated. To cover contiguous and/or widely-separated narrowband channels of the emerging 5G standards, a 65-nm CMOS 24.9-32.7 GHz wideband multi-mode LNA using one-port transformer coupled-resonators was designed. Finally, a 25.1-27.6 GHz tunable-narrowband digitally-calibrated merged LNA-vector modulator design employing transformer coupled-resonators is presented that proposes a compact, differential quadrature generation scheme for phased-array architectures.

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1 Introduction

1.1 Motivation and overview

A significant portion of a modern cell-phone radio transceiver is implemented using the standard CMOS (complementary-metal-oxide-semiconductor) technology. In current practice, illustrated in Figure 1.1(a), several dedicated, non-reconfigurable (a single unit optimized for operation only at a single standard) CMOS RF sub-blocks (for example, power amplifiers (PAs), low-noise amplifiers (LNAs), voltage-controlled oscillators (VCOs)) are employed in order to meet stringent performance requirements of the burgeoning number of cellular and wireless standards. With the rapid development of newer standards that aim to achieve higher data-rates while requiring backward compatibility, current radio solutions are forced to adopt the brute-force approach of adding new hardware for each additional narrowband frequency. Understandably, this non-scalable approach, due to its high cost and complexity, has reached its limit. We therefore seek a 'universal' solution: a multi-standard, multi-band CMOS transceiver (Figure 1.1(b)) that enables higher integration, saves power, area and cost, and facilitates a more efficient use of the available frequency spectrum [1].
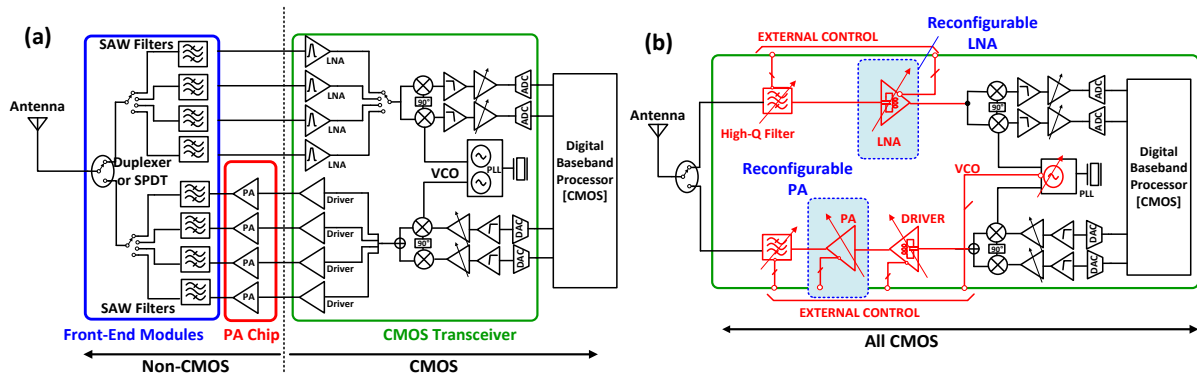
Figure 1.1 (a) Conventional multi-band radio transceiver. (b) Frequency-reconfigurable, all-CMOS integrated radio.
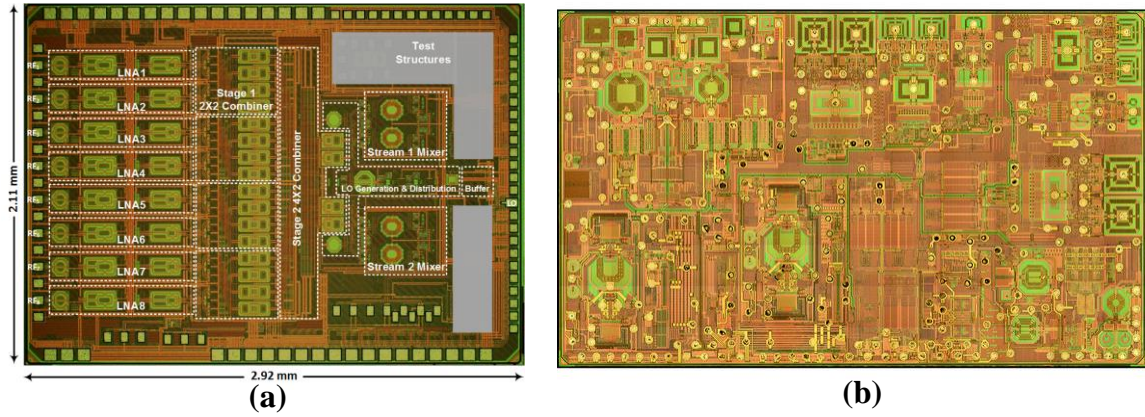
Figure 1.2 Modern RFIC designs employ dozens of inductors/transformers: (a) state-of-the-art 8-channel beamforming MIMO receiver in 65-nm CMOS [85], (b) (not drawn to scale) Qualcomm's multi-band multi-mode RF transceiver (RTR8600) (Image taken from: https://www.ifixit.com/Teardown/Apple+A6+Teardown/10528).

The primary bottleneck in realizing multi-standard transceivers is the requirement of frequency-reconfigurable RF circuits. Front-end RF blocks such as LNAs, VCOs and PAs comprise resonant circuits requiring passive structures like inductors, transformers and capacitors with high quality factors. Switching the resonant frequency of these circuits without degrading their quality factor requires the availability of a switch which simultaneously features low loss, low parasitic capacitance and additionally, high-power handling capability for large signal applications. As such, the path to achieving RF reconfigurability without incurring serious performance degradation and other functionality issues is still an open problem.

Before addressing reconfigurability in RF designs, it is worthwhile to consider the primary building blocks and a key enabling technology of modern RFIC design – integrated inductors and transformers. Figure 1.2 shows the die photos of two state-of-the-art RFIC chips – an 8-element beamformer receiver operating at 28 GHz [85], [119], and a complete multi-band Qualcomm transceiver for 3G/4G radio standards. Note the extensive use of on-chip inductors and transformers in both chips. Notably, the beamformer receiver chip of Figure 1.2 references the study of transformer coupled-resonators presented in Chapter 4 of this thesis.

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At sub-GHz frequencies, on-chip realization of inductors and transformers was impractical and economically infeasible due to the prohibitively large size of passives required (silicon area is expensive): however, this was no longer a constraint at cellular radio frequencies, and with research and development towards developing CMOS processes with higher quality passives (higher BEOL metal stacks, high resistivity substrate etc.), and advent of fast electromagnetic simulators, current RFIC designs at GHz frequencies extensively use of CMOS-integrated inductors and transformers [2]. Integrated transformers are especially versatile and their use has resulted in the development of several new and high-performance RFIC designs. While inductors are most commonly used in narrowband *LC* tanks in LNAs, VCOs, mixers and as a choke in PAs (to double the output voltage swing and consequently, boost the efficiency), transformers have been used as bandpass loads of amplifier stages with superior gain-bandwidth product (GBW), in active mixers to boost conversion gain and reduce noise figure by isolating the transconductor and switching stages, to stabilize amplifiers through transformer feedback, in multi-band and wideband VCOs, in PAs for power-combining, impedance transformation and inter-stage matching, and as integrated baluns [2]. It would be fair to say that the versatility of transformers and their use in integrated CMOS RFICs has injected fresh life into the art of RF circuit design. In fact, a look at the papers in the Wireless sessions of ISCCC (The International Solid-State Circuits Conference, the premier IEEE conference on solid-state circuits) in the recent years highlights the myriad and creative ways in which transformers have been used in RF designs that push the state-of-the-art each year. Moreover, with the recent focus on the mm-wave frequency spectrum, especially in context of the emerging 5G wireless standards [3], the use of integrated transformers will become more and more ubiquitous as size of passives at mm-wave frequencies is no longer a cause of concern [4].

This research explores the use of integrated transformers to solve the circuit challenges of designing reconfigurable RFIC designs and introduces several CMOS-integrated, transformer-based techniques whose effectiveness is validated through measurements of designed transceiver front-end low-noise (LNA) and power amplifier (PA) proof-of-concept prototypes. Specifically, we adopt two different approaches in this work. Firstly, we explore 'more-than-Moore' CMOS-compatible approaches and investigate the use of four-terminal phase-change (PC) RF switches in the design of CMOS LNAs. As a result, a novel dual-band reconfigurable LNA with transformer degeneration was developed, which led to the demonstration of the first CMOS-PC integrated LNA [5], [6]. This work is also being extended to develop a complete quad-band CMOS receiver over a 2-18 GHz range, and integrated with a multitude of RF PC switches (currently in development, with block level details in Chapter 6). Like the narrowband LNA, the design is targeted to achieve circuit performance comparable to standalone narrowband receivers. While the first part of thesis motivates the possibility of high-performance and complex CMOS-PC field-programmable transceivers, we also investigate CMOS-only transformer-based circuit techniques for frequency-reconfigurable transceiver front-ends in the second part of this work. While LNAs are a small-signal RF block, we explored frequency reconfigurability in a large-signal block like the power amplifier. Designing a switchable output network in a PA is challenging due to the large voltage/current stand-off requirements. To address this, we propose a novel transformer combiner for use in a frequency reconfigurable near-watt-level CMOS PA design, where regular CMOS switches can be inserted at adjacent, low-swing nodes which drastically reduces the voltage stand-off requirements. Notably, the proposed design can work equally work with PC switches which have demonstrated promising power handling capabilities; however, high-power PC switches are still under active study.

In the final part of the work, we investigate the use of transformer coupled-resonators in mm-wave LNA designs for the upcoming 5G bands. While numerous bands between 20 and 100 GHz have been identified for commercial use, there is high current interest in several bands between 20 and 30 GHz including 27.5-28.35 GHz (USA), 24.25-27.5 GHz (Europe), 25-29 GHz (Latin America), and 26.5-29.5 GHz (Asia) [3]. However, emerging 5G standards stipulate channel bandwidths below 500 MHz thereby making both frequency-tunable low fractional bandwidth designs and wideband high fractional designs (to simultaneously cover contiguous wideband-separated narrowband channels of the diverse 5G spectrum) probable. It should be noted that while wideband LNA solutions are compact, they have higher noise figures (lower sensitivities) and high linearity requirements (they amplify interfering signals along with the main signal). While both approaches have their pros and cons, a choice between a frequency-tunable design (which suffers from a performance-tunability trade-off) and a wideband design (lower NF, higher linearity requirement) often involves a careful system level evaluation of the intended application and the associated overheads. Without making a case for one over the other, this work explores both wideband and narrowband LNA designs using transformer coupled-resonators. While examples of the use of transformer coupled-resonators in LNA designs are abundantly available in literature, this work identifies hitherto unexplored properties of coupled-resonators, and demonstrates their applications to mm-wave LNA designs.

1.2 Thesis Contributions and Organization

The specific contributions of this thesis and its organization are detailed below:

1) **Frequency reconfiguration of RF circuits using PC switches:** In Chapter 2, it is demonstrated that by using GeTe-based PC switches with high cut-off frequencies (F_{CO}), parasitic-sensitive narrowband RF CMOS circuits such as an LNA can be stably and

reversibly reconfigured across disparate frequency bands, while simultaneously achieving RF performance approaching that of non-reconfigurable CMOS-only implementations. A compact, dual-frequency narrowband low-noise amplifier reconfigured using a four-terminal phase-change RF switch was designed and fabricated. Extensive characterization of several prototypes is presented demonstrating robustness and repeatability of the PC switch reconfiguration. This work was published in [5], [6] and [7]. [7] was co-authored with Greg Slovin (CMU) as the lead author.

2) **Frequency reconfigurable transformer combiner for CMOS PAs:** In Chapter 3, a frequency-reconfigurable transformer combiner is proposed with adjacent low swing nodes where switched tuning capacitors with regular CMOS switches can be used to realize multi-band operation. The design of a high-power switched capacitor and a triple-band CMOS PA incorporating the proposed transformer combiner is also presented. Measurement results of the triple-band (2.5/3/3.5 GHz) PA chip showed good frequency selectivity; however, when compared to simulations, a reduction in the PA's small and large signal performance was observed. Post-measurement analysis investigations identified probable causes of reduced performance in measurements. This work was published in [8].

3) **Wideband mm-wave LNA design using one-port transformer coupled-resonators:** In Chapter 4, the design of a multi-mode, wideband, low-noise amplifier (LNA) and receiver in a 65-nm process using the driving-point impedance (Z_{11}) of one-port transformer coupled-resonators is described. Design guidelines and insights are presented for the use of Z_{11} as a wideband load. Nested-layout transformers are shown to simultaneously minimize area and flatten the Z_{11} response. The effectiveness of the proposed design techniques is demonstrated through measurements of 28-GHz LNA and quadrature

receiver prototypes. This work will be submitted for publication [9]. Referencing the work presented in Chapter 4, [85] and [119] (co-authorship with Susnata Mondal, CMU as the lead author) extensively uses transformer-coupled resonators in the design of wideband gain stages in its receive path.

4) **Narrowband Merged LNA-Vector Modulator transformer coupled-resonators:** In Chapter 5, the use of wide tuning range and narrowband compact vector modulators for emerging 5G phased-array receivers is proposed. A low-Q coupled-resonator load in the LNA is used for quadrature generation, thereby avoiding the need for an explicit quadrature hybrid and facilitating an ultra-compact design. The use of phase-invariant PGAs with constant input capacitance following the LNA ensured low RMS gain and phase errors. An on-chip calibration loop is also implemented which adjusts the coupled-resonator's capacitance to generate quadrature I/Q outputs at any desired frequency in the band. This work was originally published in [10].

5) Finally, Chapter 6 concludes the thesis and identifies future directions of this work.

2 Frequency Reconfiguration of RF Circuits Using PC Switches

2.1 Introduction

Phase change (PC) chalcogenide materials like GST ($Ge_xSb_yTe_z$) and germanium telluride (Ge_xT_y) are able to undergo stable, rapid and thermally-actuated reversible phase transitions between their disordered amorphous and ordered crystalline states [11]. The two phases exhibit different reflectivities and conductivities, which has been exploited in both the optical storage and the digital non-volatile memory industries respectively [12]. In either case, the phase transition is initiated by a heating pulse followed by a cooling process. For example, in electronic PC memories, a high-intensity short dc pulse raises the PC material's temperature above the melting point due to Joule heating (I^2R) from an adjacent resistive metal electrode. Subsequent rapid quench cooling locks the atoms in a high resistance amorphous state. In contrast, lower intensity pulses of longer duration allow the PC material sufficient time for crystal growth resulting in a locally ordered low resistance state [13]. A key advantage offered by PC memories is their zero steady-state power consumption: energy is expended only to accomplish the phase transitions while the amorphous/crystalline states themselves are stable and non-volatile.

In addition to memory technology, PC materials have recently been used to develop high-performance, non-volatile RF switches for use in frequency agile RF modules [14]-[23]. In contrast to PC memory where switching speed and memory density are paramount, an RF switch also requires extremely low on-state resistance ($R_{ON} \sim$ 1-2 Ω) to minimize insertion loss and quality factor degradation (when used to switch passive inductors and capacitors), a high ON-OFF impedance ratio ($> 10^4$), and a low off-state capacitance ($C_{OFF} \sim$ 10-20 fF) to achieve high isolation [22], [23]. A figure-of-merit (FoM) commonly used to encapsulate RF switch's electrical

performance is the cut-off frequency ($F_{CO} = 1/(2 \cdot \pi \cdot R_{ON} \cdot C_{OFF})$) and is defined as the frequency above which the OFF-state impedance of the switch falls below the ON-state impedance. Thus, an F_{CO} greater than 4 THz (2 Ω R_{ON}, 20 fF C_{OFF}) is essential for close-to-ideal RF switch operation. A small form factor, simple actuation mechanism, and compatibility with CMOS technology are additional critical requirements. Failure to meet any one of these renders even a high-F_{CO} RF switch technology non-viable.

As the majority of RF front-end circuits are realized in standard CMOS processes, MOS RF switches are easiest to design and integrate. However, they fail to simultaneously achieve low R_{ON} and low C_{OFF}, and are not well-suited to act as an RF switch [23]. In contrast, PC RF switches based on GeTe (50/50 alloy) are uniquely positioned to meet all the RF switch requirements. Thin-film crystalline GeTe resistivity as low as 1.83×10^{-6} Ω-m has been reported [4], which is more than an order of magnitude lower than that of state-of-the-art field-effect transistors (FETs). Thus, very low ON-state resistances can be realized with a much smaller device geometry. Via-style PC switches based on the vertical PC memory cell were initially explored [14]-[16] and RF prototypes incorporating these switches such as a tunable inductor [22] and a wide-tuning range CMOS VCO [23] were successfully demonstrated. However, the vertical design often necessitated the use of multiple vias in parallel to achieve low RF loss and suffered from filament formation leading to incomplete transformations [18]. To avoid these issues, a new class of indirectly-heated PC switches has recently been developed [17]-[20], where the RF-signal path is electrically decoupled from the programming path through the use of a micro-heater element separated from the PC material by a thermally conductive dielectric barrier. Analogous to a FET switch with two signal terminals and an independent voltage-controlled gate terminal, these PC switches have four terminals comprising two RF terminals in the signal path connected in-line with the PC material

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and two independent heater terminals in the programming current path. With reported cut-off frequencies exceeding 12 THz [19], the GeTe PC switch compares favorably in RF performance with various other technologies like RF MEMS, PIN diodes and FET switches [18], [24]. A directly-heated four-terminal GeTe PC switch has also been developed to reduce the heater programming power at the expense of electrical isolation [21]. A performance comparison between the directly-heated and indirect heating schemes is provided in [25].

Complex and highly reconfigurable RF systems employing these high-performance GeTe PC switches are already becoming a practical reality while offering many opportunities for both inter-circuit (field-programmable routing interconnects between different RF blocks analogous to a digital FPGA) and intra-circuit (alterable circuit characteristics such as center frequency) reconfiguration. In [4], the first *in-situ* frequency reconfiguration of a dual-band LNA employing a four-terminal GeTe PC switch was reported. More recently, PC switches have also been used to a receiver with component-level reconfigurable architecture [26] where banks of functionally similar circuit blocks tuned to different circuit frequencies were placed in a sea of PC switches. The implementation in [26] is especially nosteworthy as it exploits the small form-factor of PC switches to integrate 15 switches within a single receiver chipset. A similar implementation would incur a substantial area overhead if bulkier switches available from competing technologies were used [27].

This work describes the circuit-device co-design approach adopted to realize a 3/5 GHz dual-band narrowband LNA. Previous MEMS-based and MOS-switch based reconfigurable LNA architectures suffered from large area overhead either through the use of bulky MEMS devices [28] or through the use of multiple inductors and resonators [29]-[30]. Compact narrowband implementations have been reported [31]-[34], but lossy CMOS switches resulted in large

performance variation between the frequency modes where the switches were turned on and turned off respectively. In this work, a compact dual-band LNA design, with the area footprint of a single inductively-degenerated common-source LNA, is reported. The design uses a single integrated PC switch to transition between the two frequency bands. The introduction of the PC switch was experimentally verified to have introduced minimal performance degradation. As a result, the integrated CMOS-PC LNA achieved similar RF performance in both the frequency bands. Six prototypes of the CMOS-PC LNA were developed and tested to demonstrate the repeatability and robustness of the PC switch and the integration process. The issue of switching reliability of the PC RF switches was also addressed through standalone switch measurements, and by observing changes in the integrated LNA's RF performance over several hundred switching cycles.

2.2 Four Terminal PC Switches

2.2.1 MOS vs PC Switch

As discussed in the previous section, RF circuit reconfiguration requires switches with very low ON-state resistance and minimal parasitic capacitance. In [4], a PC switch with a width of 20 µm and an effective length (RF gap) of 600 nm was reported with an on-state resistance of ~2 Ω. In contrast, a MOS switch with similar dimensions would yield an on-state resistance of the order of several hundred ohms even in deeply-scaled technologies. A low R_{ON} can be achieved by increasing the MOS device's gate-width but this would increase the area overhead, and reduce the OFF-state isolation at high frequencies due to the large source/drain junction capacitances. It is important to note that a switch can have low R_{ON} and yet exhibit a high insertion loss (IL). IL is defined as the ratio of the available power from the source to the power delivered to the load,

(a)   **(b)**
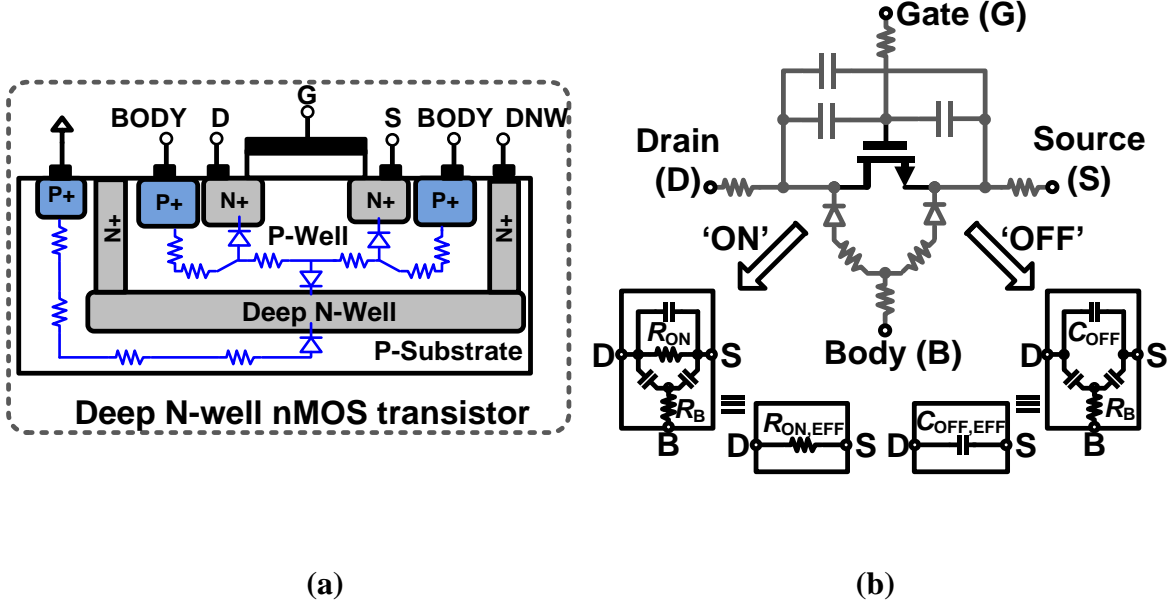
Figure 2.1 (a) Structure of a deep N-well (NDW) nMOS transistor. (b) Equivalent model of the DNW transistor in the on-state and the off-state when used as a switch

and measures the RF power loss through the switch [35]. Arguably, IL is a more meaningful measure of a switch's ON-state RF loss than R_{ON}. Thus, if the width of a MOS switch is made arbitrarily large, it will have a small R_{ON}, but RF signal loss or IL will still be high as additional power will now be lost through capacitive coupling to the grounded substrate network [36].

Modern CMOS processes offer a deep N-well transistor (DNW) for better substrate isolation (Figure 2.1(a)). Floating the body of the DNW transistor by connecting the body terminal to ground through a large resistance improves the power-handling capability [37] and reduces the insertion loss [36]. However, compared to a grounded substrate, a floating body configuration results in a worsening of the OFF-state isolation. To better understand this effect, two-port S-simulations were performed where the two ports were connected to the drain and source terminals of a DNW transistor in 28 nm CMOS. A simple-RC switch model (Figure 2.1 (b)) was assumed in order to extract the effective R_{ON} and C_{OFF} from two-port S-parameter simulations. From the simulated values of IL in the ON-state ($V_{GATE} = V_{DD}$) and isolation (S_{12}) in the OFF-state ($V_{GATE} =$
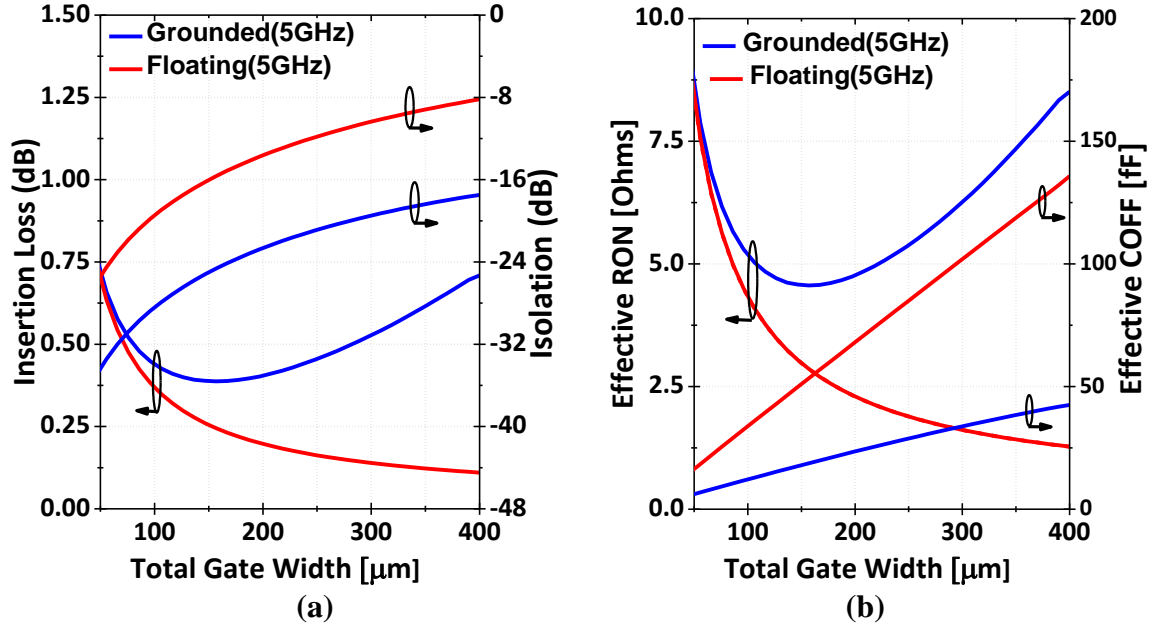
Figure 2.2 Deep N-well nMOS transistor in 28 nm CMOS: (a) simulated insertion loss and isolation, (b) extracted effective R_{ON} and C_{OFF} with grounded and floated body terminals. All simulations were performed at 5 GHz. In the floated configuration, the body terminal was connected to ground through a 10 kΩ resistor.

0 V), the values of $R_{ON,EFF}$ and $C_{OFF,EFF}$ were then calculated.

The switch FoM was then determined as $F_{CO}= 1/(2 \cdot \pi \cdot R_{ON,EFF} \cdot C_{OFF,EFF})$. Figure 2.2 shows the IL, isolation, $R_{ON,EFF}$ and $C_{OFF,EFF}$ of the DNW transistor for different gate widths with and without a floating body terminal. In the floated configuration, the body terminal was connected to ground through a 10-kΩ resistor. It was observed that large widths were helpful in reducing the insertion loss only when the body was intentionally floated. However, large widths and the attendant increase in junction capacitance resulted in the isolation of the switch falling below -10 dB. When the body was not floated, the best-case IL was only 0.39 dB ($R_{ON,EFF}$ = 4.5 Ω). To achieve an $R_{ON,EFF}$ of 2 Ω with a floating body, a 227.8 μm wide transistor was required which resulted in a $C_{OFF,EFF}$ of 77.5 fF and a F_{CO} of only 1 THz (Table 2-1). DNW transistors in 65 nm and 180 nm CMOS technologies were also characterized and the switch FoM was observed to have dropped

Node [nm]	Width [μm]	$R_{ON,EFF}$ [Ω]	$C_{OFF,EFF}$ [fF]	Insertion Loss [dB]	Isolation [dB]	*FoM* [THz]
28	227.8	2	77.5	0.17	-12.6	1.01
65	256.5	2	119	0.17	-8.2	0.69
180	407.2	2	176	0.17	-4.6	0.45

Table 2-1 Comparison of MOS switches in different technology nodes.

to 0.69 THz and 0.45 THz respectively. These results show that despite the incremental improvements afforded by the availability of DNW transistors and continued CMOS scaling, the rapid evolution of GeTe PC switches with cut-off frequencies beyond 10 THz [19] will help maintain their obvious advantages over MOS switches. It should be further noted that the ultimate performance of an RF switch is limited by the sheet resistance of the switchable channel as any performance gain accrued from a low R_{ON} will be offset by a corresponding increase in C_{OFF}. Thus, even state-of-the-art FET switches based on GaAs/GaN HEMTs and silicon-on-sapphire (SOS) technology (where the high resistivity substrate is effectively floating) fail to achieve cut-off frequencies beyond 2 THz [24] and are unlikely to approach the performance of a PC switch using GeTe (50/50 alloy) which has properties of extremely low crystalline resistivity (ρ_{ON}) and high ρ_{OFF}/ρ_{ON} [18].

2.2.2 PC Switch Design

In this section, the details of the switch design are briefly introduced. Further elaboration on the switch fabrication and design considerations are available in [7], [20], and [39], and formed the basis of the PhD thesis of a former CMU PhD student [39]. The schematic cross-section and isometric view of the designed PC switch is shown in Figure 2.3(a). As noted previously, the
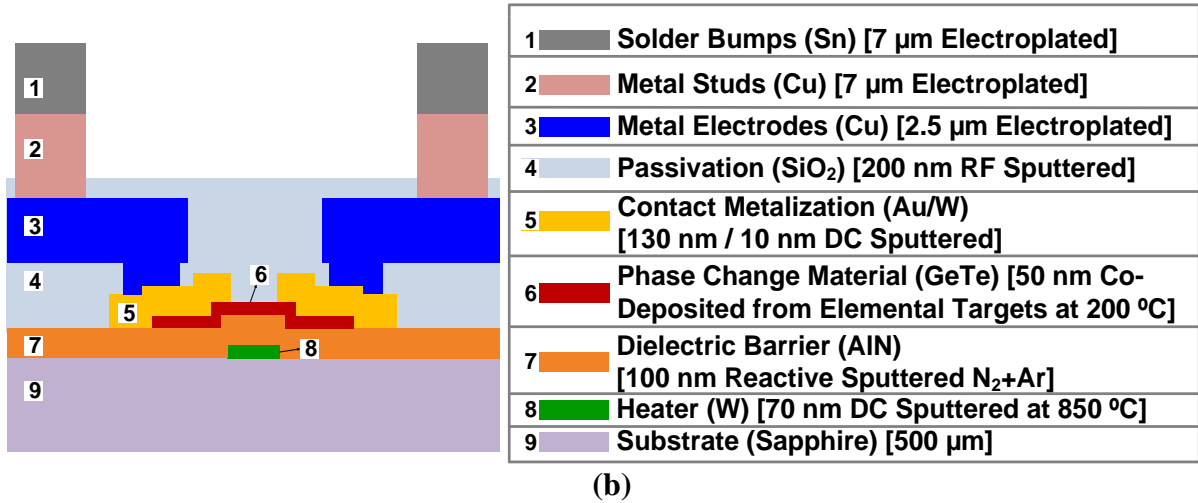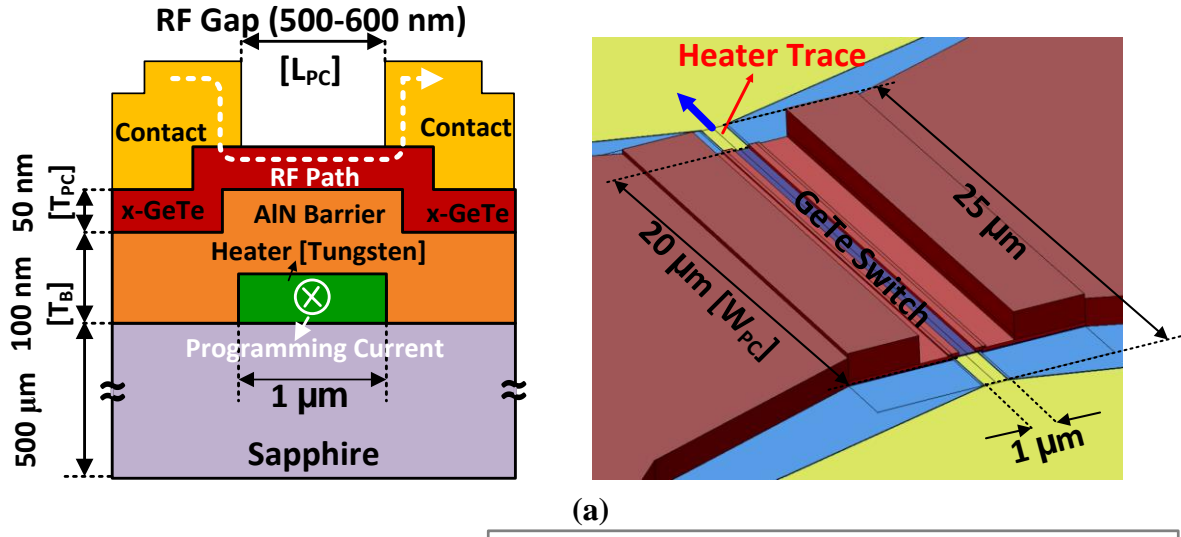
Figure 2.3 (a) Cross-section and isometric view of the four-terminal PC switch. (b) The layer stack of the PC die with the layer materials and thicknesses indicated. The figures are not drawn to scale.

switch has two RF terminals and two heater terminals. The PC switch was fabricated in a custom process. A cross-section of the PC layer stack is shown in Figure 2.3(b) with all the process steps noted. The PC material (Ge_xTe_{1-x}) was sputter deposited from elemental targets at 200 ℃ and patterned using ion milling. The composition ratio of GeTe alloy was optimized near 50/50 to achieve very low ON-state resistivity [4], [38]. From Rutherford backscattering spectrometry measurements, the percentage of Ge and Te in the deposited PC film was determined to be 45%
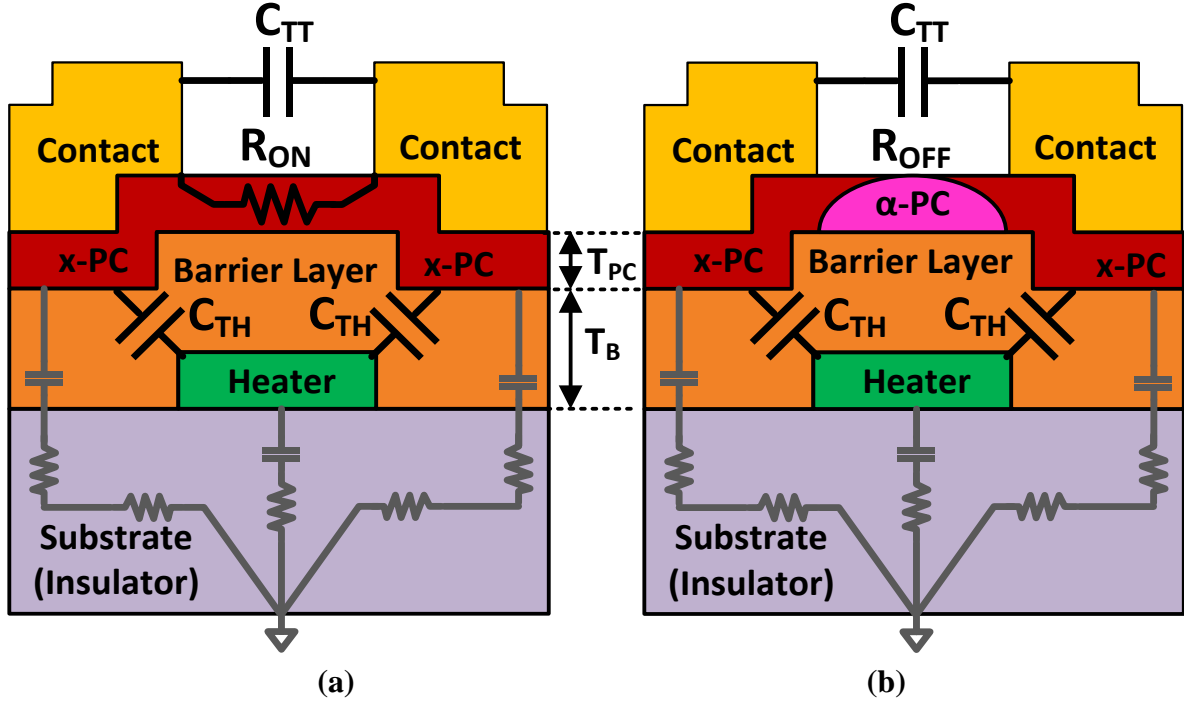
Figure 2.4 Dominant parasitics in the four-terminal PC switch in the (a) on-state, and (b) off-state.

and 55% respectively. The heater (with the heater programming current flowing out of the plane of the page in Figure 2.3(a)) is electrically isolated from the phase change material through a dielectric barrier. The dielectric material should simultaneously have high thermal conductivity k_{th}, to allow heat to flow from the heater to the PC material without a large temperature gradient, and small relative permittivity ε_r for good electrical isolation. In contrast to switches in [17]-19] which use Si_3N_4, PC switches in this work use AlN as the dielectric barrier due to their high k_{th} (285 W/m-K) and moderate ε_r of 9 [4], [20]. The heater comprised a tungsten heating element of width 1 µm and length 25 µm. Compared to NiCrSi heaters in [17]-[19], the higher melting temperature, better thermal stability, and lower resistivity of tungsten enables a more reliable heater that can transform the PC material using lower pulse voltages [39]. The use of a thermally conductive sapphire substrate (k_{th} = 35 W/m-K) resulted in quick cooling times necessary to

quench the PC material in its amorphous state and prevent unwanted crystallization after it has been heated to above its melting temperature [40]. Further details about the material choices and the fabrication process has been reported in [4]. Figure 2.4 marks the dominant parasitics of the PC switch in the ON and OFF states. Switch R_{ON} is determined by the PC material's resistivity, the length of the RF gap between the electrodes (L_{PC} in Figure 2.3(a)), as well as the thickness (T_{PC}) and width of the GeTe layer (W_{PC} in Figure 2.3(b)). The OFF-state capacitance C_{OFF} equals $C_{TT} + (C_{TH}/2)$, where C_{TT} comprises the parallel-plate and fringing capacitances between the RF terminals and C_{TH} is the capacitance between the PC material and the heater. Since the sapphire substrate is electrically insulating, the capacitance from the PC material and the heater to the substrate can be ignored. L_{PC} was optimized to be ~ 500-600 nm in order to obtain a reasonable trade-off between R_{ON} and C_{OFF}. It is easily observed that C_{TH} is a function of the heater width as well as the thickness (W_B) and dielectric constant of the barrier layer. Since W_B determines C_{TH} and the thermal coupling efficiency between the heater and PC material, it was chosen to be 100 nm even as larger values of W_B have been shown to significantly improve the cut-off frequency at the expense of higher programming power [20]. A thin GeTe layer (T_{PC} = 50 nm) was preferred to limit the volume of the transformable PC material. While thicker GeTe layers would result in better R_{ON}, they have been found to be difficult to transform in the absence of a significant improvement in the switch's thermal environment and heater reliability [18]. To achieve $R_{ON} \approx$ 1-2 Ω under conditions of perfect crystallization (where the entire volume of the PC material between the electrodes crystallizes in the ON-state), the switch width W_{PC} was fixed at 20 µm.

It should be noted that the magnitudes of the required actuation voltages are a function of the switch/heater dimensions and the heater resistance. If the heater resistance is lowered either by segmenting the switch into parallel segments or by increasing the thickness of the heater, lower

actuation voltages can be realized. However, in the work described in this paper, these approaches were not investigated. All measurements in this work were carried out at room temperature. Changes in ambient temperature will change the amount of power required from the heater to transform the PC material. Potential solutions, which include appropriate temperature feedback to heater driver and calibration of the transformation voltage profiles based on temperature, are beyond the scope of the investigation reported in this work.

2.2.3 PC Switch Characterization

To characterize the RF performance of the designed switches, one-port S-parameter measurements were made on two standalone PC switches having the dimensions given above. The two switches differed only in the length of the RF gap with $L_{PC} = 500$ nm for switch #1 and $L_{PC} = 600$ nm for switch #2. The heating profiles of the PC material are shown in Figure 2.5(a). To turn the switch on, a 1 µs wide ~4.4 V pulse (V_C) was used to raise the temperature of GeTe above its crystallization temperature (T_C). To turn off, a 100 ns wide ~9.1 V pulse (V_M) was used to raise the temperature of the PC material above its melting point temperature (T_M) after which the pulse was turned off (10 ns fall time) to quench the PC material in its amorphous state. Both the amorphization and crystallization pulses were generated using an Agilent 8114A pulse generator. Figure 2.5(b) shows the measured R_{ON}, R_{OFF} and C_{OFF} of the two switches. To ensure accurate estimation of switch parasitics and to keep the results consistent with previously reported work, the heater pads were left floating during the S-parameter measurements [19], [39]. If the heater pads were left connected to an external impedance (pulse generator), finite signal leakage to the heater pad through C_{TH} (see Figure 2.4) would lead to an incorrect evaluation of the intrinsic switch R_{ON} and C_{OFF} in the on- and off-states respectively. Through this setup, F_{CO} for the two switches was measured to be 5.5 THz and 6.4 THz respectively. The measured resistance of the heater for
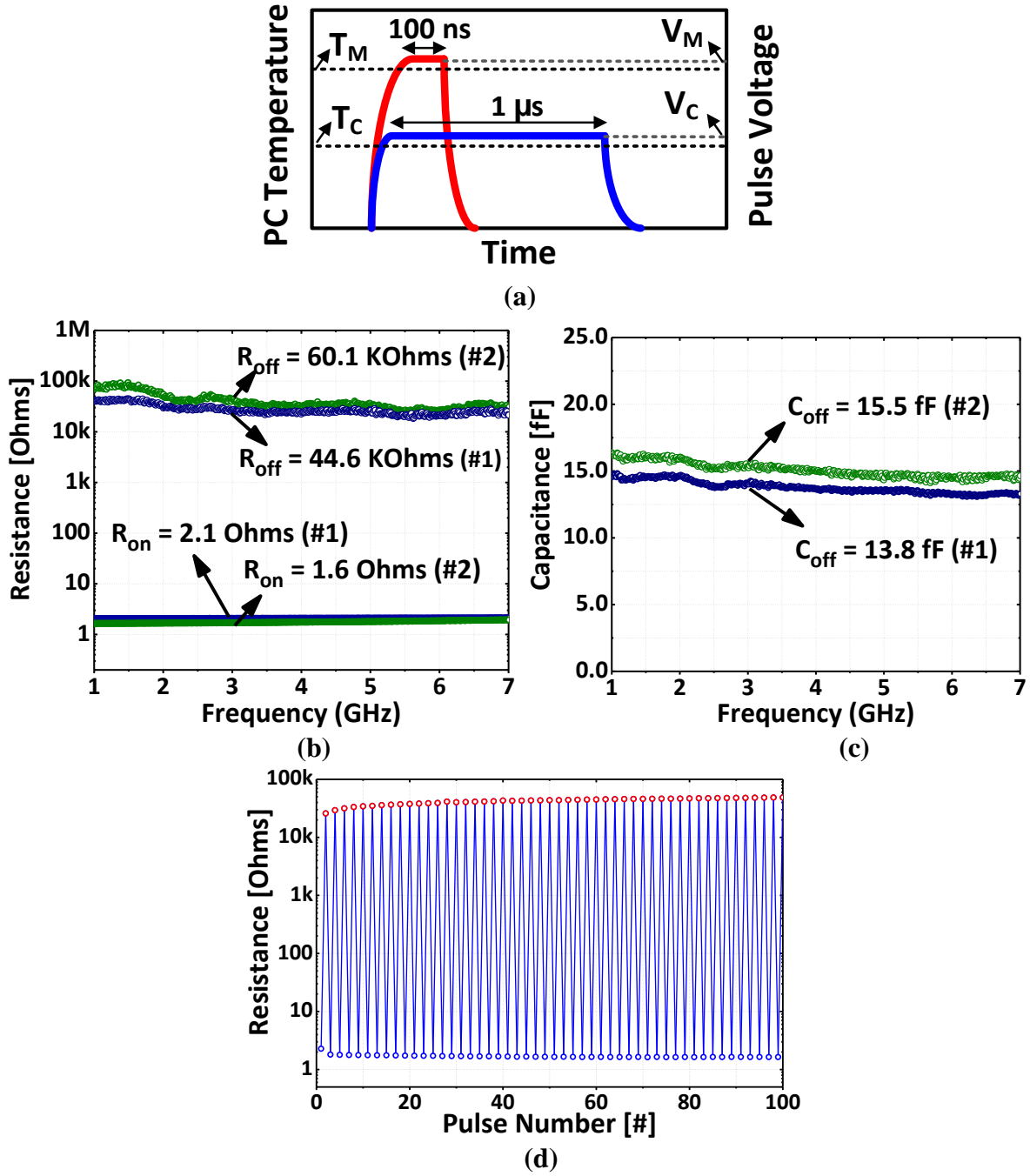
Figure 2.5 (a) Heat and voltage profiles of the amorphization (red) and crystallization (blue) programming pulses with 10 ns rise and fall times. Stand-alone measurements of two fabricated PC switches (#1, #2): (b) R_{ON} and R_{OFF}, and (c) C_{OFF}. (d) Switch #2 resistance as a function of switching pulses.

both the switches was 39 Ω. Compared to [19] (12.5 THz F_{CO}), PC switches in this work achieve

similar C_{OFF} (~15 fF). However, R_{ON} was higher (1.5-2 Ω vs. 0.9 Ω in [19]) due to the use of a

comparatively thinner GeTe layer and smaller switch width. Figure 2.5(d) shows the resistance of switch #2 as it was switched on and off 100 times through the application of successive amorphization and crystallization pulses. R_{ON} remained stable at ~ 1.6 Ω while R_{OFF} remained greater than 30 kΩ for the duration of the 50 measured switching cycles, thus exhibiting a DC resistance ratio better than 1.9×10^4:1.

2.3 Dual-band LNA Design

In a multi-standard receiver, flexibility in the operation of the LNA can be achieved in three different ways: (i) by using a narrowband LNA for each standard resulting in large area and power overheads, (ii) by using a wideband LNA concurrently covering all bands of interest, or (iii) by using reconfigurable multiband LNAs. The design specifications of wideband LNAs are very stringent: flat gain, good input matching, low NF and high linearity are required over the entire bandwidth. Moreover, due to the finite gain-bandwidth product available from an amplifier stage, a wideband LNA often requires more than one stage of amplification to achieve an RF gain approaching that of a narrowband amplifier with a high quality factor (Q) load. On the other hand, multiband LNAs preserve the frequency band selectivity of narrowband LNAs resulting in enhanced immunity to out-of-band interferers, and can theoretically achieve RF performance metrics similar to that of narrowband LNAs given the availability of RF switches with high F_{CO} (low R_{ON}, low C_{OFF}). Since reconfiguration in multiband circuits is usually accomplished by switching either a capacitance or an inductance of a resonant-LC tank, a high F_{CO} switch ensures an adequate tank Q even in the frequency bands where the switches are turned on. Multi-band LNAs using lossy MOS switches have been attempted [31]-[34] – but a significant disparity in RF

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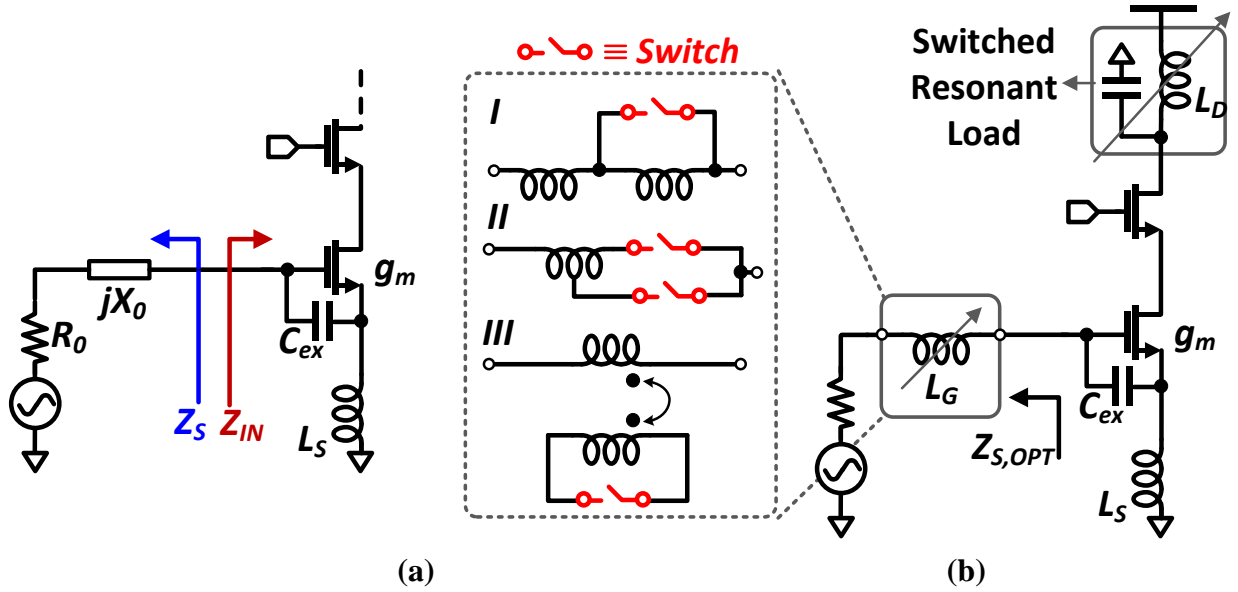
Figure 2.6 (a) Input network of a inductively degenerated CS LNA (b) CS LNA with a reconfigurable gate inductor for multi-band operation. The gate inductance is reconfigured either using a tapped-inductor (configurations *I*, *II*) or by switching the secondary coil of a transformer (configuration *III*). While CMOS switches can be used, high-F_{CO} PC RF switches are preferable to maintain RF performance when the switches are turned on.

performance between the bands limits their applicability. In section II, we established that PC RF switches are capable of achieving both low R_{ON} and C_{OFF} thereby creating several interesting possibilities for their use in reconfigurable multiband circuits. In this section, we introduce our proposed design of a dual-band 3/5 GHz LNA employing one such RF PC switch.

2.3.1 Dual-Band Simultaneous Noise and Input Match

Consider the input network of an inductively degenerated CS LNA as shown in Figure 2.6(a). The input impedance is given by:

$$Z_{IN} = R_{IN} + jX_{IN} \text{ where}$$
$$R_{IN} = \frac{g_m L_S}{C_T} \text{ and } X_{IN} = \omega L_S - \frac{1}{\omega C_T}. \tag{2-1}$$

21

Here, $C_T = C_{ex} + C_{gs}$ is the total capacitance across the gate-source terminals comprising an explicit capacitor C_{ex} and the transistor C_{gs}. To set a conjugate power match, R_{IN} must be designed to equal the source resistance R_0, and the reactance X_0 should be chosen such that $X_0 = -X_{IN}$. The latter can be achieved by realizing X_0 using a single series inductor L_G, resulting in a conjugate match at a frequency ω_1 given by

$$\omega_1 = \frac{1}{\sqrt{(L_S + L_G)C_T}}.$$

(2-2)

To minimize the noise figure, the impedance of the network driving the gate of the MOSFET must be set to an optimum value given by (to keep the expression simple, the correlation coefficient (c) between the gate-induced and channel noise current is set to zero. The reader is referred to [41] for expressions including a finite c):

$$Z_s = Z_{s,opt} = R_{s,opt} + jX_{s,opt}$$

$$\text{where } R_{s,opt} = \frac{1}{\omega C_{gs}} \frac{1}{\alpha \chi} \frac{1}{1 + \left(\dfrac{1}{\alpha \chi} \dfrac{C_T}{C_{gs}} \right)^2},$$

(2-3)

$$\text{and } X_{s,opt} = -\omega L_S + \frac{1}{\omega C_{gs}} \left(\frac{1}{\alpha \chi} \right)^2 \left(\frac{C_T}{C_{gs}} \right) \frac{1}{1 + \left(\dfrac{1}{\alpha \chi} \dfrac{C_T}{C_{gs}} \right)^2}.$$

Here, $\alpha = g_m / g_{d0}$, $\chi = \sqrt{\delta/5\gamma}$ where δ and γ are the gate and drain noise coefficients respectively. This results in a minimum noise figure given by:

$$F_{min} = 1 + 2\gamma\chi \frac{\omega}{\omega_T}, \text{ where } \omega_T = \frac{g_m}{C_{gs}}.$$

(2-4)

In order to achieve a simultaneous noise and conjugate match at a frequency ω_1 in the absence of a power constraint, C_{ex} can be set to zero so that $C_T=C_{gs}$. By then equating $R_{s,opt}$ to R_0 the required device capacitance (and hence its width) can be found from (2-3) to be:

$$C_{gs} = \frac{1}{\omega_1 R_0} \frac{\alpha\chi}{1+\alpha\chi^2}. \tag{2-5}$$

For a given bias condition (which sets the cut-off frequency ω_T), the required value of the source inductance can then be obtained using $R_0 = \omega_T L_S$. From (2-1) and (2-3), it is evident that an approximate noise match is simultaneously achieved, since $X_{IN} \approx -X_{s,opt}$. However, in deeply scaled technologies, setting $C_{ex}=0$ usually necessitates a very large device width to achieve the requisite C_{gs}. For a targeted current density, this typically results in high power consumption. Therefore, a simultaneous noise and conjugate match is desired under a power constraint. This is accomplished by using an explicit capacitor C_{ex} to realize part of the total required gate-source capacitance. It can be shown that the minimum noise figure remains unchanged with this addition [41].

Next, consider the challenge of reconfiguring this CS LNA topology to achieve a simultaneous noise and conjugate match at a lower frequency $\omega_2 < \omega_1$. If the gate inductance alone is changed from L_G to L_{G2}, while leaving unchanged the device size, the device bias and the source inductance, (2-2) indicates that the conjugate match is achieved at a new frequency $1/\sqrt{(L_{G2}+L_S)C_T}$, which can then be set to ω_2 with an appropriate choice of L_{G2}. The inductor can be reconfigured either by using a tapped gate inductor, as shown in configurations I and II in Figure 2.6(b), or by switching the secondary coil of a transformer introduced in the input path (configuration III). The latter method avoids the use of lossy switches directly in the input signal path. However, the design still suffers from a significant disparity in noise performance between the targeted bands when CMOS
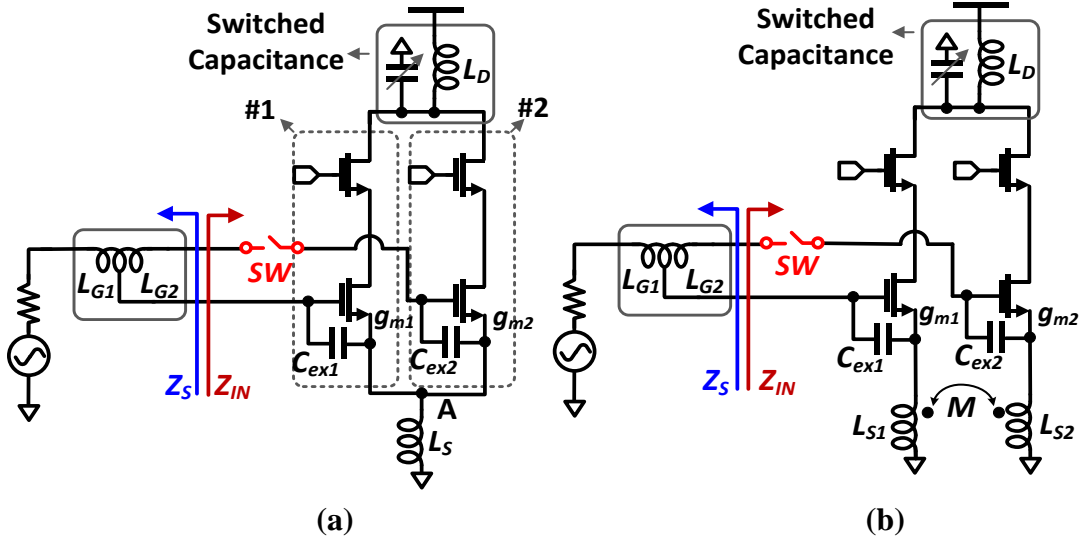
Figure 2.7 (a) Dual-band CS LNA with two CS legs and a shared source inductor (b) Dual-band CS LNA with two CS legs and coupled source inductors.

switches are used [33], [34]. Similar reconfiguration can be implemented using PC switches and can possibly reduce the performance disparity.

Nevertheless, it is important to note that a noise match is no longer achieved at ω_2, which fundamentally leads to a non-optimum design. This is evident from the expression for $R_{s,opt}$ in (2-3). If the device width is increased to maintain the same $R_{s,opt}$ as before (see (2-5)), the transconductance or the source inductance (or both) must be increased in order to maintain the conjugate match; this is evident from (2-1). Switching the source inductance to a larger value would require a second "near-ideal" RF switch (in addition to the one that is needed to switch the value of L_G), and is therefore not a desirable option. On the other hand, increasing the device size alone increases the g_m at the expense of reduced ω_T, thereby leading to an increase in F_{MIN}. However, increasing the bias current in proportion to the device width allows ω_T to remain unchanged, thus keeping F_{MIN} constant.

A possible implementation of the aforementioned reconfiguration is illustrated in Figure 2.7(a). In the high-frequency mode, branch #1 is turned on while branch #2 and the switch SW are both turned off. In the low-frequency mode, both branches and the switch SW are turned on. The branches are turned on and off by either enabling or grounding the gate of the cascode device. Note the use of a single RF switch, a shared source inductor, a tapped gate inductor, and MOS switched-capacitor tuned output tank. It is emphasized that while MOS switches can be used in the output load network, they cannot be used to reconfigure the input network because the switch appears directly in the RF signal path before the gate of the LNA transconductors, and must therefore have a very low R_{ON} to avoid degrading the LNA's NF. As discussed previously, a MOS device dimensioned to achieve such low R_{ON} is accompanied by large parasitic capacitance which results in poor matching and reduced gain. However, although simultaneous noise and input matching can be theoretically achieved at two different frequencies with this topology, the presence of a large parasitic capacitance from the transistors' source junctions at the shared source node (node A in Figure 2.7(a)) can also disrupt input matching in both the frequency modes.

A superior approach to reconfiguration is illustrated in Figure 2.7(b). A single "near-ideal" RF switch SW is sufficient to switch the tapped gate inductor to achieve conjugate matching at two different frequencies. Since the effective gate-source capacitance is increased, $R_{s,opt}$ remains unchanged, thereby preserving the noise match. Also, since the effective transconductance is increased, ω_T remains unchanged. In the absence of coupling between the source inductances L_{S1} and L_{S2}, the effective source inductance would decrease (since L_{S1} and L_{S2} are effectively in parallel), which in turn would lead to a decrease in the real part of the input impedance, thereby disrupting the conjugate match. However, if strong coupling (coupling coefficient $k \rightarrow 1$) were introduced between the L_{S1} and $L_{S2,}$ the effective source inductance in the low-frequency mode can
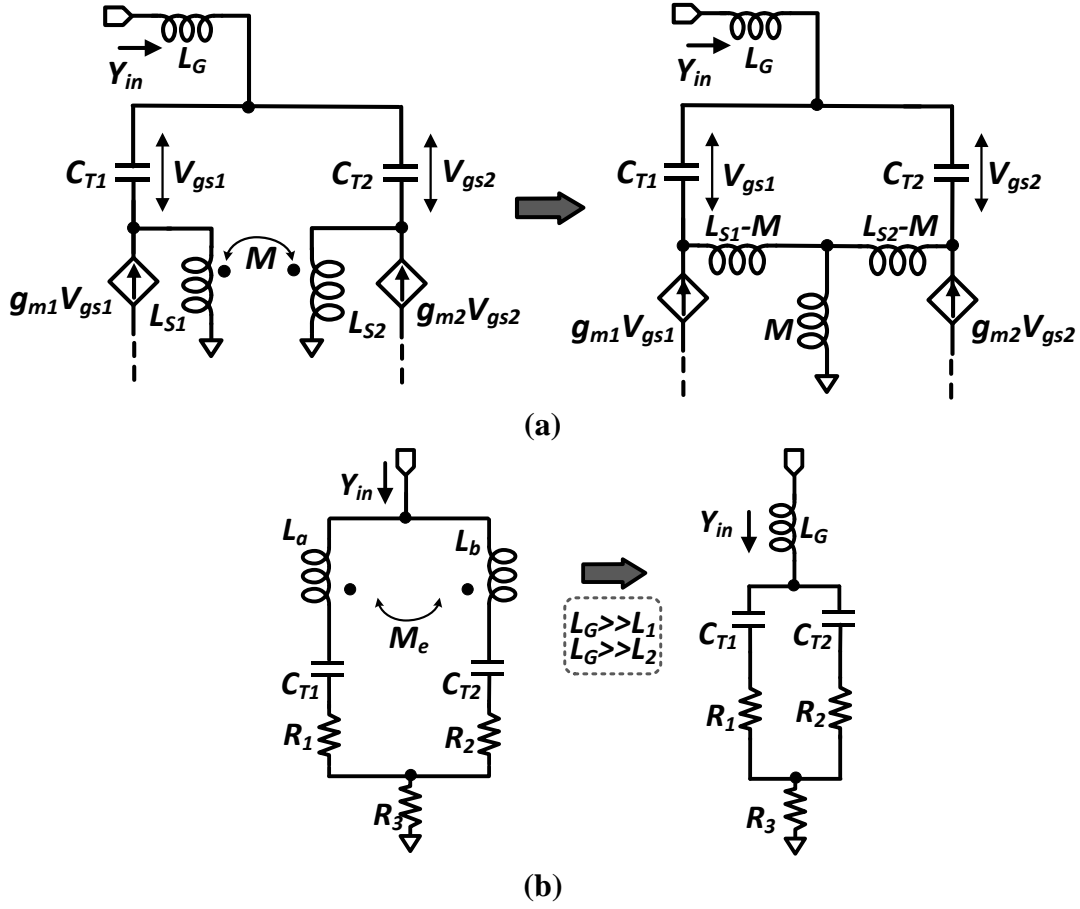
Figure 2.8 (a) Small-signal equivalent of the input matching network of a CS LNA with two CS legs, a shared gate inductor and with finite coupling between the source inductors. Effect of C_{gd} is ignored. (b) Equivalent representation with gate inductance merged into an equivalent transformer.

be designed to remain roughly unchanged since $L_{S1}+M$ and $L_{S2}+M$ are now effectively in parallel. Thus, the real part of Z_{IN} remains unaffected at the lower frequency, thereby preserving the conjugate match. Furthermore, since the introduction of strong coupling enables the implementation of the source inductors as a transformer with inter-leaved windings, an extremely compact design that occupies the footprint of a single-band LNA results. For moderately-separated frequency bands, the tapped gate inductor can be replaced by a simple gate inductor such that only the change in effective gate-source capacitance is used to realize the frequency separation. Note
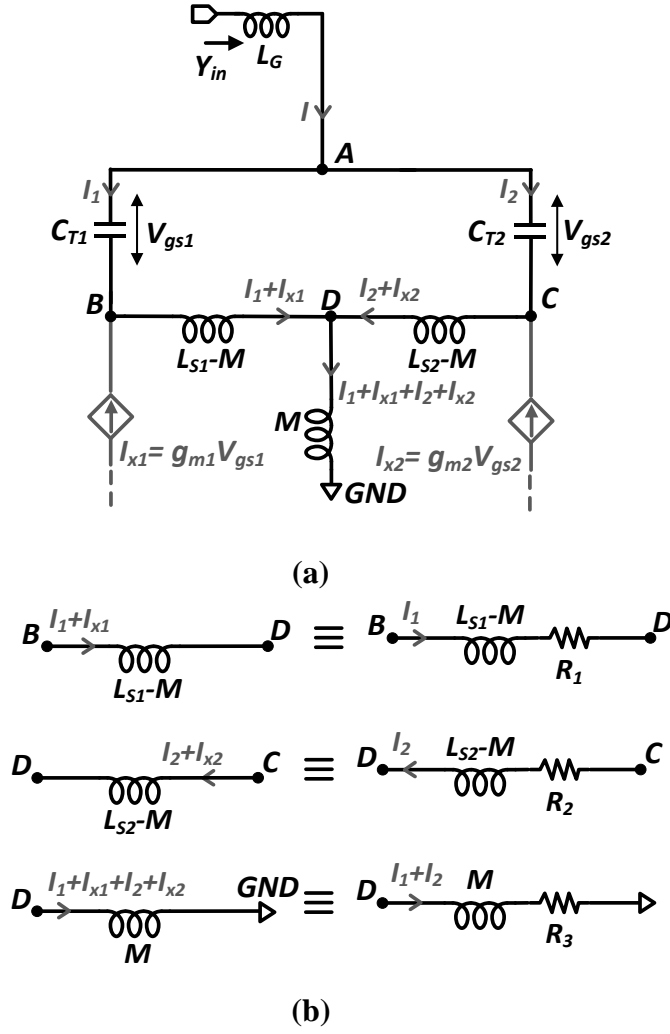
Figure 2.9 (a)Small-signal equivalent of the input network with the branch currents identified. (b) Equivalent representation of the wire-segments with inductors.

that to satisfy (2-2) and (2-5) simultaneously, a tapped gate inductor will still be necessary. However, a simple layout afforded by the non-tapped gate inductor might be preferred at the expense of a non-optimum noise match as long as the performance is within the targeted design specifications.

2.3.2 *Narrowband Matching with Coupled Source Inductors*

Our objective is to design a 3/5 GHz LNA using the topology introduced in the previous section. Since the frequency separation between the high and low bands is moderate, a simple gate inductor
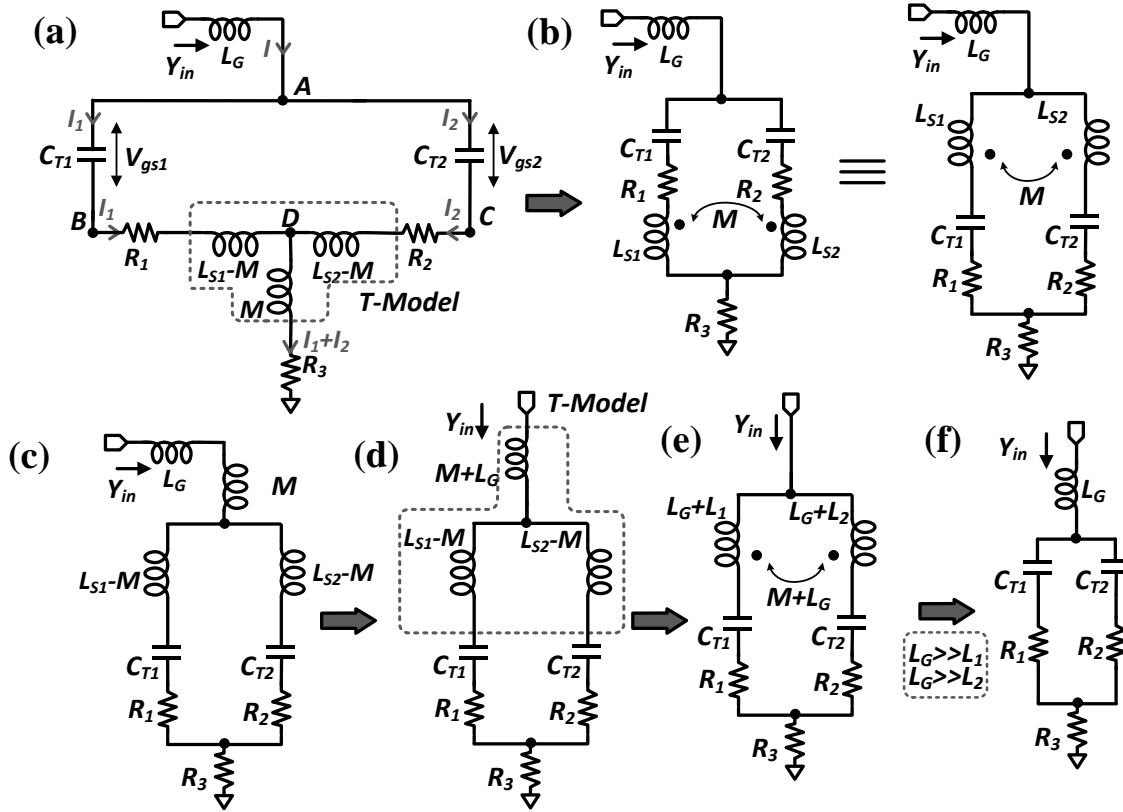
Figure 2.10 Reduction of the small-signal equivalent of the input network to a canonical representation.

was preferred to avoid complexity. Figure 2.8(a) shows the small-signal equivalent of the input matching network of such an LNA in the low frequency band (an ideal short is assumed in lieu of the 'on' RF switch). The small-signal equivalent in the high frequency band follows from the conventional CS LNA configuration in Figure 2.6(a) and hence is not shown. By first replacing the coupled inductors with an equivalent transformer T-model, and then accounting for the frequency-independent resistances generated due to reactive feedback from the source inductors, the input network can be reduced to a fourth-order system with two parallel series-RLC branches (Figure 2.8(b)) where the inductors L_a ($= L_{S1}+L_G$) and L_b ($= L_{S2}+L_G$) are coupled through a mutual inductance M_e ($=L_G+M$). Thus, the effective coupling factor k_e may be written as

$$k_e = \frac{L_G + M}{\sqrt{(L_{S1} + L_G)(L_{S2} + L_G)}}$$ (2-6)

Figure 2.9(a) shows an equivalent representation of the input network of the proposed CS LNA architecture, where the coupled inductors of Figure 2.8(a) are replaced by the transformer T-model. While an expression for the input admittance Y_{in} can be derived, the resulting expression is too complicated to derive useful insight. However, the network can be reduced to a canonical representation through simple transformations. If he currents flowing in the two branches are assumed to be I_1 and I_2, it is straightforward to express their ratio as:

$$\frac{I_1}{I_2} = \frac{\left(\dfrac{1}{sC_{T2}}\right) + s(L_{S2} - M) + \left(\dfrac{g_{m2}(L_{S2} - M)}{C_{T2}}\right)}{\left(\dfrac{1}{sC_{T1}}\right) + s(L_{S1} - M) + \left(\dfrac{g_{m1}(L_{S1} - M)}{C_{T1}}\right)}.$$ (2-7)

At the lower mode frequency where capacitive impedances dominate, a reasonable simplifying approximation is to assume that the current division at node A is determined primarily by the ratio of C_{T1} and C_{T2}, and (2-7) can be rewritten as:

$$\frac{I_1}{I_2} \approx \frac{\left(\dfrac{1}{sC_{T2}}\right)}{\left(\dfrac{1}{sC_{T1}}\right)}.$$ (2-8)

Thus, I_1 and I_2 can be expressed in relation to I as:

$$I_1 = \left(\frac{C_{T1}}{C_{T1} + C_{T2}}\right) I = aI, \; I_2 = \left(\frac{C_{T2}}{C_{T1} + C_{T2}}\right) I = bI.$$ (2-9)

Next, the wire segments with inductors, B-D, C-D and D-GND, can be redrawn with resistors in series such that the transistor drain current injections at nodes B and C are accounted for and the voltages across the segments remain unchanged (Figure 2.9(b)). The values of the resistances R_1, R_2 and R_3 can be expressed as (2-10)-(2-11):

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$$R_1 = \frac{g_{m1}(L_{S1} - M)}{C_{T1}}, \quad R_2 = \frac{g_{m2}(L_{S2} - M)}{C_{T2}} \tag{2-10}$$

$$\text{and } R_3 = a\left(\frac{g_{m1}M}{C_{T1}}\right) + b\left(\frac{g_{m2}M}{C_{T2}}\right). \tag{2-11}$$

Thus, the network of Figure 2.9(a) can be redrawn as shown in Figure 2.10(a), (b) by replacing the T-model with an equivalent three-terminal transformer. The gate inductor L_G can then be combined resulting in a new transformer, shown in Figure 2.10(e) with an effective coupling factor defined as in (2-6). The resulting structure comprises two magnetically-coupled series-RLC branches, and hence is a fourth-order system. Now, if $L_G \gg L_{S1}$ and $L_G \gg L_{S2}$, the transformer in Figure 2.10(e) reduces to an inductance L_G, resulting in the simplified structure of Figure 2.10(f). To generate the 50 Ω real part required for input matching as per (2-1), the value of source inductance L_S is usually restricted to small values [42]. On the other hand, to satisfy (2-2) at low RF frequencies (< 5 GHz), a large gate inductance is required. Therefore, $L_G \gg L_{S1}$ and $L_G \gg L_{S2}$ is generally true, and k_e approaches 1, as is evident from (2-6). Thus, the transformer with coupling k_e now reduces to a gate inductance L_G, as is shown in **Figure 2.8**(b) and **Figure 2.10**(f) . Since C_{T1} and C_{T2} now appear in parallel, the approximate values of the high and low band frequencies can be written as:

$$F_L \approx \frac{1}{2\pi\sqrt{L_G(C_{T1} + C_{T2})}} ; F_H = \frac{1}{2\pi\sqrt{L_G C_{T1}}} \tag{2-12}$$

This result can also be proved analytically. The overall expression for the input admittance can be described by (2-13) where: $\omega_1 = 1/\sqrt{L_a C_{gs1}}, \omega_2 = 1/\sqrt{L_b C_{gs2}}, Q_1 = (\omega_1 L_a)/R_1, Q_2 = (\omega_2 L_b)/R_2$. If we now reconsider under the constraint that $L_G \gg L_1$ and $L_G \gg L_2$ such that $k_e \rightarrow 1$, we find that the s^4 term in the numerator of Y_{in} disappears.
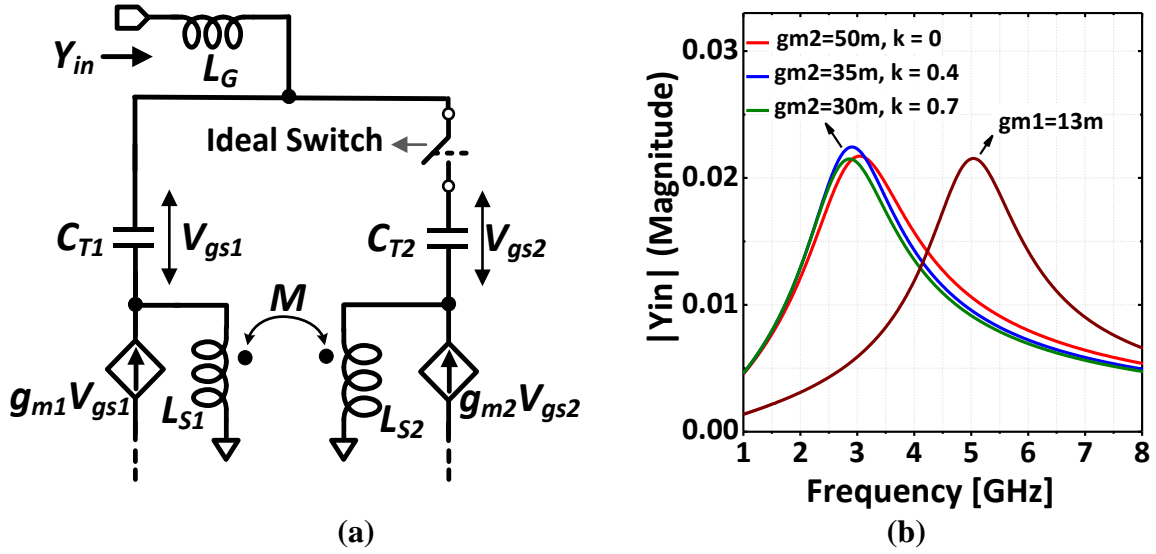
Figure 2.11 (a) Design example of a dual-band input network using ideal elements and a single switch. (b) Magnitude of input admittance for different values of coupling factor 'k' between the source inductors L_{S1} and L_{S2}.

$$Y_{in} = \frac{s\left[s^2 C_{gs1} C_{gs2}\left(L_a + L_b - 2k\sqrt{L_a L_b}\right) + s\left(\frac{C_{gs1}}{Q_2 \omega_2} + \frac{C_{gs2}}{Q_1 \omega_1}\right) + \left(C_{gs1} + C_{gs2}\right)\right]}{s^4\left(\frac{\left(1-k_e^2\right)}{\omega_1^2 \omega_2^2}\right) + s^3\left(\frac{1}{Q_1 \omega_1 \omega_2^2} + \frac{1}{Q_2 \omega_1^2 \omega_2}\right) + s^2\left(\frac{1}{Q_1 Q_2 \omega_1 \omega_2} + \frac{1}{\omega_1^2} + \frac{1}{\omega_2^2}\right) + s\left(\frac{1}{Q_1 \omega_1} + \frac{1}{Q_2 \omega_2}\right) + 1}$$

$$(2\text{-}13)$$

Note that (2-12) would also be valid with uncoupled source inductors or with low coupling; however, strong coupling is preferred for reasons already discussed in the previous section. The above result demonstrates that in addition to the simultaneous power and noise match which the proposed topology facilitates, we are also able to approach narrowband behavior in both frequency bands. This behavior is demonstrated through a simple design example. Consider the circuit in Figure 2.11(a) in which we model a 3/5 GHz input matching network using ideal circuit elements and a single switch. In the 5 GHz mode, the switch is off and $g_{m2} = 0$. In the 3 GHz mode, the switch is turned on, a finite g_{m2} is assumed, and the coupling factor (k) between the source inductors is varied to observe the effect on input admittance (Y_{in}). For narrowband matching at 5 GHz, the following designs parameters were initially chosen: $g_{m1} = 13$ mS, $C_{T1} = 210$ fF, $L_{S1} = 750$ pH, L_{S2}

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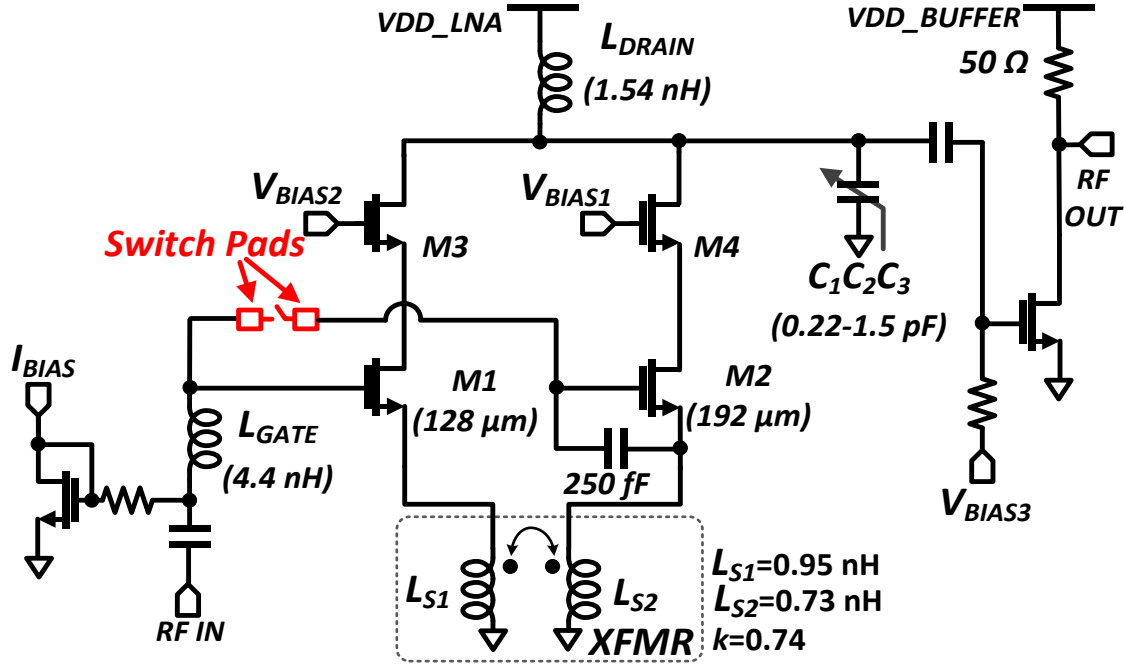
Figure 2.12 Schematic diagram of the 3/5 GHz LNA designed in a 0.13 μm process.

= 750 pH, and L_G = 4 nH. In the next step, C_{T2} was chosen to be 450 fF to satisfy the resonance condition at 3 GHz as per (2-12). Figure 2.11(b) shows the Y_{in} magnitude as the coupling factor (*k*) between the source inductors was varied between 0 and 0.7. While the g_{m2} values had to be adjusted with higher *k* requiring lower g_{m2}, the resonance frequency itself did not deviate from 3 GHz. With this simple model as the starting point, the design was further optimized for noise and gain based on principles discussed in the previous section and in [41].

2.3.3 Design Details

The circuit schematic of the LNA is shown in Figure 2.12. The LNA comprises two inductively-generated cascode common-source (CS) legs, with strong coupling introduced between the source inductors through a compact, high-*k* transformer as shown in Figure 2.13(a). While both primary and secondary coils were initially designed to be two-turn inductors tightly interleaved with each other, an additional turn - implemented in the top metal - was added to the primary coil during the design optimization phase to realize the source inductance required at 5 GHz. The transformer coupling factor *k* at 3/5 GHz was simulated to be 0.74 (Figure 2.13(b)). The PC RF switch, inserted

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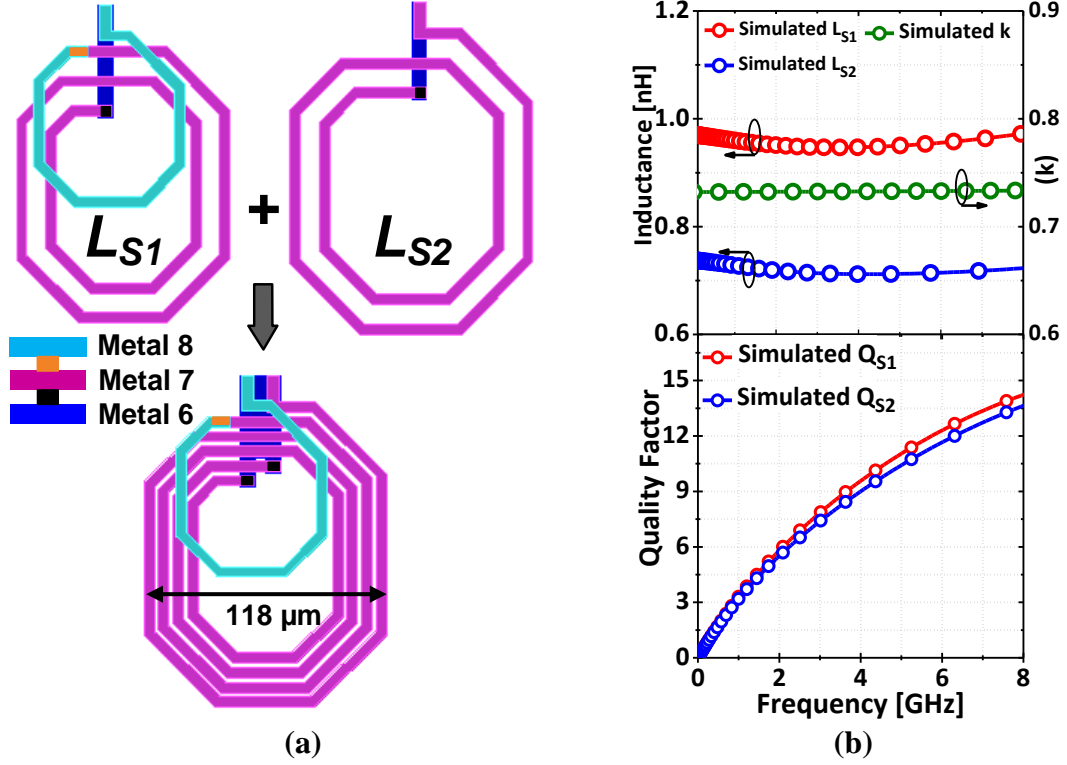
Figure 2.13 (a) Layout implementation of three-terminal the high-*k* source transformer with interleaved windings. (b) Simulated values of primary and secondary coil inductances and quality factors, and the transformer coupling efficient *k*.

between the gate inductor and one of the CS stages, removes it from the input signal path when turned off during operation in the higher band (5 GHz). To enable the lower band (3 GHz) operation, the PC switch is turned on and both CS stages are included. An explicit capacitor of 250 fF was inserted between the gate and source of M2 to satisfy matching requirements in the 3 GHz mode. Band selection at the output is performed by switching the capacitance of an *LC*-tank load. The size and R_{ON} of the CMOS switches in the capacitor bank (controlled by a three-bit digital word $C_1C_2C_3$) pose a trade-off between the output tank's quality factor and the off-state capacitance. However, wide CMOS switches can be employed in the capacitor bank by ensuring that the off-state capacitance is accounted for during operation in the 5 GHz mode. Metal-insulator-metal (MIM) capacitors available in the process displayed high *Q*s (> 80) at 5 GHz; therefore, the overall tank *Q* suffered only minor degradation with the use of MOS-switched capacitors.

(a)

(b)
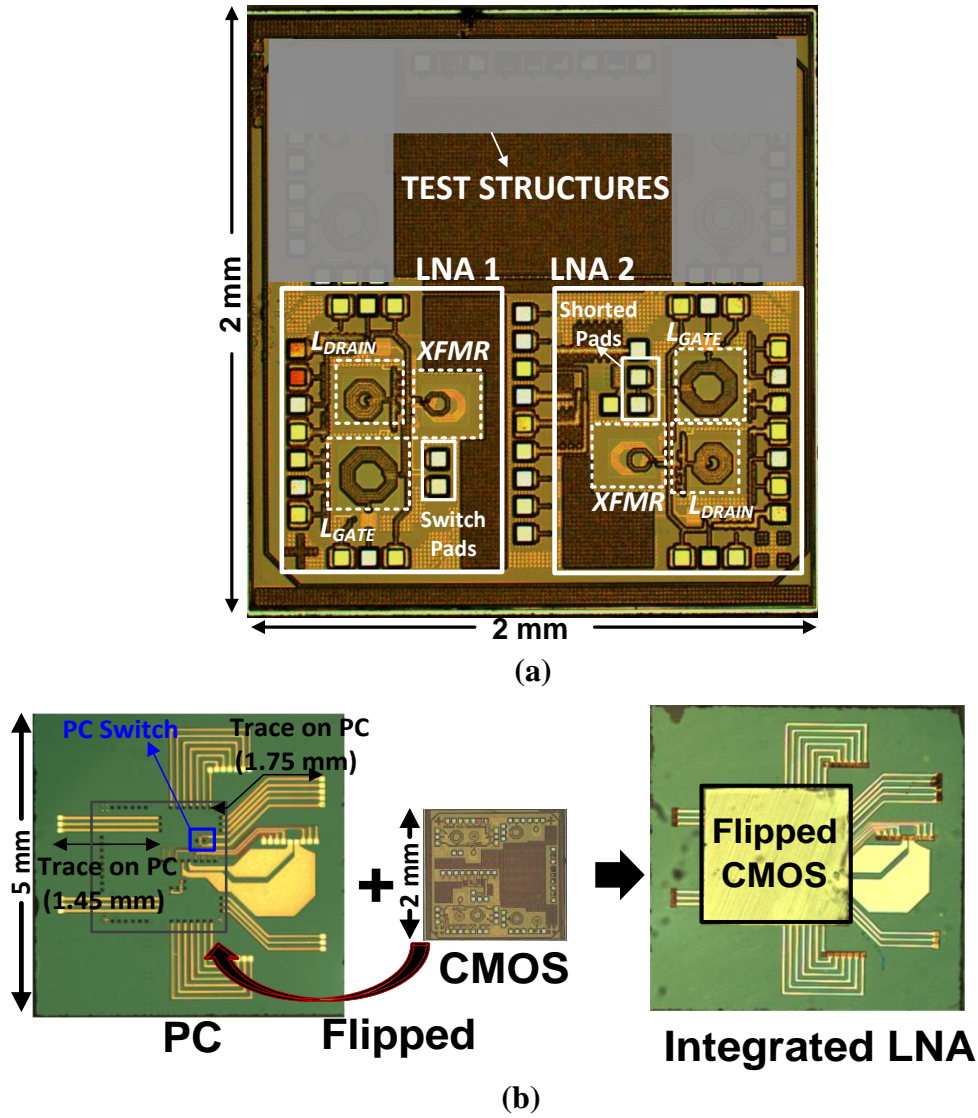
Figure 2.14 (a) Die photo in 0.13 μm CMOS. LNA #1 has open switch pads for integration with PC switch and for CMOS testing in the 5 GHz mode. LNA #2 has shorted switch pads for 3 GHz mode testing. (b) Die photo of the integrated LNA.

2.4 Measurement Results

2.4.1 PC Wafer Fabrication and Integration with CMOS

The PC chips were fabricated in two batches. In the first batch (B1), the PC switches used in the

LNA had width $W_{PC} = 20$ μm, gap length $L_{PC} = 600$ nm and PC layer thickness $T_{PC} = 50$ nm. In

the second batch (B2), two wafers B2-W1 and B2-W2 were fabricated with PC layer thicknesses

$T_{PC} = 50$ nm and $T_{PC} = 75$ nm respectively. The PC material (Ge_xTe_{1-x}) was sputter deposited at
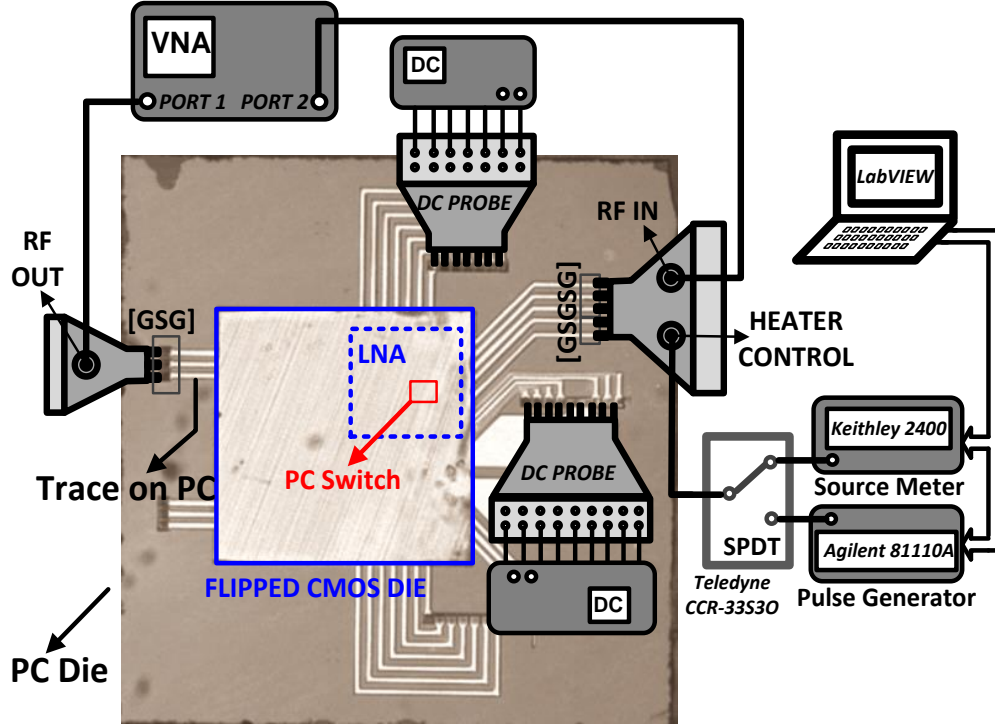
Figure 2.15 Measurement setup of the integrated LNA-PC chip using two RF and two DC probes.

160 °C instead of 200 °C as in the first batch. The tungsten heater was 25 µm long and 1 µm wide in all cases. In both batches, a thermally conducting, electrically insulating aluminum nitride (AlN) barrier layer of thickness $T_B = 100$ nm was used. All wafers used copper metallization on pads; however, a ~200 nm thick gold layer was additionally sputtered on top of the copper pads in B2-W1 and B2-W2. The device cross-section of B2 devices was similar to Figure 2.3(b), except the addition of the gold layer between the Cu electrode and the Cu metal stud.

A substrate-agnostic design of a PC switch has been discussed in [26]. Monolithic integration of the PC switch stack (Figure 2.3(b)) with the backend of a CMOS process is preferable to minimize the parasitics associated with integration of the switch with the rest of the circuit. However, the thermal environment and associated heat sinking required for reliable transformation of such a switch remains the subject of a future study. Therefore, the PC switch used herein was fabricated in-house on a sapphire substrate due to its high thermal conductivity and high electrical resistivity.

The CMOS part (Figure 2.12) of the system was fabricated in a 0.13 µm RF-CMOS foundry technology, and was flip-chip bonded to the PC chip using an in-house integration process [4], [39]. To obtain baseline measurements of CMOS-only LNA's in each mode, two separate CMOS LNA's (#1, #2), shown in Figure 2.14(a), were fabricated. Both LNA's had two switch pads to enable integration with the PC switch fabricated on a separate die. In LNA #2, the switch pads were shorted on the CMOS die by a thick metal trace thus resulting in a hardwired 3 GHz operation. LNA #1 with open switch pads was used both for higher band CMOS-only testing, for integration with the PC switch and to serve as a control LNA for the 3/5 GHz modes, as described below. To isolate the effects of the flip-chip integration on the RF performance, and estimate the impact of the PC switch itself, two additional "control" chips were fabricated. In control chip #1, the PC material was replaced with metal (Au) to mimic an ideal short. In control chip #2, the GeTe layer was completely removed to mimic an ideal open circuit.

A total of six functional CMOS-PC LNA's (two per wafer) were available between the three wafers. The open/short circuits used in the control LNA's were fabricated on the B1 wafer.

2.4.2 Measurement Setup

All measurements were performed using on-wafer probing. Details of the setup for the control and CMOS-PC LNA's are shown in Figure 2.15. Power supplies and biases to the circuitry on the CMOS chip were provided via the PC chip using two DC probes. Two-port S-parameter measurements were made using an Agilent N5247A PNA-X vector network analyzer and two calibrated RF probes at the input and output of the LNA. To enable a fair comparison, the biasing conditions were adjusted slightly to keep the power consumption of the CMOS-PC and control

LNA identical to that of the CMOS LNA. All the LNAs were operated from a 1.2 V supply. The PC switch was transformed by using an Agilent 8114A pulse generator to apply voltage pulses to the heater through two pads on the PC chip. During characterization, the heater resistance was
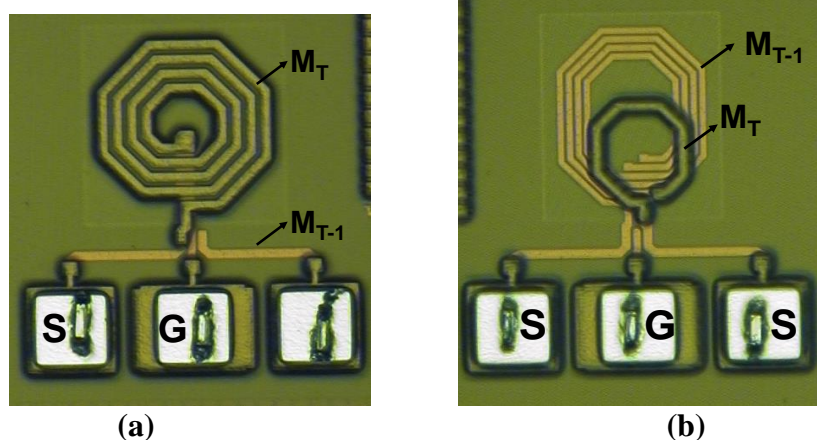
Figure 2.16 (a) Micrograph of the single-ended inductor test structure (drain inductor of the implemented CMOS LNA). (b) Micrograph of the high-*k* transformer test structure (source transformer of the implemented CMOS LNA). M_T = Top Metal.
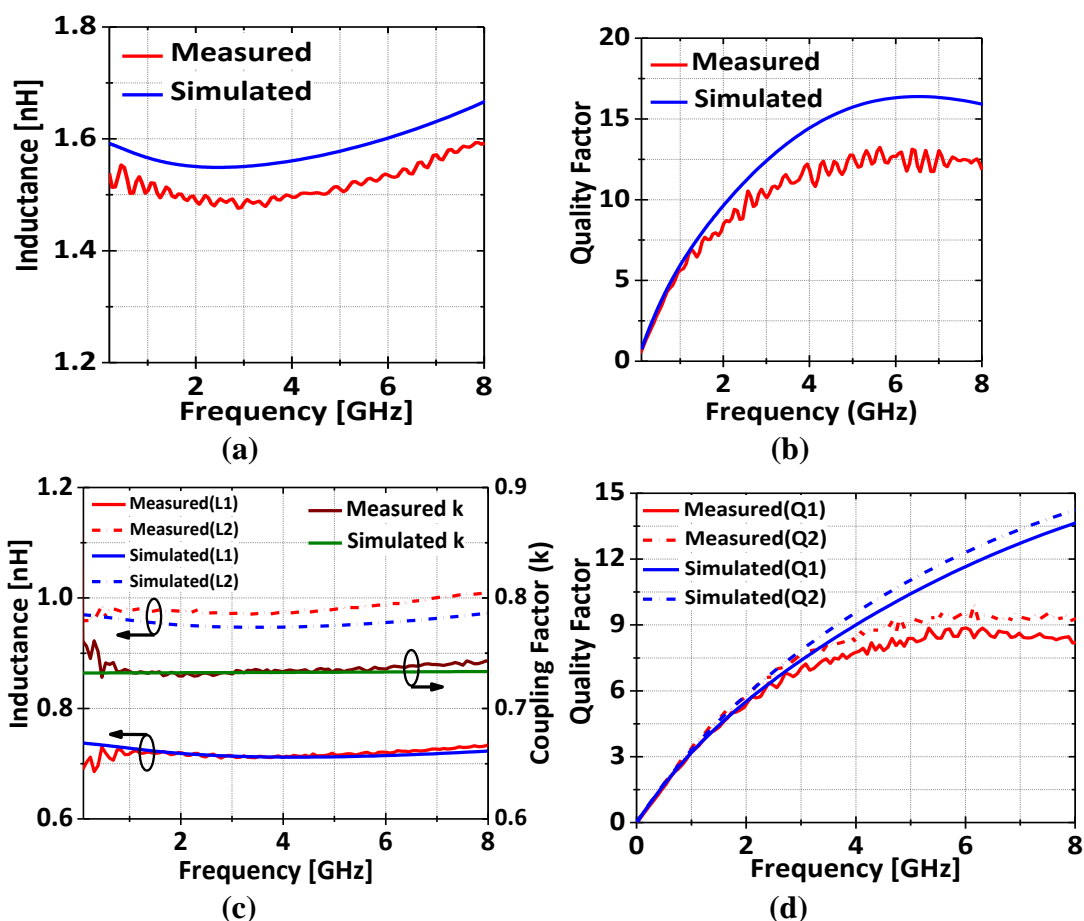
Figure 2.17 Measured and simulated (a) inductance, and (b) quality factor of the inducto test structure. Measured and simulated (a) inductances, coupling factor, and (b) qualit factor of the coils in the transformer test structure.

measured to ensure that no inadvertent breakdown had occurred in the heater path due the high

temperature stresses of the switching process.

	Band [GHz]	Peak S_{21} [dB]	Min S_{11}[1] [dB]	Min NF [dB]	Power[2] [mW]
Baseline LNA [CMOS only]	3	20.6	-9.6	1.9	7.2
	5	21.6	-9.9	2.25	3.6
Control LNA [CMOS + Open/Short on PC]	3	20.2	-6.5	2.55	7.2
	5	20.8	-6.9	2.8	3.6
CMOS-PC LNA	3	19.5	-8.1	2.85	7.2
	5	20.1	-6.0	2.86	3.6

Table 2-2 Summary of measured gain and NF of B1 devices.

(a)   (b)
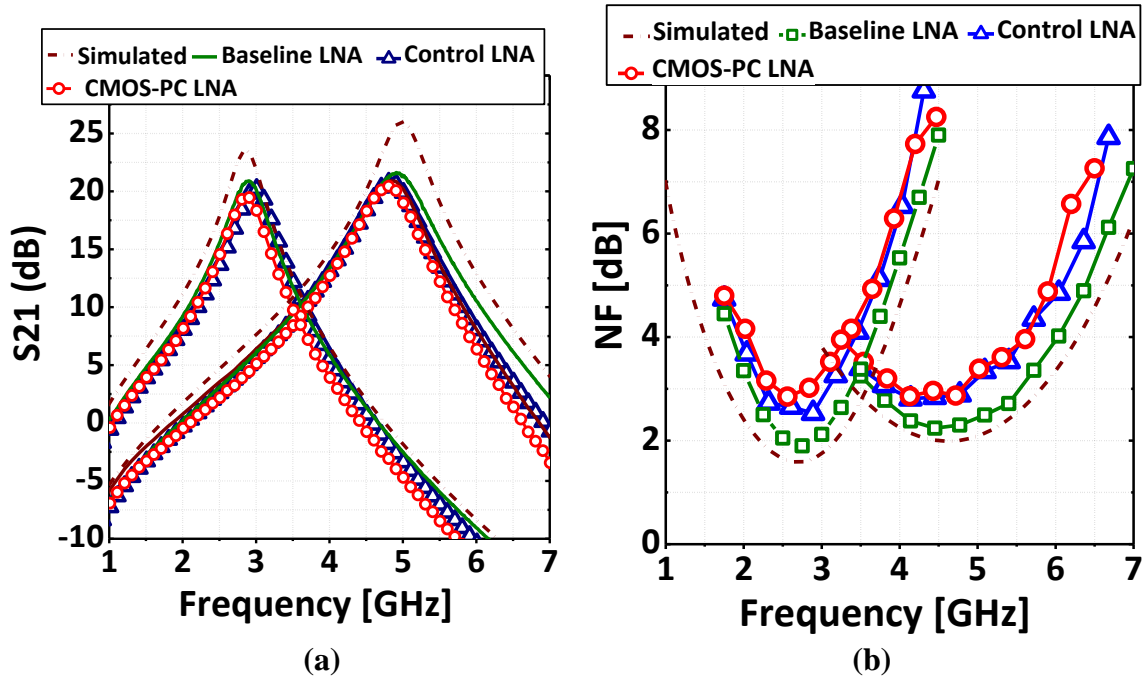
Figure 2.18 Measured (a) S_{21} and (b) NF of the CMOS-only baseline, control and the B CMOS-PC LNAs. Simulated LNA performance is also shown.

2.4.3 Characterization of Stand-alone Passive Structures

To verify the accuracy of our electromagnetic (EM) simulations, two stand-alone test structures with the same layouts as those of L_{DRAIN} and XFMR in Figure 2.16(a) were also fabricated on the same CMOS chip. Measured and EM simulated inductance and quality factor of L_{DRAIN} is shown in Figure 2.17, with <5 % error in the inductance value but with up to 20% error in Q values at 5 GHz. A proportional reduction in the LNA gain between simulations and measurement is therefore
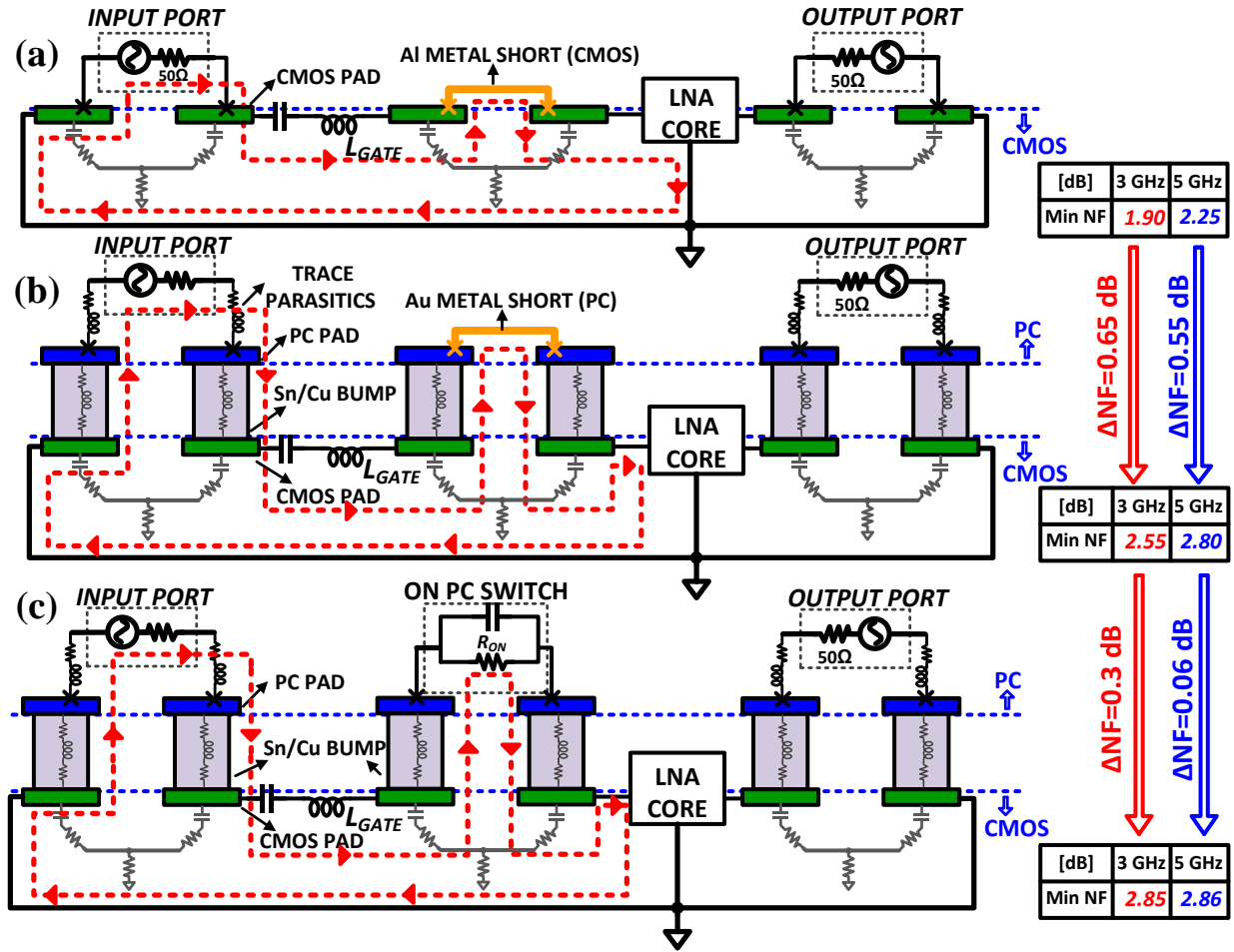
Figure 2.19 Illustration of the input signal return path (marked in dashed red line) in the 3 GHz mode for (a) baseline CMOS with a metal short, (b) control LNAs with Au metal short on the PC die, and (c) CMOS-PC LNA. In the 5 GHz mode, the input signal return path bypasses the switch pads completely, the metal shorts in (a) and (b) are absent, and the PC switch in (c) is in the off-state. The magnitude of change in the minimum NF observed in the three configurations is also shown.

expected. A similar trend was observed in the measurements of the primary/secondary coils of XFMR. The measured value of transformer k was same as the simulated value of 0.74. It is possible that the lower measured Q at higher frequencies was due to a higher bulk substrate resistivity assumed in our simulations.

2.4.4 Gain and NF Characterization of B1 and Baseline LNAs

Our first objective was to quantify the degradation caused by the flip-chip interconnect parasitics, and then to quantify the effect of the PC reconfiguration. This was done by comparing

the gain (S_{21}) and noise figure of the control LNA's and the CMOS-PC LNA against the baseline CMOS LNA. The chips used in this measurement, fabricated on the B1 wafer, were the same as

those reported in [4]. The results are plotted in Figure 2.18 and summarized in Table 2-2. The S_{21} includes the output buffer whose gain was simulated to be 0.95 with a 50 Ω load.

The peak S_{21} of the baseline LNAs was 20.9 (21.6) dB in the 3 (5) GHz mode, while the peak gain of the control LNAs was comparatively lower at 20.2 (20.8) dB in the 3 (5) GHz modes respectively. This level of degradation is expected since the addition of the bump bonds introduces additional resistances in the input/output signal paths and the power/ground network. The S_{21} of the CMOS-PC LNA was measured to be 19.5 dB and 20.1 dB in the two modes respectively. Simulations showed that a switch with R_{ON} ~ 2-4 Ω was unlikely to have caused the observed gain drop between the control and CMOS-PC LNAs. The reason for the excessive degradation was attributed to a weak solder joint in the CMOS-PC chip which led to increased contact resistance between the solder bumps and copper bond pads on the PC chip. To minimize the contact resistance, a layer of gold was coated on the copper pads before the bonding process in the second batch (B2). A consistently higher S_{21} was observed in the B2 devices (discussed in the next section), thereby verifying the finite effect of the bump bond contact resistances on the gain of the integrated LNAs.

The addition of solder bumps at the CMOS-PC interface also had a significant impact on the noise figure. Going from the baseline to the control LNA's, the NF was observed to increase from 1.9 (2.25) dB to 2.55 (2.8) dB in the 3 (5) GHz modes. To quantify this degradation due to flip-chip integration parasitics, an equivalent circuit was constructed for the baseline, control and CMOS-PC LNA's, as shown in Figure 2.19. Both the control and the CMOS-PC versions add four bump bonds into the signal path, and the traces on the PC chip contribute to additional parasitic
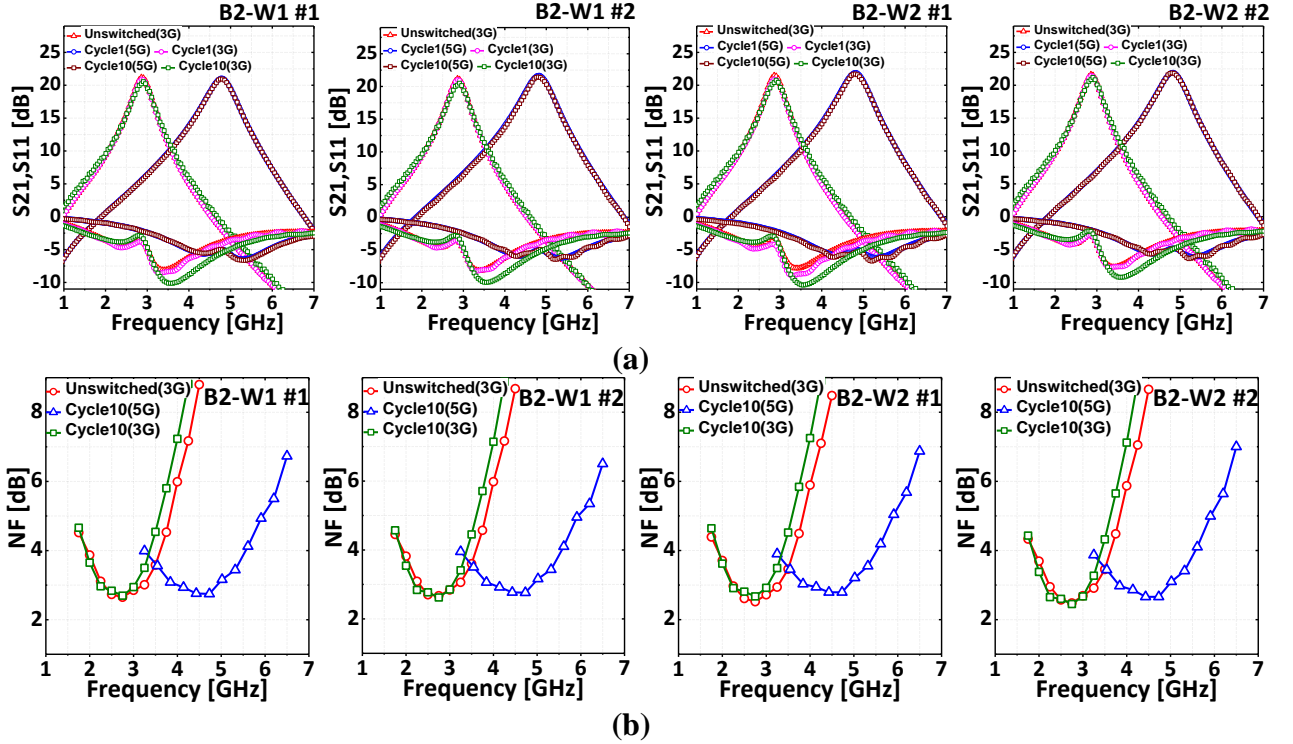
Figure 2.20 (a) Measured S_{21}, S_{11} and (b) NF of 4 CMOS-PC LNAs (batch 2) in the 3/5 GHz modes before switching, and after one/ten switching cycles.

# [T_{PC}]	Heater Properties			Band [GHz]	Peak S_{21} [dB]			Min S_{11}[3] [dB]			Min NF [dB]		IIP3[4] [dBm]	
	Resistance [Ohms]	Amorphization Pulse Voltage[1] [V]	Crystallization Pulse Voltage[2] [V]		Before Switching	After 1 cycle	After 10 cycles	Before Switching	After 1 cycle	After 10 cycles	Before Switching	After 10 cycles	Before Switching	After 10 cycles
B2-W1 #1 [50 nm]	32.7	8.0	4	3	21.2	20.9	20.2	-8.1	-8.6	-10.1	2.65	2.70	-12.1	-11.6
				5	–	21.1	21.0	–	-5.7	-6.6	–	2.75	–	-13.4
B2-W1 #2 [50 nm]	37.1	7.6	4	3	21.2	21.0	20.5	-8.2	-8.2	-10.0	2.67	2.65	-12.0	-11.6
				5	–	21.7	21.4	–	-5.9	-6.4	–	2.76	–	-13.6
B2-W2 #1 [75 nm]	23.4	8.7	4.8	3	21.5	20.9	20.8	-7.9	-8.9	-10.4	2.52	2.67	-12.6	-11.8
				5	–	21.9	21.7	–	-5.8	-6.8		2.79	–	-13.0
B2-W2 #2 [75 nm]	21.8	8.9	4.9	3	21.6	21.5	21.2	-7.7	-7.7	-9.2	2.46	2.48	-12.7	-12.5
				5	–	21.9	21.9	–	-6.1	-6.4		2.66	–	-13.8

Table 2-3 Performance summary of CMOS-PC LNAs fabricated in batch 2.
[1]The amorphization pulse is 100 ns wide. [2]The crystallization pulse is 1 µs wide. [3]S_{11} values reported at 3.4/5.3 GHz. S_{11} shift is discussed in section IV(E). [4]Two-tone test with RF inputs at 3/3.001 GHz and 5/5.001 GHz.

resistance, inductance and capacitance. In going from the control to the CMOS-PC LNA, additional parasitics are accrued due to the R_{ON} and C_{OFF} of the PC switch. A simple, approximate expression can be derived for the NF of the CMOS-PC LNA relative to the control LNA due to excess resistance caused by the insertion of the PC switch:
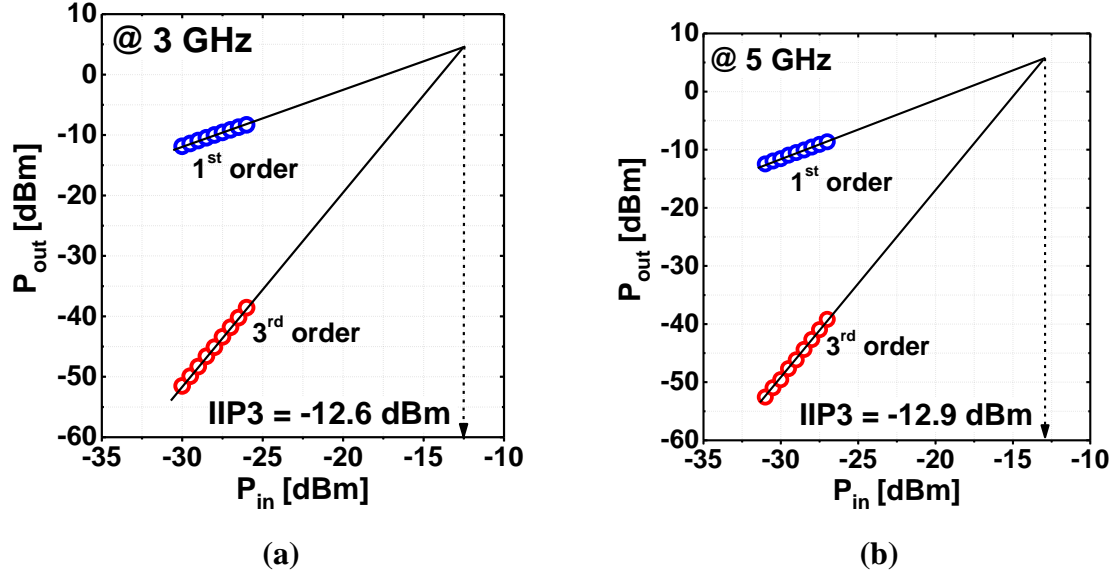
Figure 2.21 Measured IIP3 of the baseline LNA (CMOS-only) in (a) 3 GHz, and (b) 5 GHz modes.

	Technology		Peak S_{21} [dB]	Min NF [dB]	IIP3 [dB]	Power [mW]
[31]	0.18 µm CMOS	2.4	10.1	2.9	4	11.7
		5.2	10.9	3.7	-5	5.7
[32][1]	0.13 µm CMOS	2.4	22.1	2.8	-18.2	
		3.96	24	2.4	-18.5	4.6
		5.4	24.8	3.1	-20.4	
[33]	0.13 µm CMOS	2.4	9.4	2.8	-4.3	2.8
		6	18.9	3.8	-5.6	
[34][2]	0.13 µm CMOS	2.8	16.1	2.4	-4.0	
		3.3	14.2	3.0	-2.0	6.4
		4.6	14.2	3.7	-3.2	
[28][1]	0.35 µm BiCMOS+ MEMS varactor	2.7	7.7	4.2	-0.5	2.5
		3.1	10.2	4.7	-3	
This Work[3]	0.13 µm CMOS + PC switch	3	21.2	2.5	-12.5	7.2
		5	21.9	2.7	-13.8	3.6

Table 2-4 Performance summary and comparison.
[1] Continuous tuning (only select bands shown).[2] Only narrowband modes of LNA shown.[3] LNA B2-W2 #2 after 10 switching cycles.

$$NF_{CMOS-PC} = NF_{Control} + \frac{R_{PC}}{R_S}. \tag{2-14}$$

From the measurement data in Table 2-2, an excess resistance of 6.5 Ω is estimated for the Batch #1 CMOS-PC LNA. This is well in excess of the expected value of ~2 Ω due to the intrinsic R_{ON} of the PC switch. As discussed previously, this can be attributed to a weak solder joint in the Batch #1 CMOS-PC LNA. Indeed, NF measurements on Batch #2 devices revealed a degradation of only 0.1-0.2 dB for the CMOS-PC-LNA relative to the control LNA, (see next section), which results in a more reasonable estimate of $R_{PC} \sim$ 2-4 Ω. Taken together, these measurement results show that the integration of the CMOS-PC chips resulted in a tolerable degradation in the LNA's gain and noise performance despite flip-chip integration parasitics. These metrics also compare favorably with that of non-reconfigurable LNAs at similar frequencies [43].

2.4.5 Characterization of B2 CMOS-PC LNAs

Extended gain and NF measurements were conducted on batch 2 CMOS-PC LNA's as well. Each of the two wafers in batch 2 had two LNAs (B2-W1-#1, #2 and B2-W2-#1, #2). The LNAs were first measured in the as-fabricated condition before the application of switching pulses (deposited GeTe is in its crystalline state) and then after the first and tenth switching cycles, respectively. Each switching cycle comprised one amorphization pulse and one crystallization pulse. The measured S_{21}, S_{11} and NF of the four CMOS-PC LNAs are plotted in Figure 2.20. It can be observed that there was little or no change in the gain and the NF of all four LNAs between the and the tenth switching cycles, suggesting stable and reversible transformations. Table 2-3 summarizes the performance of the four CMOS-PC LNAs. Compared to B2-W1, the use of a thicker GeTe layer in B2-W2 LNAs resulted in a slight improvement in S_{21} and NF. Furthermore, compared to B1, B2 devices of same GeTe thickness (W1) also showed an improvement in S_{21} and NF due to the use of gold-coated pads. The input-referred third-order intercept point (IIP3) was measured before the first and after the tenth switching cycles, and is also summarized in Table 2-3.
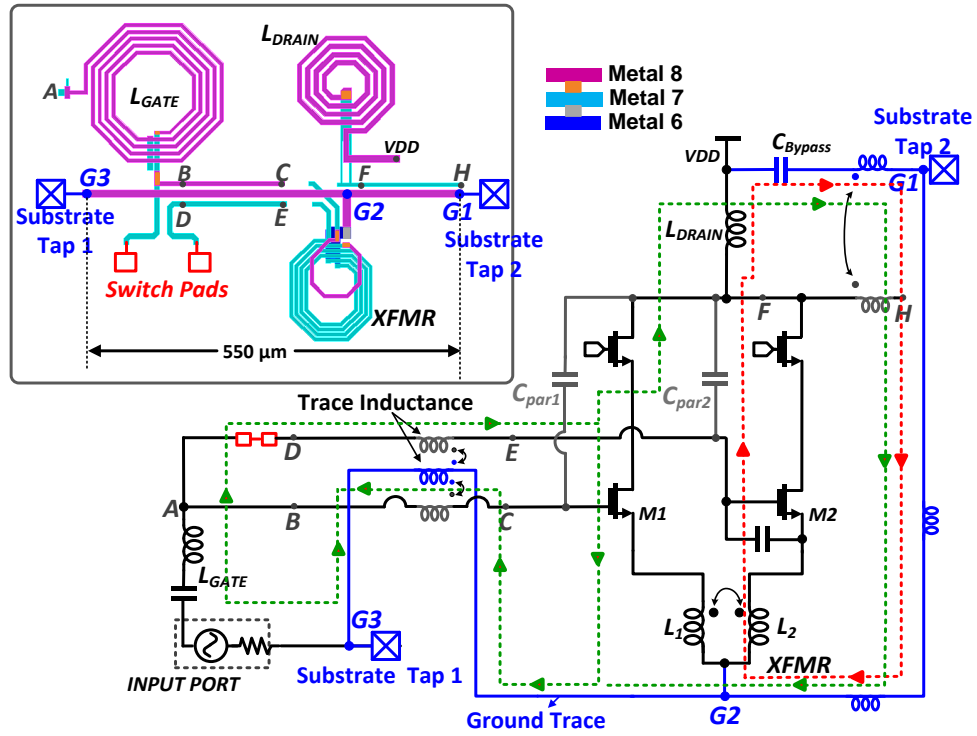
Figure 2.22 Circuit and layout floorplan of the LNA. The buffer is not shown. Two possible AC current loops (external input loop in green, internal loop through bypass capacitance in red) are marked by dashed lines. Interconnect segment *G1-G2-G3* with substrate taps on either end is the ground trace drawn in the top metal layer.

The two-tone tests were performed with RF inputs at 3/3.001 GHz and 5/5.001 GHz for the 3 GHz and 5 GHz modes respectively. The linearity of stand-alone PC switches was not characterized in this paper and has been characterized in [25] for similar switches. Since the standalone IIP3 of the PC switches is much higher than that of typical LNAs, they can be expected to have minimal impact on the overall linearity of the CMOS-PC LNA. Expectedly, the IIP3 of the baseline LNA (Figure 2.21) was nearly identical to the IIP3 of the CMOS-PC LNA reported in Table 2-3. In Table 2-4, the integrated LNA's performance is compared with previously reported CMOS and CMOS-MEMS multi-band LNAs. It is evident that due to the employed design techniques and a superior RF switch, the CMOS-PC LNA achieves identical gain, noise and linearity performance in both bands, an attribute missing from previously reported multi-band LNAs.
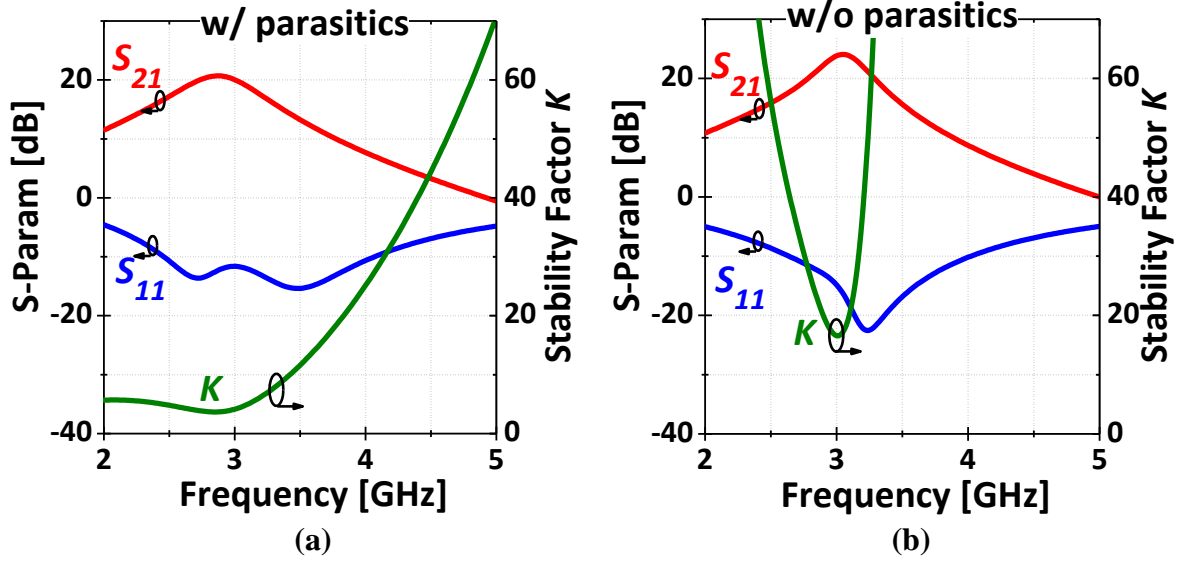
Figure 2.23 Schematic simulations of the LNA in the 3 GHz mode (b) with and (c) without an EM model of the input/output and ground metal traces and parasitic capacitances C_{par1} and C_{par2}. Both C_{par1} and C_{par2} were assumed to be 20 fF.

2.4.6 *Input Matching*

In Figure 2.20, it is shown that S_{11} of the CMOS-only baseline LNA was measured to be ~ -10 dB in both modes: this was higher than the simulated values and showed a frequency misalignment with the S_{21} peak. Furthermore, the stability factor [44], K, at the peak gain frequencies dropped below 5 (with $|\Delta| < 1$, where $\Delta = S_{21}S_{12} - S_{11}S_{22}$). In a single-ended LNA design, parasitics on the current return paths must be tightly controlled and minimized to avoid adverse impact on performance [45]. Figure 2.22 shows the circuit and layout floorplan of the LNA. Note that the substrate taps at either end of the LNA layout (marked as substrate taps 1 and 2) are connected through a long metal trace (*G1-G2-G3*) in the top metal instead of a low-impedance ground plane. This ground trace also runs parallel to the input and output feedlines creating parasitic magnetic couplings which can degrade the reverse isolation (S_{12}). Furthermore, the presence of parasitic capacitances (C_{par1}, C_{par2} in Figure 2.22) across the input-output terminals can also lower the gain, disrupt the input matching and further lower the isolation. These factors were erroneously
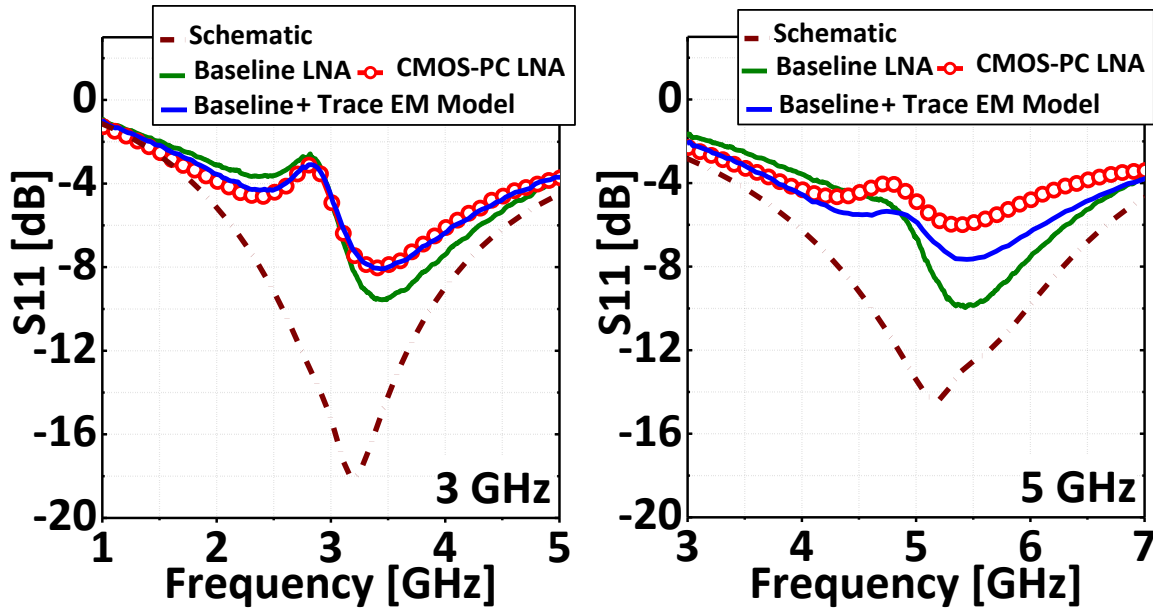
Figure 2.24 Effect of the addition of an EM model of the input traces on PC die on the S_{11} of the baseline CMOS-only LNA and its comparison with S_{11} of the B1 CMOS-PC LNA. Simulated S_{11} of the LNA schematic (comprising foundry-provided RF models of the transistor and capacitors, and EM models of the input/output pads, gate, drain inductors and the source transformer) is also shown.

overlooked during the design phase, thereby creating higher order effects, evidenced by S_{11} deviation from narrowband behavior and a reduction of stability factor K. While identification of all the parasitic capacitances and ground return paths proved to be difficult, diagnostic schematic-only simulations of the LNA (Figure 2.23(a), (b)) in the 3 GHz mode with and without an electromagnetic (EM) model of the trace parasitics and explicitly added C_{par1}, C_{par2} (each equal to 20 fF) showed that the aforementioned reasons were likely responsible. The parasitic capacitance values in simulations were chosen to match the S_{11} frequency shift observed in measurements.

Flip-chip integration also caused degradation of the S_{11} of the control LNA and the CMOS-PC LNA relative to the baseline LNA, as can be observed from Figure 2.24. This degradation is attributed to the long traces which were required on the PC chip at the input and the output of the LNA. Note that the parasitics from the bump bonds and PC pads were not significant enough to
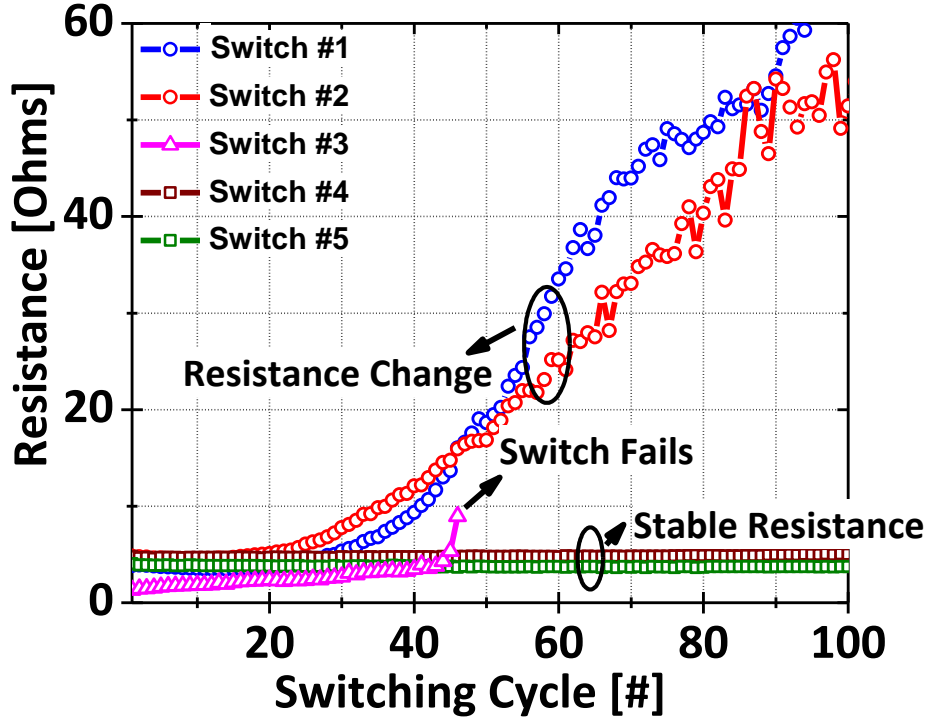
Figure 2.25 Measured resistance change of 5 standalone-switches over 100 switching cycles.

alter the input network characteristics. In Figure 2.14(b), it is shown that each of the input traces is > 1.75 mm long (standalone inductance of ~ 1.35 nH). Since the integrated LNAs were wafer-probed, such long traces, appearing in series with the CMOS input network, were necessary to provide sufficient clearance between the DC and RF probes. When the EM model of the input traces was added to a simulation setup comprising measured S-parameters of the baseline LNA, the degradation in S_{11} was similar to that observed in the CMOS-PC LNA (Figure 2.24). These results show that the relatively higher S_{11} of the integrated LNAs can be avoided in practice by wire-bonding to the PC chip rather than wafer probing, thereby eliminating the aforementioned traces.

2.4.7 Cyclability

Although GeTe switches show exceptional RF performance, they have been known to either stop switching completely or show an increase in its R_{ON}, especially after a period of continuous
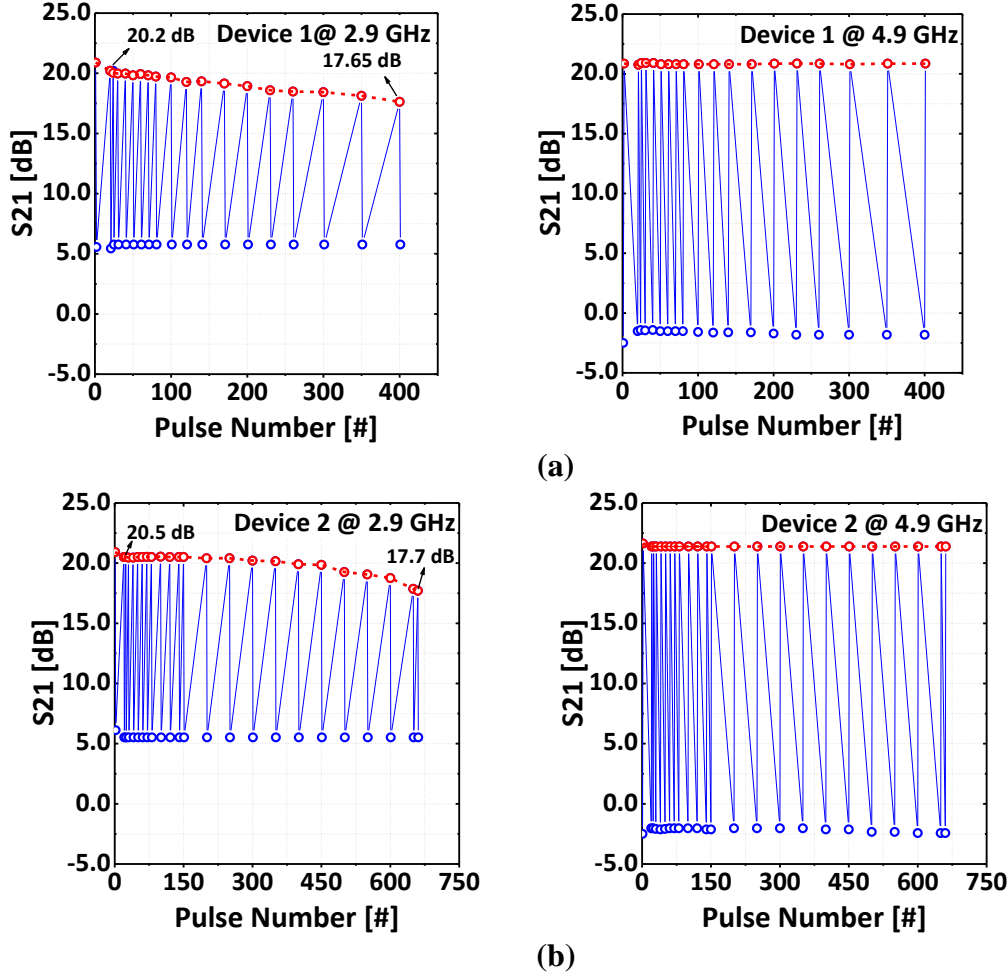
Figure 2.26 (a) Measured LNA-PC B2-W1 #1 S_{21} at 2.9 GHz and 4.9 GHz over 200 switching cycles (total number of pulses = 400). Each switching cycle comprises one amorphization and one crystallization pulse. (b)Measured LNA-PC B2-W1 #2 S_{21} at 2.9 GHz, and 4.9 GHz over 330 switching cycles (total number of pulses = 660).

switching activity. Switch failures can be attributed either to a heater breakdown from temperature stresses or due to the degradation of the GeTe material into an intermediate state between the amorphous and crystalline phases [46]. The slow increase in R_{ON} observed in some switches may be similarly attributed to pockets of amorphous GeTe developing within the crystallized volume eventually leading to switch failure. To characterize this behavior, ON- and OFF-state resistances of several stand-alone switches were studied over 100 switching cycles. It was observed that the switches behaved in one of three ways:

(1) R_{ON} remained stable only for a few cycles after which a steady increase in its value was observed. The number of cycles with stable R_{ON} as well as the subsequent rate of increase was different for different switches, even though they were designed to have similar dimensions. This behavior, observed for most of the switches, is represented by switches marked #1 and #2 in Figure 2.25. (2) R_{ON} remained stable for a few cycles after which the switches failed immediately. This behavior, less common than (1) and mostly attributable to heater failure, is represented by switch #3 in Figure 2.25. (3) R_{ON} remained stable for the entire duration of switching measurements. This behavior, again less common than (1), is represented by switches #5 and #6 in Figure 2.25. Note that, for most of the switches, the heater resistance itself showed little change even after 100 switching cycles. The improvement in heater reliability can be attributed to the use of the thermally conductive AlN as the barrier layer in this work. To observe the impact of the R_{ON} drift, the RF performance of two of the batch 2 CMOS-PC LNAs (B2-W1 #1 and B2-W1 #2 in Figure 2.20) was characterized over several hundred switching cycles. The S_{21} results are shown in Figure 2.26, and the NF results in Figure 2.27. CMOS-PC LNA #1 showed little change in lower-band S_{21} up to 100 cycles, after which a more rapid deterioration was observed. No change was observed in the higher band S_{21} as it does not depend on R_{ON}. The experiment was stopped at 200 cycles, at which point the S_{21} had already degraded by over 2.5 dB. NF, measured after 200 cycles, had increased to 4.4 dB from 2.65 dB, measured after 10 cycles. On the other hand, LNA #2 showed stable RF performance for larger number of cycles: the start of S_{21} degradation was observed only after 225 cycles. It is evident that the degradation in LNA performance with increasing switching activity can be attributed to the increase in R_{ON} observed in Figure 2.25. Unfortunately, the RF performance of other functional CMOS-PC LNA's could not be similarly characterized as they were lost prematurely due to an ESD event. Obviously, future revisions of the PC switch design
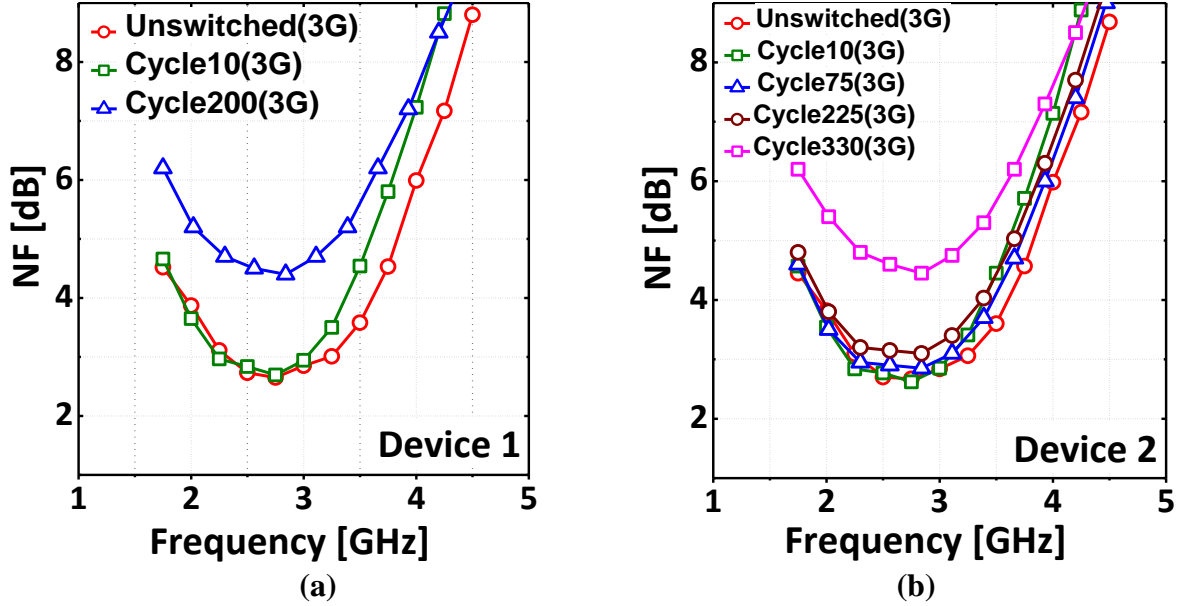
Figure 2.27 Measured NF in the 3 GHz mode of (a) LNA-PC B2-W1 #1, and (b) LNA-PC B2-W1 #2 over large number of switching cycles.

address the issue of R_{ON} drift to improve their switching reliability well beyond what has been reported here and in the related state-of-the-art [17], [46]. While this will be an important task in the development of this technology, no attempt was made to optimize or engineer the cyclability of the devices presented here, nor to understand the source of the R_{ON} drift. Thus, the behavior of these devices should not be taken as seriously limiting the potential application of this technology. Recently, Sb-Te based phase-change switches with improved fabrication and heater construction has demonstrated switching cycle endurance greater than 300,000 [47] for the first time by a commercial lab thereby strengthening the case for phase-change material based RF switches.

2.5 Integrated CMOS-PC LNA Summary

This work has demonstrated that by using GeTe-based PC switches with high cut-off frequencies (F_{CO}), parasitic-sensitive narrowband RF C MOS circuits such as an LNA can be stably and reversibly reconfigured across disparate frequency bands, while simultaneously achieving RF performance approaching that of non-reconfigurable CMOS-only implementations. A compact, dual-frequency narrowband low-noise amplifier reconfigured using a four-terminal phase-change

RF switch has been designed and fabricated. Extensive characterization of several prototypes is presented demonstrating robustness and repeatability of the PC switch reconfiguration. Finally, this work highlights the importance and feasibility of adopting a circuits-technology co-design approach towards the development of new integrated systems such as CMOS-PC as an enabling technology for complex field programmable transceivers.

3 A Triple-Band (2.5/3/3.5 GHz) Power Amplifier with a Frequency Reconfigurable Power Combiner

3.1 Introduction

Modern cellular applications require power amplifiers (PA) with multi-watt output power levels. To facilitate integration, there has been a strong push to realize multi-watt PAs in standard CMOS processes. However, this is a challenging problem due to the low quality factor of integrated passives and the low breakdown voltage of active devices. The latter limits the driving capabilities of CMOS amplifiers, thereby mandating the use of a passive combiner network. The combiner is usually transformer-based [48]-[49], and is usually categorized as series-combining or parallel-combining, depending on whether voltage or current is combined at the load [50]. In other words, a series-combining structure combines voltages (Figure 3.1(a), while a parallel-combining structure combines currents Figure 3.1(b)). Current-combining ensures channel symmetry and compared to voltage combiners, suffer from lesser efficiency degradation due to amplitude and phase mismatches between the unit amplifiers [51]-[53]. Voltage combiners are more common as they facilitate the transformation of a 50Ω load to a low impedance at the unit

(a)	(b)
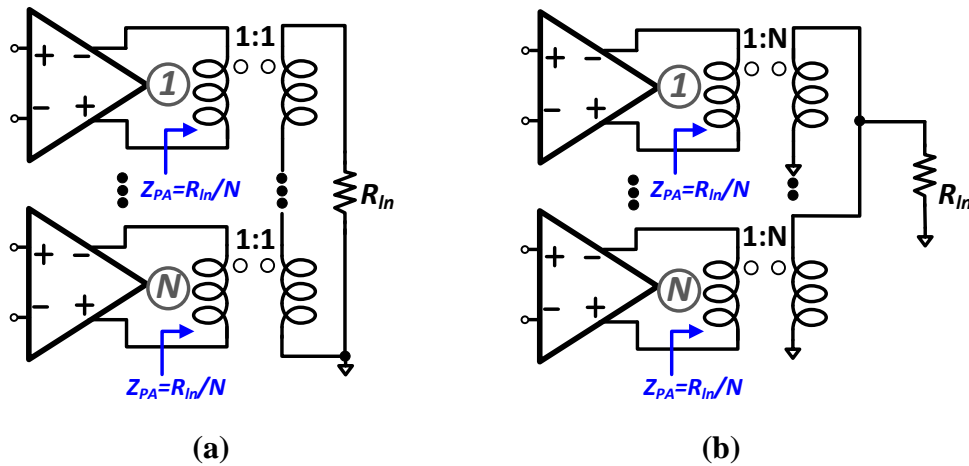
Figure 3.1 Transformer-based power combiners. (a) Voltage combiner, and (b) current combiner with 1:N turns ratio.
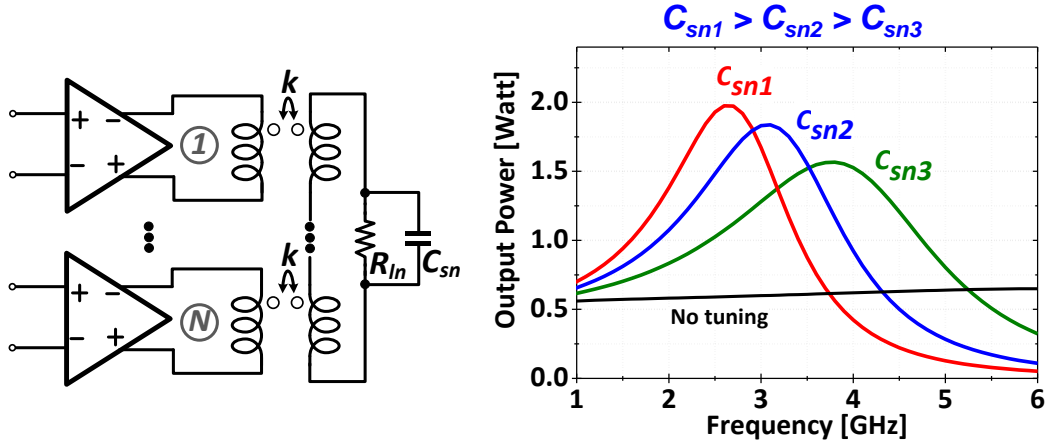
Figure 3.2 Secondary tuning capacitance in a voltage transformer combiner and its effect on output power level.

amplifier output, resulting in high output power delivery from each unit PA. On the other hand, current combining results in a higher PA output impedance resulting in a reduction of power delivered from each unit PA. Thus, the unit transformer in a current combiner requires a 1:N turns ratio in order to present the same impedance to the unit amplifier and deliver the same power to a 50Ω load as an N-way voltage combiner with 1:1 unit transformers (Figure 3.1). Realizing a turns ratio greater than 1 is usually not possible in standard CMOS processes with a single thick metal. Therefore, due to their ease of implementation, we limit our analysis in this work to series-combining networks / voltage combiners for sub-5 GHz frequencies. Phase and amplitude mismatches between unit amplifiers are likely to be much worse at mm-wave frequencies, and current-combining then might indeed prove to be a better choice of implementation despite the layout challenges [51], [53].

In previous implementations of voltage combiners, the values of the coil self-inductances are optimized at a given frequency, and a fixed tuning capacitor (C_{sn} in Figure 3.2) is inserted in the secondary network to minimize the insertion loss [48]-[49]. While the capacitor can also be placed in series with the load, a shunt capacitor is preferred for narrowband applications [54]-[56]. If a

(a)

(b)
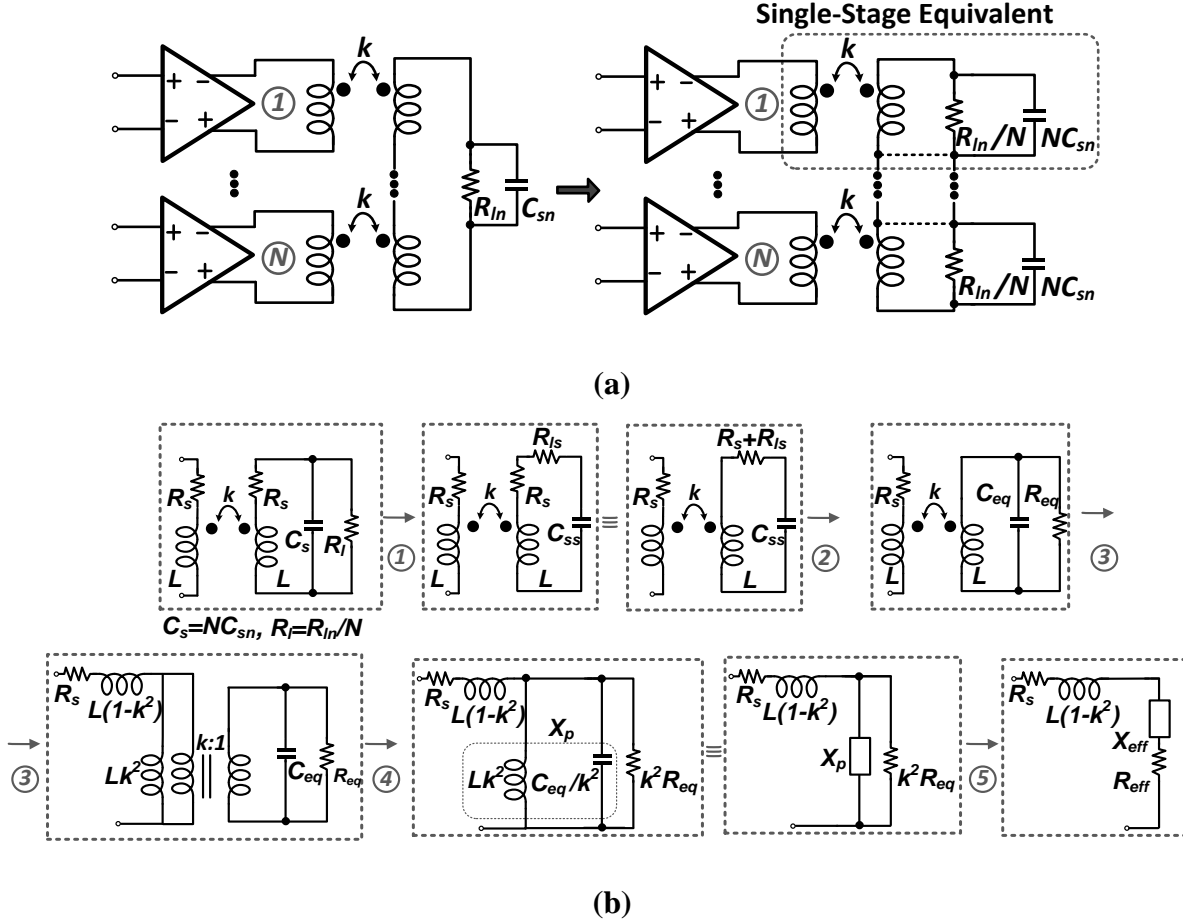
Figure 3.3 (a) Single-stage equivalent of the transformer combiner. (b) Transformation steps to derive a simplified equivalent network of a single-stage of the transformer combiner.

series capacitor is used, the efficiency curve shows a high-pass response, and is more suited for broadband applications. However, the combiner then loses its frequency-shaping characteristics favorable in narrowband applications to suppress higher harmonics. Thus, while using a shunt capacitor is useful for narrowband applications, it limits the use of a PA with a large-footprint transformer network to a single standard. This is because of a lack of high-voltage CMOS switches to enable switching of the shunt capacitance between different standards. In this work, we show that by switching capacitances inserted between low-swing nodes of the secondary coil of the combiner network, the voltage stand-off requirement on the switches is vastly reduced, and the

same transformer combiner can be used to realize multi-standard operation using regular CMOS switches.

3.2 Power Combiner Efficiency

The efficiency of the amplifier stage and the combiner network together determine the overall power efficiency of the PA. The amplifier efficiency depends on the amplifier class as well as the presence of optimal load impedance (Z_{opt}) at the amplifier output. The passive combiner often functions as a matching network to transform the antenna load to the required Z_{opt} of the amplifier. In order to design the combiner for maximum efficiency, we begin by considering a single-stage equivalent of an N-way power combiner [Figure 3.3(a)]. The simplified structure with a transformer and output network is also shown in Figure 3.3(b). Note that k and R_s represent the coupling factor and the low-frequency series loss of the coils respectively. R_l ($= R_{ln}/N$) is the load at the secondary side while C_s ($= NC_{sn}$) is the secondary parallel capacitance. A sequence of transformation steps, comprising successive parallel-to-series and series-to-parallel conversion steps is performed to absorb the secondary coil loss into an equivalent output network comprising a shunt-RC load (C_{eq} and R_{eq}). Note that after the first transformation step, we have:

$$R_{ls} = \frac{R_l}{1+\left(\omega_0 C_s R_l\right)^2}; \; C_{ss} = C_s\left\{1+\left(\frac{1}{\left(\omega_0 C_s R_l\right)^2}\right)\right\}. \tag{3-1}$$

Here, ω_0 represents the frequency of operation. Since the secondary-side load (R_l) can be considered a constant (= 50 Ω) for simplicity, the secondary-side efficiency can be written as a function of ω_0, L, Q_0 and C_s as follows:

$$\eta_s = \frac{R_{ls}}{R_{ls} + R_s} = \frac{1}{1 + \left(\dfrac{\omega_0 L}{Q_0}\right)\left\{\dfrac{1 + \left(\omega_0 R_l C_s\right)^2}{R_l}\right\}}$$

(3-2)

$$\Rightarrow \eta_s = f_1\left(\omega_0, L, Q_0, C_s\right),$$

where Q_0 represents the quality factor of a coil with self-inductance L at ω_0. After the second transformation step, R_{eq} and C_{eq} are given by:

$$R_{eq} = \left\{R_s + R_{ls}\right\}\left(1 + Q_1^2\right); \quad C_{eq} = \frac{C_{ss} Q_1^2}{\left(1 + Q_1^2\right)},$$

$$\text{where } Q_1 = \frac{1}{\omega_0 C_{ss}\left(R_s + R_{ls}\right)}.$$

(3-3)

In the third transformation step, the transformer is then replaced by its T-model equivalent structure comprising an ideal transformer. Finally, in the fourth transformation step, the secondary impedances are reflected to the primary side. Thus, the transformer network along with the load is reduced to an equivalent structure represented by an effective resistance R_{eff} in series with a residual reactance X_{eff}. Now, the primary-side efficiency also be written as a function of ω_0, L, Q_0 and C_s as follows:

$$\eta_p = \frac{R_{eff}}{R_s + R_{eff}} = f_2\left(\omega_0, L, Q_0, C_s\right), \text{ where}$$

$$R_{eff} = \left\{\frac{X^2 k^2 R_{eq}}{X^2 + \left(k^2 R_{eq}\right)^2}\right\}, \quad X = \left\{\omega_0 k^2 L\right\} \parallel \left\{\frac{k^2}{\omega_0 C_{eq}}\right\}$$

(3-4)

Thus, from (3-1)-(3-4), the overall efficiency can be derived as:

$$\eta_{overall} = \eta_s \eta_p = f\left(\omega_0, L, Q_0, C_s\right).$$

(3-5)
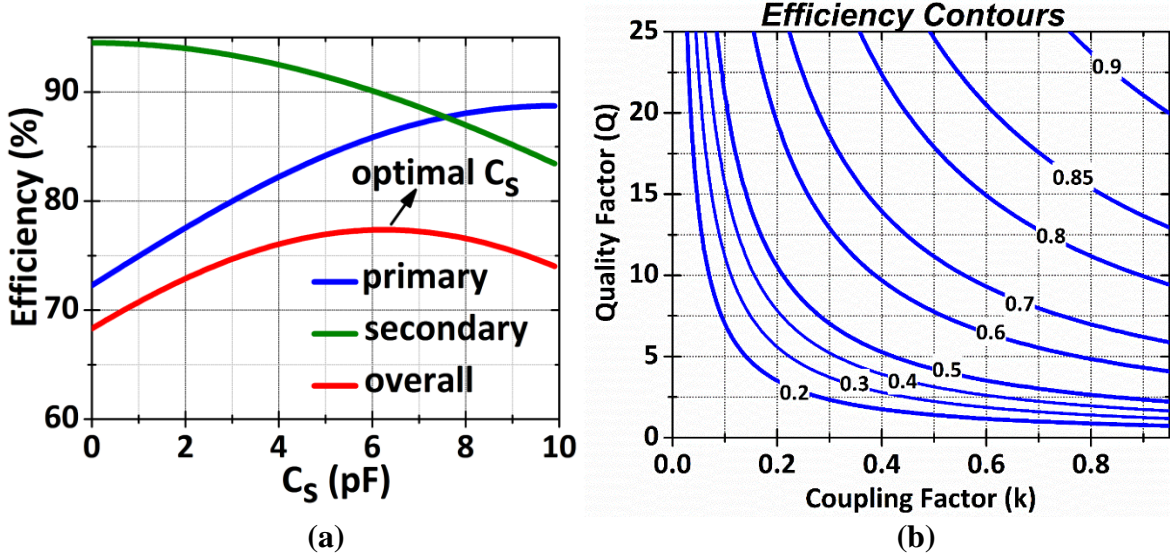
Figure 3.4 **(a) Variation of transformer efficiency with C_s. Here, $L = 0.68$ nH, $k = 0.7$, $Q_0 = 12$, $\omega_0 = 2$ GHz. (b) Transformer maximum efficiency contours in the (k,Q) design space.**

Using (3-2)-(3-4) in (3-5), it is observed that the overall efficiency is also a function of ω_0, L, Q_0 and C_s. However, as the best achievable Q_0 for a given inductance L is constrained by the process's metal stack, we can deduce that the transformer efficiency at any given frequency ω_0 and fixed k is a function of only two parameters: L and C_s. **(a)**

(b)

Figure 3.4 Figure 3.4 shows the variation of the primary-side and secondary-side efficiencies of a transformer with 0.68 nH inductors with different values of C_s at 2 GHz. Observe that while primary-side efficiency improves with C_s, the secondary-side efficiency degrades. Therefore, at each value of L, there exists an optimal value of $C_s(C_{s,opt})$ at which the overall efficiency is maximized. By taking the derivative of the expression in (3-5) with respect to C_s, the $C_{s,opt}$ value is determined to be

$$C_{s,opt} = \frac{1}{\omega_0^2 L(1+k^2+Q_0^{-2})} \stackrel{Q>>1}{\approx} \frac{1}{\omega_0^2 L(1+k^2)}. \tag{3-6}$$

Similarly, by taking the derivative of the expression in (3-5) with respect to L, the L_{opt} value is determined to be

$$L_{opt} = \frac{Q_0 R_l}{\sqrt{\omega_0^2 \left(\left(k^2 + 1 \right) Q_0^2 + 1 \right) \left(C_s^2 R_l^2 \omega_0^2 + 1 \right)}} \, .$$

(3-7)

Next, the value of C_s and L that satisfy both (3-6) and (3-7) simultaneously is found to be:

$$L_{opt} = \frac{Q_0 R_l \sqrt{1 + \left(k Q_o \right)^2}}{\omega_0 \left(1 + Q_o^2 (1 + k^2) \right)}, \quad C_{s,opt} = \frac{Q_o}{R_l \omega_0 \sqrt{1 + \left(k Q_o \right)^2}}$$

(3-8)

Therefore, for a given Q_0 and k (both limited by process characteristics), one can find the maximum achievable efficiency (η_{max}) by using the values of $C_{s,opt}$ and L_{opt} from (3-8) in (3-5) resulting in (3-9) where the dependency of η_{max} on the transformer's kQ product is clearly seen:

$$\eta_{max} = \frac{k^2 Q_o^2 - 2\sqrt{k^2 Q_o^2 + 1} + 2}{k^2 Q_o^2} = \left(\frac{\sqrt{1 + \left(k Q_o \right)^2} - 1}{k Q_o} \right)^2 \, .$$

(3-9)

Figure 3.4(b) plots η_{max} contours in the (k, Q) design space. In a typical CMOS process, inductor Q is usually less than 15, and the best achievable coupling factor k is usually between 0.6 (co-planar primary/secondary coils in a process with a single thick RF metal) and 0.75 (overlaid coils in a process with two thick RF metals). Thus, η_{max} is usually between 60% (insertion loss of -2.2 dB) and 80% (insertion loss of -0.97 dB).

3.3 Optimum Combiner Design

To choose an optimum value of L and C for operation at a particular frequency, the following procedure was adopted: using (3-6), $C_{s,opt}$ values for different values of L ranging from 0.1 nH to
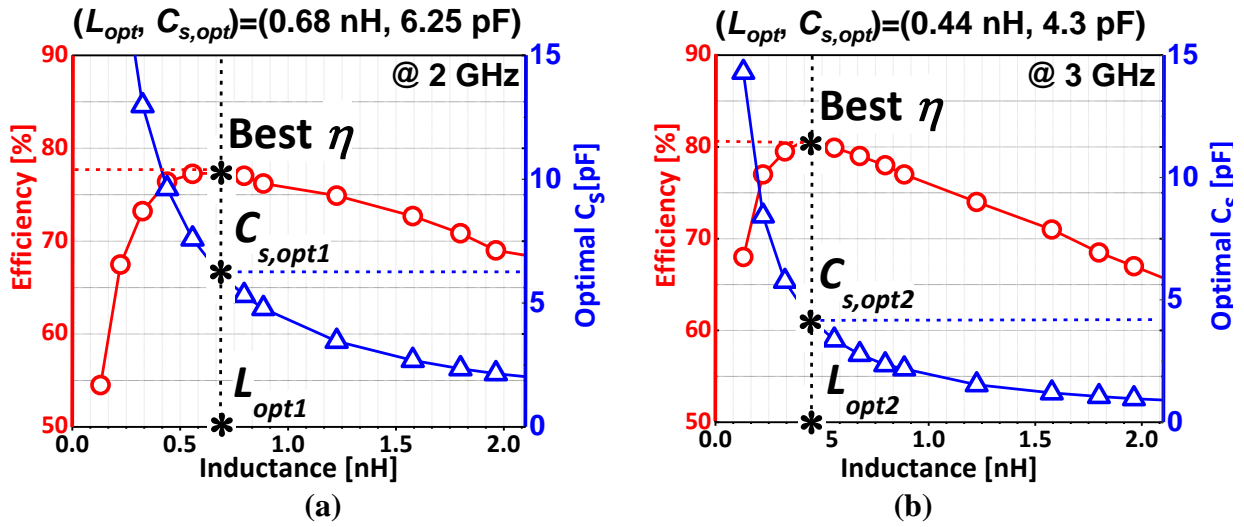
Figure 3.5 Transformer efficiency for different values of coil self-inductance (*L*) at (a) 2 GHz, and (b) 3 GHz.

ω_o		$[L, C_s]$ (nH, pF)	η (%)
2 GHz	Optimized L, C_s	[0.68, 6.3]	77.5
3 GHz	Fixed L, C_s	[0.68, 6.3]	71.5
	Switch only C_s	[0.68, 2.8]	79
	Switch L and C_s	[0.44, 4.3]	81
3 GHz	Optimized L, C_s	[0.44, 4.3]	81
5 GHz	Fixed L, C_s	[0.44, 4.3]	69
	Switch only C_s	[0.68, 1.5]	81
	Switch L and C_s	[0.22, 3.0]	82

Table 3-1 Efficiency comparison of dual-band transformer combiner with optimized values of *L* and *Cs*.

2 nH at 2 GHz and 3 GHz were calculated. Q values at these frequencies were determined from single- and two-turn inductors available in a standard non-RF 65 nm CMOS process. Since the maximum coupling realizable with planar transformer structures is known to be less than 0.75, a k value of 0.7 was used in this analysis. The variation in the transformer efficiency at different values of L is shown in Figure 3.5. The values of $(L_{s,opt}, C_{s,opt})$ for which efficiency is maximized are (0.68 nH, 6.3 pF) and (0.44 nH, 4.3 pF) at 2 GHz and 3 GHz respectively. Now, consider the
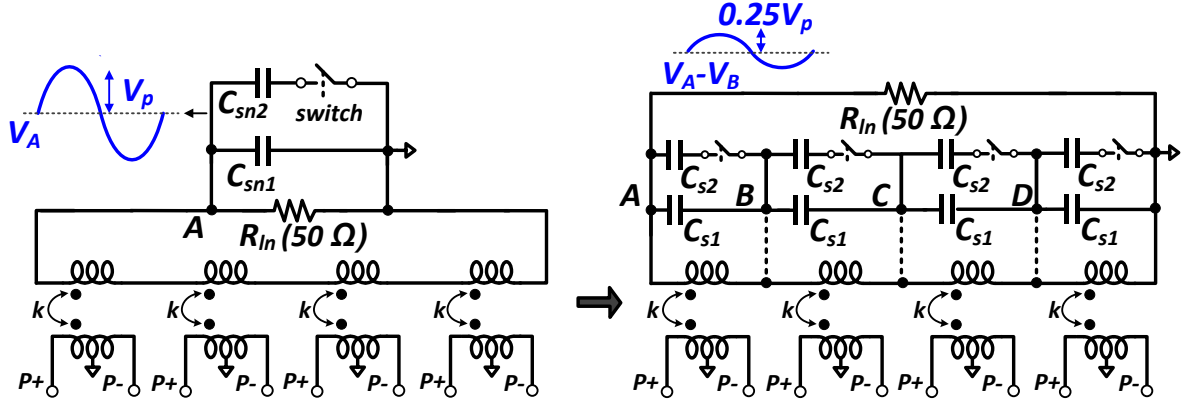
Figure 3.6 Capacitance-switched dual-band power-combining PA.

implications when this optimized transformer network is to be used in a dual-band PA. We begin

with optimized L and C_s values at 2 GHz (3 GHz), using the procedure outlined above, and then

study the impact on efficiency if only L or C_s or both were selectively optimized for operation at

3 GHz (5 GHz). Optimally, both L and C's will have to be switched to transition between the

bands. However, we observed that as long as the center frequencies of the intended multi-band

operation were not too far apart (within 2-3 GHz of each other), switching both L and C_{sn} resulted

in only a minor improvement in efficiency compared to the case when only C_{sn} was switched (see

Table 3-1). Switching capacitive elements only is preferable since inductor switching complicates

the combiner layout and requires reconfiguration switches with very low on-state resistance to

avoid severely affecting the network quality factor and efficiency. However, switching C_{sn} imposes

challenging voltage-handling requirements on the switch. For example, even at an output power

level of 0.25W, the peak voltage swing across the switched capacitor in the off state will be ~5V,

which is beyond the breakdown voltages of thin/thick-oxide CMOS transistors. While the voltage

swing across the switches can be reduced by using stacked switched capacitors (Figure 3.6), this

is still impractical as very wide switches would be required in a stacked configuration to minimize

loss thereby introducing significant parasitics. In this analysis, we assume that the same amplifier
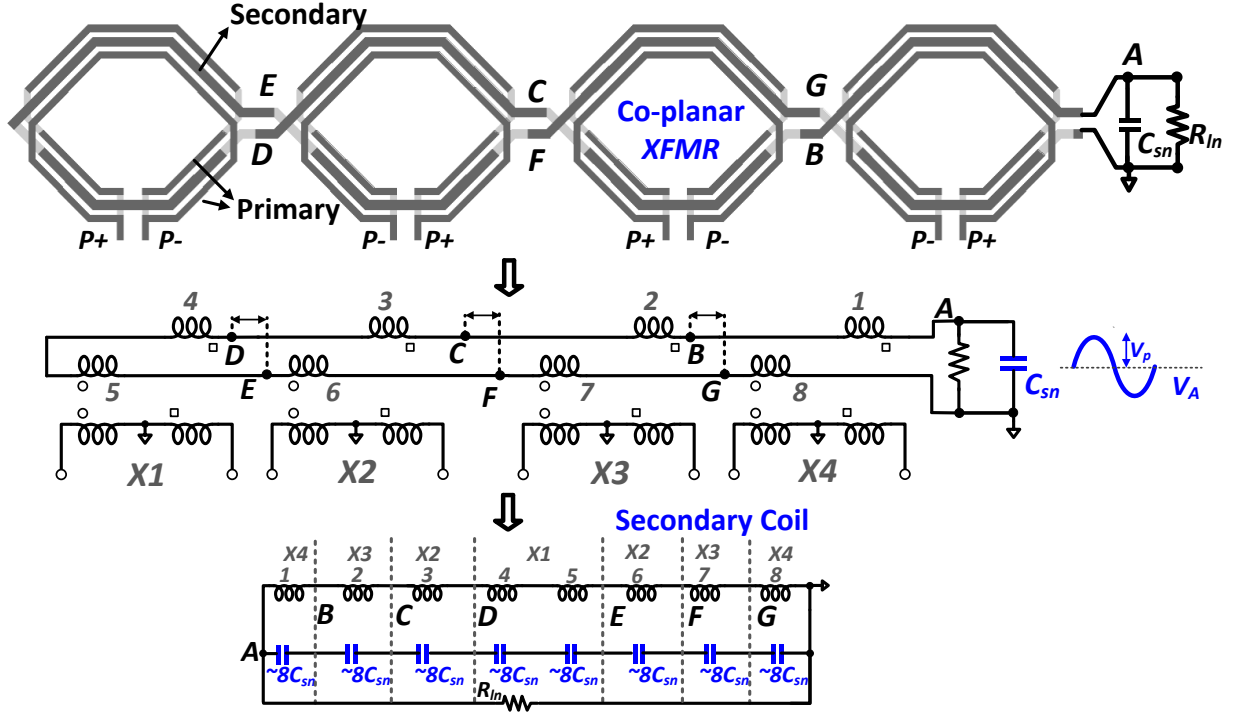
Figure 3.7 Figure-8 combiner and its equivalent circuit representation.

stage can be used at both the frequencies as the optimal impedance Z_{opt}, to a first order, is broadband [57].

3.4 Proposed Reconfigurable Transformer Combiner

The transformer combiner layout, and hence its equivalent circuit representation, generally differs significantly from the simplistic representation in Figure 3.6. In order to realize low insertion loss transformer combiners in standard CMOS processes, a 'figure 8' layout was proposed in [49]. This layout minimizes the negative mutual coupling between adjacent primary leads and current crowding effects, resulting in better coupling and efficiency. A similar 'figure 8' 4-way transformer combiner in a 9-metal 65 nm process without any special RF process options (Figure 3.7). Both the primary and secondary coils were laid out in the top thick metal (M_T) with underpass elements in the lower metal layer (M_{T-1}). From the equivalent circuit representation of the combiner, it is observed that given a value of secondary tuning capacitance C_{sn}, an effective
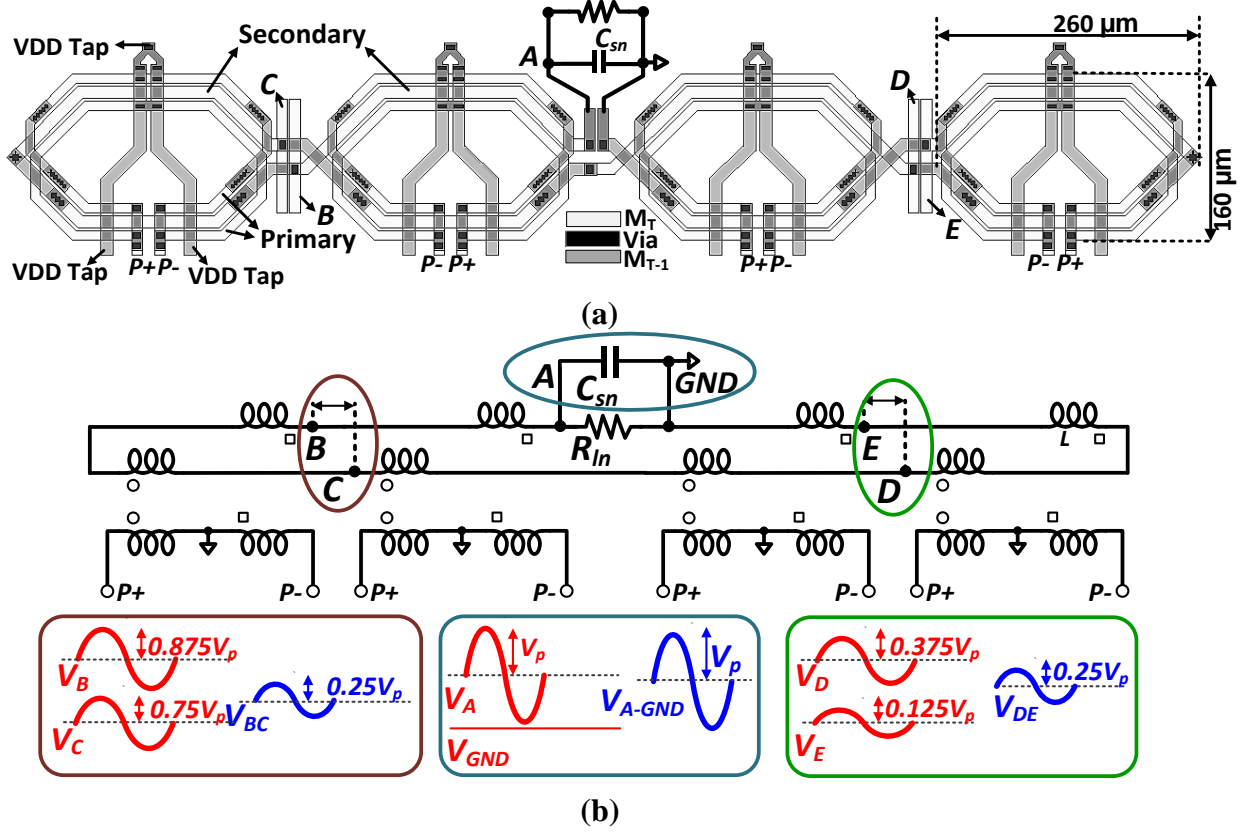
Figure 3.8 (a) Modified 'figure-8' layout of the designed transformer combiner for low insertion loss and high coupling. The locations of two pairs of low-swing nodes (B-C and D-E) are also shown. (b) Equivalent circuit representation.

capacitance $4C_{sn}$ appears across each of the unit transformers. To make this transformer reconfigurable, the value of C_{sn} will have to be switched, which has been discussed to be infeasible in the previous section.

In contrast to the original design in [49], our proposed design places the secondary coil taps at the center of the combiner resulting in a more symmetric design. The combiner layout and the equivalent circuit representation is shown in Figure 3.8. Optimal C_{sn} values for maximum efficiency at 2.5 GHz, 3 GHz and 3.5 GHz were determined to be 1.3 pF, 0.9 pF and 0.6 pF respectively (Figure 3.9(a)), and the frequency-dependent efficiency curves with the optimized C_{sn} values were plotted (Figure 3.9(b). Thus, an efficiency of approximately 70% represents the maximum achievable non-reconfigurable performance of the designed power combiner at the two
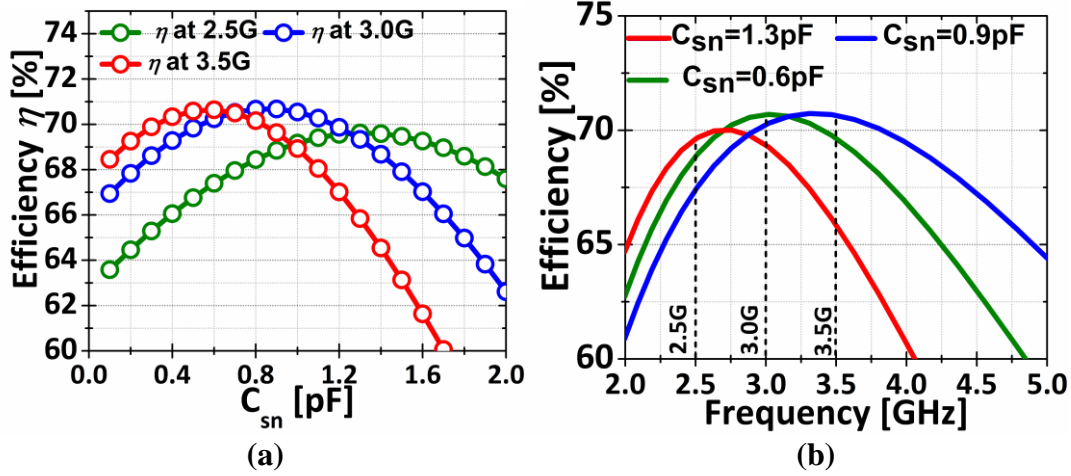
Figure 3.9 **(a) Optimal values of *C_{sn}* (*C_{sn,opt}*) at 2.5/3/3.5 GHz. (b) Efficiency variation with frequency for different values of *C_{sn,opt}*.**

frequencies (Figure 3.9 (b)). Higher efficiencies (~80%) have been reported in literature, but this is only possible with dedicated RF processes where the availability of multiple thick metals and higher resistivity substrates improves both the inductor quality factor as well as the transformer coupling factor [48].

A major benefit of our proposed layout is the presence of two pairs of low-swing nodes (B and C, D and E) in close proximity to each other. From Figure 3.8, it can be observed that if the voltage swing at the single-ended antenna load is V_p, the swings between B-C and D-E will only be ~0.25V_p. Here, we assume that all sections of the secondary network have the same self-inductance. Since we have already determined that directly switching C_{sn} is an unfeasible approach to realize frequency reconfigurability, we propose to exploit the spatial proximity of the low-swing nodes B-C and D-E by introducing two switched tuning capacitors (C_{sn2}, C_{sn3}) between them (Figure 3.10(a)) for triple-band operation. This approach also validates our modified 'figure 8' layout as any extraneous lead inductances that would negatively impact the efficiency from the addition of

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Figure 3.10 (a) Operation of the triple-band transformer combiner and the equivalent circuit representation (b)-(d) of the secondary coil in the three frequency bands. Simulated efficiency curves of the designed transformer combiner assume ideal switches and the following capacitance values: $C_{sn1} = 0.55$ pF, $C_{sn2} = 2.35$ pF and $C_{sn3} = 2.8$ pF.
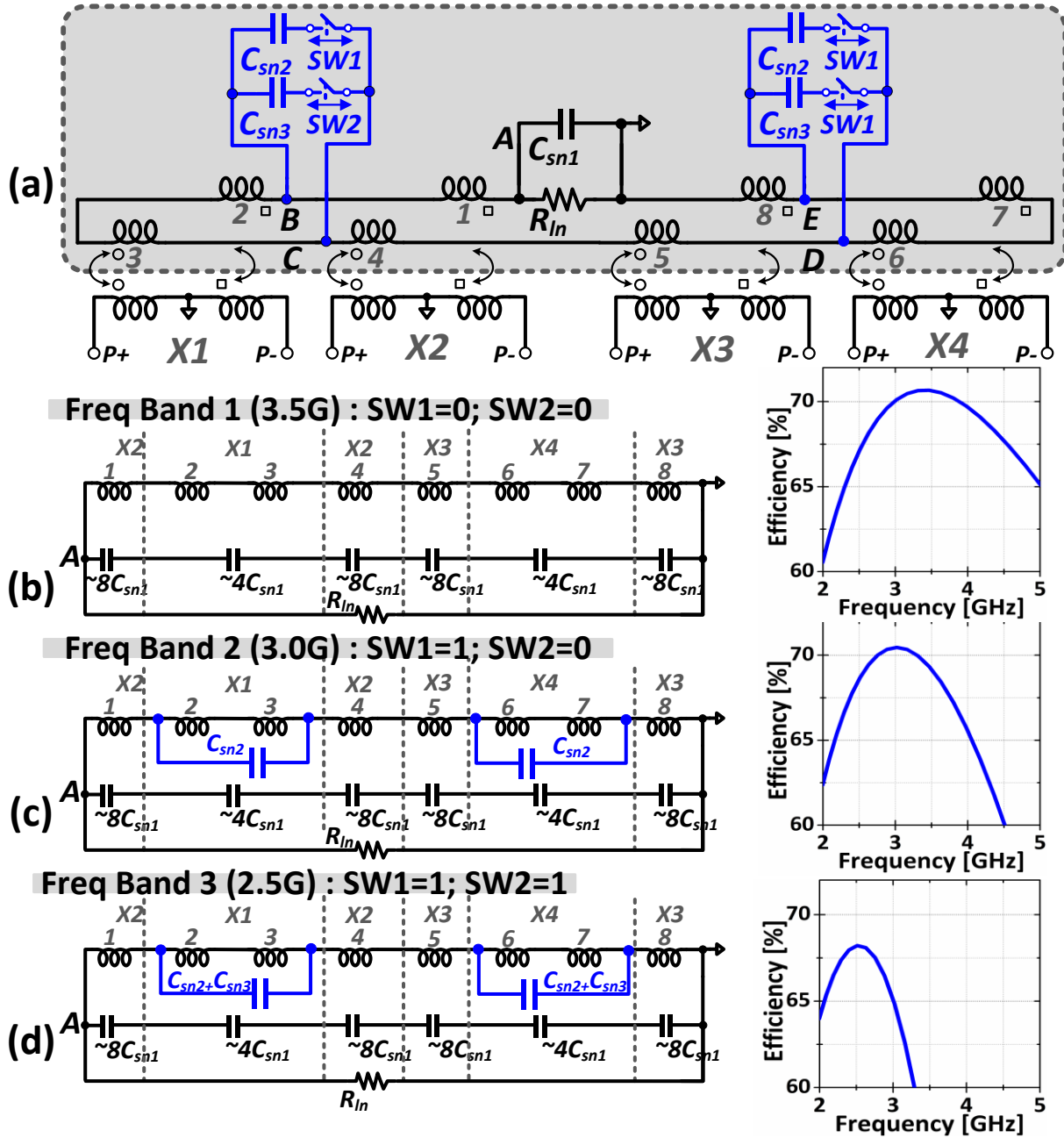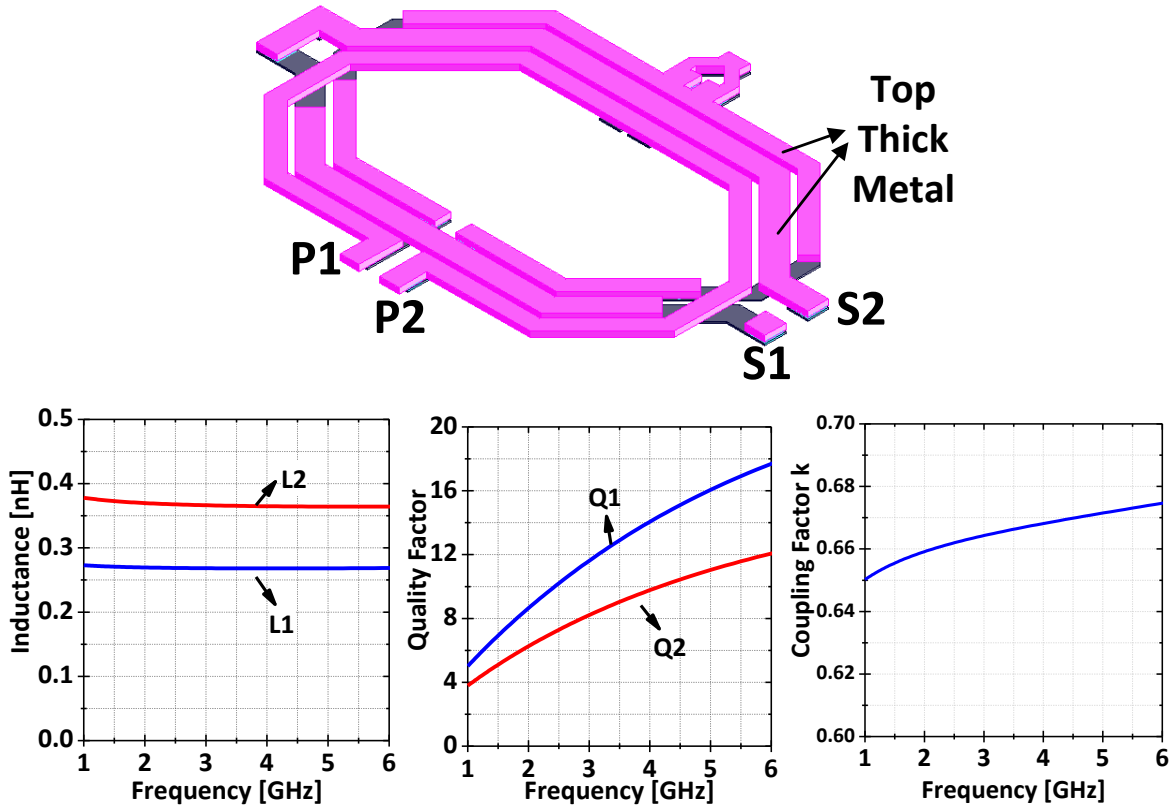
Figure 3.11 Layout of the unit transformer of the combiner, and the EM-simulated inductance, quality factor of the primary and secondary coils and the coupling factor.

these additional capacitances are now minimized. Notice in Figure 3.10(b) that when the switches are off, an effective C_s ($=4C_{sn1}$) appears across each stage (*X1-X4*). Since this mode of operation is similar to the non-reconfigurable case, the value of C_{sn1} is chosen to be 0.55 pF for optimal efficiency at 3.5 GHz. When one of the switches is turned on on (3 GHz mode), an effective secondary capacitance equal to $C_{sn2} + 4C_{sn1}$ appears across the stages *X2* and *X4* (Figure 3.10(c)). Since C_{sn1} is fixed by the 3.5 GHz mode, C_{sn2} can now be optimized to maximize efficiency of these stages (and the overall combiner efficiency) at 3 GHz. Similar arguments apply to the case when both the switches are turned on (2.5 GHz) Moreover, due to the vastly reduced swing across the switched capacitors, the switches can now be implemented with regular CMOS devices. Figure 3.10 also shows that the efficiency of the designed combiner in the three modes of operation is

~70%, which is similar to the non-reconfigurable case of Figure 3.9. Finally, Figure 3.11 shows the EM-simulated performance of the unit transformer of the combiner. At 3 GHz, the quality factor of the primary and secondary coils was simulated to be 12 and 8 respectively, while the coupling factor between the coils was 0.65. It should be noted that these values are limited by the process, and availability of an RF process with thicker metals and possibility of overlaying the primary/secondary coils on top of each other would have resulted in better coupling and coil quality factors.

3.5 Combiner Switched Capacitor

The switched capacitor was implemented using metal-insulator-metal (MIM) capacitors and stacked deep N-well thin-oxide transistors as shown in Figure 3.12. High-value resistors were used to allow independent dc biasing of transistor terminals [58] and to facilitate the use of a feedback capacitor (C_f) bootstrapping the large voltage excursions at the drain onto the gate terminal [59]. This eliminates large relative voltage swings between the transistor terminals and improves reliability (Figure 3.13(a)). Deep N-well transistors are preferred, and two of them were stacked to improve isolation. In this CMOS process, thick-oxide transistors (rated for operation at 2.5V) had a minimum channel length of 280 nm. Therefore, when compared to regular thin-oxide transistors (channel length 60 nm), the thick-oxide transistor required greater than 4 times the width to achieve similar on-state resistance. Due to the resulting large transistor size and parasitic capacitances, capacitor switches with thick-oxide transistors result in poor C_{ON} to C_{OFF} ratio [58]. To improve isolation in the off-state, the source/drain terminals are biased at a value greater than 0V (0.6V in this design) to strongly turn-off the transistor, reduce the bias-dependent drain/source depletion capacitances and also improve linearity. The simulated capacitance and quality factor of the designed switched capacitor with different incident power levels are shown in Figure 3.13(b)

	D1	G1	S1	D2	G2	S2
OFF (CTRL=0)	0.6V	0V	0.6V	0.6V	0V	0.6V
ON (CTRL=1)	0V	1.2V	0V	0V	1.2V	0V
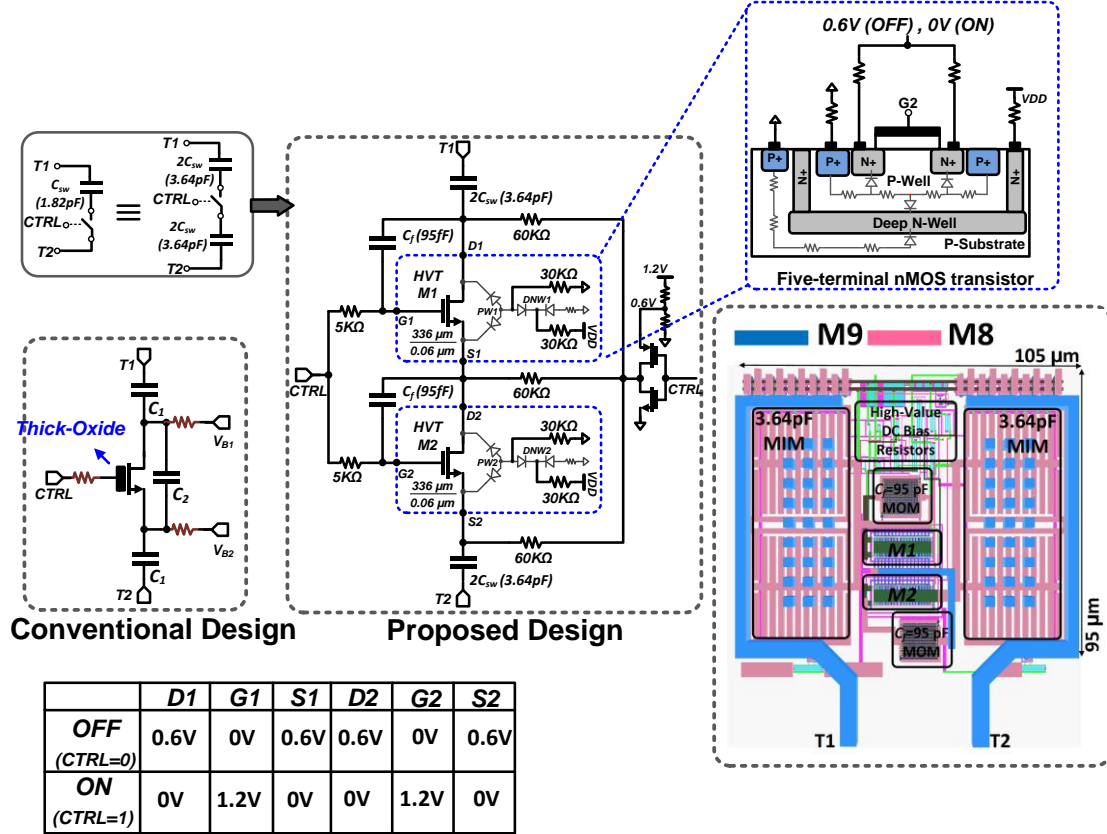
Figure 3.12 Design of the three-terminal (T1, T2, CTRL) CMOS switched capacitor used in the transformer combiner. DC bias values of the transistor terminals in the ON and OFF states is also shown.

and (c) respectively. It achieved an on-to-off capacitance ratio better than 12, with a reasonable on-state Q of 9.5. The simulated value of the allowable voltage swing before channel formation in the off-state switch (marked by rapid increase in capacitance and decrease in Q) was ~3.2V. These simulations were performed using one-port large-signal SP (LSSP) simulations with the harmonic balance (HB) simulator in Cadence SpectreRF [60]. In contrast to small-signal SP simulations, LSSP simulations are sensitive to incident power levels. From the real and imaginary parts of S_{11} values so obtained ($S_{11} = A + jB$), C and Q values were extracted using the following equation:

$$Z_{11} = R + \frac{j}{sC} = \frac{1 + S_{11}}{1 - S_{11}} = \frac{1 - A^2 - B^2}{(1 - A)^2 + B^2} + j\frac{2B}{(1 - A)^2 + B^2}; \quad Q = \frac{1}{\omega RC}. \qquad (3\text{-}10)$$
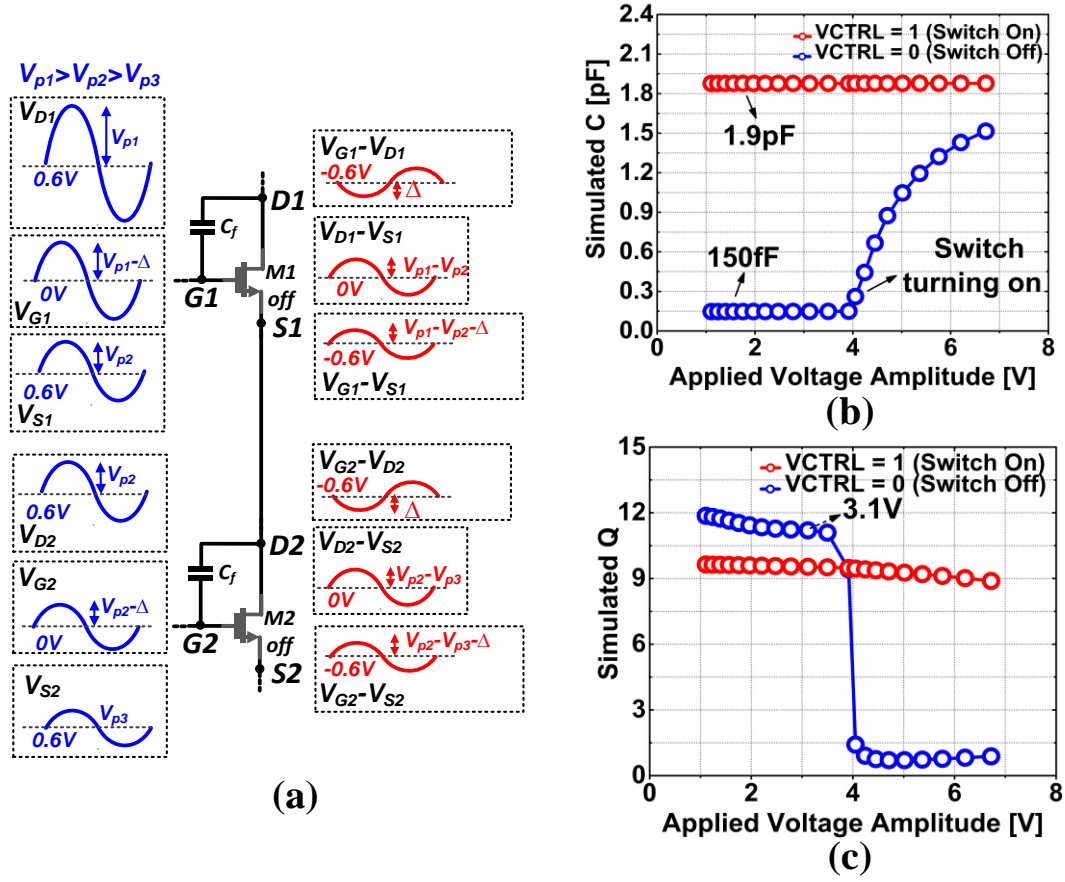
Figure 3.13 (a) Illustration of the terminal-to-terminal RF swings in the capacitor off state. (b) Simulation capacitance and quality factor with different incident power levels.

To understand the impact of the transistor switch size, we can consider a first-order shunt-RC model ($C_p // R_p$) of the switch [23], applicable to both the modes of operation. R_p represents the on- or the off-state resistance while C_p represents the effective capacitance appearing across the drain and source terminals. As illustrated in Figure 3.14(a), a parallel-to-series transformation can be performed to reduce the model to an equivalent series-RC network. Since $Q_p << 1$ in the on state, the switch quality factor is given by $1/(2\pi C_{sw} R_{ON})$, as shown below:

$$R_{ON,S} = \frac{R_{ON}}{\left(1 + Q_p^2\right)}; \quad C_{ON,S} = C_{ON}\left(1 + Q_p^{-2}\right),$$

$$\text{where } (Q_p = \omega_0 C_{ON} R_{ON}) << 1$$

$$\Rightarrow R_{ON,S} \approx R_{ON}; \quad C_{ON,S} \approx C_{ON} Q_p^{-2} \rightarrow \infty \tag{3-11}$$
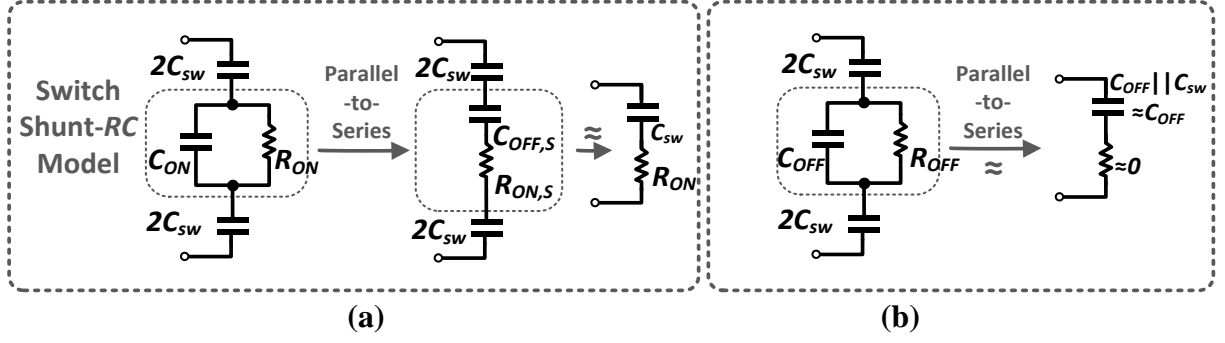
Figure 3.14 Equivalent Circuit of the switched capacitor in the (a) on and (b) off states assuming a shunt-RC model for the transistor switch.

Each 336 µm thin-oxide deep N-well transistor (see Figure 3.12) was simulated to have an R_{ON} of 0.95Ω. Thus, the stack of two HVT transistors would have an R_{ON} of ~2 Ω, resulting in a Q of ~16 at 2.5 GHz. After layout, Q dropped to ~10, as observed in the simulations of Figure 3.13(b). In the off-state, the switch's isolation is determined completely by C_{OFF} as shown below and in Figure 3.14(b):

$$R_{OFF,S} = \frac{R_{OFF}}{\left(1+Q_p^2\right)}; \ C_{OFF,S} = C_{OFF}\left(1+Q_p^{-2}\right),$$

(3-12)

$$\text{where } (Q_p = \omega_0 C_{OFF} R_{OFF}) >> 1 \Rightarrow R_{OFF,S} \approx 0; \ C_{OFF,S} \approx C_{OFF}$$

A stand-alone test structure of the switched capacitor (95 µm × 115 µm) was fabricated in the 65 nm process (Figure 3.15(a)), and its large-signal performance was characterized for incident power levels up to 15 dBm (limited by set-up) using two-port measurements from an Agilent E8364A PNA-X Network Analyzer. A 50 Ω shunt resistor was placed in parallel to switched capacitor on-chip to provide a better impedance match to the 50 Ω port of the network analyzer. Measured capacitance values (extracted using (3-10), and shown in Figure 3.15(c)) showed good agreement with simulation data. At 15 dBm of incident power (1.8V applied voltage amplitude), the proposed structure only shows a minor increase (18%) in its off-state capacitance value.

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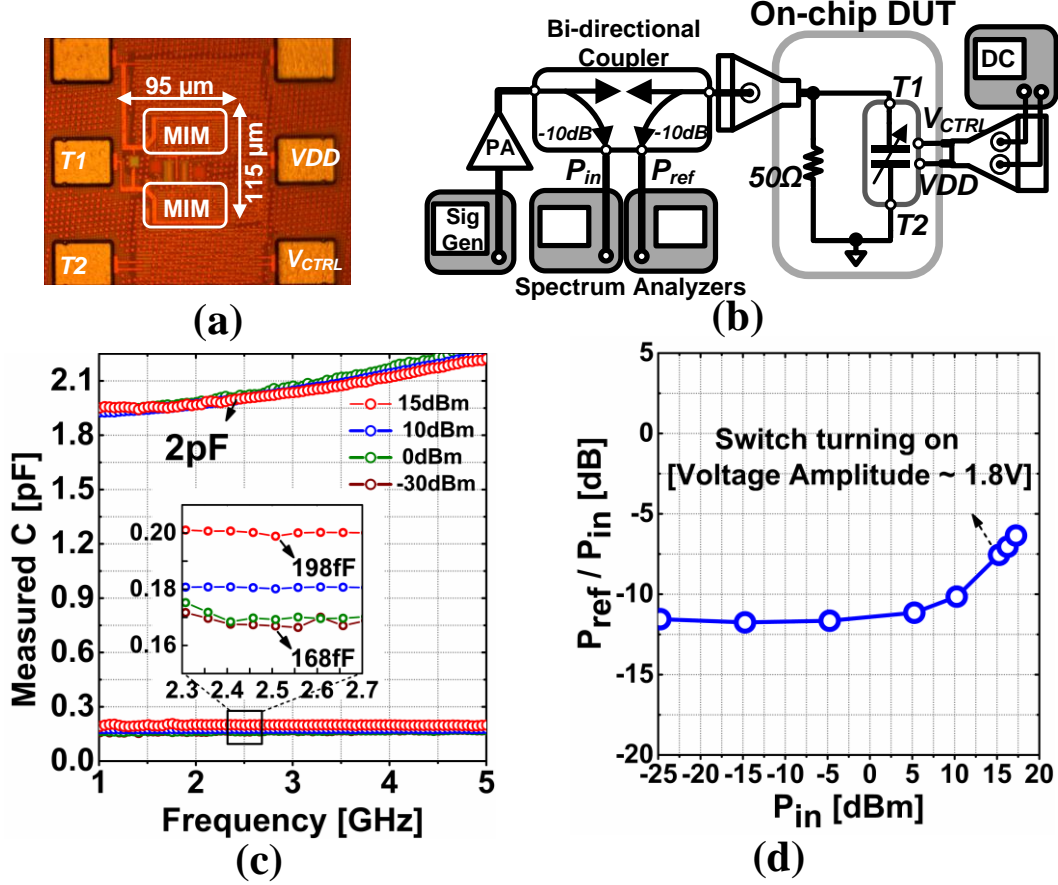
Figure 3.15 (a) Die photo of the standalone combiner switched capacitor. (b) Large-signal measurement set-up. (c) Measured ratio of reflected and incident power for different incident power-levels. (d) Measured off-state and on-state capacitance values for different incident power levels.

Incident (P_{in}) and reflected power (P_{ref}) for the switched capacitor were also measured using the setup in Figure 3.15(b). A change in the impedance of the on-chip DUT due to the turning-on of the switched capacitor at high incident voltage levels is indicated by a change in P_{ref}/P_{in} [58], as shown in Figure 3.15(c). However, a proportional increase in off-state capacitance was only observed at 3.3V of applied voltage in simulations. Discrepancy between measured and simulated value of peak voltage stand-off might be attributed to inaccurate large-signal modeling of the transistors provided by the foundry [61] – for example through an improper capture of diode behavior resulting in earlier turn-on of junction diodes of the nMOS switch resulting in a lower voltage-swing handling capability [62].
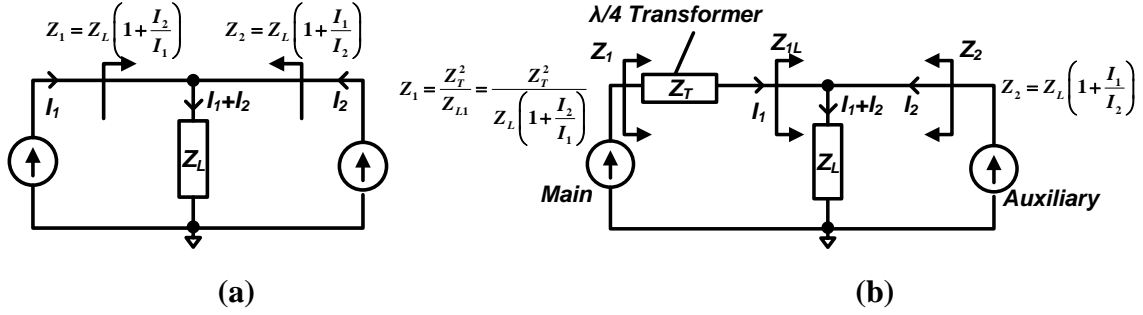
Figure 3.16 (a) Active load-pull using two coherent sources. (b) Operation of a Doherty amplifier.

3.6 Triple-band Power Amplifier

3.6.1 Doherty PA Basics

Conventional power amplifiers are designed to have maximum efficiency at a single power level, which usually corresponds to the maximum output power. Backing-off from this power level also results in a rapid drop in the efficiency. For example, consider the problem of operating a simple Class B amplifier at back-off. It is well known that at peak power, the efficiency of a Class B amplifier is $\pi/4$ or 78.5%. However, as the input drive-level is reduced by a factor of p, it can be shown that while the output power drops by a factor of p^2, the efficiency also drops by a factor of p. Thus, at 3-dB power back-off, the efficiency reduces to 55.5% [64]. Intuitively, this happens because as the input drive level is reduced, the DC power reduces by the same factor (p), but the RF power reduces by a factor of p^2. If the output impedance seen by the PA can be increased dynamically such that the RF power also falls in proportion to p, the peak efficiency of $\pi/4$ will be maintained. This concept of dynamic load modulation is the basis of operation of a Doherty PA (DPA).

In order to understand the operation of a DPA exploiting dynamic load modulation, it is important to understand the active load-pull technique shown in Figure 3.16(a). If we assume that both sources are phase-coherent, it is easily proved that the impedance seen by each of the
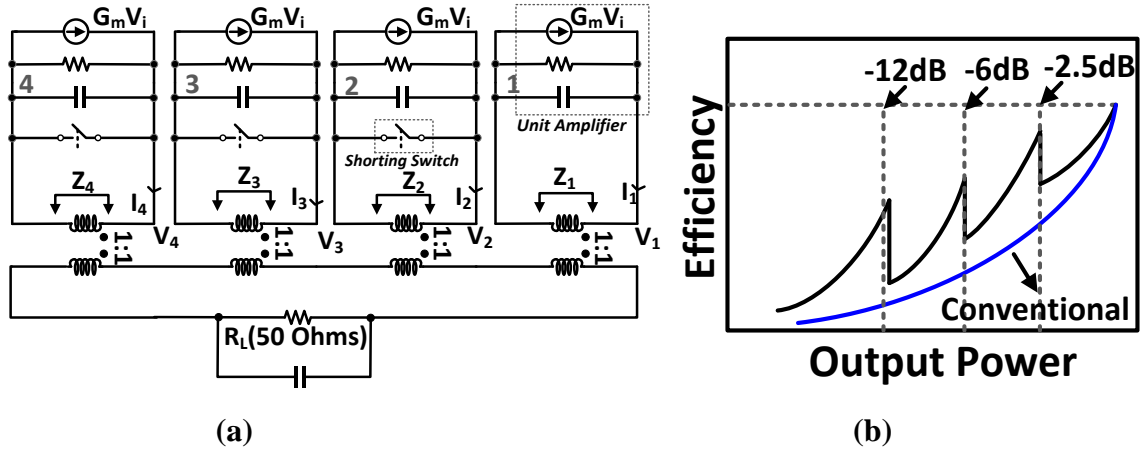
Figure 3.17 (a) Model of a four-way power-combining PA. (b) Efficiency behavior at back-off.

generators can be controlled through the ratio of the two source currents. Thus, when source 2 is off, source 1 sees a load of Z_L. However, when both source 1 and 2 are on such that $I_1=I_2$, both sources now see an impedance of $2Z_L$. A Doherty PA employs dynamic load modulation using a similar configuration of Figure 3.16(a), with the exception that a $\lambda/4$-impedance transformer is additionally introduced between one of the sources and the load impedance (Figure 3.16 (b)). Such a configuration enables two modes of operation, each corresponding to operation in the low-power and high-power modes. In the low-power mode, the auxiliary source in Figure 3.16(b) is turned off ($I_2=0$). Thus, the main source sees an impedance of $4Z_L$ (if the characteristic impedance of the impedance transformer is $2Z_L$). In the high-power mode, the auxiliary source is turned on, and it is easily seen that at peak power (when $I_2=I_1$), the impedance seen by each of the sources is $2Z_L$. Since the impedance seen by the main amplifier increases from $2Z_L$ in the high-power mode to $4Z_L$ in the low-power mode, the main amplifier can maintain peak efficiency between peak power and 6-dB back-off point. Additionally, since half of the active devices (auxiliary amplifier) contributing to the peak power is turned-off in the low-power regime and hence not drawing any DC power, efficiency at lower power levels is also improved compared to using a single amplifier. Since the auxiliary amplifier is required only in the high-power regime, a Doherty PA is generally

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realized by combining a relatively linear (Class AB/B) main amplifier with a relatively non-linear (Class C) auxiliary amplifier. The gain-compressive behavior of Class AB/B amplifier combines with the gain-expansive behavior of the non-linear Class C amplifier to extend the linear range of operation of the PA [65], [66].

3.6.2 Load Modulation in Power Combining PA

We have already seen the benefits of using a power combining PA to realize high output power levels in modern CMOS processes with low-breakdown voltages. Interestingly, a power-combining PA also exhibits the useful property of dynamic load modulation explained in the previous section, enabling higher efficiencies at back-off. To understand this, consider a simple 4-way combiner depicted in Figure 3.17(a). It is easily seen that at peak power-level when all unit amplifiers are on, the impedance seen by each unit amplifier is $R_L/4$ (assuming all unit amplifiers are identical). Thus, if we neglect the output impedance of the amplifier, the output voltage from each amplifier is $G_m V_i (R_L/4)$, where V_i is the input drive voltage. Now, to operate at a lower-power level, we begin to turn-off the unit amplifiers one-by-one. When a single unit amplifier is turned off, then the output impedance seen by each of the still-on unit amplifiers would increase to $R_L/3$. Thus, if now the input drive level is reduced to $3V_i/4$, the output voltage from each amplifier is still $G_m V_i (R_L/4)$, similar to the peak power case. Therefore, in principle, the efficiency of each still-on amplifier is maintained. Similarly, when two unit amplifiers are turned off and input drive level is reduced to half, the output power is reduced to half (6-dB back-off) while the efficiency of each turned-on unit amplifier is identical to the peak-power case [48]. However, due to higher transformer losses and finite resistance of the shorting switches at back-off, the efficiency behavior degrades from the ideal case [67]. Nevertheless, on account of load modulation due to the transformer action, a power-combining PA exhibits superior back-off characteristics compared to a conventional PA, as illustrated in Figure 3.17(b).

Freq Mode	SW1	SW2	Power Mode	SW3	Main Amp,Driver	Aux Amp,Driver
2.5G	On	On	HP	Off	On	On
3.0G	On	Off	LP	On	On	Off
3.5G	Off	Off				
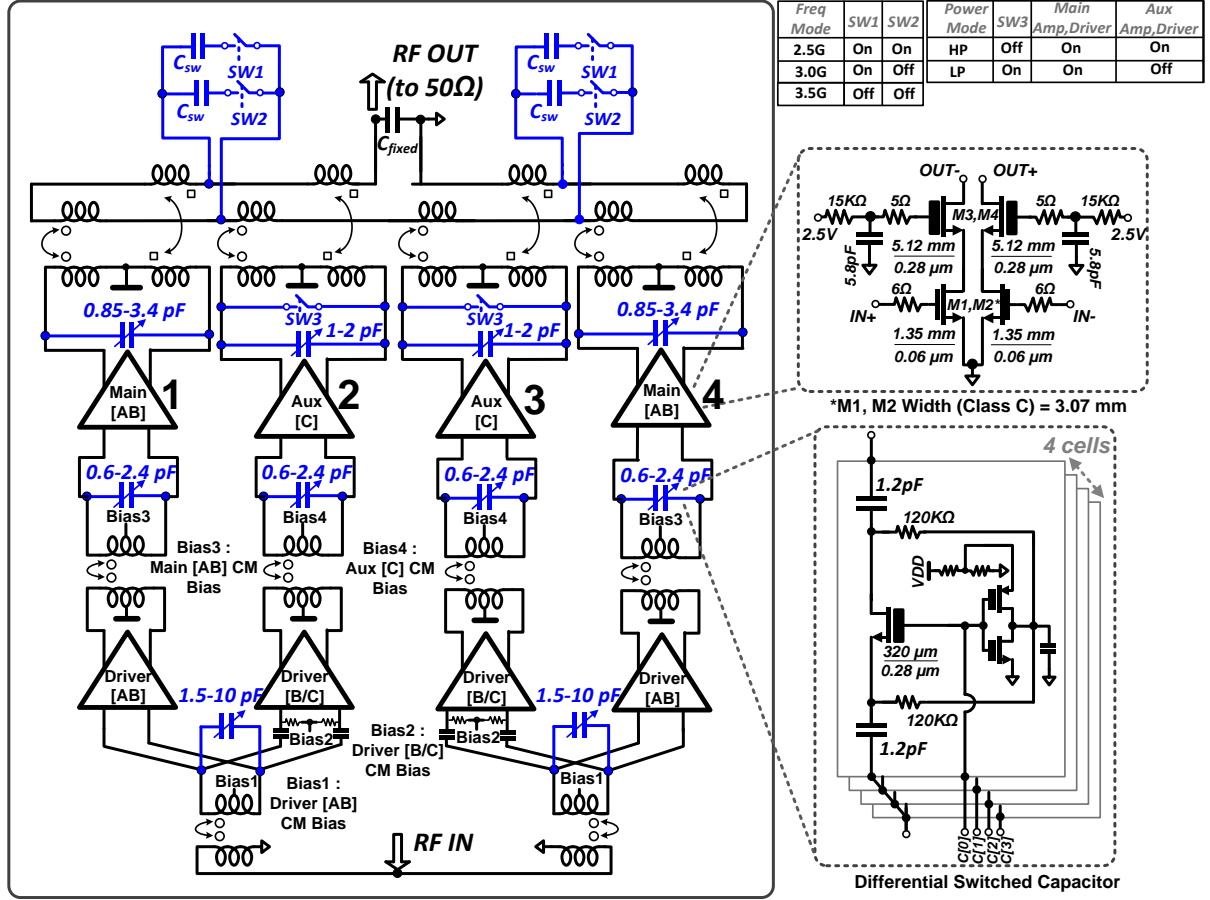
Figure 3.18 Schematic of the implemented triple-band PA with a digitally-tuned, 4-way transformer combiner in the output stage.

3.6.3 4-way Power Combining PA

A triple-band (2.5/3/3.5 GHz) power-combining PA incorporating the four-way power combiner and the combiner switched capacitor was designed. Shown in Figure 3.18, the combiner uses switches *SW1* and *SW2* to move between the different frequency modes. Amplifiers 1 and 4 are biased in Class AB, while the larger amplifiers 2 and 3 are biased in Class C to enable transformer-based Doherty operation [63], [68]. In the low-power (LP) mode, amplifiers 2 and 3 are turned off and their primary coils shorted by switches *SW3*. Thus, only amplifiers 1 and 2 contribute to output power in the LP mode. In the high-power (HP) mode, switches *SW2* are opened, and auxiliary amplifiers 2 and 3 are turned on.
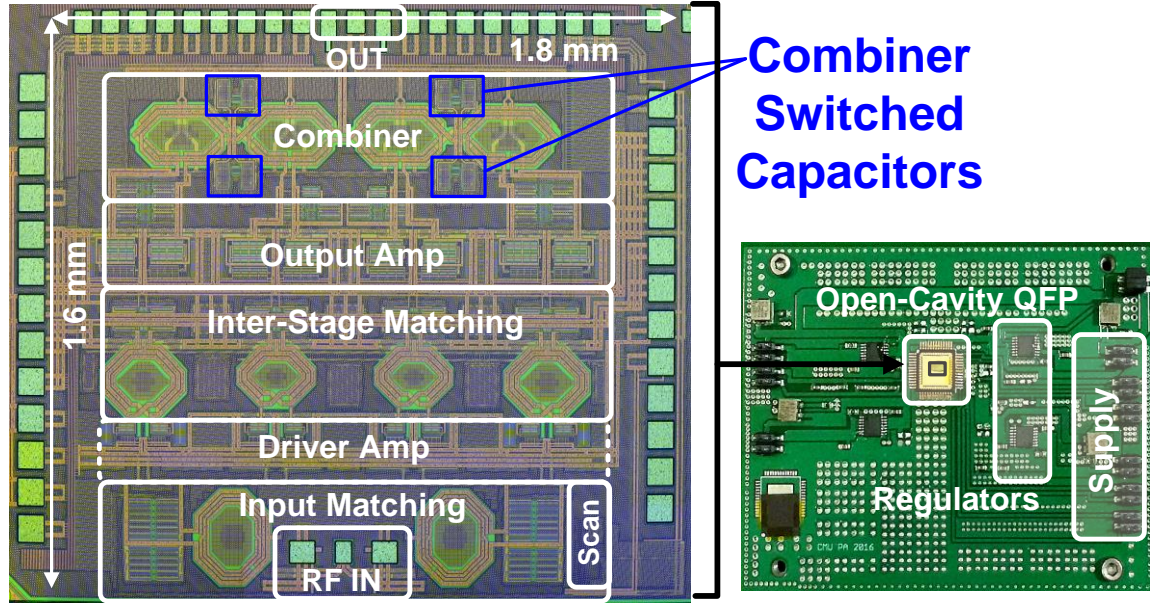
Figure 3.19 PA die photo and PCB test board.

In addition to the output stage, an input matching and driver stages were also designed. Differential digitally-switched capacitors with thick-oxide CMOS switches were used in the inter-stage matching network and the primary-side tuning capacitance of the output transformer. Each unit XFMR of the power combiner had a coupling ratio of ~0.65. Each Class AB output stage comprised a differential cascode stage where the CS stage transistors were sized to be 1.35mm/0.06µm (thin-oxide) and the cascode stage transistors were sized to be 5.12mm/0.28µm (thick-oxide). Each Class C output stage comprised a differential cascode stage where the CS stage employed 3.07mm/0.06µm thin-oxide transistors and the cascode stage (CG stage) employed 5.12mm/0.28µm thick-oxide transistors. A sufficiently large shunt capacitance (5.8pF) was added to the gate of the cascode transistor to form a capacitive feedback network with the drain-gate capacitance. Hence, a part of the drain voltage swing appeared at drain gate thereby improving reliability while allowing an independent DC bias of the cascode transistor from the drain voltage [69]. Series resistors of ~5Ω were used before the gates of both the CS and CG stages to improve
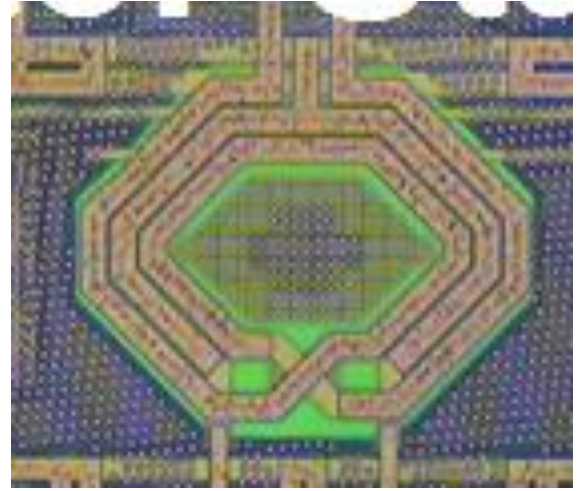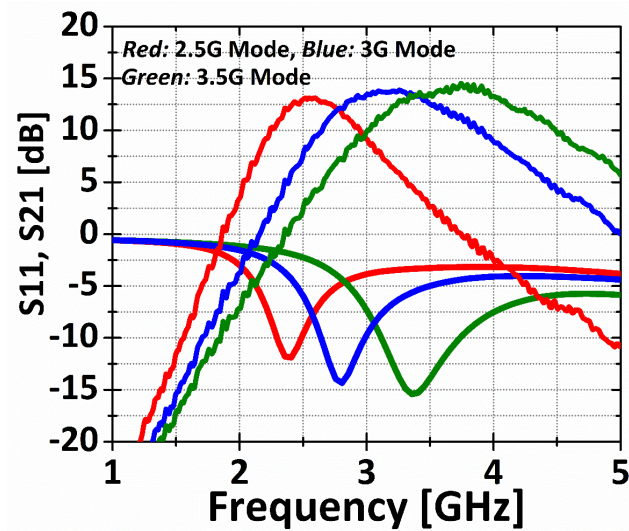
Figure 3.20 (a) Measured PA small-signal performance. (b) Close proximity of thick transformer coil traces (< 4 μm) to high-density fill structures in top and lower level metal layers. All transformer coil traces were 12 μm wide.

stability [70]. Class AB bias was fixed close to 0.45V, while the class C bias was fixed at 0.22V.

The PA was operated of a 1.2 V supply, and designed to deliver a peak power of 26.5 dBm.

3.6.4 CW Measurement Results

Figs. 3.19 and 3.20(a) show the chip photograph and the measured small-signal PA performance respectively. The PA chip occupied an area of 2.88 mm^2. The chip was packaged in a 52-pin open-cavity QFP package. The supply, ground, and digital pins were wire-bonded to the QFP package, while the input and output RF pads were wafer-probed. During large-signal measurements, a 2-to-8 GHz co-axial driver amplifier (ZVE-8G+ from Mini-Circuits) [71] was placed before the PA and after the signal generator to deliver adequate power to the input of the PA. The PA showed a peak gain of ~15dB in the three modes while the simulated value was ~20-21dB. Since the DC current draw of the PA under different biasing conditions closely mirrored simulations, thereby ruling out excessive resistive loss in the power/ground network, a probable cause for the discrepancy in the small-signal gain is the impact of the metal fill on the inter-stage and the output
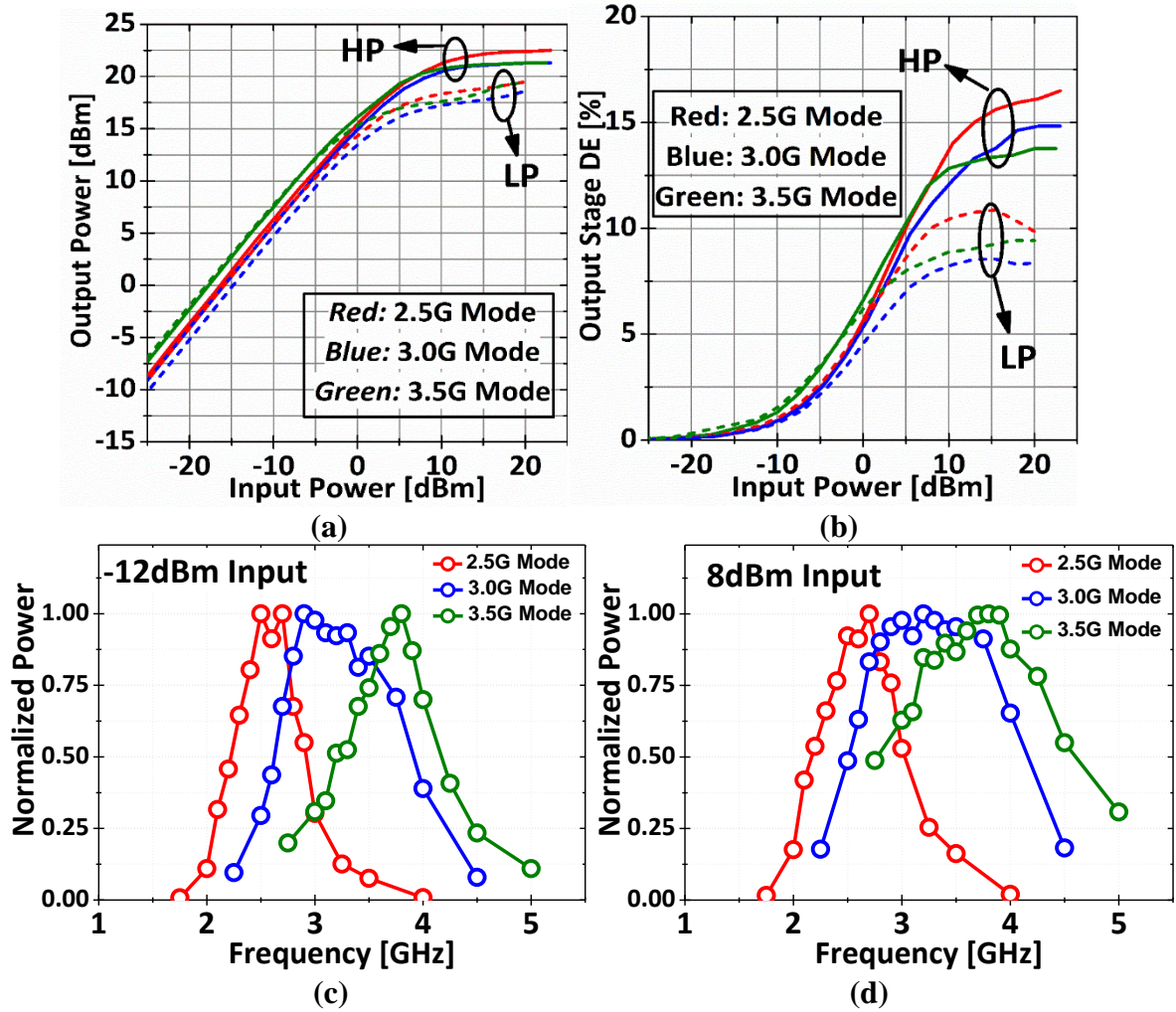
Figure 3.21 Measured PA (a) output power and (b) output stage drain efficiency in the three frequency modes with 2.6/3/3.65 CW signals respectively. Measured frequency selectivity of the PA at low (-12 dBm input) and high (8 dBm) input power levels in the three frequency modes.

transformers. Due to stringent fill requirements of this process, high-density fill structures had to be placed very close (<4 µm) to the thick primary and secondary coil metal traces (Figure 3.20(b)). The small-signal performance was then simulated with different transformer coupling factors where a strong dependence of the PA gain on the coupling factor was observed. This will be further investigated in the next section. It is probable that due to the excessive transformer loss in the driver stage, amplifiers 2 and 3 could not be fully pushed towards Class C operation and failed to contribute adequate power to the lossy power combiner. The following observation was supported
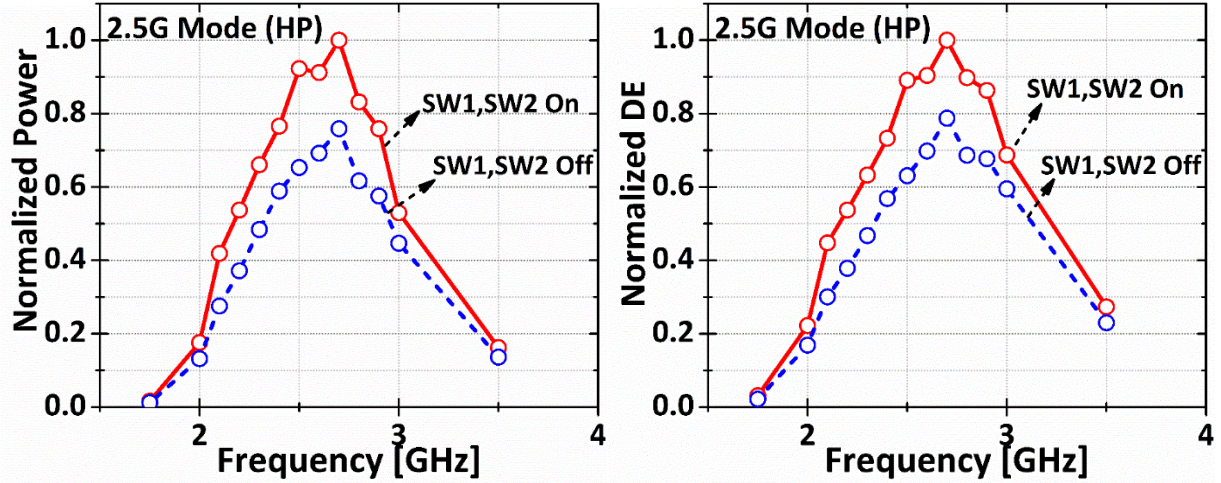
Figure 3.22 PA behavior in the 2.5 GHz mode with the combiner switches turned on and off respectively.

by the fact that while the rate of increase in the DC current draw of the AB amplifiers with increasing input power level matched simulations, the current draw of the non-linear Class C amplifiers did not show the characteristic rapid increase in DC current draw with rising input power expected from Class C behavior.

As shown in Figure 3.21, the measured peak output power was only 22.5 dBm (16.5% drain efficiency DE with a 1.2V supply) in the 2.5 GHz mode, and 21.5 dBm (15% DE) in the 3 GHz/3.5 GHz modes. To demonstrate the frequency reconfigurability of the PA, the output power was measured at low and high input powers at different frequencies (Figure 3.21(c), (d)). Excellent selectivity was observed for low input power, while a degradation in frequency selectivity was observed in the 3/3.5 GHz high-power modes attributable to the finite power handling capability of the various off-state switched capacitors. To isolate the influence of the frequency-tuned input and driver gain stages, the output power was measured in the 2.5 GHz HP mode with only the power combiner intentionally mistuned to operate in the 3.5 GHz mode (*SW1*, *SW2* off). As shown in Figure 3.22, frequency selectivity is maintained due to the driver stage gain shaping. However,
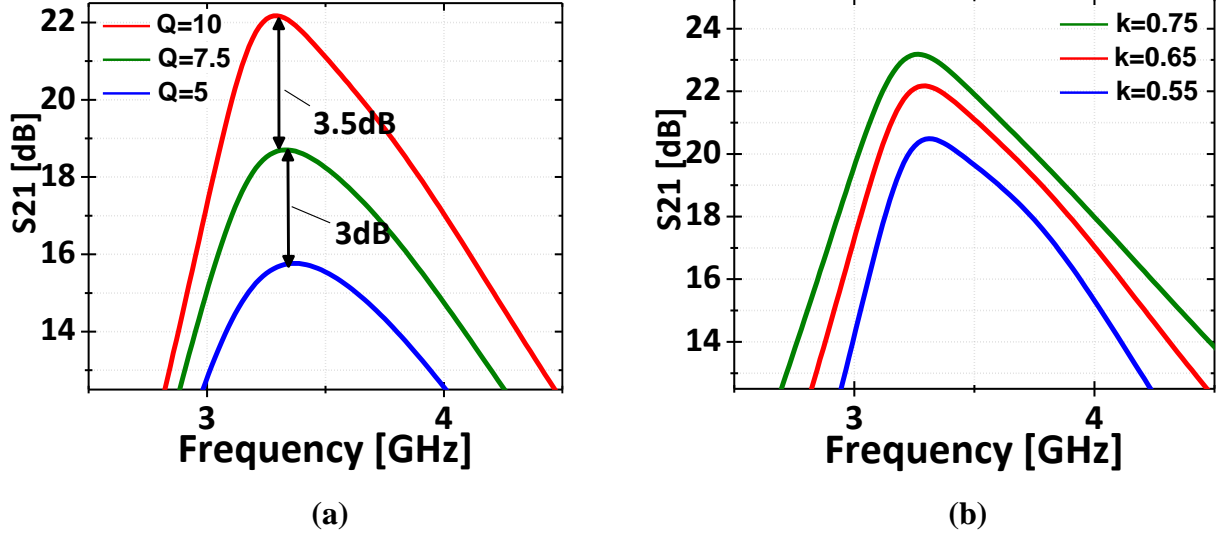
Figure 3.23 Simulated small-signal PA gain in the 3.5 GHz mode with different (a) inductor *Q*s and (b) transformer coupling factors (These simulations included C-extracted transistor caliber and power/ground routing parasitics).

the peak output power and drain efficiency with combiner switches off reduces to 0.8X of the

values with the combiner switches on, thereby illustrating the impact of combiner tuning.

3.6.5 Post-Measurement Analysis

Measurement results discussed in the previous section reveal that while the frequency

reconfigurability of the PA behaved as designed, there was a significant reduction in both the PA's

small signal and large signal RF performance. In this section, we investigate the various reasons

that could have been responsible for the low PA efficiency, and the reduction of the small-signal

gain and output power between measured and simulated PA performance.

3.6.5.1 *Effect of Transformer kQ*

Equation (3-9) relates the transformer's insertion loss to its '*kQ*' product. The implemented PA

uses transformers in the final combiner, as well as in the input and inter-stage matching networks.

In the previous section, it was mentioned that high-density fill had to be placed very close to the

transformer metal traces to satisfy metal density requirements. While some studies have
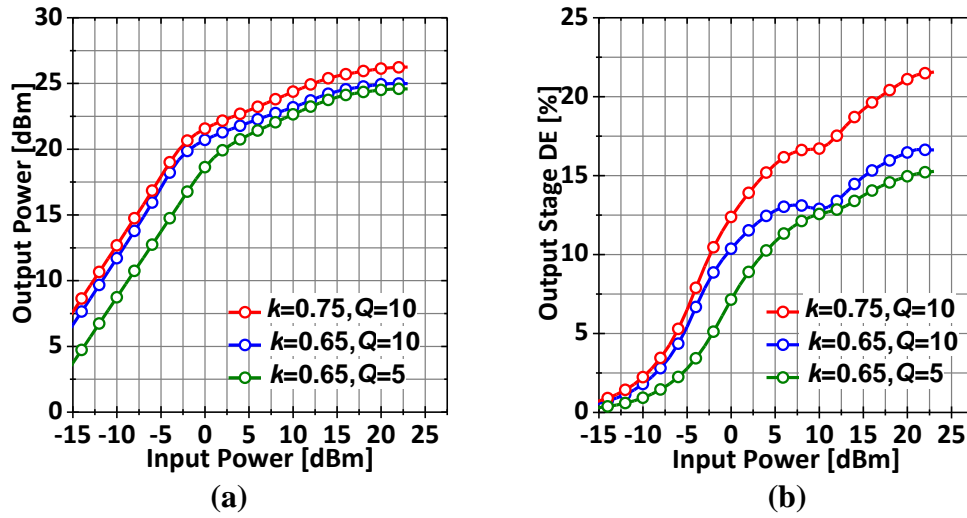
Figure 3.24 Simulated PA power and output stage drain efficiency in the 3.5 GHz mode with different (a) inductor *Q*s and (b) transformer coupling factors (These simulations included C-extracted transistor netlists and power/ground routing parasitics).

investigated the impact of fill on inductor/transformer performance [72]-[75], a clear consensus is not available, and some designers prefer to include fill structures in their EM simulations (which makes simulations memory intensive and time consuming) or resort to experimental characterization to account for their effects. Eddy currents in the fill structures at high frequencies affect inductor performance by lowering inductance, quality factor, self-resonance frequency (for example, see Appendix A) and even by disrupting the coupling in the transformer. Figure 3.23 shows the simulated small-signal performance of the PA with different transformer inductor *Q*s and coupling factors. In these simulations, all transformers in the design were replaced with simple lumped-element models so that their *k* and *Q* values could be readily changed. A strong dependence of the overall gain on *k* and *Q* was observed. For example, lowering the Q of the inductors from 10 to 7.5 reduced the small-signal gain by nearly 3.5 dB. It is likely that a combination of these two factors were responsible for the higher observed loss. Figure 3.24 shows
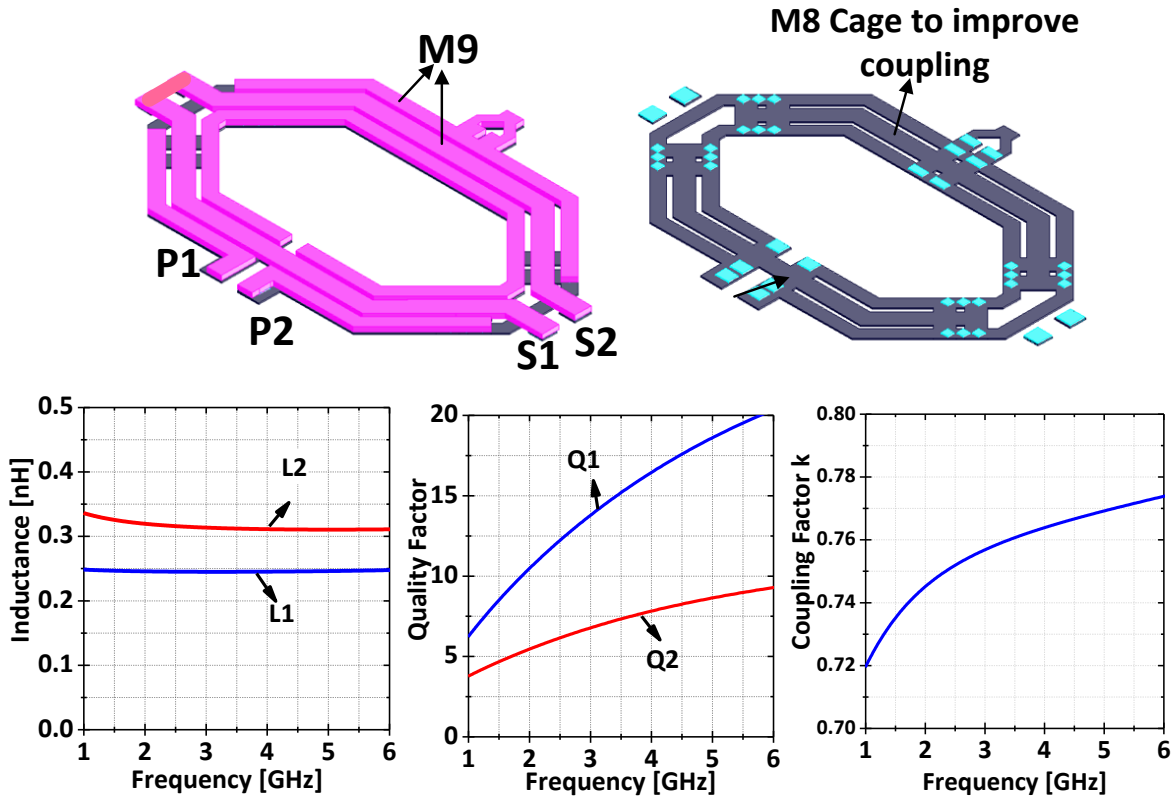
Figure 3.25 Layout of the unit transformer of the combiner, and the EM-simulated inductance, quality factor of the primary and secondary coils and the coupling factor.

the simulated output power and output stage's drain efficiency (DE) for different values of transformer k and Q. Increase in k from 0.65 to 0.75 improved the peak DE by over 5% and the peak output power by 0.5 dB. Since high coupling factors are critical, a better design would involve a more carefully-designed unit transformer in the combiner, for example as shown in Figure 3.25. The modified transformer layout in Figure 3.25 employs M8 metal straps in the primary coil (M9 is the top metal) to improve coupling. Thus, compared to the previous transformer design of Figure 3.11, the coupling factor improves to 0.75 from 0.65. However, due to increase in parasitic capacitance to the substrate, the self-resonance frequency drops. Additionally, an optimized approach to fill should have been adopted [75] to satisfy fill requirements while minimizing the effect on inductor Qs.
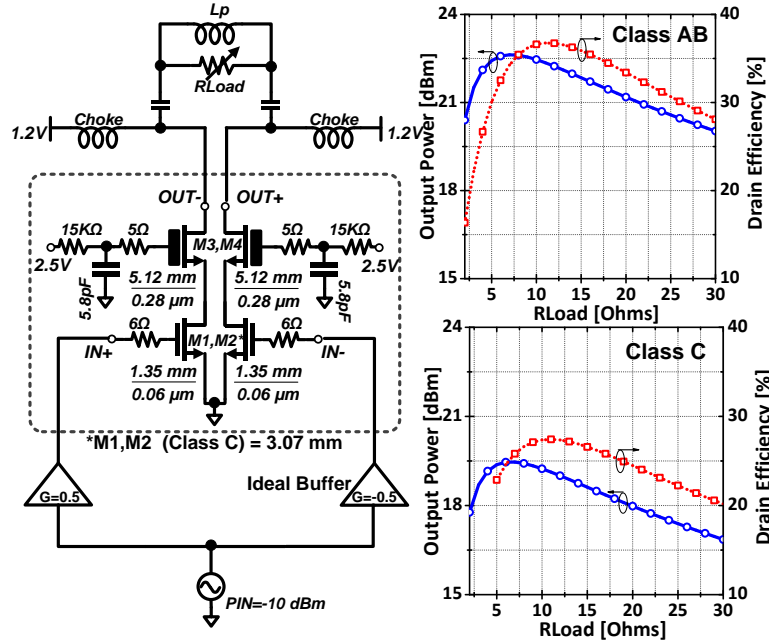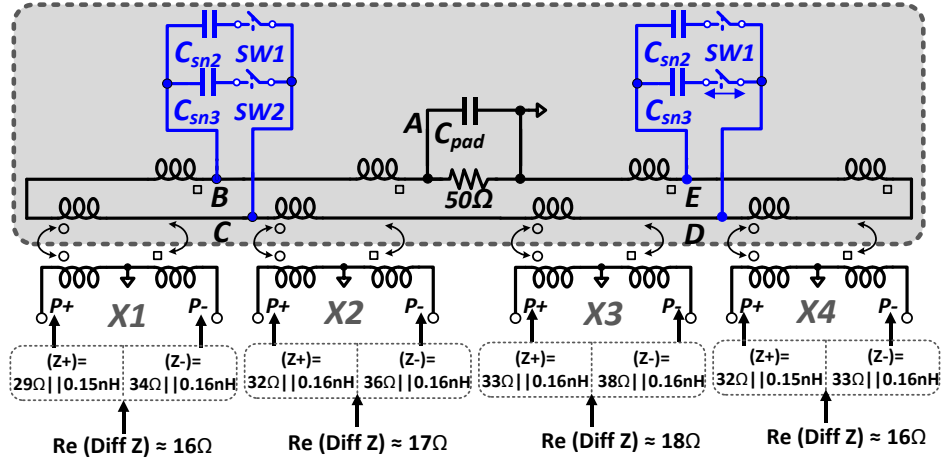
Figure 3.26 (a) Load-pull simulation setup of unit amplifiers. (b) Simulated impedances at the input of the designed transformer combiner.

3.6.5.2 *Amplifier Optimum Impedance*

Figure 3.26(a) shows the load-pull simulation setup of the unit amplifiers to determine the optimal load impedance (Z_{opt}) at which the amplifiers deliver maximum power and efficiency. The simulations were performed at 3.5 GHz and an inductance (L_p) was added in parallel to R_{Load} to resonate with the device's output capacitance [76]. Due to the finite knee voltage, the load delivering the maximum output usually does not coincide with the load delivering maximum
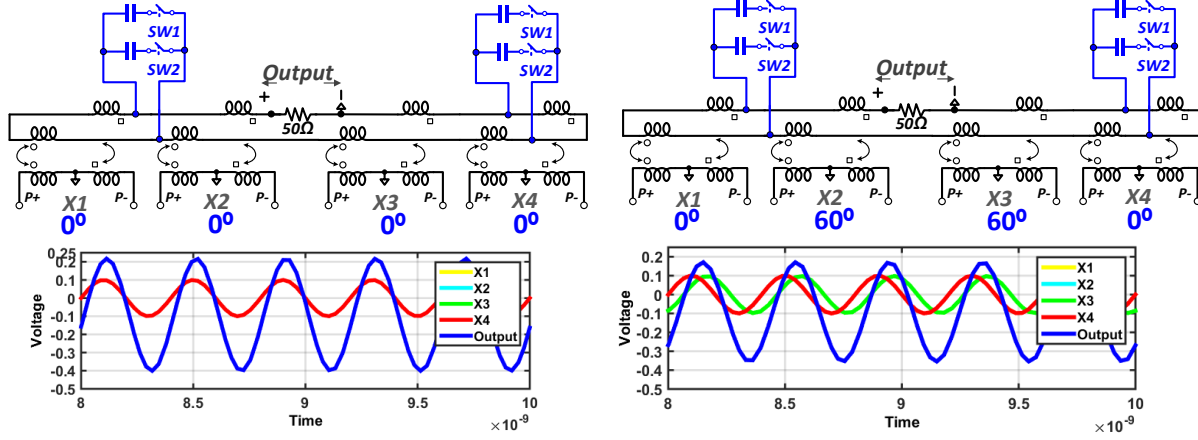
Figure 3.27 Transient simulation demonstrating the effect of phase imbalance between the class AB and class C amplifiers on voltage combining in the designed transformer combiner. The combiner is in the 3.5 GHz mode (all combiner switches are turned off).

efficiency. The load corresponding to maximum efficiency is a higher value and often pushes the load line into the knee region for a part of the cycle, and is therefore not recommended [77]. In Figure 3.26(a), it is seen that an R_{opt} of ~10Ω represented an ideal compromise between output power and efficiency for both the class AB and class C amplifiers. In Figure 3.26(b), the impedance presented by each input port of the transformer combiner is shown. While some impedance imbalance exists between the positive and negative terminals of each primary-side coil, the resulting amplitude and phase imbalance is likely to be significant enough only a mm-wave frequencies to affect the power combining efficiency [78]-[79]. It is also observed in Figure 3.26(b) that each unit amplifier would see a differential load impedance of ~16Ω due to the impedance transformation of the 50Ω load due to the 4-way combiner, while the desired R_{opt} was ~10Ω. Two conclusions can therefore be drawn from these simulations. First, either the design of the amplifier or of the combiner could have been modified to reduce the mismatch between the load presented by the combiner and each unit amplifier's R_{opt}. Second, although the increase in R_{opt} reduces the power delivered by each unit amplifier, and perhaps resulted in an undesirable early onset of

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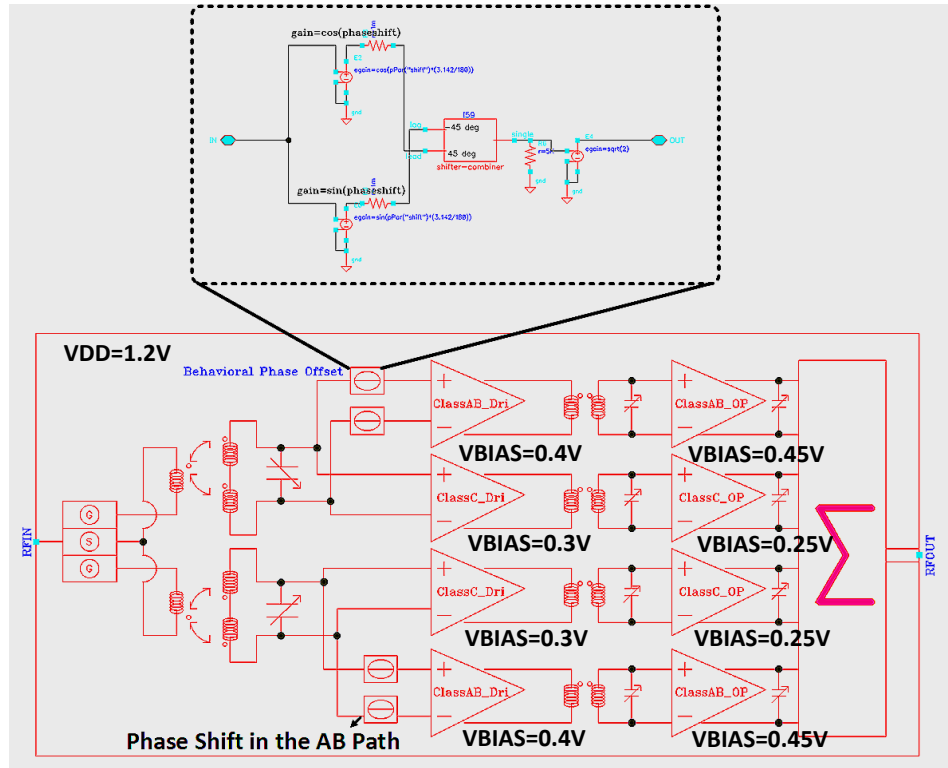
Figure 3.28 Top-level PA simulation setup with behavioral phase offsets added in the main Class AB amplifier path. The phase offsets are inserted before the Class AB driver stage.

compression, this alone cannot explain the reduction in power and efficiency observed in the design and in measurements.

3.6.5.3 *Phase Misalignment between Unit Amplifiers*

In a Doherty configuration like the one adopted in this design, power from a class AB/B carrier amplifier is combined with power from a class C amplifier. However, the class AB and class C biases and the difference in the amplifier sizes creates very different amplitude-dependent phase distortion (AM/PM) characteristics in the carrier and peaking paths. This phase imbalance between the output signal of the class AB and larger class C biased amplifier in a Doherty network creates several issues like output power loss, improper load modulation thereby bringing down efficiency [80]. As an example, Figure 3.27 shows a standalone transient simulation of the designed combiner with a phase mismatch of 60° between the input ports corresponding to the Class AB and Class C
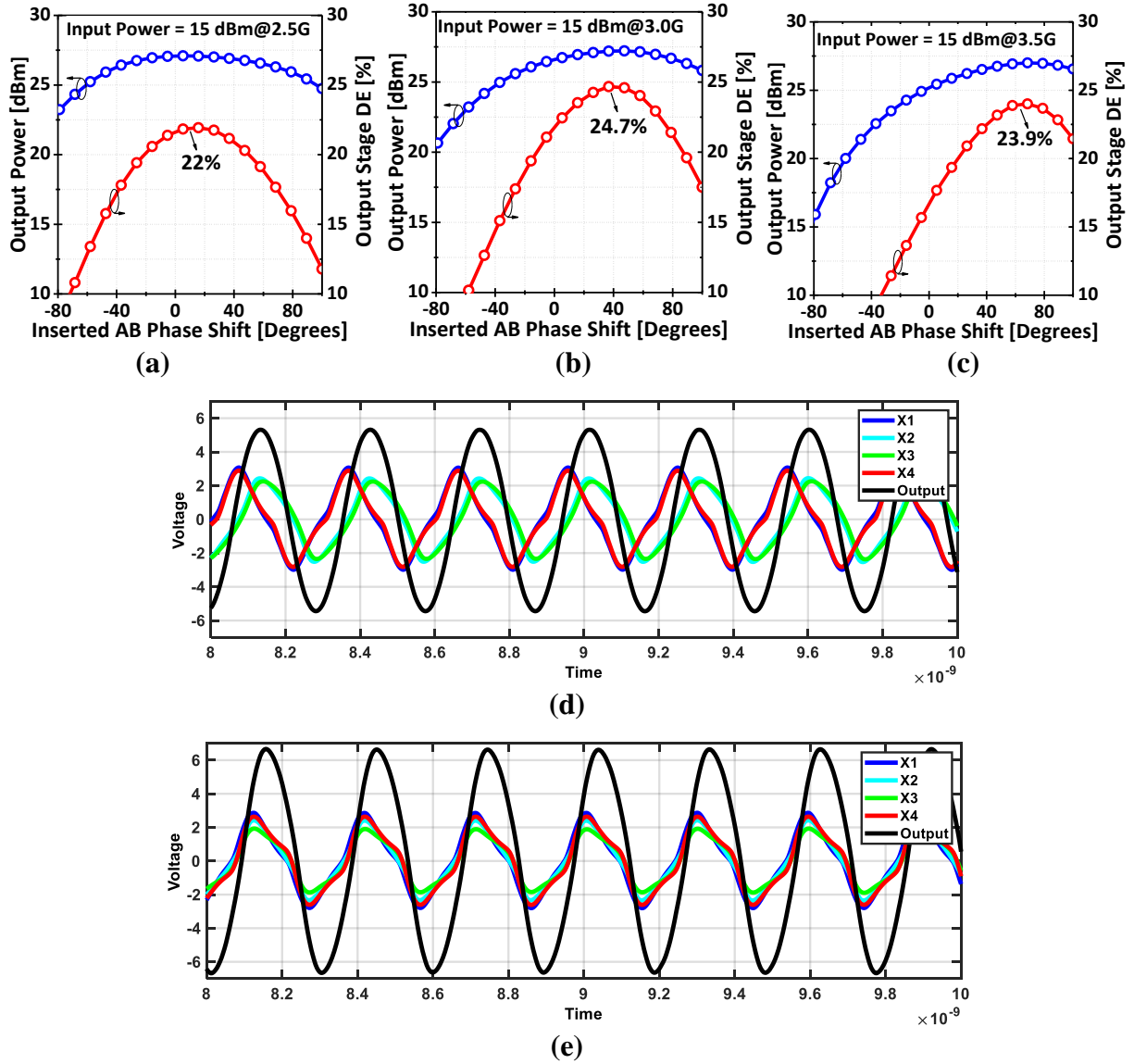
Figure 3.29 Top-level PA simulation: Output power and output stage DE in the (a) 2.5 GHz, (b) 3 GHz, and (c) 3.5 GHz modes with different amounts of phase offsets in the main amplifier path. Transient simulations showing the voltages developed at the output of the Class AB amplifiers (X1, X4) and Class C amplifiers (X2, X3) (a)without any phase offset, and (e) with 60° phase offset in the main amplifier path in the 3.5 GHz mode. All simulations are based on the setup shown in Figure 3.28.

amplifiers. A clear reduction in the output voltage amplitude due to the non-ideal summation of

the unit amplifier voltages is observed. Therefore, phase-compensation techniques are necessary

to ensure voltages are combined in accurate phase [65], [80]- [81], for example, through the use

of transmission-line based offset lines. However, this critical point was overlooked during the

design-phase of the PA, and a finite phase imbalance existed between the output voltage amplitudes of the class AB and class C amplifiers due to the different biasing, differing sizes of the class AB/C unit amplifiers and drivers and the different inter-stage matching networks As is common in Doherty implementations, an improved design would have to incorporate a single or multiple offset lines to correct the phase imbalance between the AB-C amplifiers. The most common technique is to insert a phase offset line at the input of either the main or the peaking amplifier to correct for the phase imbalance at average power level [136], [137].

To study the impact of this phase imbalance in the present design, a simulation setup as shown in Figure 3.28 was constructed. Behavioral phase offsets were inserted before the main (Class AB) driver stages, and the offset value was swept to determine the required phase correction in the three frequency modes. Figure 3.29 (a), (b) and (c) shows the simulation results at an input power level of 15 dBm which resulted in an output power close to saturated power. It was observed that in the 3.5 GHz mode, a phase offset of 60° was necessary to achieve the maximum achievable output stage efficiency of ~24% (the output power increased by ~1.8dB). Without any offset, the present design only achieved a peak efficiency of ~16.4%. In the 3 GHz mode, a phase offset of 40° was necessary for the peak efficiency of 24.7%. The 2.5 GHz mode was close to peak efficiency even without any phase offset. Figure 3.29 (d) and (e) shows the transient simulation results in the 3.5 GHz mode with and without 60° phase offset in the main amplifier path. It is evident that as the output voltages of the unit amplifiers are aligned in phase after adding the phase offsets, the output voltage swing has improved compared to the case when there was no phase mismatch correction. These results demonstrate that while phase compensation is necessary, the offset lines should also have to be made tunable, for example, through tunable passive lumped-element π-networks. Furthermore, it is also conceivable to implement a digital loop that detects the power levels of the
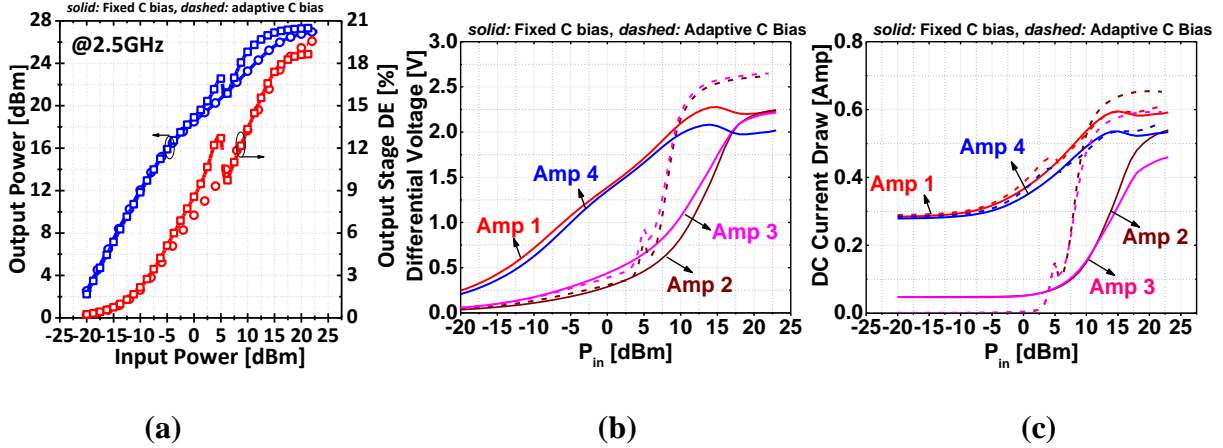
Figure 3.30 Simulated (a) output power, output stage drain efficiency, (b) differential voltage amplitude of the unit amplifiers, and (c) DC current draw with and without adaptive C bias in the 2.5 GHz mode. Amp 1 and 2 are the class AB unit amplifiers, while Amp 3 and 4 are the class C amplifiers. The adaptive bias circuit adopted in these simulations was like the one implemented in [67].

auxiliary and peaking amplifiers (examples of integrated implementations of RF power detectors and peak detectors), which then automatically adjusts the digital settings of a tunable phase offset line to maximize output power.

In conclusion, the implemented design showed a peak efficiency of 20% or below even in simulations: the phase imbalance between the AB and C amplifiers was one of the contributing factors. Simulations with behavioral offsets revealed that the efficiency could be improved by over 7.5% in the 3.5 GHz mode. An improved design would have to incorporate tunable offset lines to ensure the design approached best-case efficiency in the three frequency modes. Further efficiency drops observed in measurements was likely due to the reduction in the transformer's kQ product due to fill, as explained in Section 3.6.5.1.

3.6.5.4 *Adaptive Class C Biasing*

In a Doherty configuration, the class-C biased peaking amplifier turns on only when the output voltage from the carrier amplifier saturates (near the power-back-off or the PBO point). As such, the class-C unit amplifier must be sized 2-3 times the carrier amplifier to ensure that it remains

turned-off before PBO, but should provide a rapidly increasing current after PBO when it turns on [64]. However, even after upsizing, the behavior still deviates from Doherty-like operation due to insufficient power delivered by the class C amplifier. Recently, adaptive biasing of the class C amplifier has been proposed to overcome this problem [67], [82]. An on-chip adaptive bias circuit can be implemented by using a pMOS rectifier pair to extract the envelope of the input signal, followed by a low-pass filter to adaptively change the DC bias of the class C amplifiers [67]. Thus, the auxiliary amplifier remains biased below the threshold voltage at low input signal levels and the bias voltage increases rapidly with increasing power after PBO. Although an adaptive bias circuit was not implemented in the final design, Figure 3.30 compares the large-signal performance of the designed PA with and without an adaptive C-bias. Noticeably, the C-amplifier turn-on is accelerated with an adaptive C-bias and it can therefore contribute higher power after PBO, leading to a slight increase in output power. However, the impact on overall performance was not significant. Thus, while an adaptive C-bias was useful in increasing output power and approaching Doherty-like behavior, its absence was not critical in this design.

3.7 Summary

In summary, this work proposes a frequency-reconfigurable transformer combiner with adjacent low swing nodes where switched tuning capacitors with regular CMOS switches can be used to realize multi-band operation. The design of a high-power switched capacitor and a triple-band CMOS PA incorporating the proposed transformer combiner is also presented. Measurement results of the triple-band PA chip showed good frequency selectivity; however, when compared to simulations, a reduction in the PA's small and large signal performance was observed. Post-measurement analysis revealed that the presence of high-density fill around the various transformer structures in the design could have resulted in a substantial increase in transformer's

insertion loss bringing down the small-signal gain. The PA was designed to achieve transformer-based Doherty-like operation: however, phase mismatch between the carrier and peaking amplifiers was unfortunately overlooked during the design phase. Simulations confirmed the need to include phase compensation blocks in a Doherty-like PA design for optimum performance.

4 A 28 GHz Wideband Receiver Design Using One-Port Transformer-Coupled Resonators

4.1 Introduction

Phased-array transceivers [83]−[85] are required to overcome path loss and to realize advanced MIMO communication in emerging 5G networks in the 28/38 GHz bands [86]−[87]. Since antenna arrays with high element count are needed, it is important for the transceiver circuits to be compact, scalable and energy-efficient. Figure 4.1 shows a typical implementation of a sliding-IF receiver architecture with a wideband low-noise amplifier (LNA). The use of a wideband LNA results in a cost- and area-efficient flexible RF front-end which is easily integrated into a multi-element system and covers contiguous as well as widely-separated narrowband channels of a diverse spectrum [85]. Emerging 28 GHz 5G standards stipulate channel bandwidths below 500 MHz thereby requiring wideband LNA solutions to support the multiple narrowband 5G channels [86]. A wideband LNA also obviates the need to make the LNA frequency reconfigurable. While several wideband solutions have been reported for bands beyond 60 GHz [88]−[89], the design of
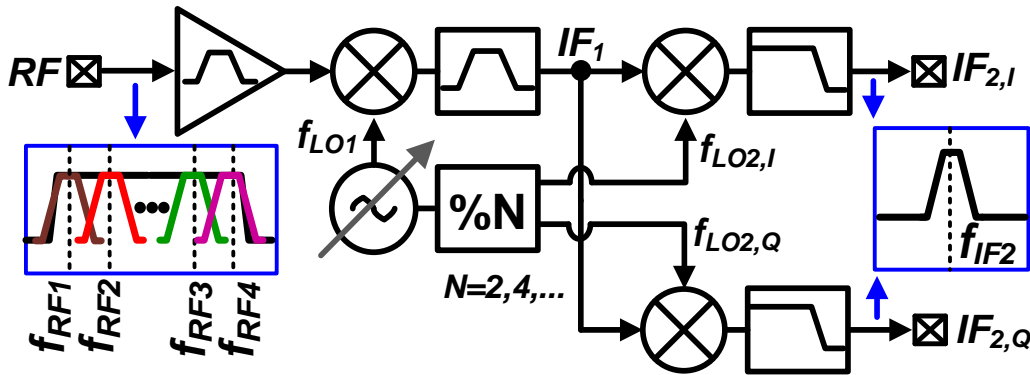
Figure 4.1   Block diagram of a sliding IF quadrature receiver adopted to relax the requirements of LO generation and distribution. In a direct-conversion and low-IF implementation, the first mixing and divide-by-N stages are omitted. A wideband LNA offers the flexibility of covering both contiguous and non-contiguous narrowband channels using the same RF front-end.

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wideband CMOS LNA's for the 28 GHz band is of high current interest due to a lack of high-performance designs in literature so far.

There is currently renewed interest in coupled *LC*-resonators whose application to mm-wave circuits including wide-tuning voltage-controlled oscillators (VCO) [91]−[92], power amplifiers (PA) [93] and LNAs [85], [88]−[90], [94] has been recently investigated. While various types of coupling (capacitive, inductive and magnetic)) are possible between the resonators, each resulting in a fourth-order transfer function, magnetic coupling is often preferred since it results in a lower ripple for a given bandwidth [89], and compact transformers provide dc isolation between stages besides saving area. The focus of this work is therefore on the design of transformer coupled-resonators.

Recently, mm-wave LNA designs have been reported that exclusively use the trans-impedance (Z_{21}) of weakly-coupled two-port transformer coupled-resonators as wideband loads of amplifier stages [85], [88]−[90]. However, prior literature has overlooked the fact that in addition to Z_{21}, the input driving point impedance (Z_{11}) of a one-port coupled-resonator is also a fourth-order function with two pairs of complex poles, and can potentially be used in wideband system design. Except for [94], there have been no reports to date on the use of Z_{11} as a wideband load.

In this work, the properties of Z_{11} and Z_{21} responses are compared, and design techniques are introduced to facilitate the use of Z_{11} as a wideband load. A detailed analysis is to show that in weakly-coupled transformer coupled-resonators, adopting the use of Z_{11} over Z_{21} can result in a higher gain-bandwidth product (GBW) if the Z_{11} response's in-band gain ripple is adequately tempered. Motivated by this insight, an effective transformer design technique is introduced to reduce the ripple in the Z_{11} response. It is shown that the Z_{11} gain ripple has a strong dependence on the quality factor of the transformer's secondary coil, and this property is exploited in compact,
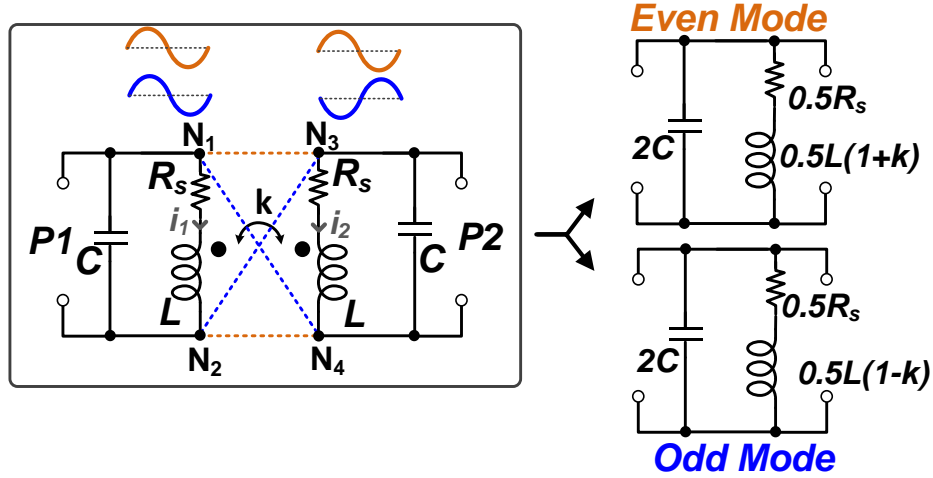
Figure 4.2 Even and odd resonant modes of a transformer coupled-resonator. Since the current flowing in the primary and secondary coils are in phase (out of phase) in the even (odd) mode, the voltage amplitudes developed across nodes N_1-N_2 and N_3-N_4 are identical. Nodes N_1 and N_2 can either be respectively electrically connected to N_3 and N_4 in the even mode, or with N_4 and N_3 in the odd mode, resulting in equivalent parallel-*RLC* networks from which the resonant mode frequencies can be deduced.

 nested-layout transformers to realize coupled-resonators with superior GBW. The design of a wideband LNA using these ripple-compensated Z_{11} wideband loads and its use in a quadrature receiver are described. Characterization results of the 65-nm CMOS prototypes show that the design achieves competitive performance with the smallest LNA footprint among comparable inductor and transformer-based designs [85], [94]−[98].

4.2 Transformer Coupled-Resonator Wideband Loads

4.2.1 One-port vs Two-port Configuration

 The driving point impedance (Z_{11}) and the trans-impedance (Z_{21}) of a pair of magnetically-coupled *LC* resonators can be written as:

$$Z_{11}(s) = \omega_0^2 L \frac{\left(s + \omega_{z1}\right)\left(s^2 + \frac{\omega_{z2}}{Q_{z2}}s + \omega_{z2}^2\right)}{\left(s^2 + \frac{\omega_{p1}}{Q_{p1}}s + \omega_{p1}^2\right)\left(s^2 + \frac{\omega_{p2}}{Q_{p2}}s + \omega_{p2}^2\right)}. \tag{4-1}$$

	Location	Quality Factor
LHP Zero	$\omega_{z1} = \frac{\omega_0}{Q}$	−
Complex Pole 1	$\omega_{p1} = \frac{\omega_0}{\sqrt{1+k}}$	$Q_{p1} = Q\sqrt{1+k}$
Complex Zero	$\omega_{z2} = \frac{\omega_0}{\sqrt{1-k^2}}$	$Q_{z2} = Q\frac{\sqrt{1-k^2}}{1+k^2}$
Complex Pole 2	$\omega_{p2} = \frac{\omega_0}{\sqrt{1-k}}$	$Q_{p2} = Q\sqrt{1-k}$

Table 4-1 Parameter values in canonical expressions of (4-2) and (4-3) with identical primary and secondary coil quality factors.

$$Z_{21}(s) = kL \frac{s}{\left(s^2 + \frac{\omega_{p1}}{Q_{p1}}s + \omega_{p1}^2\right)\left(s^2 + \frac{\omega_{p2}}{Q_{p2}}s + \omega_{p2}^2\right)}. \qquad (4\text{-}2)$$

Since these transfer functions have two complex poles, there are two possible resonant modes, called the 'even' and 'odd' modes (Figure 4.2). The currents in the two coils (i_1 and i_2) are in phase in the lower frequency even mode, and out of phase in the higher frequency odd mode [99]. From (4-1), it can be seen that Z_{11} has a real and a complex zero, while Z_{21} has a zero at the origin of the s-plane. The poles and the zeros of the two transfer functions are summarized in Table 4-1 in terms of the un-coupled resonant frequency ω_0, component quality factor Q and coupling coefficient k (characterizing a bandpass response in terms of resonator resonances, quality factors and coupling factors instead of specific values of L, C and R is often referred to as the 'k and Q approach [100], [101]). Figure 4.3 shows representative Bode magnitude responses of Z_{11} and Z_{21}. It is seen that if the ripple between the pole frequencies is not too severe, the coupled-resonator can be used as a wideband load in an amplifier by either configuring it as a one-port network (Z_{11}) [94] or a two-port network (Z_{21}) [88]−[90].

Figure 4.4 shows the important response characteristics as captured though the gain ripple R, the -3-dB bandwidth Δf_{-3dB}, separation of peak frequencies Δf_p, gain at the peak frequencies $- |Z|_{p1}$ and

$|Z|_{p2}$, and the maximum gain $|Z|_{max}$.
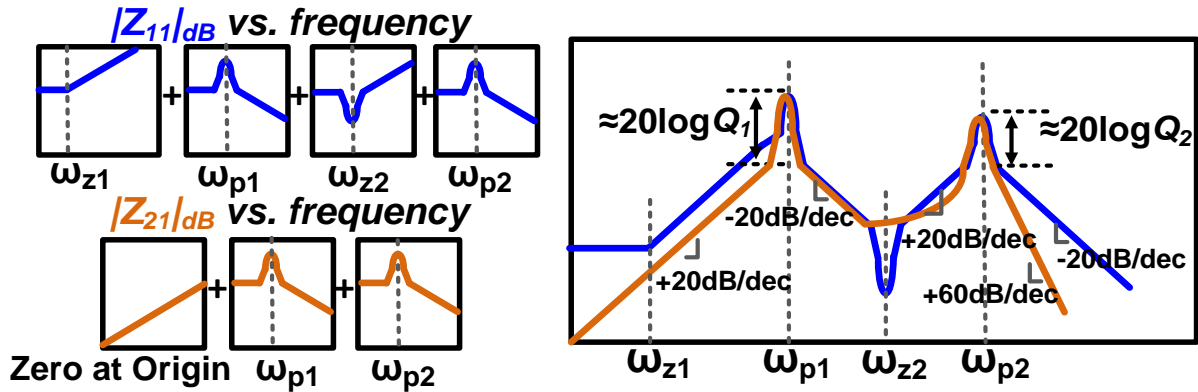
Figure 4.3 Representative bode amplitude plots of Z_{11} and Z_{21} of a transformer coupled-resonator.
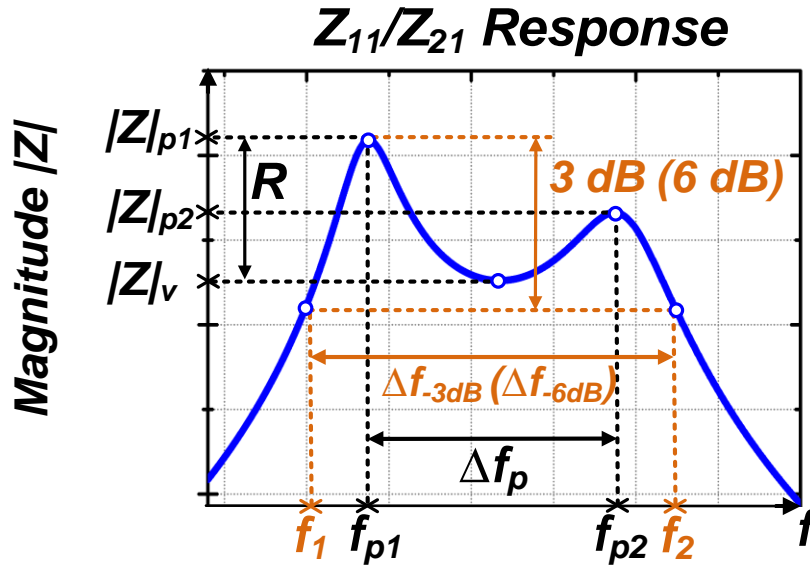
Figure 4.4 Typical frequency response of magnitudes of Z_{11} and Z_{21} of transformer coupled-resonator. f_{p1} and f_{p2} are the locations of the complex pole pairs, and Δf_p represents their frequency separation. $|Z|_{p1}$ and $|Z|_{p2}$ are the values of the gain peaks, $|Z|_v$ is the minimum value of gain within Δf_p (where $f_{p1} \le f \le f_{p2}$). The 3-dB bandwidth, marked as Δf_{-3dB} in the figure, is defined with respect to $|Z|_{max} = \max(|Z|_{p1}, |Z|_{p2})$. In a similar manner, Δf_{-6dB} can also be defined. $R = |Z|_{max} - |Z|_v$ represents the gain ripple.

Several observations can now be made:

1) *Complex Zero:* The presence of a complex zero (see (4-1) and (4-2))) located between the

   complex pole frequencies causes a notch in the Z_{11} response. Since a complex zero is not present

in Z_{21}, its response only shows a -20 dB/decade drop in the pass-band resulting in a less severe gain roll-off. The amount of peaking at the complex pole and zero frequencies are related to their respective quality factors, which are proportional to Q, as is evident from Table 4-1. Thus, while higher Q's will increase the gain ripple R, the effect will manifest more rapidly in the Z_{11} response due to presence of the complex zero in the passband.

2) *Amplitude Mismatch:* The different quality factors (Q_{p1} and Q_{p2} in Table 4-1) cause an amplitude mismatch in the vicinity of the pole frequencies [88]. If k increases, both Δf_p and R, and the amplitude mismatch increase as well. Therefore, most applications exploiting the wideband response of a transformer coupled-resonator usually have $k \sim$ 0.1-0.25 [85], [88]−[89], [93]−[94]. To simultaneously achieve high gain and large fractional bandwidths at mm-wave frequencies, multiple stagger-tuned gain stages, each employing a low-k coupled-resonator load, must then be cascaded [88]-[89], [94]. The use of cascaded frequency-offset stages relaxes the constraint on R. In other words, even if individual stages are constrained to have R less than 6 dB (instead of 3 dB), an overall flat response can be achieved [94]. Therefore, to facilitate analysis, this paper assumes that the wideband condition of a coupled-resonator's frequency response is violated only when $R > 6$ dB ($\Delta f_{-6dB} < \Delta f_p$). When $R > 6$ dB, a condition typically encountered for high values of k or Q, and more commonly for Z_{11}, the response is no longer wideband and should instead be considered as being concurrently narrowband at the two pole frequencies.

3) *Shape Factor (SF)*: SF, defined as the ratio of the -3-dB bandwidth to the -60-dB bandwidth, is a degree of measure of the steepness of the stopband skirts [102]. Note in Figure 4.3 that the Z_{11} response is symmetrical around the passband: both the upper and lower frequency transition-
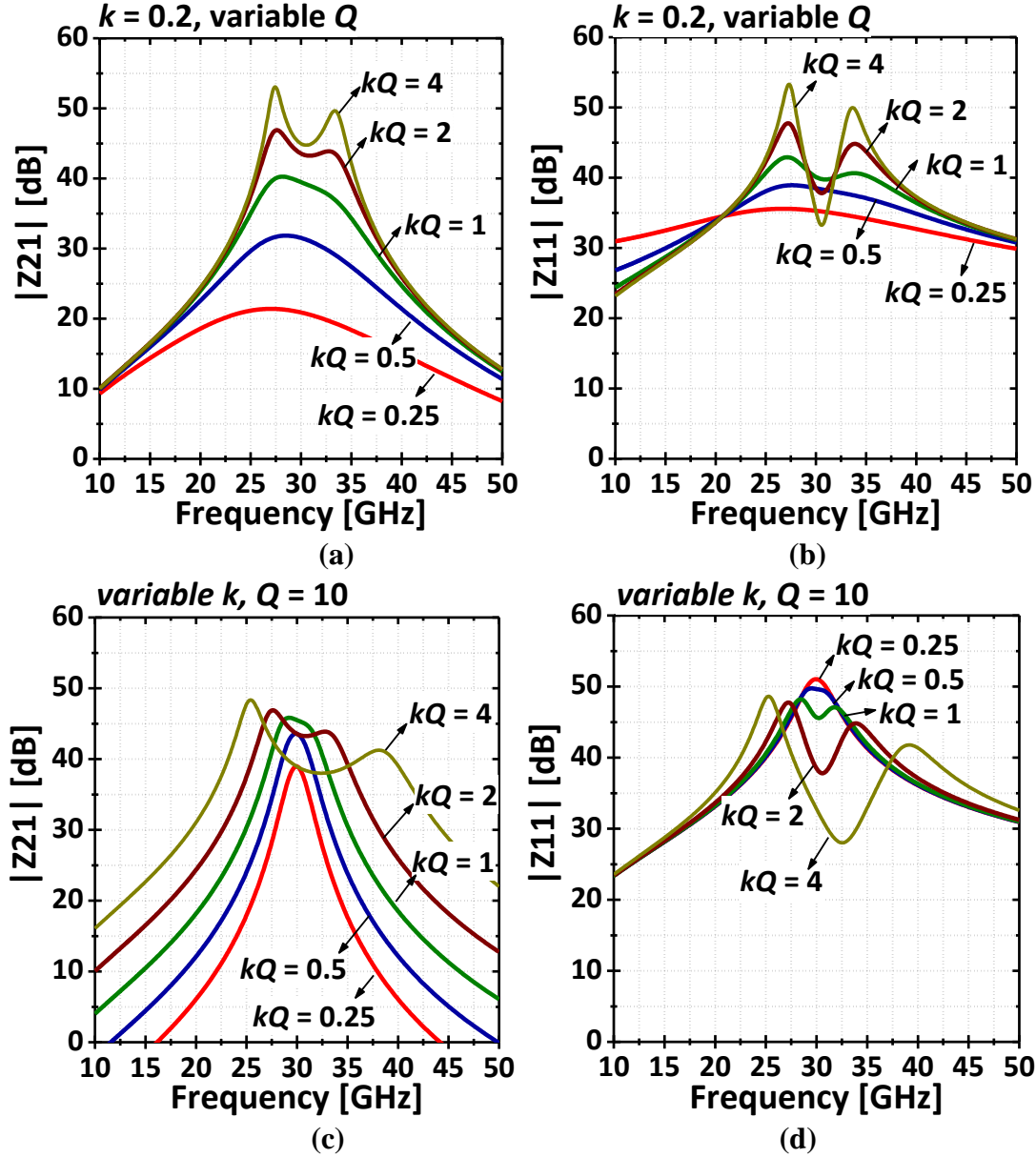
Figure 4.5 Variation of $|Z_{21}|$ and $|Z_{11}|$ with different values of 'kQ' product. In (a) and (b), Q was varied while k was kept constant at 0.2. In (c) and (d), k was varied while Q was kept constant at 10. Here, L = 200 pH, C = 140.7 fF. Inductor loss R_s was adjusted for different Qs at 30 GHz. All simulations were performed using ideal circuit elements.

 band skirts plummet down at the rate of -20 dB/decade. On the other hand, the Z_{21} response is

skewed with the upper frequency portion decreasing at -60 dB/decade resulting in a lower value

of SF (compared to Z_{11}). The -60 dB/decade skirt together with the zero at the origin lower the

effective -3-dB (Δf_{-3dB}) and -6-dB (Δf_{-6dB}) passband bandwidth of Z_{21}, which is a limitation in the context of wideband system design.

These observations are borne out by simulations shown in Figure 4.5 which plots the magnitudes of Z_{11} and Z_{21} for different values of the kQ product. An important point to note is that all applications of the transformer coupled-resonator as a wideband load satisfy $kQ > 1$, which corresponds to the over-coupled condition where a wide bandwidth is obtained at the expense of some in-band gain ripple [103]. As kQ drops below 1 (under-coupled), the response is either effectively narrowband ($k \rightarrow 0$) or shows high insertion loss ($Q \rightarrow 0$), and is therefore avoided in practice. From Figure 4.5, it is observed that for very high values of kQ, both the Z_{11} and Z_{21} responses violate the wideband condition ($R < 6$ dB). For moderate kQ values ($kQ \sim 2$), only Z_{11} violates the wideband condition due to the complex zero peaking. At lower values (for example, see $kQ = 1$), both the Z_{11} and Z_{21} responses are wideband. However, the Z_{11} response has a higher GBW as it not only exhibits a higher Δf_{-3dB} and Δf_{-6dB}, which is expected from the discussion of shape factors earlier, but a higher $|Z|_{max}$ as well. For example, it was observed in Figure 4.5(b) that when $kQ = 1$ ($k = 0.2$, $Q = 5$), the Z_{11} -3-dB (-6-dB) GBW was 2.1 (2.3) times the corresponding GBW of Z_{21}. A similar observation holds for Figure 4.5(d) as well. This rapid increase in the difference between the Z_{11} and Z_{21} magnitudes at low kQ values can be studied mathematically by expressing the ratio of Z_{11} and Z_{21} using (4-1), (4-2) and the values in Table 4-1 as:

$$\frac{Z_{11}(s)}{Z_{21}(s)} = \frac{1}{ks}\left(\frac{(1-k^2)}{\omega_0^2}s^3 + \frac{2}{Q\omega_0}s^2 + \left(1+\frac{1}{Q^2}\right)s + \frac{\omega_0}{Q}\right) \tag{4-3}$$

If we assume low coupling such that the middle of the passband is approximately at ω_0, then on substituting $s = j\omega_0$ in (4-3) results in:

$$\left|\frac{Z_{11}(j\omega_0)}{Z_{21}(j\omega_0)}\right| = \sqrt{k^2 + \frac{1}{Q^2}\left(\frac{1}{(kQ)^2} + 2\right) + \frac{1}{(kQ)^2}} \tag{4-4}$$

Equation (4-4) demonstrates that the ratio of the Z_{11} and Z_{21} magnitudes at ω_0 indeed shows a strong inverse dependence on kQ. It should be noted that the above analysis is limited to low values of kQ (≤ 1) where both the pole separation and the gain ripple are small and the Z_{11} and Z_{21} magnitudes at ω_0 can be considered representative of their passband magnitudes. The design predicament in the use of Z_{11} is thus evident: in a real application, the value of kQ is generally greater than 1 while the benefit of Z_{11}'s higher GBW only manifests at kQ values close to or below 1. It is also understood from the preceding discussion that the complex zero peaking in the Z_{11} passband is the main reason limiting its wideband application. The next section introduces a technique which reduces the ripple due to the complex zero and extends Z_{11}'s GBW advantage to higher kQ values.

4.2.2 Reduction of Complex Zero Peaking

Consider the transformer coupled-resonator of Figure 4.2, but with the primary and secondary coil inductors having different quality factors at $\omega_0 - Q_1$ and Q_2 respectively. The Z_{11} expression can be derived as shown in (4-5):

	Location	Quality Factor
LHP Zero	$\omega_{z1} = \dfrac{\omega_0}{Q_1}$	$-$
Complex Pole 1	$\omega_{p1} = \dfrac{\omega_0}{\sqrt{1+k}}$	$Q_{p1} = \dfrac{2Q_1Q_2\sqrt{1+k}}{Q_1+Q_2}$
Complex Zero	$\omega_{z2} = \dfrac{\omega_0}{\sqrt{1-k^2}}$	$Q_{z2} = \dfrac{Q_1Q_2\sqrt{1-k^2}}{Q_1+k^2Q_2}$
Complex Pole 2	$\omega_{p2} = \dfrac{\omega_0}{\sqrt{1-k}}$	$Q_{p2} = \dfrac{2Q_1Q_2\sqrt{1-k}}{Q_1+Q_2}$

Table 4-2 Parameter values in Z_{11} canonical expression of (4-5) and (4-3) with different primary and secondary coil quality factors.

$$Z_{11}(s) = \omega_0^2 L \frac{\frac{(1-k^2)L}{\omega_0^2}s^3 + \frac{\omega_0}{1-k^2}\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)s^2 + \frac{\omega_0^2}{1-k^2}\left(1+\frac{1}{Q_1Q_2}\right)s + \frac{\omega_0}{Q_1(1-k^2)}}{s^4 + \frac{\omega_0}{1-k^2}\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)s^3 + \frac{\omega_0^2}{1-k^2}\left(2+\frac{1}{Q_1Q_2}\right)s^2 + \frac{\omega_0^3}{1-k^2}\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)s + \frac{\omega_0^4}{1-k^2}} \quad (4\text{-}5)$$

By comparing (4-5) with the canonical form of (4-1), the frequency and quality factor of the complex poles and zero can be determined, as shown in Table 4-2. A key result follows from the expression of the quality factor of the complex zero (Q_{z2}) in Table 4-2: for low values of k, Q_{z2} has a much stronger dependence on Q_2 than on Q_1. Thus, to alleviate the impact of complex zero peaking, it is sufficient to merely reduce Q_2. Note that reducing Q_2 also reduces the quality factor
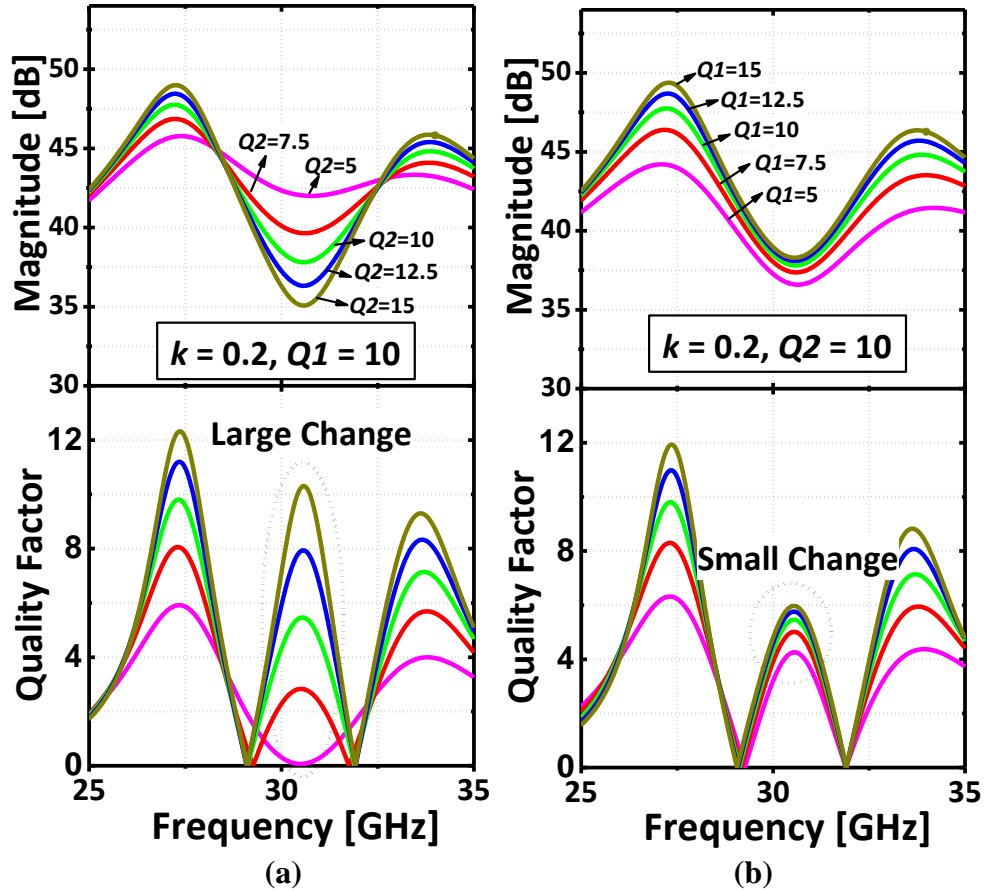
Figure 4.6 Z_{11} **magnitude and quality factor of a transformer coupled-resonator with different series losses in the primary and secondary coils. In (a), Q of the primary coil (Q_1) was fixed at 10, while Q of the secondary coil (Q_2) was varied between 5 and 15. In (b), Q_2 was fixed at 10, while Q_1 was varied between 5 and 15. Here, L = 200 pH, C = 140.7 fF. Inductor loss R_s was adjusted for different Qs at 30 GHz.**
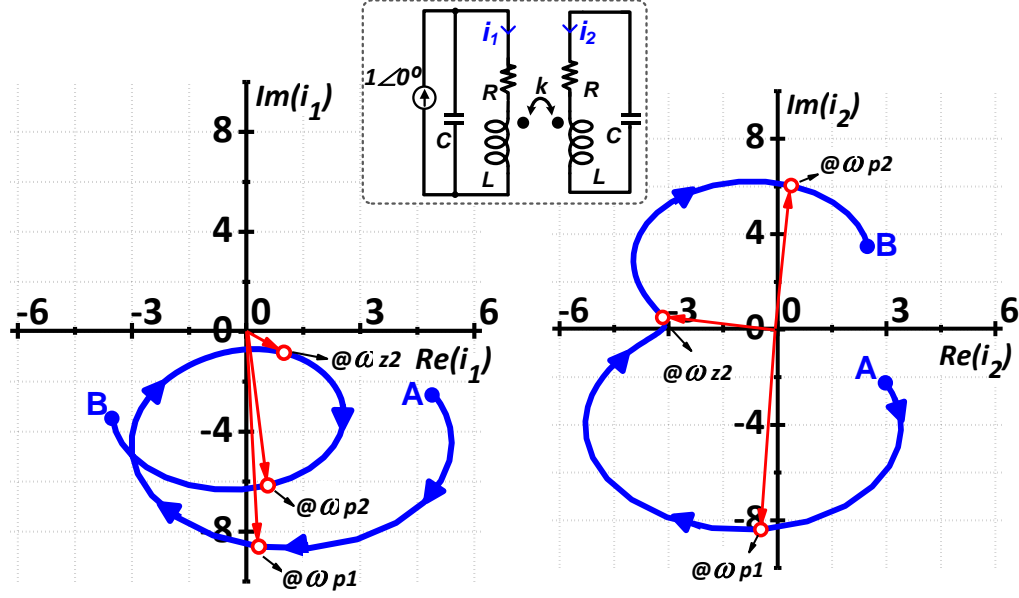
Figure 4.7 Movement of the primary and secondary coil current phasors in the complex plane as the frequency is varied between 25 GHz (marked as point A) and 37 GHz (marked as point B). Simulation setup is shown as an inset. i_1 and i_2 are the currents in the primary and secondary coils respectively. Current phasors near the complex pole and zero frequencies are also marked. Here, $L = 200$ pH, $C = 140.7$ fF, $k = 0.3$, and $R = 2.5\ \Omega$.

of the poles $(Q_{p1,p2} \propto Q_1 \| Q_2)$: however, the effect on GBW is less pronounced as de-Qing of the Z_{11} response curve around the gain peaks also increases the bandwidth. In Figure 4.6, the Z_{11} magnitude and quality factor is plotted for different values of Q_1 and Q_2. The quality factor was determined from the Z_{11} phase response [104]. As expected, the quality factor near the complex zero frequency changes rapidly with Q_2 if Q_1 is kept constant (Figure 4.6(a)) but shows only a minor change with Q_1 if Q_2 is kept constant (Figure 4.6(b)).

The strong dependence of Q_{z2} on Q_2 for low k values can be intuitively understood by observing the currents flowing in the primary and second coils near the complex zero frequency. In Figure 4.7, the movement of the primary (i_1) and secondary coil (i_2) current phasors in the complex plane with frequency is shown. When driven by a constant current source, as in Figure 4.7, the induced voltage across the primary coil near the complex zero frequency should be real-valued. Therefore, i_2 is nearly opposite in phase and approximately M/L ($= 1/k$, since mutual inductance $M=kL$) times
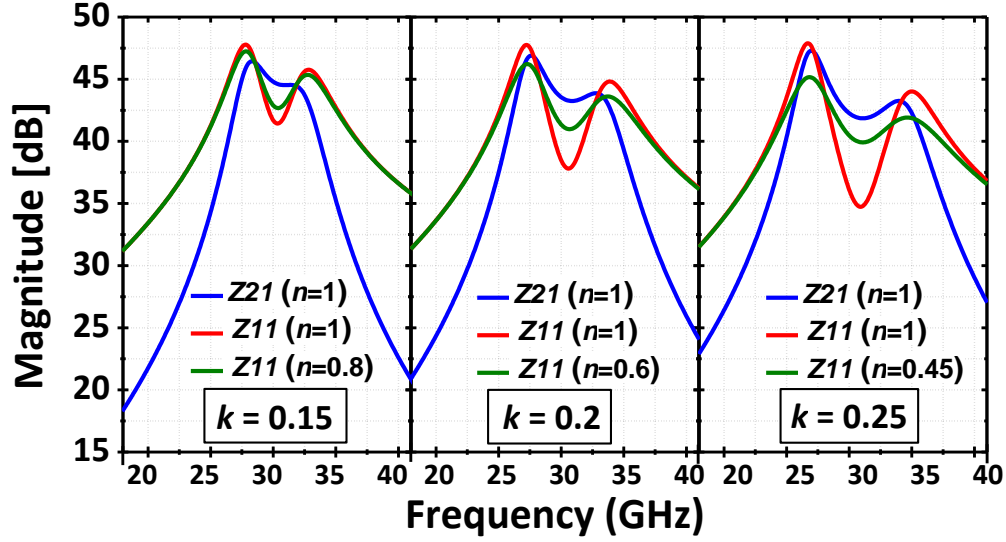
Figure 4.8 $|Z_{21}|$ and $|Z_{11}|$ for different values of k. The ripple-compensated Z_{11} response (n <1) is also overlaid. Here, $L = 200$ pH, $C = 140.7$ fF, $Q_1 = 10$.

larger with respect to i_1 to cancel the frequency-dependent voltage induced across the primary coil

due to i_1. This result can also be derived analytically: by solving the expressions for the mesh

currents i_1 and i_2, their ratio reduces to:

$$\frac{i_2}{i_1} = \frac{-k\left(\frac{s}{\omega_0}\right)^2}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q_2}\left(\frac{s}{\omega_0}\right) + 1} \tag{4-6}$$

From Table 4-2, the frequency of the complex zero is given by:

$$\omega = \omega_{z2} = \frac{\omega_0}{\sqrt{1-k^2}} \tag{4-7}$$

On substituting (4-7) in (4-6) and letting $s = j\omega$, (4-6) reduces to:

$$\left|\frac{i_2}{i_1}\right| = \left|\frac{k}{k^2 - j\left(\frac{\sqrt{1-k^2}}{Q_2}\right)}\right| \approx \frac{1}{k} \text{ (high } Q_2) \tag{4-8}$$

In a similar manner, on substituting the values of the complex pole frequencies, the ratio of i_2 to i_1

can be found to evaluate to ± 1 (assuming high Q_2). Therefore, we find from (4-8) that the ratio of
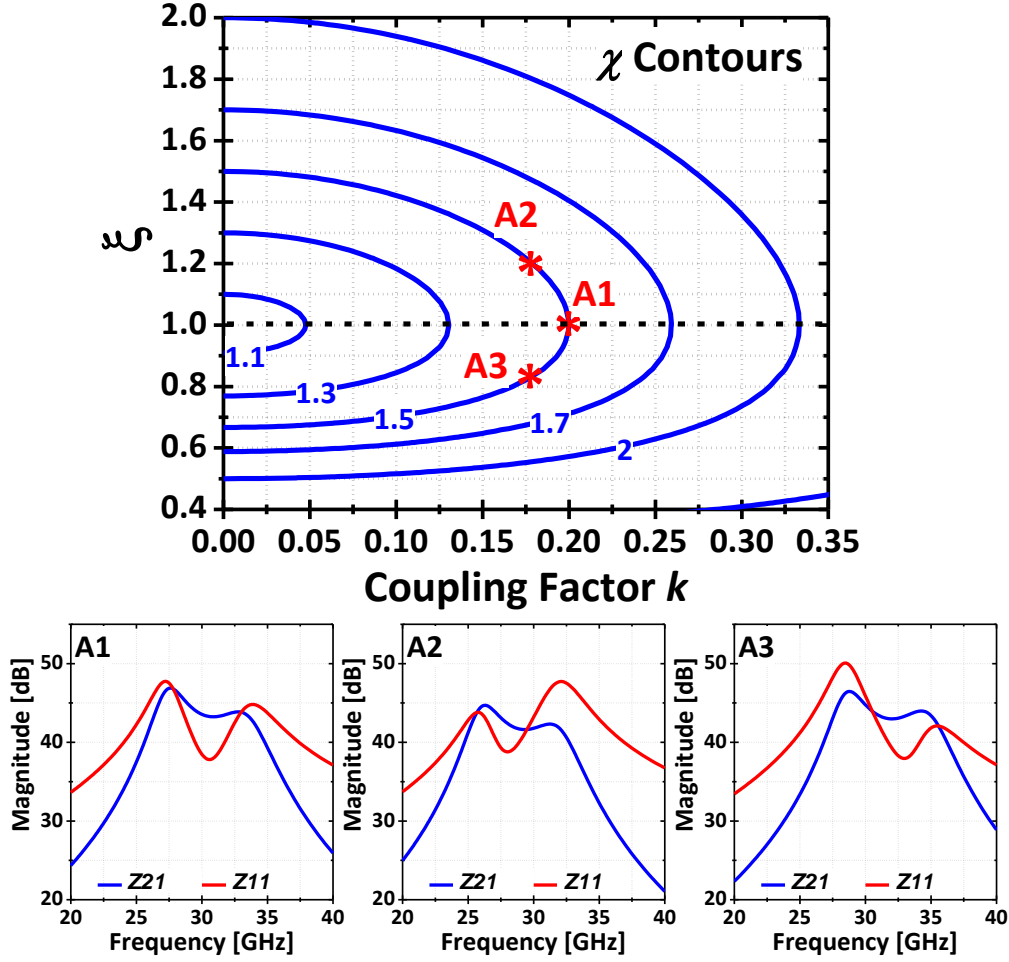
Figure 4.9 (k, ξ) **design space of a transformer-based resonator where** $\xi = (\omega_1/\omega_2)^2$ **and** k **is transformer coupling factor.** ω_1 **and** ω_2 **are the individual resonant frequencies of the uncoupled tanks. Contour plots of** $\chi = (\omega_{p2}/\omega_{p1})^2$ **are marked in blue (**ω_{p1} **and** ω_{p2} **are respectively the even- and odd-mode resonant frequencies of the coupled tanks). Contours assume high-**Q **conditions.** Z_{11} **and** Z_{21} **magnitude plots for three points A1 (**$k = 0.2$, $\xi = 1$**), A2 (**$k = 0.18$, $\xi = 1.19$**), and A3 (**$k = 0.18$, $\xi = 0.83$**) on** $\chi = 1.5$ **contour are shown (**$Q = 10$**).**

the i_2 to i_1 magnitudes near the complex zero frequency increases when k is lowered. Consequently,

the resonator power loss (and hence its Q) comes to be dominated by the loss in the larger current-

carrying secondary coil thereby creating a strong dependence of the resonator Q on Q_2.

Figure 4.8 overlays the ripple-compensated Z_{11} response with the Z_{21} and the uncompensated Z_{11}

responses of a low-k coupled-resonator ($k = 0.15$, 0.2, 0.25) where the coil Q-ratio $n = Q_2 / Q_1$.

Since this work uses cascaded stagger-tuned stages to realize a bandwidth larger than that available

form a single stage [94], a *k* of 0.2 resulted in a reasonable trade-off between gain ripple and bandwidth. It was observed that the Z_{11} gain ripple at larger *k* values was difficult to compensate adequately without adversely affecting the gain. When *k* = 0.25, an *n* of 0.45 was required; however, this noticeably reduces the peak gain at the pole frequencies. Therefore, the transformer coupled-resonator designs in this paper have $k \approx 0.2$ and $n \approx 0.6$-0.7.

4.2.3 (k,ξ) Design Space

In [91]-[92], it has been previously shown that the ratio of the transformer coupled-resonator's odd- and even-mode resonant frequencies, denoted here by χ for convenience, can be expressed as a function of the coupling factor *k* and ξ, where $\xi = (\omega_1/\omega_2)^2$ and ω_1, ω_2 are the resonant frequencies of the uncoupled tanks, as:

$$\chi = \left(\frac{\omega_{p2}}{\omega_{p1}}\right)^2 = \left(\frac{1+\xi+\sqrt{\left(1-\xi\right)^2 + \left(4k^2\xi\right)}}{1+\xi-\sqrt{\left(1-\xi\right)^2 + \left(4k^2\xi\right)}}\right) \tag{4-9}$$

The above expression assumes high-*Q* conditions. Figure 4.9 shows the contour plots of χ contours in the (k, ξ) design space. If the uncoupled tanks have the same resonant frequency ($\xi = $ 1), then under conditions of low coupling, the complex zero frequency (ω_{z2}) is approximately at the center of the Z_{11} passband. Since Q_{p1} is always greater than Q_{p2}, it is expected that the even-mode gain peak should always be higher than the odd-mode peak (for example, case A1 in Figure 4.9). This assumption holds only if the complex zero either has minimal or equal effect on both the pole frequencies. However, by choosing $\xi \neq 1$, we find that ω_{z2} can now be positioned either close to ω_{p1} ($\xi > 1$, case A2 in Figure 4.9) or close to ω_{p2} ($\xi < 1$, case A3). The effect of a proximate complex zero near the pole frequencies creates two different kinds of Z_{11} gain responses: in case A2, the even-mode peak is lower than the odd-mode peak while the behaviour reverses in case A3. Thus, a transformer coupled-resonator with a fixed *k* (chosen at design time) but with tunable

capacitors (and hence tunable ξ) can be configured to work at different points in the (k, ξ) design space, thereby providing an important post-fabrication design knob to control the Z_{11} frequency response. Notably, the Z_{21} response lacks a complex zero, and hence lacks this flexibility (in Figure 4.9, the Z_{21} gain profile does not change with ξ).

4.2.4 Design Example

To further illustrate the design guidelines developed in the previous sections, consider the circuits in Figure 4.10 which model an amplifier having two cascaded stagger-tuned stages using ideal circuit elements. In Figure 4.10(a), the Z_{21} responses of transformer coupled-resonators with coil Q-ratio $n = 1$ are used as wideband loads, while in Figure 4.10(b), the Z_{11} responses of ripple-compensated transformer coupled-resonators ($n = 0.6$) are used. Z_{11}'s GBW advantage is apparent: when compared to Figure 4.10(a), the amplifier gain profile in Figure 4.10(b) clearly has a larger

Figure 4.10 (a) Design example showing stagger-tuned and cascaded gain stages with coupled-resonator loads using ideal elements. In (a), Z_{21} wideband loads are used. Transformer coil Q-ratio $n = 1$ and $\xi = 1$ where $\xi = (\omega_1/\omega_2)^2$, and ω_1 and ω_2 being the individual resonant frequencies of the uncoupled tanks. In (b) and (c), Z_{11} wideband loads are used. Transformer coil ratio $n = 0.6$. In (b), $\xi = 1$. In (c), the second stage coupled-resonator is designed with $\xi > 1$ as $\omega_1 > \omega_2$.

Figure 4.11 (a) 15fF MOM capacitor constructed using M7, M6 and M5 metal layers. (b) Impact of MOM capacitor switching on the quality factor of an *LC* tank in 65 nm CMOS. The tank quality factor was determined from the phase stability factor. *Q* of the 230-pH inductor was 19 at 30 GHz.

bandwidth with similar peak gains. In Figure 4.10(c), the second stage uses a coupled resonator with $\xi >1$ (where the odd-mode gain peak is higher than the even-mode peak) to flatten the gain response further.

4.2.5 Design Tunability

To counter the effects of manufacturing line variations and dummy metal-fill structures, post-fabrication corrections using tunable switched capacitors are often necessary. Since metal-
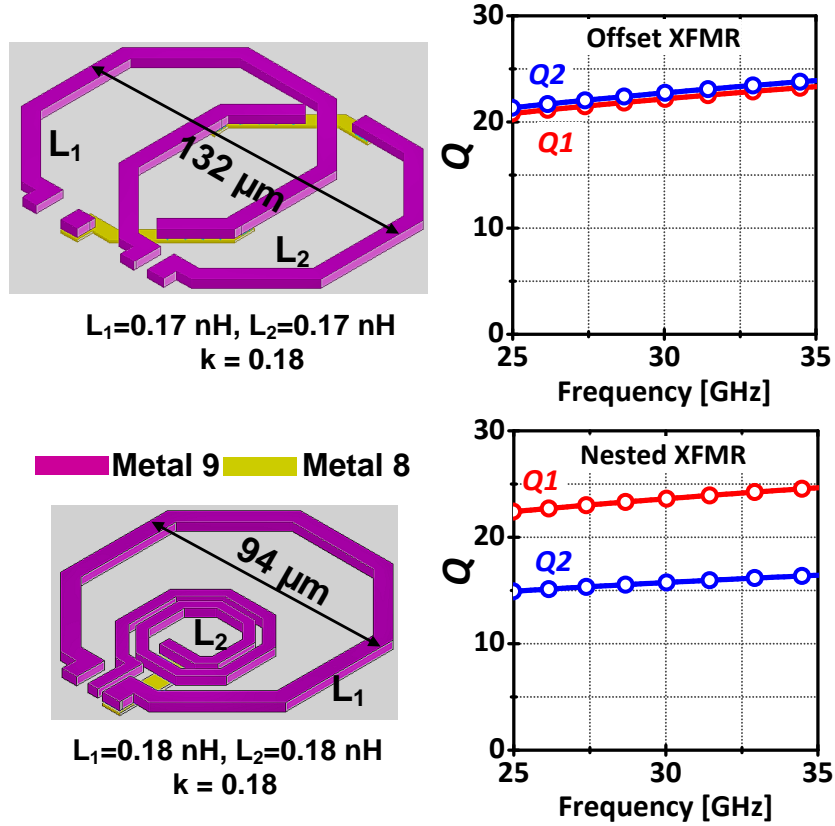
Figure 4.12 Offset and nested low-*k* transformer layouts with the simulated quality factors of the primary and secondary coils.

insulator-metal (MIM) capacitors (density > 1 fF/µm^2) are lossy at mm-wave frequencies [105], coupled-resonator's capacitances were realized as inter-digitated metal-oxide-metal MOM capacitors designed using the fifth, sixth and seventh metal layers (each 0.22 µm thick) of a 9-metal 65 nm process. A 15 fF MOM capacitor unit cell occupied an area of 4.9 µm×4.9 µm (density ~ 0.63 fF/µm^2, Figure 4.11(a)), and achieved a standalone *Q* of 65 at 30 GHz. A good design strategy is to use fixed MOM capacitors with high *Q*s along with switched MOM capacitor banks to simultaneously achieve high overall capacitor *Q* and post-fabrication tunability. *LC* resonators, designed using this strategy (see Figure 4.11(b)), were found to have *Q*s above 12 while allowing the resonance frequency to be adjusted by ± 10%.
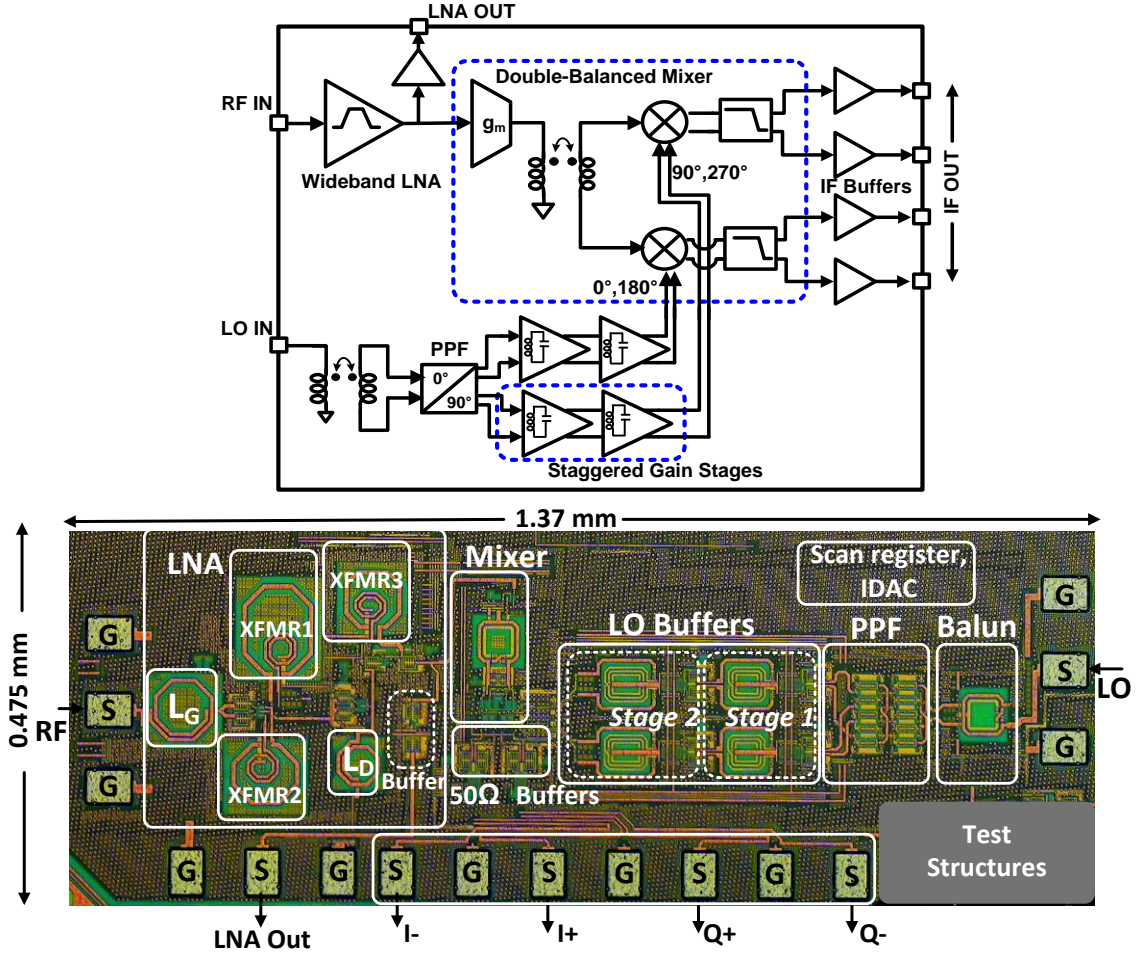
Figure 4.13 Block diagram and die photo of the receiver chip in 65 nm CMOS.

4.2.6 Transformer Layout

For a compact layout of transformer coupled-resonators, it is instructive to consider the various low-k implementations. Spatially-offset inductors are commonly used [85], [88]−[89], [94] in which case both the primary and secondary coils exhibit similar Qs (Figure 4.12). However, the area penalty can be severe, especially for low-k designs. A nested layout is also shown in Figure 4.12. Since $L_1 \approx L_2$, L_2 has two turns while L_1 has one. While low coupling factors can be achieved, the secondary coil has a smaller Q when compared to the primary coil as current-crowding effects in multi-turn inductors are known to limit Q at high frequencies. However, the overall area is limited to that of a single one-turn inductor and thus exhibit a better area vs. Q tradeoff. In addition,
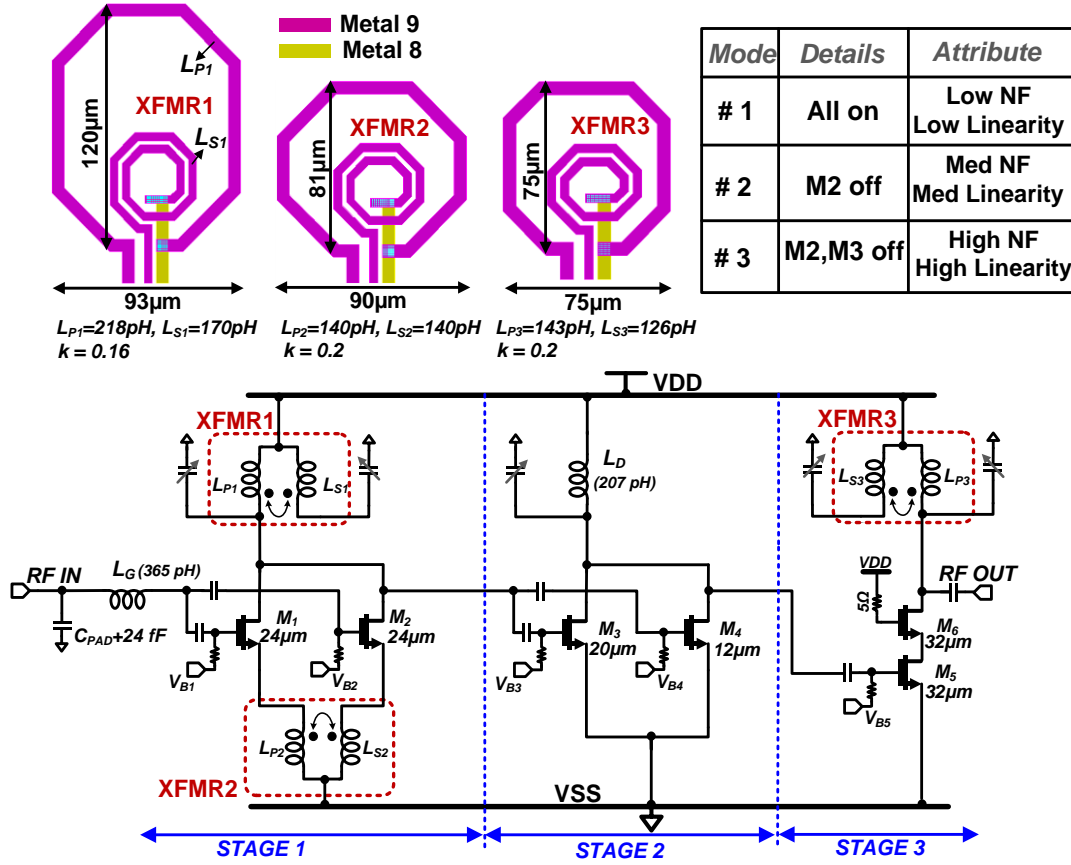
Figure 4.14 Circuit schematic and layout of the three-stage LNA. Layouts of the transformers employed in the design are also shown. All transistors are of minimum length (60 nm).

they inherently exhibit a coil Q-ratio less than 1 ($n = 0.65$ in Figure 4.12). As such, no special techniques are required to reduce the secondary coil Q. Therefore, the Z_{11} response of a coupled-resonator with a nested-layout transformer (where the high-Q primary coil is the input port) can be readily employed in wideband system design.

4.3 Wideband Receiver Design

The previously discussed techniques were used to implement a wideband LNA, employed in a quadrature low-IF receiver designed in a 65-nm CMOS process. Figure 4.13 shows the receiver die photograph and the block diagram.
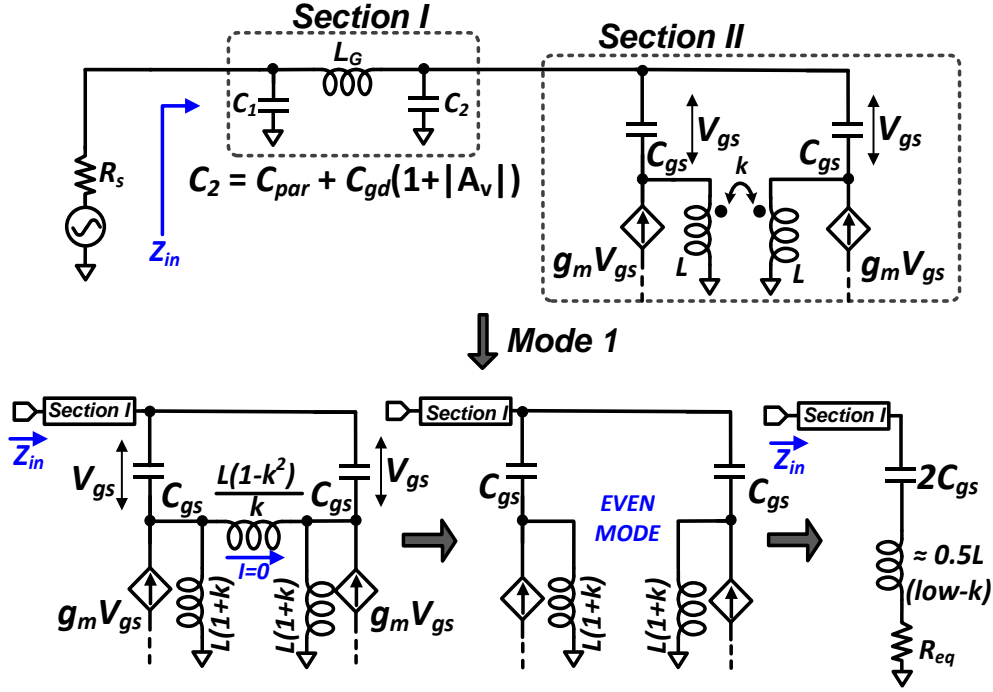
Figure 4.15 Equivalent circuit model of the input matching network. Note that in mode 1, section II only has an 'even' mode of operation due to symmetry and reduces to a series-*RLC* resonant circuit.

4.3.1 Low-Noise Amplifier

The proposed wideband LNA architecture employing three gain stages is shown in Figure 4.14.

The first stage of the LNA comprises two inductively-generated cascode common-source (CS)

legs – *M1* and *M2*, degenerated by source inductors L_{P2} and L_{S2}. In contrast to a conventional LNA,

weak coupling is introduced between the two inductors ($k \sim 0.2$), laid out in nested configuration

to save area. The two CS legs are designed to be symmetrical with same transistor sizes (24 µm)

and degenerating inductances (142 pH). To avoid the noise penalty, a cascode transistor was not

used. Stage 1 employs a coupled-resonator load (*XFMR1*) comprised of a nested transformer and

a combination of fixed and tunable MOM capacitors on the primary and secondary terminals. The

second CS stage, comprising two transistors *M3* and *M4* in parallel, uses a simple *LC* resonator

and serves to correct the droop in the frequency response of the first stage. A final third stage with

a coupled resonator load (*XFMR3*) extends the bandwidth of operation. Cascoded transistors *M5*

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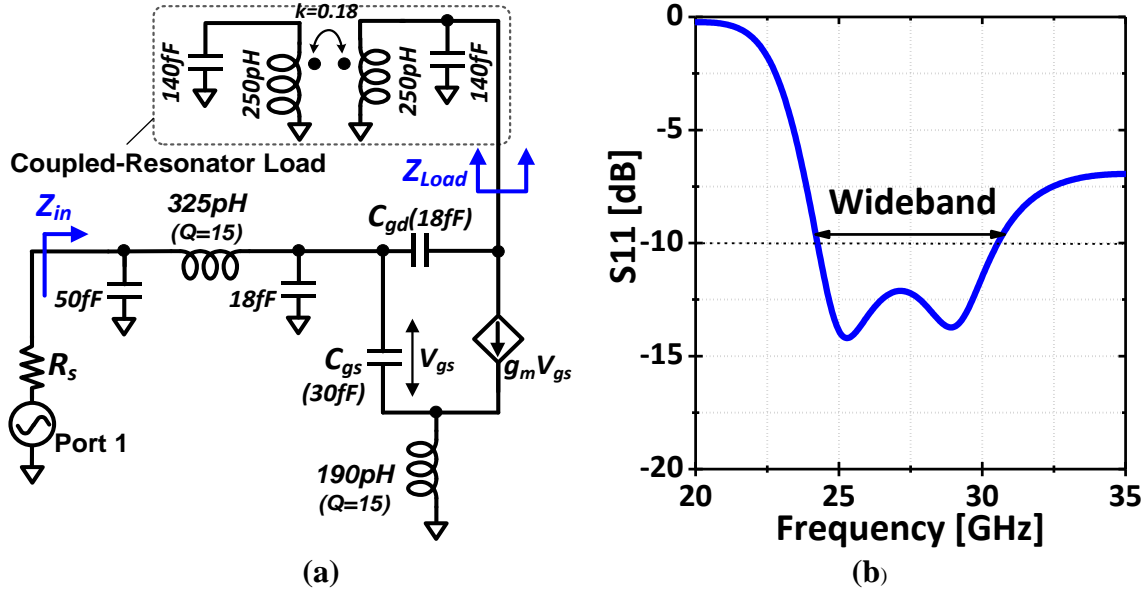
Figure 4.16 (a) Design example of a wideband input network using ideal elements. (b) Simulated S_{11}. Here, g_m = 35 mS and Q of inductors in the coupled-resonator is 12. Other component values are noted in the figure.

and *M6* are used in the third stage to improve the reverse signal flow. It is advantageous to design

XFMR3 with $\xi > 1$ as in the design example of Figure 4.10(c): however, due to the increase in

capacitance seen at the output node of the third stage from the following circuits, *XFMR3*'s

response was offset from but similar to *XFMR1* (as in Figure 4.10(b)). Each of the CS transistors

(*M1-M5*) was biased through a digitally-controlled current DAC, thereby allowing independent

control of the parallel CS branches in stages 1 and 2. The design of the LNA is often governed by

the need to accommodate large input signals due to the presence of large interferers. In this design,

higher linearity modes could be enabled by turning off parts of stage 1 and stage 2 respectively

(Figure 4.14). Thus, linearity could be traded for noise and voltage gain in discrete steps though

simple digital control.

Figure 4.15 shows the equivalent circuit model of the LNA's input matching network. To

facilitate analysis, the input network can be partitioned into two sections. The first section

comprises the gate-inductor L_g in a π-configuration with two capacitances, C_1 and C_2. C_1 is the

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capacitance from the input trace and pads and a purposely added 24 fF capacitor, while C_2 represents the sum of the trace parasitics and the miller-reflected gate-to-drain capacitance (C_{gd}) of the first-stage's CS transistors. The second section comprises the CS stage with transformer source degeneration. When one half of CS stage is off, the second section reduces to a series-*RLC* resonant circuit. Since the two CS stages were designed to be symmetrical, the second section reduces to a second-order system when both CS stages are on (Figure 4.15). While a shared source inductor could have been employed, the use of a source transformer with a nested layout avoids the large parasitic capacitance from a shared source node at no additional area overhead. The presence of the π-network reduces the value of the gate inductance required for input matching [106]. Cascading the low-*Q* π-network with a low-*Q* series-*RLC* second section, as in Figure 4.15, results in wideband input matching [94]. However, in the absence of a cascode transistor, the fourth-order response of the first stage's transformer-coupled load modifies the input match through the miller-reflected C_{gd}. This behavior is demonstrated through a simple design example in Figure 4.16(a) where the input network is modelled using ideal circuit elements. The higher-order response of the transformer-coupled load can be seen reflected in the simulated S_{11} in Figure 4.16(b). With this model as the starting point, the input network was further optimized for noise and gain [94], [106]. Since close to -10 dB S_{11} was observed in the three modes, no additional wideband input matching techniques were employed.

4.3.2 RF Mixer and I/Q LO Generation

A double-balanced Gilbert cell mixer was used to perform the mixing operation (Figure 4.17(a)). The first stage of a mixer, a single-ended transconductance (g_m) stage, was coupled to the switching quad through a single-ended to differential balun. Additional common-gate transistors were inserted between the secondary winding of the balun and the switching quad to improve RF-to-LO
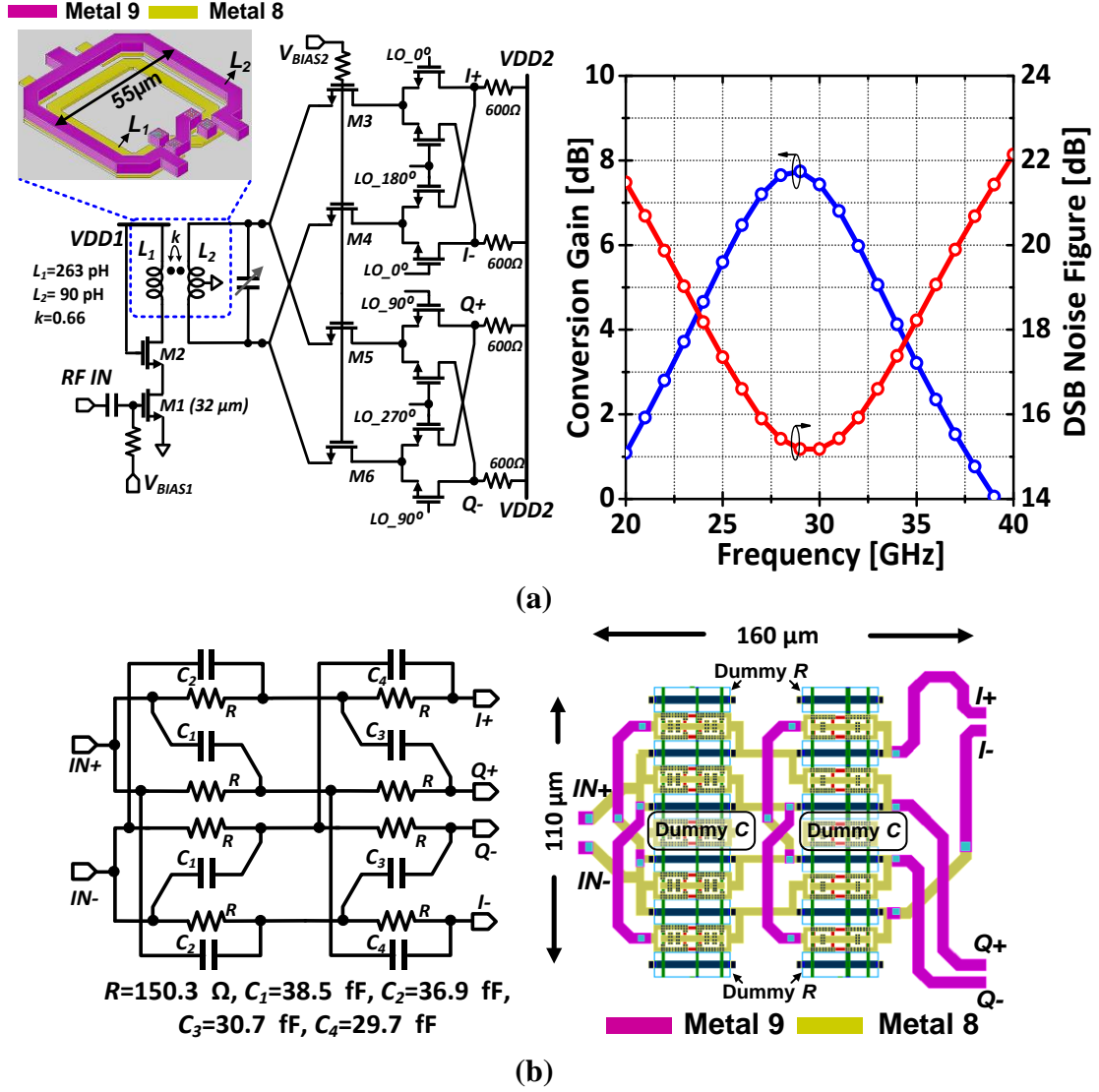
Figure 4.17 (a) Circuit schematic, and simulated conversion gain and DSB noise figure of the double-balanced mixer. All transistors are of minimum length (60 nm). IF frequency = 1 GHz. (b) Circuit schematic and layout of the two-stage wideband PPF.

isolation [107]. The use of a balun isolates the dc current of the switching stage from that of the g_m-stage, which allows for a higher load resistance at the output of the mixer and consequently, a higher conversion gain [84]. The mixer was simulated to have a conversion gain of 7.7 dB at 28 GHz, while consuming ~11 mA of current. The mixing stage was followed by 50Ω IF buffers to drive the instrument load.
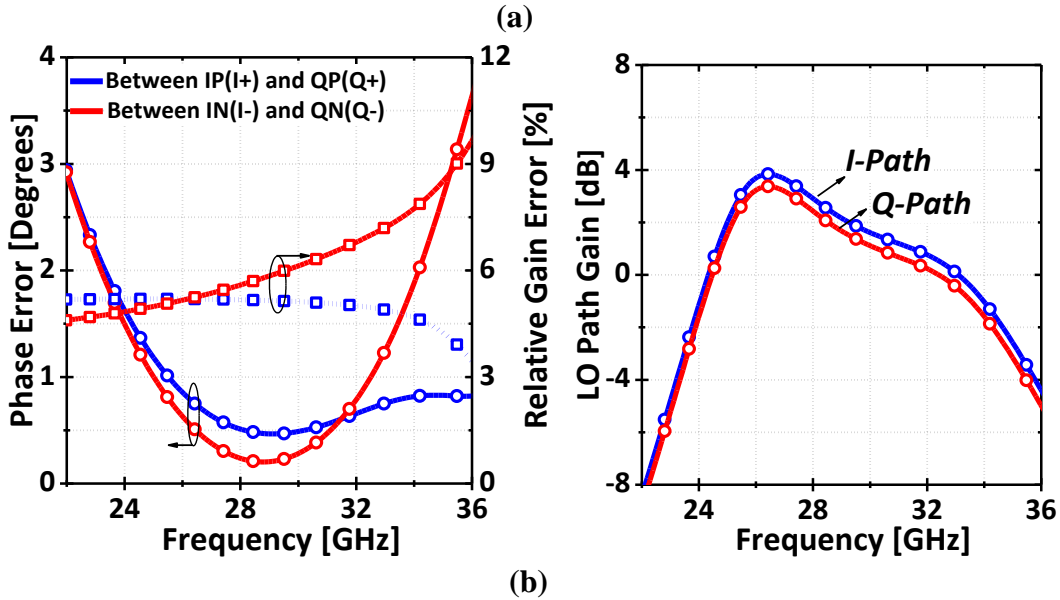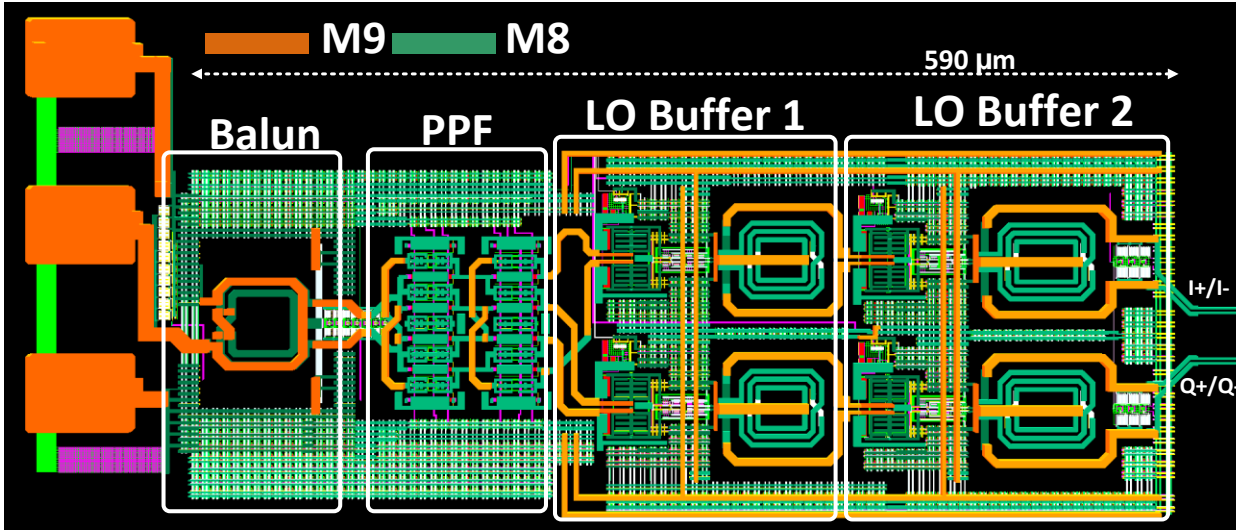
Figure 4.18 (a) Complete LO Path layout. (b) Relative gain error, phase error between I+/Q+ and I-/Q-, and the single-ended to differential I-path and Q-path gains.

To simplify the measurement setup, quadrature LO signals for the mixer were generated on-chip using an external sinusoidal LO signal source. An input balun provided input-matching, and converted the single-ended LO input to a differential signal. A two-stage polyphase filter (PPF) followed the balun. Layout and parasitic compensation techniques, introduced in [108], were

followed to improve the PPF's *I/Q* accuracy over a wide bandwidth. The circuit schematic and layout of the PPF are shown in Figure 4.17(b). To compensate for the high signal loss in the two-stage PPF, two differential staggered-gain stages (LO Buffers 1 and 2, see Figure 4.18(a)) followed the PPF which ensured a reasonable voltage swing at the mixer inputs. Image rejection ratio (IRR) of the LO path was simulated to be better than 29 dB in the 25-32 GHz frequency range. The relative gain error and phase error are plotted in Figure 4.18(b). Each LO buffer consumed 13.5 mA from a 1.1V supply.

4.4 Measurement Results

Although the LNA was fabricated along with the rest of the receiver, a measurement buffer was added at the output of the LNA to facilitate standalone characterization. The LNA was measured in each of its three modes of operation with a power supply of 1.1 V. To demonstrate low-power operation, mode 1 performance was also measured at reduced supply voltages of 0.95 V and 0.85 V respectively. Figure 4.19(a), (b) shows the measured gain and input match of the LNA. The voltage gain was determined from the measured S-parameters [109], and the simulated loss of the measurement buffer was de-embedded from the measurement. The addition of the LNA measurement buffer as well as a long interconnect between the LNA and the mixer resulted in a slight reduction in bandwidth. Good correlation between the simulations and measurements was observed. The input match was measured to be smaller than -7.5 dB throughout the band in each of the linearity modes.

The linearity of the LNA was characterized through its input referred input compression point (iP1dB). Figure 4.19(c) shows the improvement in the linearity performance of the LNA between mode 1 and mode 3. At an RF frequency of 28 GHz, mode 1 iP1dB was measured to be -23 dBm while the mode 3 iP1dB was measured to be -19 dBm. The group-delay variation in mode 1 was

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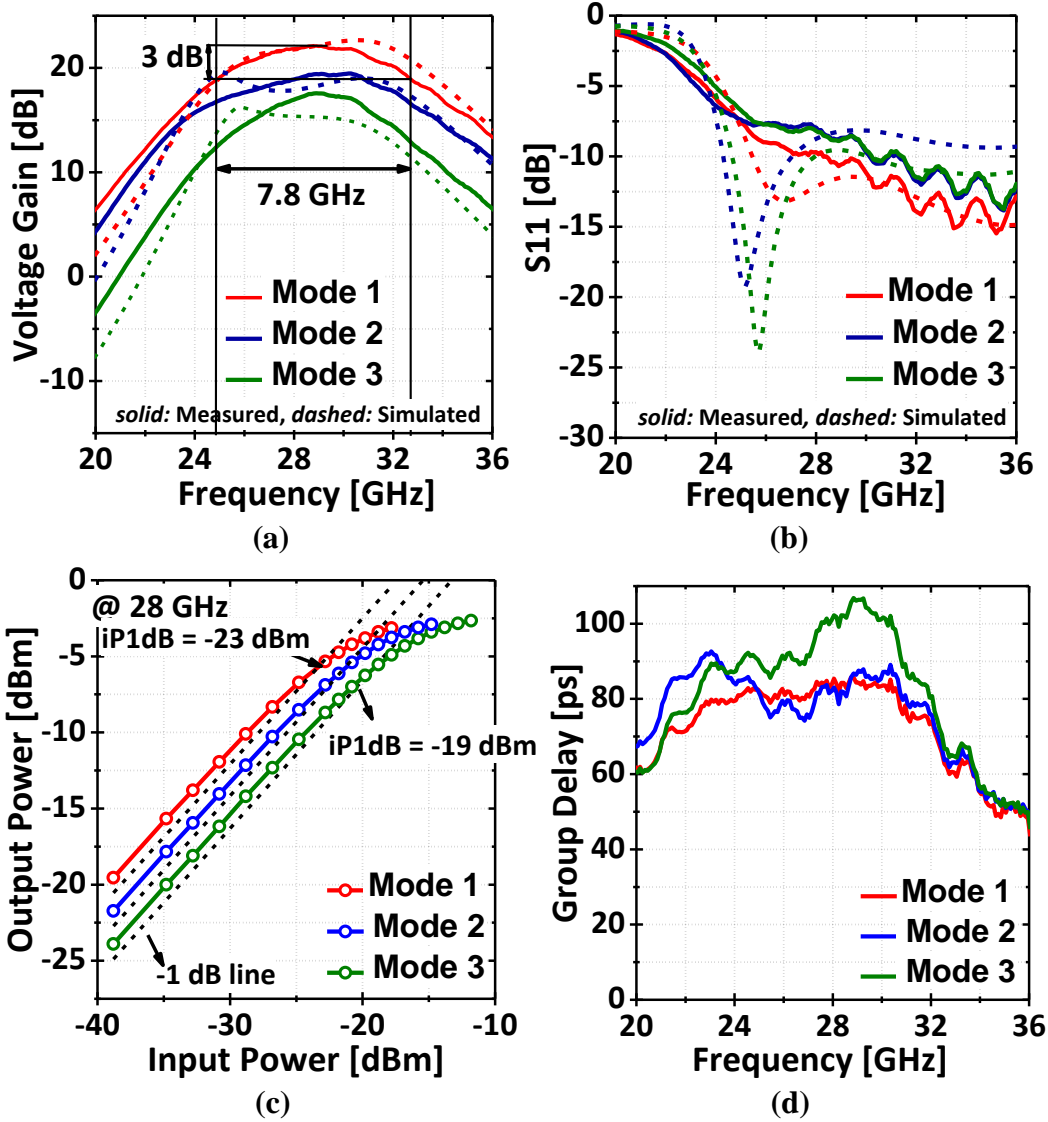
Figure 4.19 LNA measurement results in different modes: (a) gain, (b) S_{11}, (c) input-referred 1-dB compression point (iP1dB) at 28 GHz, and (d) group delay variation.

measured to be 73±13 ps over the -3-dB bandwidth, as shown in Figure 4.19(d). The variation of

the LNA's iP1dB and NF with RF frequency is shown in Figure 4.20. A *Noisecom NC346V* noise

source in conjunction with an *Agilent E4440A* spectrum analyser was used for NF measurement.

Due to the upper frequency limit of the measurement set-up, NF could only be measured up to

26.5 GHz.
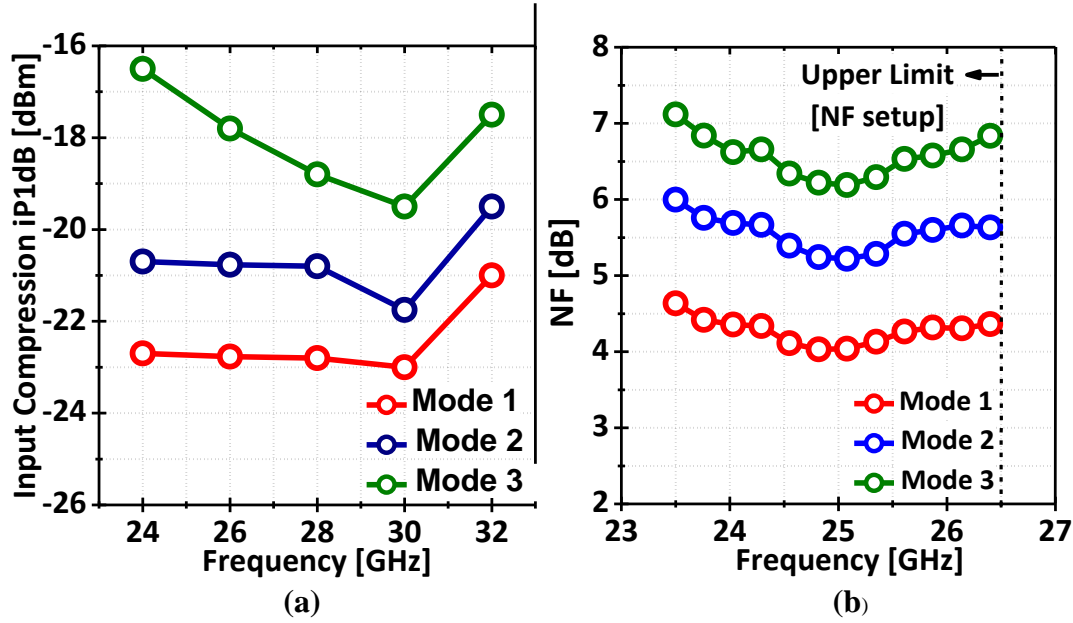
Figure 4.20 Variation of LNA (a) iP1dB, and (2) NF with RF frequency.

In the low-NF mode 1 of operation, a minimum NF of 4 dB was observed at 25 GHz. As expected, NF increases to 6.2 dB in the high-NF high-linearity mode 3 of operation. Over 55% reduction in power was observed in the low-power mode (0.85 V supply). Use of local current mirrors (sharing the LNA VDD) resulted in lowering of transistor biases at reduced supply voltages, thereby further reducing the power.

Like the standalone LNA measurement, the receiver was also measured with the LNA configured to be in each of its three linearity modes. Figure 4.21(a), (b) shows the measured conversion gain (CG) and the DSB NF. A maximum CG of 29.5 dB and a minimum DSB NF of 5.3 dB was measured in mode 1 of operation. The output IF buffer's loss was de-embedded from the measurement results. In the receiver's low-power mode, where the LNA operates in mode 1 at a reduced supply voltage of 0.85 V, peak CG of 24.7 dB and a minimum DSB NF of 6.5 dB was measured. When the LNA is configured to operate in its high-linearity mode 3, an improvement of 5 dB in the measured iP1dB is observed. The receiver achieved an RF bandwidth of 6 GHz between 26.5 GHz and 32.5 GHz. Reduction in the RF bandwidth of the receiver, compared to the
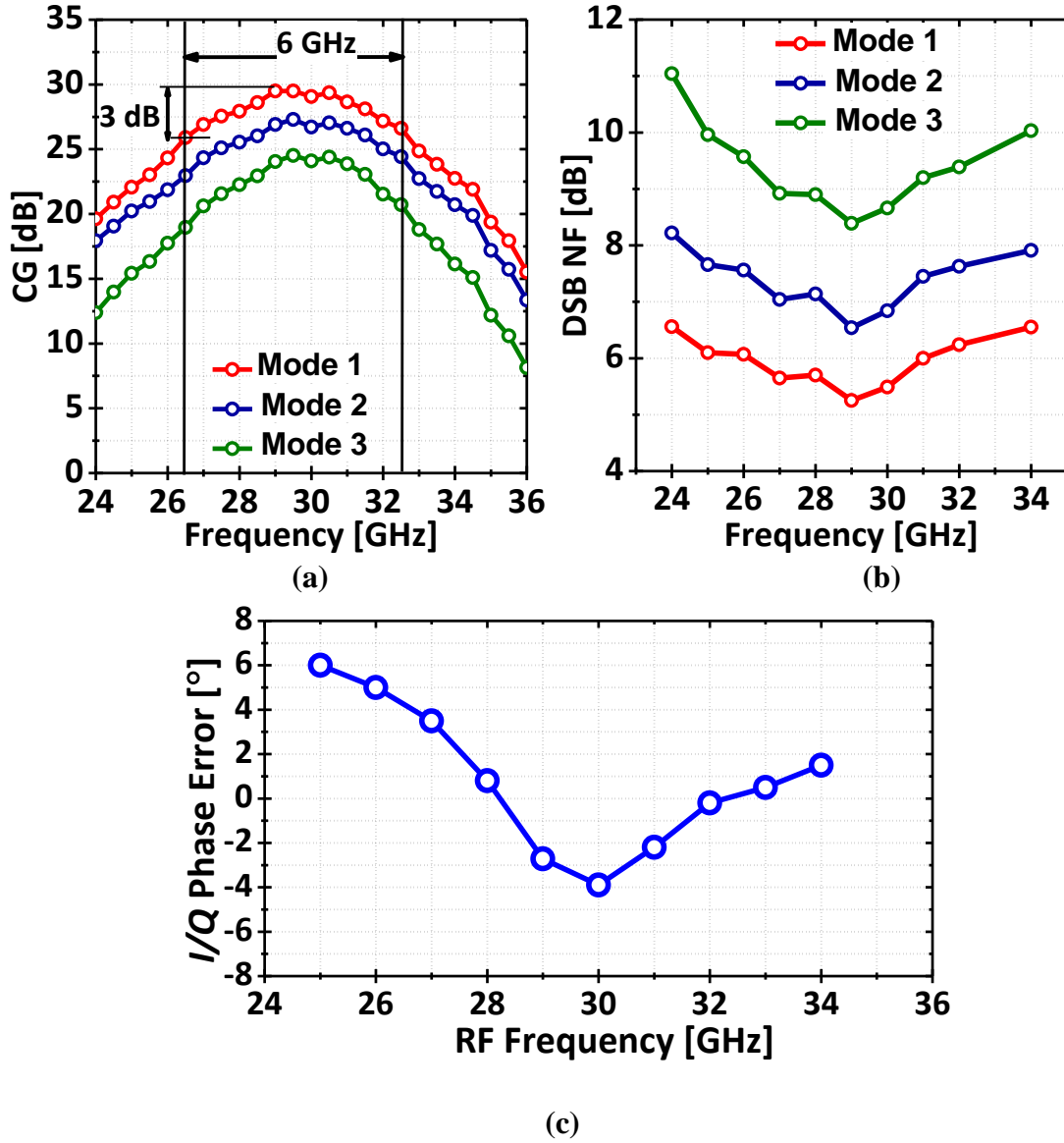
Figure 4.21 **Receiver measurement results (a) conversion gain (IF = 1 GHz), (b) DSB NF (IF = 2 GHz). (c)** *I/Q* **phase mismatch measured at the IF output at a low IF frequency of 50 MHz.**

LNA, can be attributed to the non-wideband design of the mixer's g_m-stage. The upper limit of the IF frequency, limited by the pole at the mixer's output, was measured to be 2.5 GHz. The quadrature phase error of the LO path with the wideband PPF was also estimated by measuring the phase difference between the *I+* and *Q+* IF outputs. Note that the LO phase error appears

		LNA								**Receiver front-end**					
	Tech.	VDD [V]	Freq [GHz]	Gain [dB]	NF min [dB]	iP$_{1dB}$ [dBm]	Power [mW]	Area [mm²]	FoM	Freq [GHz]	CG (Max) [dB]	NF min DSB [dB]	iP$_{1dB}$ [dBm]	Power [mW][4]	I/Q Phase Error[9]
Mode 1		1.1		22.1	4.0[1]	-23[2]	22[3]		3.0		29.5	5.3	-28	33	
	65 nm CMOS	0.95	24.9-32.7	20.2	4.4[1]	-23[2]	14[3]		3.2	26.5-32.5	27.0	5.7	-27	22.3	
		0.85		18.3	4.6[1]	-22[2]	9.9[3]	0.12	3.4		24.7	6.5	-26	16.7	≤5°
Mode 2		1.1	24.6-32.8	19.5	5.2[1]	-21[2]	19.3[3]		1.7	26.5-32.5	27.3	6.5	-25	30.4	
Mode 3		1.1	25.9-32	17.6	6.2[1]	-19[2]	16[3]		0.9	27-32	24.5	8.4	-23	27	
[70] Simulation	65 nm CMOS	1.0	25-30	18	3.7	–	10	0.135	2.95						
[82]	90 nm CMOS	1.0	27.6-30.2	20	2.9	-17	16.25	0.67[5]	2.5						
[83]	90 nm CMOS	1.2	1.6-28	10.7[6]	3.7	-9	21.6	0.14[8]	3.1						
[81]	0.13 µm CMOS	1.2	17.3-29.3	18[6]	4.7	>-20.6[7]	14.4	0.19	3.4						
[84]	0.18 µm CMOS	-	14.3-29.3	9.9[6]	4.3	-12	13.9	0.54	2.0						
[78]	0.18 µm BiCMOS	1.5	23-32	12	4.5	>-15.9[7]	13	0.25	1.5						

$$FoM \text{ [GHz/mW]} = \frac{Gain_{mag} * BW[in \text{ GHz}]}{(NF_{mag} - 1) * P_{DC}[in \text{ mW}]}$$

Table 4-3 Measurement results and comparison.

[1]Measured up to 26.5 GHz, [2]Measured at 28 GHz, [3]Excludes the LNA buffer, [4]Excludes IF buffer, [5]Transmission line-based design [6]Calculated from reported S_{21} assuming ideal input match (S_{11} = 0), [7]Calculated from IIP3, [8]Including pads, [9]Measured at low IF of 50 MHz.

directly at the IF output while the LO gain error is mostly rejected by the mixer at sufficiently large LO amplitudes. To minimize the contributions from the signal path layout mismatches and the measurement setup to the LO *I/Q* phase error, the measurement was carried out at a low IF of 50 MHz. The *I/Q* phase error, shown in Figure 4.21(c), was measured to be smaller than 5° in the 26-33 GHz band. The gain imbalance was smaller than 0.32 dB.

4.5 Summary

A summary of the LNA and receiver performance and benchmarking against similar work is provided in Table 4-3. The LNA demonstrates a best-case *FoM* [74], [81] of 3.4, highest among similar designs, while occupying the smallest area. While the use of Z_{11} wideband loads was previously proposed in [94], this paper studies their properties and application in significant detail, and proposes an effective technique to reduce their gain ripple by lowering the secondary coil *Q*.

It would also be fair to note that the advantages of Z_{11} are less obvious in applications where the inter-stage network capacitances can be very large: for example, the driver stages of a power amplifier. However, this investigation was beyond the scope of this paper.

In summary, this work describes the design of a multi-mode, wideband, low-noise amplifier (LNA) and receiver in a 65-nm process using the driving-point impedance (Z_{11}) of one-port transformer coupled-resonators. Design guidelines and insights are presented for the use of Z_{11} as a wideband load. Nested-layout transformers are shown to simultaneously minimize area and flatten the Z_{11} response. The effectiveness of the proposed design techniques is demonstrated through measurements of 28-GHz LNA and quadrature receiver prototypes. The LNA achieves ~7.8 GHz -3-dB RF bandwidth, >22 dB peak voltage gain consuming 20 mA of current, and compares favorably with state-of-the-art while occupying the smallest area compared to similar inductor-based wideband designs.

5 A 25.1-27.6 GHz Frequency-Tunable Merged LNA Vector Modulator Using Transformer-Coupled Resonators

5.1 Introduction

Emerging 5G mm-wave networks require multi-antenna beamforming systems to overcome path loss and facilitate directional communication. RF-domain gain and phase control (complex-weighting) of each received signal results in better energy-efficiency for simple phased-array beamforming compared to a full digital implementation. RF phase control is achieved through RF phase shifters which can be realized using several different topologies [110]-[122]. The requirements of phase shifters include large phase-control range (360°), small phase-shift step size, low insertion loss, and orthogonal phase and gain control for simultaneous beam steering and sidelobe control [110] (in other words, gain variation over all phase states and phase variation over
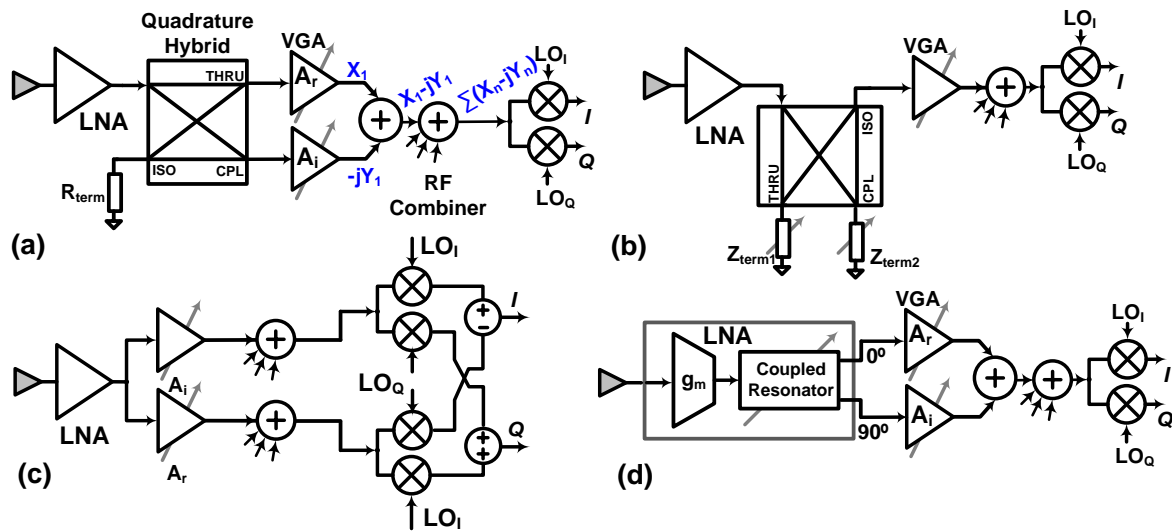
Figure 5.1 Architectures of a homodyne *N*-element RF-path phase-shifting phased array receiver: (a) traditional vector modulator/interpolator using a quadrature hybrid and Cartesian combining, (b) reflection-type phase shifter (RTPS), (c) complex mixing based Cartesian phase shifting, (d) proposed merged LNA-vector modulator using a coupled-resonator for I/Q generation.

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all gain states should be low). Additionally, phase-shifting architectures must be scalable (small area and power footprint) and be amenable to easy and inexpensive calibration.

A passive approach composed of cascaded switched LC networks [111]-[112] can achieve discrete phase shifts. The advantages of a passive approach include low power and high linearity. However, they require large area, which can become prohibitively large if higher phase-shifting resolutions are required. Additionally, the use of MOS switches at mm-wave frequencies is challenging (an ideal RF switch should simultaneously achieve low insertion loss and high isolation, which has been proven to be a problem even in advanced CMOS nodes in Chapter 2). Vector modulator (VM) based active architectures employing multibit programmable gain amplifiers (PGA) enable high-resolution RF beamforming thereby enabling advanced array signal processing techniques and are widely adopted in phased-array implementations [113]-[119]. The vector modulator/interpolator creates variable gain and phase shift using a cartesian combining technique [113], [117] using weighted in-phase (I) and quadrature-phase (Q) vectors (in Figure 5.1(a), the magnitude and phase of the weight are given by $A = \sqrt{A_r^2 + A_i^2}$ and $\theta = \tan^{-1}(A_i / A_r)$ respectively). However, a limitation of VM-based complex-weighting is the need for large, lossy quadrature hybrids in each receive channel, which are usually realized using polyphase filters or lumped-element microwave couplers. The quadrature hybrid can be re-purposed for use in a reflection-type phase shifter (Figure 5.1(b)) [120]-[122]; however, RTPS-based designs suffer from phase-dependent signal loss requiring complex gain calibration.

To overcome the problems of traditional phase shifters, the $90°$ phase shift function can be realized through complex downconversion (Figure 5.1(c)) [117], [118] which results in a compact, wideband solution. An additional benefit of this approach is that direct-conversion and complex image-reject receivers must generate quadrature LO signals which can be readily utilized to realize

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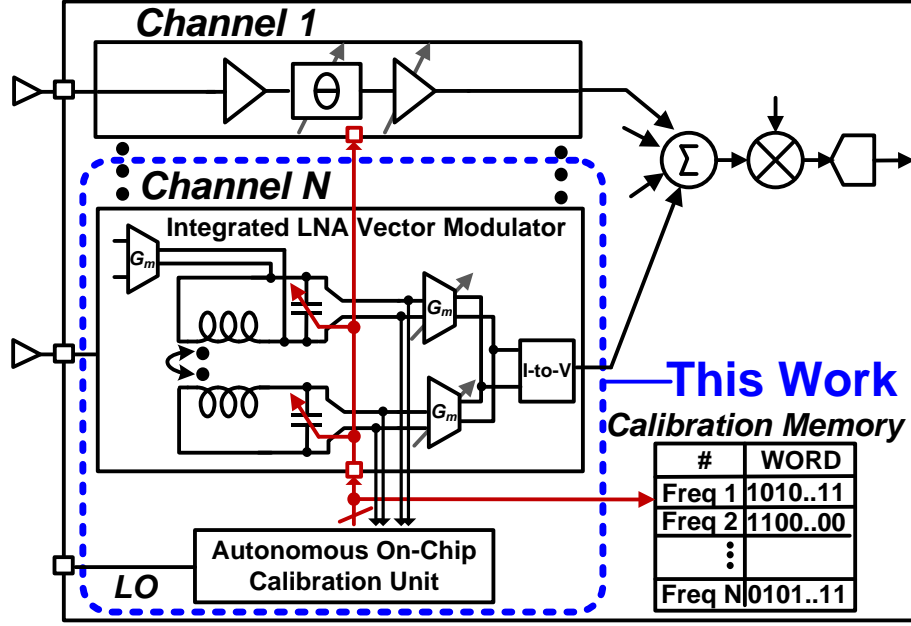
Figure 5.2   Block diagram of an *N*-channel phased-array receiver with proposed integrated LNA-VM and on-chip calibration.

complex-mixing based Cartesian combining. However, a drawback of this approach is the constraint on mixer linearity: the mixers are exposed to large spatial interferers. This is in contrast to quadrature-hybrid based architectures as RF combining before complex downconversion ensures the interferer is heavily attenuated before reaching the mixer.

In this work, we propose an ultra-compact merged LNA-VM [10] where quadrature generation is absorbed into the gain stage of an LNA (Figure 5.1(d)). In contrast with previous RF phase shifters, the proposed scheme is compact, frequency-reconfigurable and narrowband. Emerging 28 GHz 5G standards stipulate channel bandwidths below 500 MHz thereby making frequency-tunable low fractional bandwidth designs like ours both viable and desirable [123]. An on-chip calibration unit is also implemented to autonomously update a digitally-controlled capacitance bank in the LNA for quadrature operation at a desired frequency. As shown in Figure 5.2, the overhead for this calibration is small: in a phased-array chip, only one such calibration unit would be required irrespective of the number of channels where the I/Q outputs taken from a single

channel's LNA generates the calibration code shared by all channels. In addition, the proposed scheme enables compact differential quadrature generation (I+/I-/Q+/Q-): this is contrast with differential architectures which resort to the use of a couple of quadrature hybrids for differential I/Q generation [119] or elaborate passive structures [127].

5.2 Wideband vs. Narrowband Vector Modulator

The operating bandwidth (BW) of a VM can be defined by the frequency range over which sufficiently low quadrature phase error (QE) is maintained. To calculate the tolerable QE over our required bandwidth (~ 0.4-0.5 GHz bandwidth), it is first important to understand and quantify the impact of QE on a phased-array system. In this context, two key array performance parameters – null-depth/sidelobe-suppression and main-lobe array-gain degradation can be examined to specify how much QE is tolerable over a target BW.

As shown in Figure 5.1(a), after RF combining, the combined output of an N-element array's array factor can be written as $F(\theta) = \sum(X_n - jY_n)$, where X_n and Y_n are the Cartesian expansions of the nth element vector. This is represented as a function of the incident angle θ, as the phase shifters have to be respectively set to phase shifts of n$(2\pi/\lambda)(\lambda/2)\sin(\theta)$, to achieve peak directivity at angle θ in a linear N-element array with $\lambda/2$ interelement spacing. Note that θ=0 corresponds to broadside in this analysis. However, if we now assume a global quadrature error δ (same QE across all elements), then the combined signal can be written as [119]:

$$
\begin{aligned}
F(\theta,\delta) &= \sum(X_n - je^{j\delta}Y_n) \\
&= \frac{(e^{j\delta}+1)}{2}\left[\sum(X_n - jY_n)\right] + \frac{(e^{j\delta}-1)}{2}\left[\sum(X_n + jX_n)\right] \\
&= \frac{(e^{j\delta}+1)}{2}F(\theta) + \frac{(e^{j\delta}-1)}{2}F_{im}(\theta)
\end{aligned}
\tag{5-1}
$$
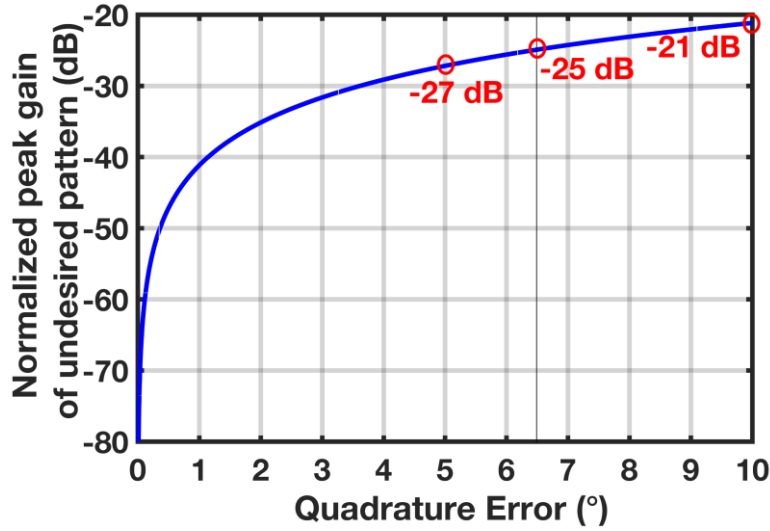
Figure 5.3 Normalized peak gain of undesired pattern plotted against quadrature error (MATLAB simulations of an 8-element array).

Here, $F(\theta)$ represents the desired beam pattern, while $F_{im}(\theta)$ represents the undesired beam pattern, where the resulting beam is represented as a summation of the weighted desired and undesired patterns, with the respective weights governed by the QE δ. The undesired beam pattern $F_{im}(\theta)$ is the conjugate of $F(\theta)$: in other words, $F(\theta)$ results in a peak directivity at $-\theta$ (the image angle), while the desired beam pattern results in a peak directivity at θ (the incident angle). Now, if we assume that the incident angle is θ_0 and a null exists at the image angle $-\theta_0$, we then have:

$$F\left(\theta,\delta\right)\big|_{\theta=-\theta_0} = \frac{(e^{j\delta}+1)}{2}F\left(-\theta_0\right)+\frac{(e^{j\delta}-1)}{2}F_{im}\left(-\theta_0\right)$$

$$= \frac{(e^{j\delta}-1)}{2}F_{im}\left(-\theta_0\right), \text{ if } F\left(-\theta_0\right)=0 \tag{5-2}$$

It is evident from (5-2) that for a finite δ, a finite value of $F(\theta,\delta)$ will result at $-\theta_0$ due to the non-zero weighting factor $0.5(e^{j\delta}-1)$. The presence of $F_{im}(\theta)$ in (5-1) therefore results in a poorer peak-to-null ratio in the presence of a quadrature error, due to null degradation at the image angle. Note that if $\delta=0$ (no quadrature error) or is so small that $e^{j\delta}\approx1$, $F(\theta,\delta)$ at $\theta=-\theta_0$ is close to zero implying
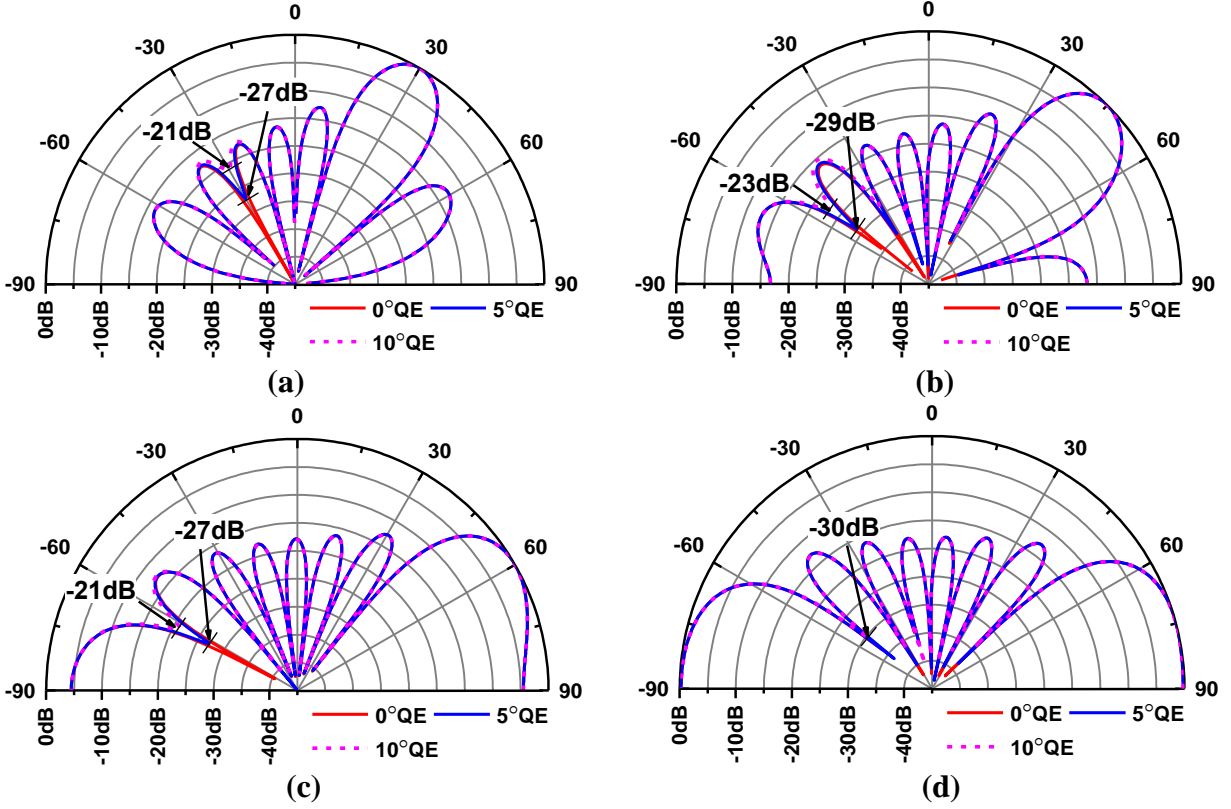
Figure 5.4 MATLAB simulations of the impact of quadrature error (QE) on mainlobe, sidelobes and nulls in the beam pattern of a linear 8-element array (interelement spacing: λ/2) for incident angles, (a) 30°, (b) 45°, (c) 60°, and (d) 75°.

negligible null degradation. Thus, to keep the null at least R dB below the main desired lobe, we set the weights such that [119]:

$$20\log\left|\frac{e^{j\delta}+1}{2}\right| - 20\log\left|\frac{e^{j\delta}-1}{2}\right| = R$$

$$\Rightarrow R(\text{in dB}) = 10\log\left(\frac{1-\cos\delta}{1+\cos\delta}\right), \quad \delta=\text{Quadrature Error} \tag{5-3}$$

This is plotted in Figure 5.3 which shows the peak gain of the undesired pattern R against quadrature error based on (5-3). It is seen that 6.4° QE ensures that the undesired pattern is at least 25 dB below than the desired beam, and will be used to define the tolerable QE (for defining bandwidth) of a narrowband VM in this work. Figure 5.4 shows the MATLAB simulations of an 8-element uniform linear phased-array (directed towards 30°, 45°, 60°, and 75° angles w.r.t normal)
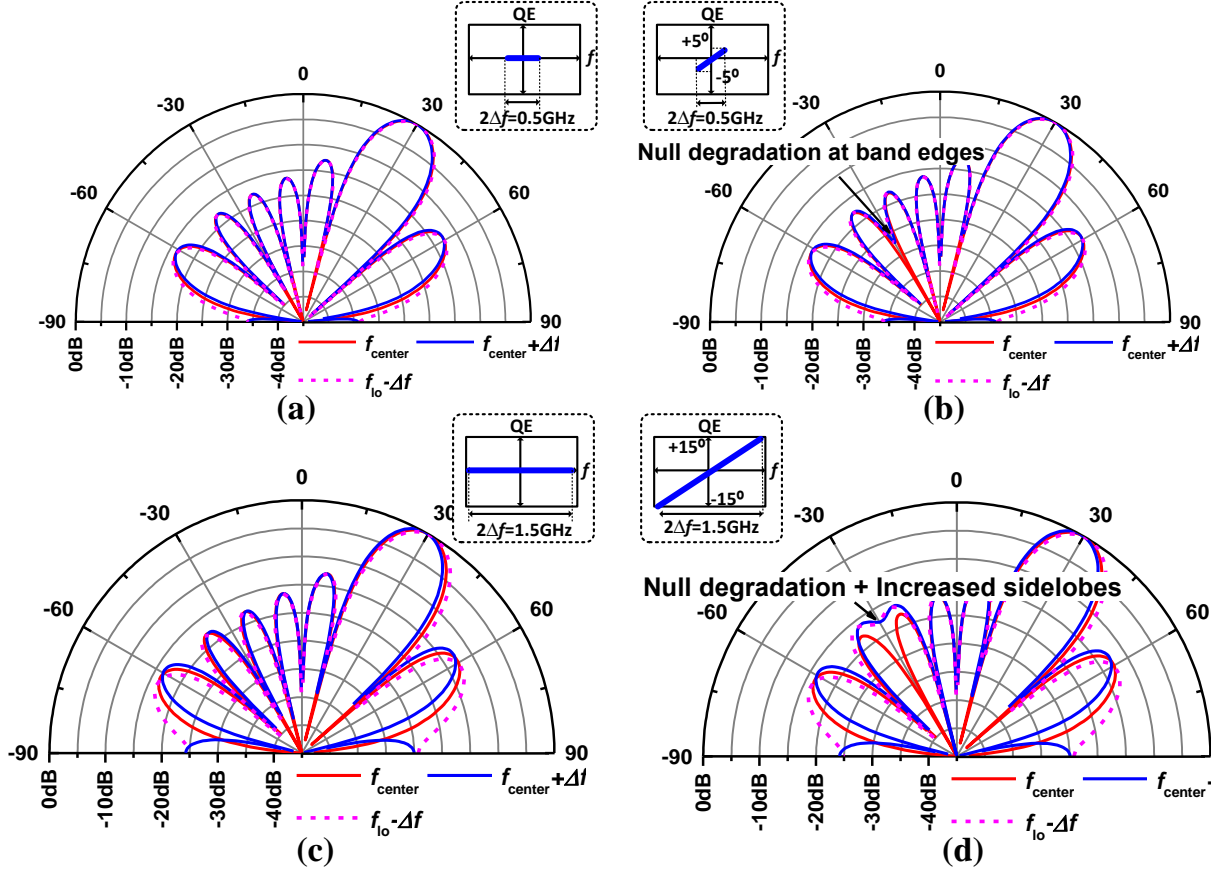
Figure 5.5 MATLAB simulations of linear 8-element array: (a) wideband VM with zero QE over 0.5GHz bandwidth, (b) narrowband VM with ±5° QE over 0.5 GHz bandwidth, (c) wideband VM with zero QE over 1.5GHz bandwidth, and (d) narrowband VM with ±15° QE over 1.5 GHz bandwidth. Incident angle is 30° (with respect to normal).

and simulated for 0°, 5° and 10° QE. It is seen that severity of null degradation is highest for $\theta=30°$ and $\theta=60°$, where as predicted by Figure 5.3, the null at the image angle gets degraded by -27 dB for and -21 dB for QEs of 5° and 10° respectively. Since $\theta=30°$ represents the worst-case peak-to-null ratio, subsequent simulations only consider $\theta=30°$.

Figure 5.5 compares the performance of ideal wideband vector modulators (ideal quadrature hybrid with zero QE over bandwidth) with that of narrowband vector modulators (finite QE over bandwidth, with QE assumed to be linear with frequency offset). We show later that the designed LNA-VM suffers from a QE that is nearly linear with frequency offset around the center frequency, and is therefore a reasonable assumption for MATLAB simulations of this analysis. For ±5° QE

over a 0.5 GHz bandwidth, we observe that the both the wideband and narrowband cases demonstrate similar main lobe and side lobe levels, with negligible peak-array-gain degradation at the band-edges due to beam squinting. The only observable impact is the null degradation at the image angle at the band edges (where the QE is maximum): this is expected from our previous analysis. Now, if ±15º QE is assumed over a much larger 1.5 GHz bandwidth, both the pointing error and gain reduction due to beam squinting are still negligible for both the narrowband and wideband cases; however, the narrowband design has significant unwanted array gain around the image angle. It can therefore be inferred that a narrowband vector modulator design, supporting greater 400-500 MHz of channel BW (set by 5G requirements) with ~±5-6º QE can be an attractive alternative to wideband quadrature hybrids as it can achieve similar beam patterns except for null degradation at the image angle at band edges which reduces its ability to reject wideband interferers incident at the image angle. Furthermore, it is easy to see that the narrowband paradigm being proposed in the work becomes much more appealing if the design is ultra-compact and the center frequency at which the quadrature is generated can be tuned over a wide frequency range to support multiple 5G channels. Therefore, a compact, narrowband frequency-tunable design with ~0.5 GHz bandwidth are the design targets pursued in this work.

5.3 Coupled-Resonator Quadrature Generation

As demonstrated in the previous chapter, mm-wave LNA designs that use loosely-coupled (low coupling coefficient k) LC resonators loads have become popular to achieve a wideband frequency response [89]. The frequency response of Z_{11} of a coupled resonator has a real zero, a complex zero and two complex pole pairs, while the Z_{21} response has a zero and the same two complex pole pairs. Figure 5.6 shows sketches of Bode phase plots of Z_{11} and Z_{21}, while Figure 5.7 shows the simulated Z_{11} and Z_{21} phase responses of coupled-resonator with symmetric LC tanks and their
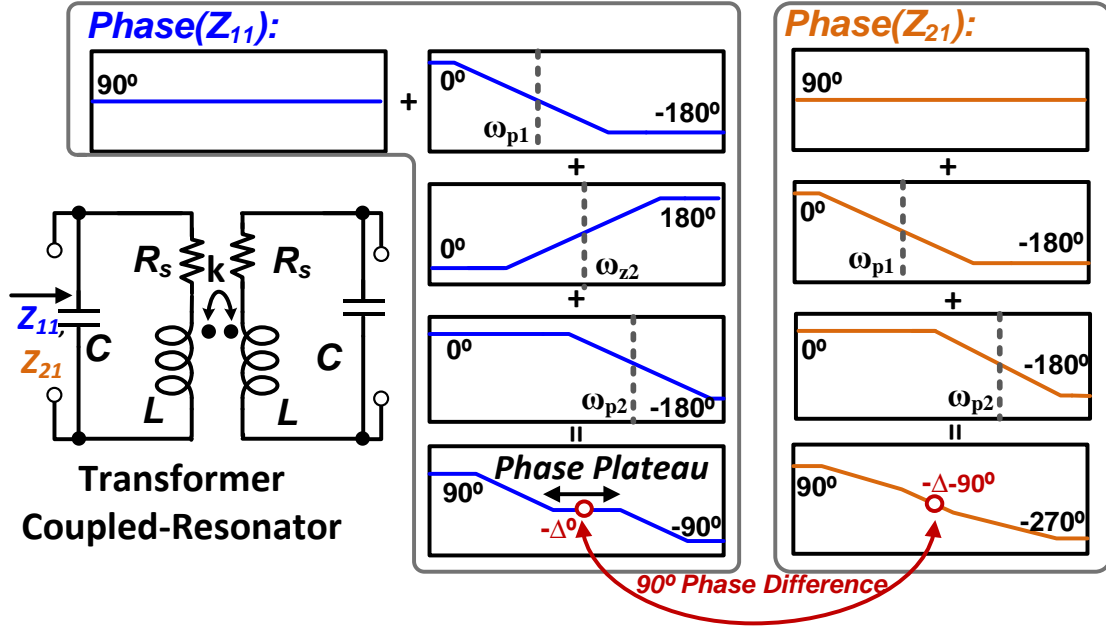
Figure 5.6 Phase plots of Z_{11} and Z_{21} of a low-k transformer coupled resonator.

phase difference for different values of kQ for $Q=5$ and $Q=10$. We observed that imposing a $kQ=1$ (critical coupling condition for maximally flat response [93]) constraint created a 'phase plateau' [124] in the Z_{11} phase response due to the combination of the phase contributions from the complex pole pairs and the complex zero. On the other hand, the Z_{21} phase response is roughly linear with frequency (since the Z_{21} phase changes from $90°$ to $-270°$, it approaches $-90°$ around the center frequency). Therefore, as shown in Figure 5.6, there always exists a frequency where the Z_{21} and Z_{11} phase responses are close to quadrature.

Since both Z_{11} and Z_{21} of a coupled-resonator can be used as LNA loads, we can exploit this property to generate the I/Q signals required for VM based Cartesian complex-weighting Figure 5.2). The width of the Z_{11} phase plateau as well as the rate of Z_{21} phase change can be related to the Q factor (the quality factor of the poles and zeroes are proportional to Q) [124]. In Figure 5.7(a), we see that choosing $Q=5$ and $k=0.2$ ($kQ=1$) resulted in better than $90°±5°$ phase difference over a 0.6 GHz range. On the other hand, choosing $Q=10$ dropped the range to 0.25 GHz. Thus, while a higher value of Q would be beneficial to achieve a higher LNA gain, it also reduces the
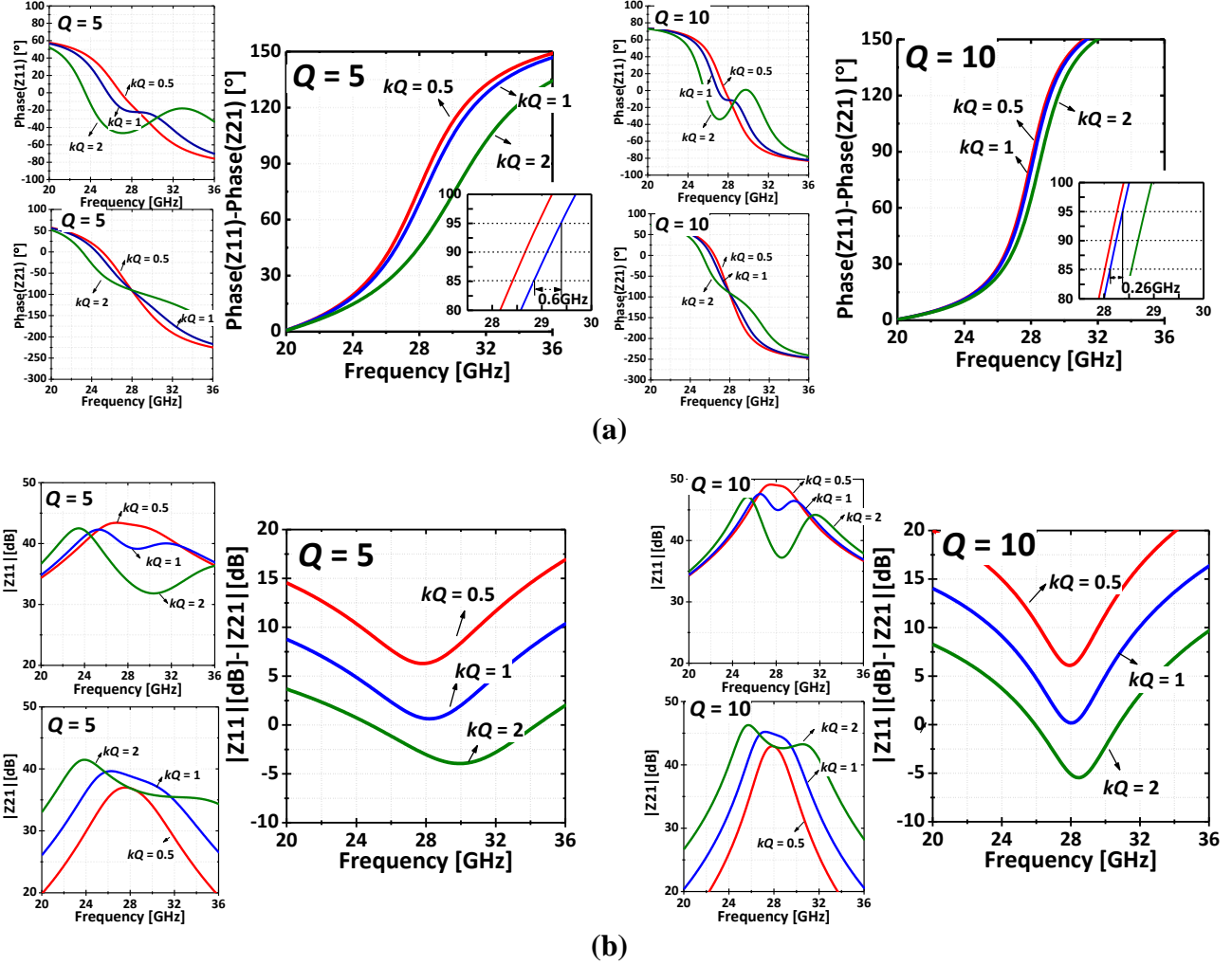
Figure 5.7 Variation of Z_{11} and Z_{21} (a) phases and (b) magnitudes for different 'kQ' values for two different Q values, 5 and 10 ($L = 200$ pH, $C = 161.6$ fF).

frequency span over which the Z_{21} and Z_{11} phase responses are close to quadrature. It is also observed in Figure 5.7(b) that the magnitude difference between Z_{21} and Z_{11} is small at the quadrature frequency only when kQ=1 (maximally flat condition). It should be noted that small amplitude imbalance is necessary to ensure expected VM performance with low RMS gain and phase errors. Thus, $kQ \approx 1$ with $Q \approx 5$ was chosen as our design point. Figure 5.7(b) illustrates the Z_{21} and Z_{11} magnitude responses under this constraint, where the amplitude imbalance was observed to be between 0.64 to 1.2 dB over a 0.6 GHz bandwidth (phase difference was 90°±5°). A
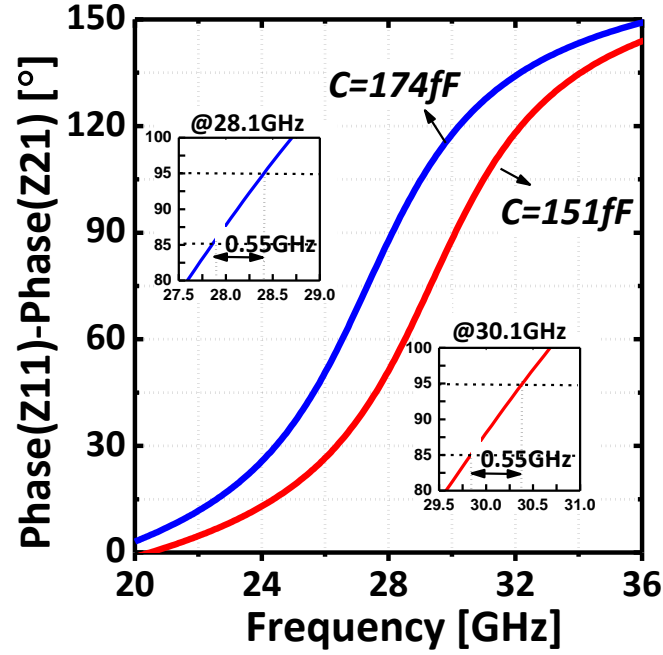
Figure 5.8 Z_{11} and Z_{21} phase difference for two different C values, 151 fF and 174 fF ($L = 200$ pH)

major benefit of this scheme is frequency tunability: digitally-switched capacitor banks can be

employed in the coupled-resonator tanks to tune the quadrature frequency over a wide range. In

Figure 5.8, it is observed that when the simulation of Figure 5.6(a) is repeated with two different

values of C, the quadrature frequency shifted by 2 GHz (from 28.1 GHz to 30.1 GHz) while the

$90°\pm5°$ range remained nearly constant at 0.55 GHz (this simulation assumes no change in the tank

quality factor with change in C).

5.4 Digitally-Calibrated Merged LNA Vector Modulator

The proposed method of quadrature generator using a coupled resonator load was used to

implement a frequency-reconfigurable merged LNA vector modulator (LNA-VM), designed in a

65-nm CMOS process. Figure 5.9 shows the block diagram and chip photograph of the merged

LNA-VM test chip. The digitally-controlled capacitance in the LNA capacitance bank was updated
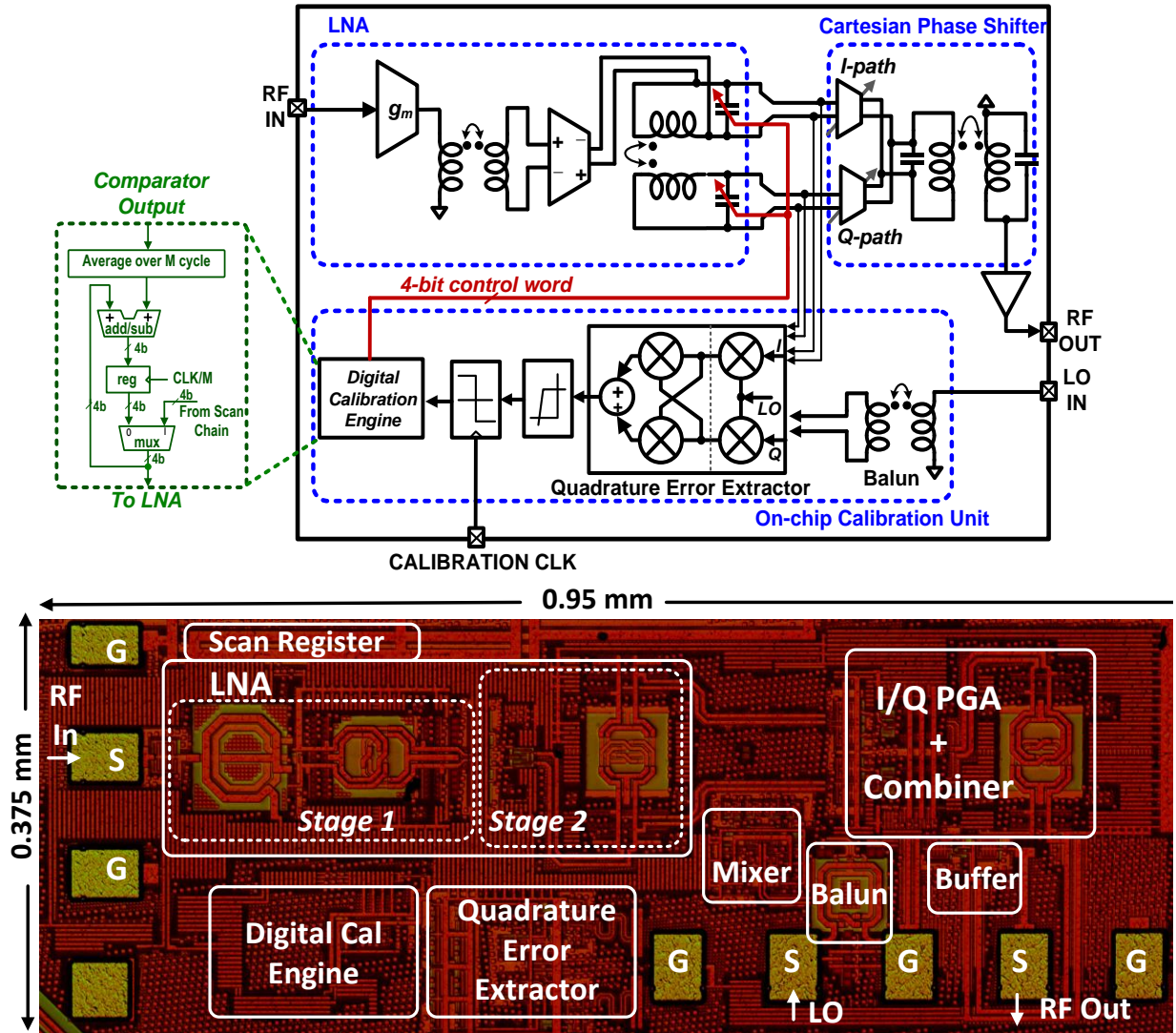
Figure 5.9 Block diagram and die photo of the merged LNA-VM chip in 65 nm CMOS.

by an on-chip calibration unit to obtain quadrature outputs from the LNA at a desired frequency. The overall design comprised the merged LNA-VM (LNA with the Cartesian phase shifter), a quadrature error extractor, and a digital calibration engine. In the following sub-sections, the design of each component of the LNA-VM is discussed.

5.4.1 Merged LNA-VM

Figure 5.10 shows the circuit schematic of the merged LNA-VM. The LNA comprises a g_m-boosted common-gate (CG) first stage followed by a common-source (CS) second stage. Passive
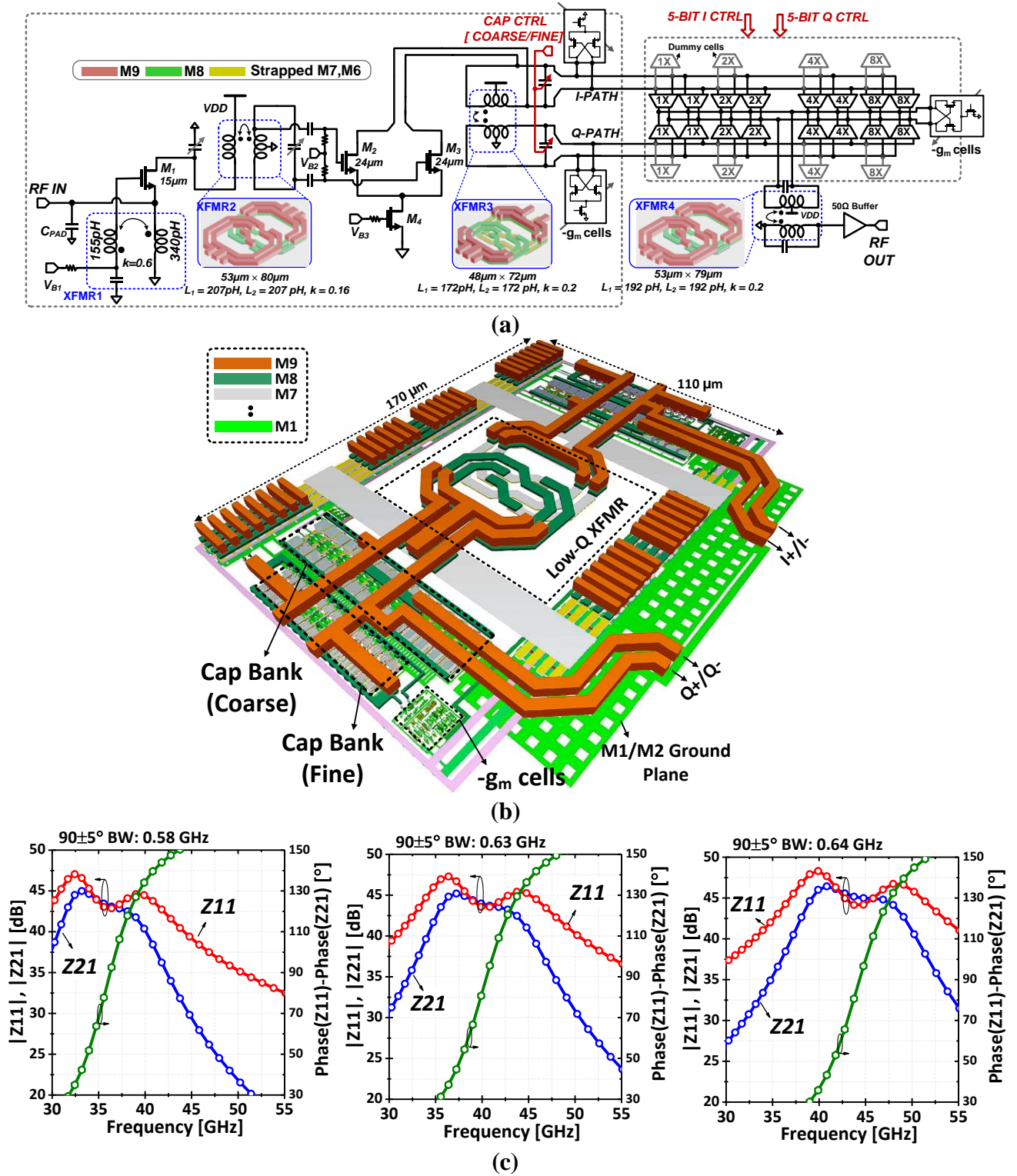
Figure 5.10 (a) Circuit schematic of the merged LNA-VM. (b) Layout of low-*k* coupled resonator load. (c) *Z21* and *Z11* response and phase difference of the low-*k* coupled resonator load under three different capacitance settings.

transformer-based (*XFMR1*) g_m-boosting [125] improves voltage gain, and a low-k coupled resonator (*XFMR2*) provided single-ended to differential conversion. *XFMR1* was designed to have a turns ratio $n=1.5$ ($=\sqrt{L_2/L_1}$) and $k=0.6$, thereby resulting in an effective turns ratio of $nk=1.05$, and boosting the effective transconductance G_m to $g_m(1+nk)$. The low-k coupled resonator in stage 2 (*XFMR3*) is used for quadrature generation where a portion of the layout was laid out in lower-level metals to reduce Q and satisfy the $kQ\approx1$ design requirement. Digitally-switched metal-oxide-metal capacitor array banks were employed to enable frequency tuning. Coarse and fine frequency tuning (over 30fF and 8fF respectively) was achieved using 4-bit control words. Due to the use of compact two-turn inductors, the entire LNA core area was only 0.48 mm $\times$ 0.18 mm or 0.086 mm^2. Negative resistance cells were added to the LNA I/Q outputs to enable post-fabrication tank quality-factor control. The use of negative resistance cells helped to counteract the the tank quality factor degradation due to switching on of MOM capacitor banks. The entire layout of the low-k coupled resonator stage is shown in Figure 5.10(b), and its standalone Z_{11}/Z_{21} characteristics (without loading from the LNA transconductor and succeeding stage) at three different capacitance settings are shown in Figure 5.10(c). With the additional loading from the transconductor and succeeding PGA stages, the LNA was designed to be tunable over 3 GHz with ~10 dB peak voltage gains at the I/Q outputs (Figure 5.11(a)), while consuming 15 mA from a 1.1 V supply. Post-layout simulations showed that the first stage had a minimum noise figure (NF) of 4 dB, while the overall LNA NF was ~5.5-5.9 dB (Figure 5.11(a)). LNA's input-referred 1-dB compression point was simulated to be -8 dBm. Note that the LNA gain can be improved by using larger (single-turn) inductors with higher-Q in *XFMR2* (for example, as implemented in [118]): however, this trade-off between gain and area was not exercised in this
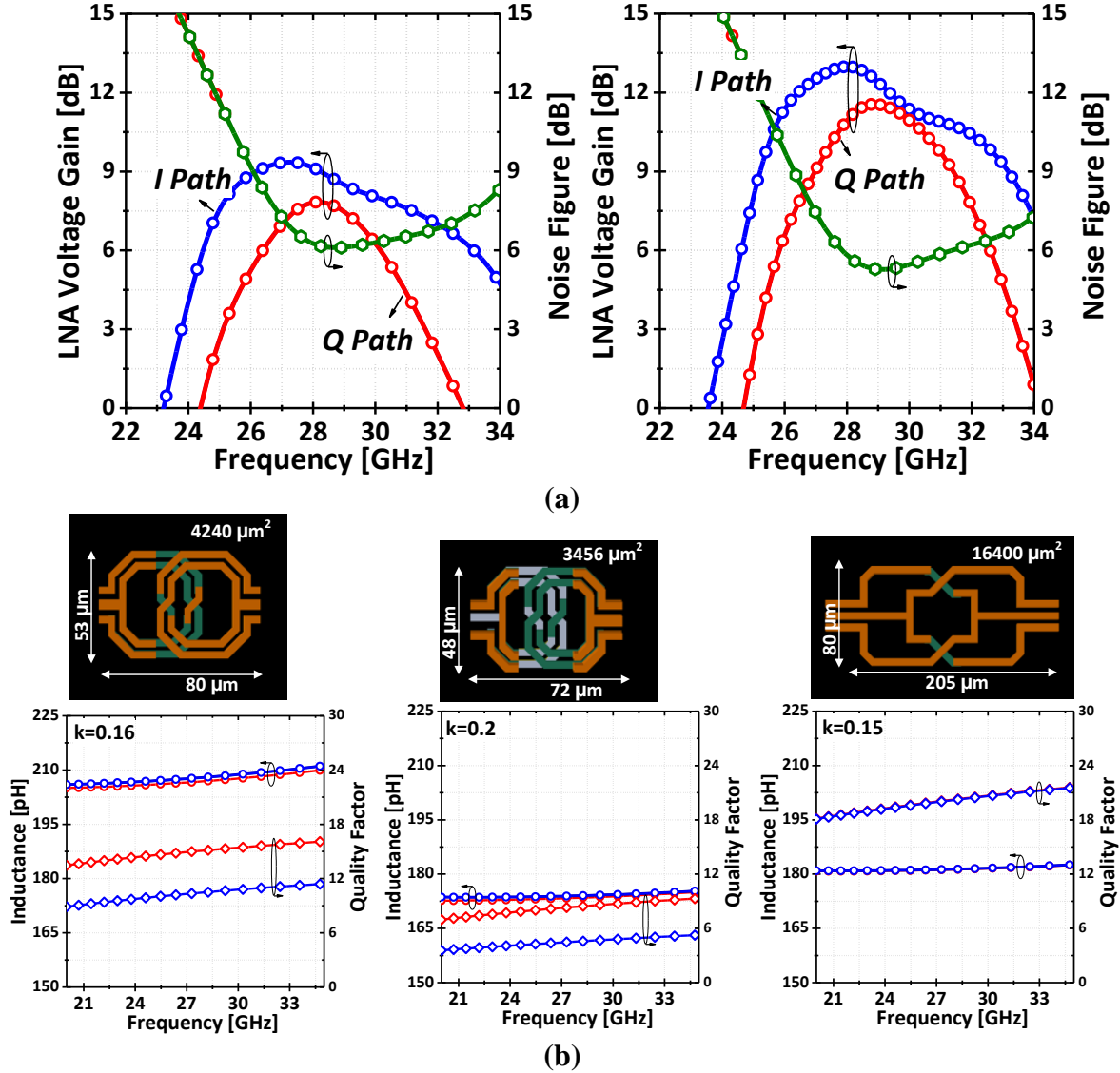
Figure 5.11 (a) Simulated LNA voltage gain with quadrature frequency at 28 GHz and 30 GHz respectively. (b) EM-simulated inductance and quality factor of transformer coils (a) *XFMR2* (b) *XFMR3*, and (c) a low-*k* high-*Q* transformer design adopted from [110] with similar *k* as *XFMR2*.

implementation. As can be seen in Figure 5.11(b), use of high-*Q* coils in the transformer improved

the quality factor by over 25%, when compared to *XFMR2*.

The two LNA outputs are followed by 5-bit I and Q- path PGAs with their output currents

combined using a low-*k* coupled resonator load (*XFMR4*). The LSBs of the PGA control word

control a binary-weighted array of unit G_m-cells while the MSB determines the sign (turning on

one of the two identical but oppositely connected unit G_m-cell). To ensure that a constant input capacitance is presented to the LNA I/Q outputs over all possible VGA gain settings, dummy G_m-cells were inserted [85], [118]. Negative resistance cells were added to ensure that the output resistance of the G_m-cells is constant – this is necessary to avoid phase and gain distortion from a varying PGA output conductance. The I/Q VGA current settings were independently controlled, thereby enabling tuning of the gain ratio of the two VGAs to further reduce any I/Q gain magnitude mismatch.

5.4.2 Quadrature Error Correction

The quadrature error (QE) between the LNA I/Q outputs needs to be detected, and the error fed into a calibration engine to update the LNA capacitance word. A quadrature error extractor (see Section 5.4.3) was designed to convert the QE into a voltage. As shown in Figure 5.9, a comparator followed the QE extractor to extract the sign of the error voltage. A digital calibration engine following the comparator averages the comparator output over M cycles of the calibration clock (M=32 or 64) to increase or decrease the LNA coarse word such that the QE is minimized. To understand the calibration flow, as an example, consider that the initial state of the coarse word is set for a quadrature frequency for 27 GHz while the desired frequency of operation is 28 GHz. As such, also assume that the I/Q phase difference at the LNA output is 70°. This large QE error would result in a comparator output of -1, which would then direct the digital engine to decrement the coarse control word. After this update, the quadrature frequency would move to a frequency higher than 27 GHz (quadrature frequency shifts by ~150 MHz per LSB increase of coarse word), and the I/Q phase difference would be closer to 90° than the initial state. This algorithm would continue until the QE reduces below one LSB phase-step, at which point the comparator output would start toggling between +1 and -1 every alternate calibration cycle. This will be detected by the digital logic, and the calibration would be terminated. It is straightforward to extend this calibration
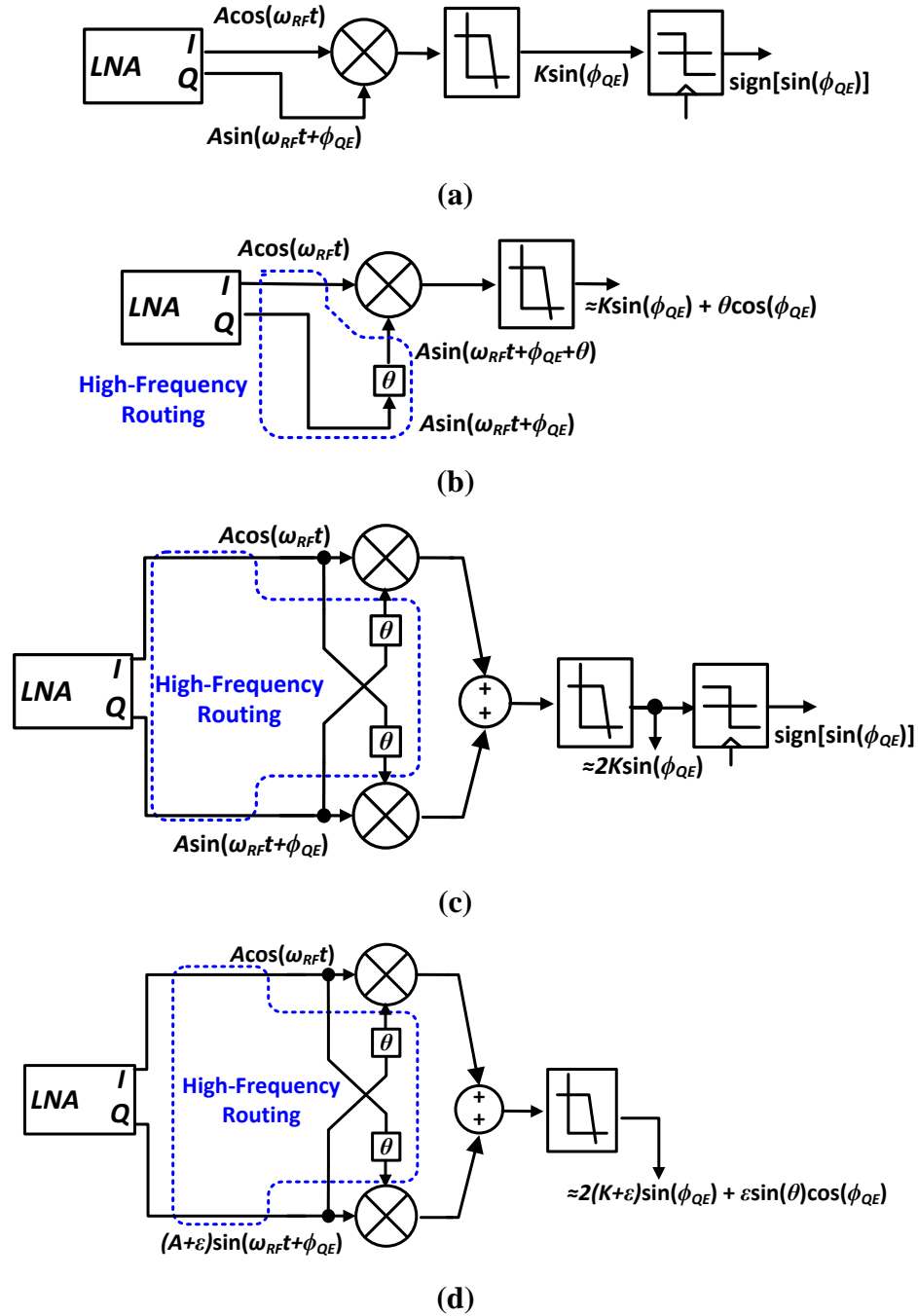
Figure 5.12 (a) QE extraction using a single mixer. (b) QE extraction using a single mixer in presence of external phase mismatch (θ). (c) QE extraction using a cross-coupled mixer pair. (d) QE extraction using cross-coupled mixer pair in presence of amplitude mismatch.

technique to include the LNA fine word to reduce the calibrated QE error to even smaller values; however, this scheme was not implemented in the present design.

5.4.3 Quadrature Error Extractor

Consider the challenge of extracting the QE (ϕ_{QE}) between a pair of quadrature signals (at a frequency, say f_{RF}, which can then be represented as $I \equiv A_I \cos(2\pi f_{RF})$ and $Q \equiv A_Q \sin(2\pi f_{RF} + \phi_{QE})$ respectively). One straightforward way of doing this is to multiply the quadrature signals by feeding them to the RF and LO port of a mixer (Figure 5.12(a)), whose output $f(\phi_{QE})$ can then be represented as:

$$f\left(\phi_{QE}\right) = K \cos(2\pi f_{RF} t) \sin(2\pi f_{RF} t + \phi_{QE})$$
$$= (K/2)\left\{ \sin(\phi_{QE}) + \underbrace{\sin(2\pi\left(2f_{RF}\right)t + \phi_{QE})}_{\text{removed by LPF}} \right\} \qquad (5\text{-}4)$$
$$= (K/2) \sin(\phi_{QE}).$$

Here, $A_I = A_Q = A$ (no amplitude mismatch), and K is proportional to A. Thus, $f(\phi_{QE})$ is an odd function w.r.t ϕ_{QE}, and monotonically increasing with QE (here, $-\pi/2 < \phi_{QE} < \pi/2$). Thus, the sign of QE can be extracted by slicing the mixer output with a comparator. If comparator offset is assumed to be 0, then the comparator output can be written as:

$$OUT = \text{sgn}\left\{ (K/2)\sin(\phi_{QE}) \right\} = \text{sgn}\left\{ \phi_{QE} \right\}. \qquad (5\text{-}5)$$

Since we only care about the sign of ϕ_{QE}, the digital calibration engine following the comparator would work correctly. However, now consider the situation in Figure 5.12(b), where there is an additional phase mismatch (θ) between the RF and LO port of the mixer. It should be noted that this external phase mismatch is unavoidable due to unequal loading at the RF and LO ports, and layout-induced delay mismatches, which are exacerbated at mm-wave frequencies. This can be understood by considering that a given delay mismatch would lead to larger phase mismatches at higher frequencies [126]. (5-4) can now be written as:

$$f\left(\phi_{QE},\theta\right)=K\cos(2\pi f_{RF}t)\sin(2\pi f_{RF}t+\phi_{QE}+\theta)$$

$$=(K/2)\left\{\sin(\phi_{QE}+\theta)+\underbrace{\sin(2\pi\left(2f_{RF}\right)t+\phi_{QE}+\theta)}_{\text{removed by LPF}}\right\}$$

$$=(K/2)\sin(\phi_{QE})\cos(\theta)+(K/2)\cos(\phi_{QE})\sin(\theta)$$

$$\approx(K/2)\sin(\phi_{QE})+\underbrace{(K/2)\cos(\phi_{QE})\sin(\theta)}_{\text{offset}}.$$

(5-6)

Thus, there is now a varying offset present in the QE extractor's output, which will compromise the correct functionality of the calibration algorithm. We also observed thCaat due to the parasitic capacitance stealing away a portion of the RF current at the drain of the transconductor in the active cell mixer used in our design, a large offset was already present even in the absence of any layout-induced mismatches. This offset could be minimized by resonating out the capacitance with an inductor [42] but this would increase the layout area significantly. To eliminate the effect of this external phase mismatches, a cross-coupled mixer pair can be employed (Figure 5.12(c)), and their outputs summed together such that the input to the comparator can now be written as:

$$f\left(\phi_{QE}\right)=K\cos(2\pi f_{RF}t)\sin(2\pi f_{RF}t+\phi_{QE}+\theta)+K\cos(2\pi f_{RF}t+\theta)\sin(2\pi f_{RF}t+\phi_{QE})$$

$$=(K/2)\left\{\sin(\phi_{QE}+\theta)+\sin(\phi_{QE}-\theta)\right\}$$

$$=K\sin(\phi_{QE})\cos(\theta)\approx K\sin(\phi_{QE}).$$

(5-7)

The output of the QE extractor is again an odd function of ϕ_{QE}, and the calibration can work correctly. For the same reason, the effect of the parasitic capacitance will also be cancelled out as it would now result in similar phase shifts in both the I and Q paths. However, in the present calibration scheme, amplitude mismatches between the I/Q signals will be present at the start of the calibration operation if the initial LNA cap settings are far from the required value. Unfortunately, it was observed that in the presence of amplitude mismatch (ε) (Figure 5.12(d)), an offset would again be present in the QE extractor output, which can be written as:
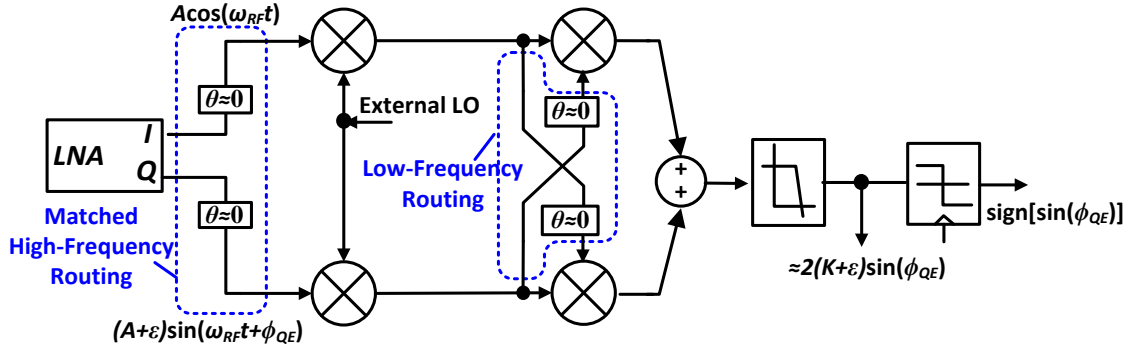
Figure 5.13 Proposed QE extractor robust against phase and amplitude mismatches.

(a)

(b)
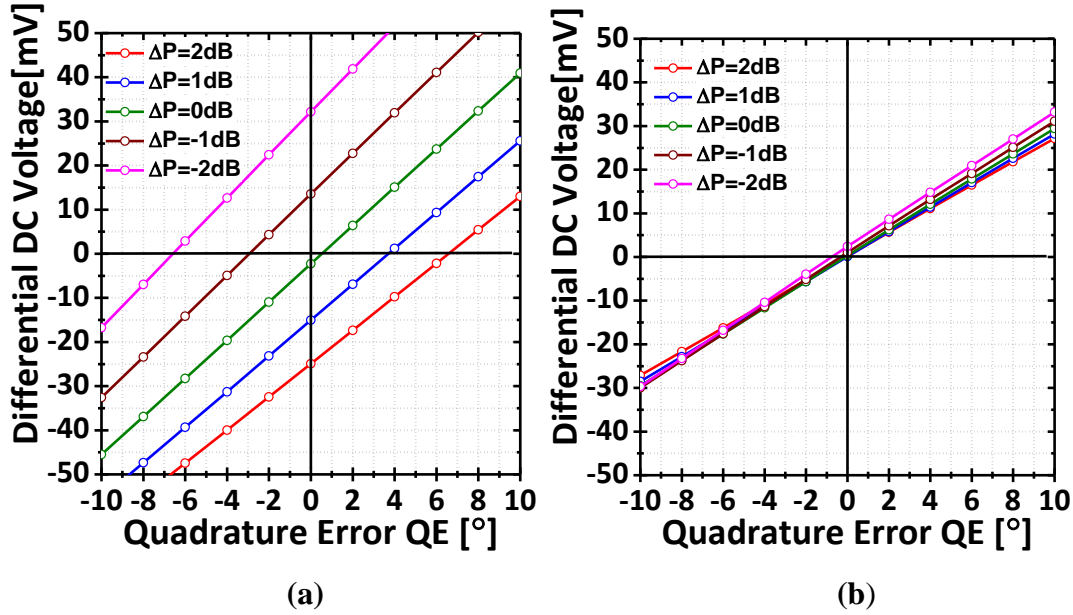
Figure 5.14 Differential DC voltage output of the QE extractor plotted with QE in the presence of amplitude mismatch (a) without, and (b) with initial downconversion.

$$f\left(\phi_{QE},\theta,\varepsilon\right) \approx 2(K+\varepsilon)\sin(\phi_{QE}) + \underbrace{\varepsilon\sin(\theta)\cos(\phi_{QE})}_{\text{offset}} \tag{5-8}$$

(5-8) is interesting because it reveals that if we can reduce θ to 0, then the problematic offset disappears. Then, the QE output again reduces to an odd function of ϕ_{QE}, and a correct calibration operation is possible. In Figure 5.13, our proposed method of QE extraction is shown. In this scheme, the LNA outputs are first downconverted to a low IF frequency (~0.5 GHz) using
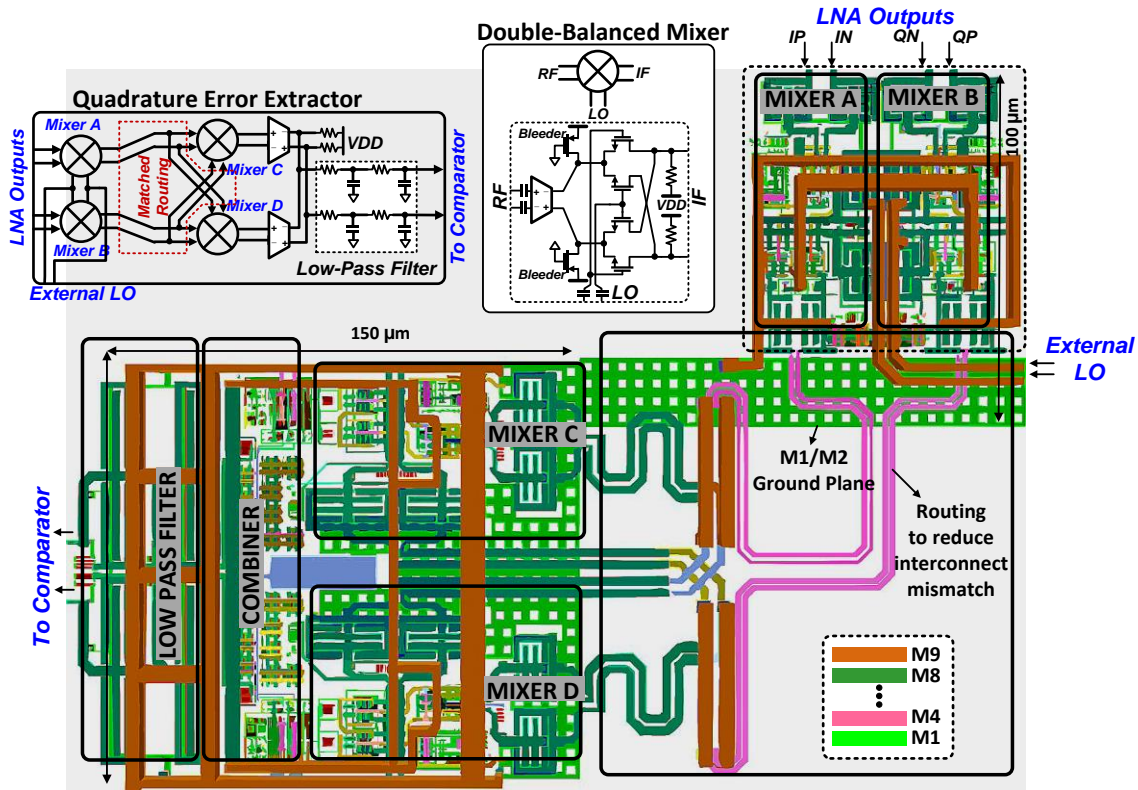
Figure 5.15 Schematic and layout of the proposed quadrature error extractor.

a mixer pair driven by an external LO signal. The downconverted outputs are then fed to the cross-coupled mixer pair. Initial downconversion ensures there is only a small phase mismatch due to routing or different port loadings (since delay mismatches create low phase mismatches at low frequencies). Since the cross-coupled mixer pair routing sees a low-frequency signal, layout-dependent mismatches are reduced. Therefore, amplitude mismatches between the I/Q signals will not compromise the integrity of the calibration operation. It is important to note that we still use a cross-coupled pair after the initial downconversion to improve robustness to any residual phase mismatch θ, which will inevitably remain. In Figure 5.14, the output of the QE extractor is plotted against QE in the presence of amplitude mismatch (upto ± 2 dB) with and without initial downconversion. It is evident the effect of the amplitude mismatch on the QE extractor's output is significantly reduced due to the downconversion.
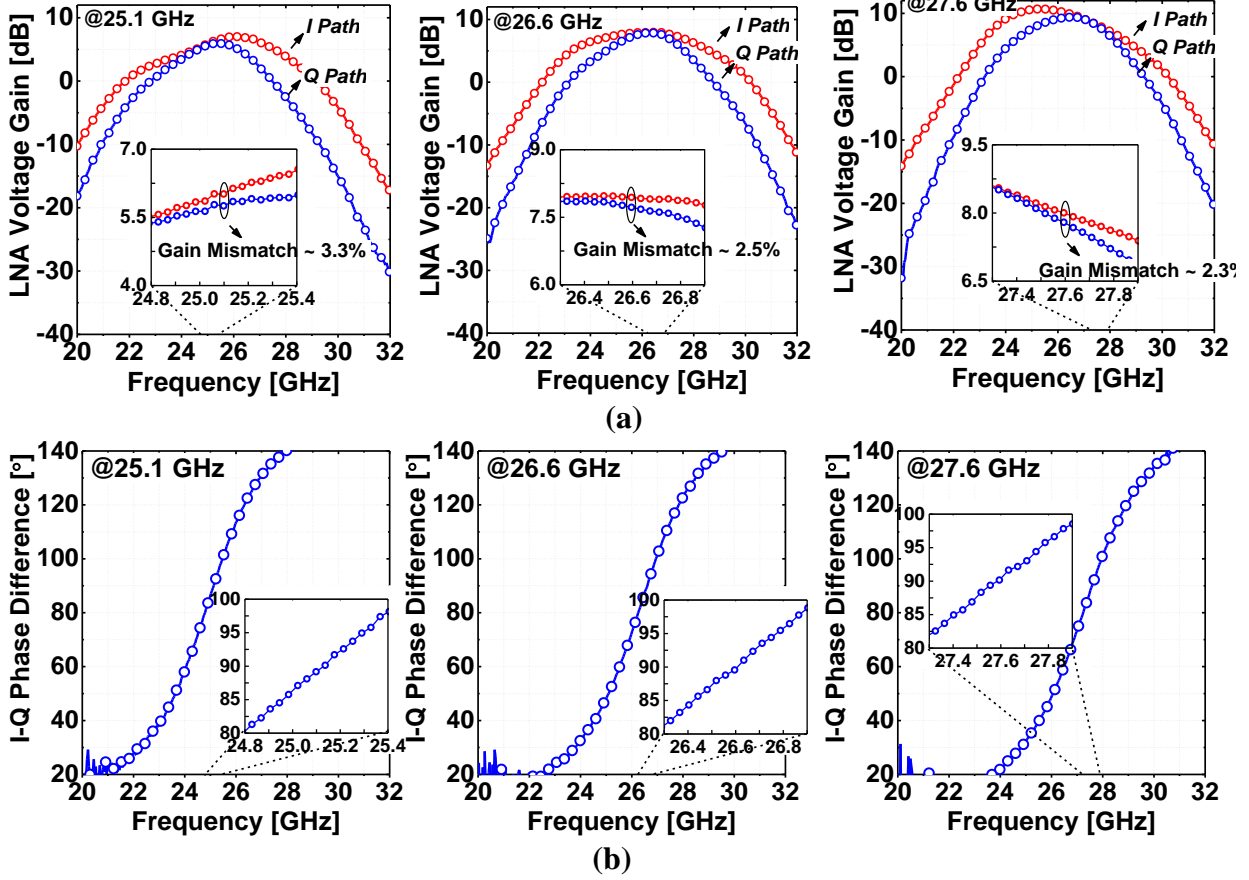
Figure 5.16 Measured (a) LNA voltage gain, and (b) I/Q phase difference of the merged LNA-VM at three different frequencies.

The schematic and the layout of the proposed designed QE extractor is shown in Figure 5.15. The routing interconnects were carefully laid out to reduce mismatch. The use of additional mixers for downconversion (and the requirement of an external LO signal) increases the overhead: however, it is a necessary trade-off to ensure robustness of the calibration operation. In addition, as shown in Figure 5.2, the overhead for the proposed calibration scheme is small. In a complete phased-array chip with multiple elements, only one such unit would be required where the I/Q outputs from a single channel's LNA can be used to generate the calibration code, stored in the on-chip memory [116], and then shared by all the channels.

5.5 Measurement Results

The measured LNA voltage gain, and the I- and Q- path phase difference at three different settings of the LNA's capacitance word (quadrature frequency = 25.1 GHz, 26.6 GHz, and 27.6 GHz respectively) is summarized in Figure 5.16. The LNA voltage gain was calculated from the measured S-parameters ($=S_{21}/(1+S_{11})$, with $S_{11,dB} \approx$-10 dB), and the simulated loss of the PGA and buffer was de-embedded from the measurement. The voltage gain was measured to be between 5.8 dB and 8 dB across the entire frequency tuning range. Compared to simulations, a reduction in the gain, as well as the shift of the frequency range to lower frequencies was observed. This might be attributed to the routing interconnects to the quadrature error extractor, which were not carefully accounted for during the design simulations. The I/Q phase difference was measured by successively turning on only the I-path and Q-path PGAs, measuring the calibrated two-port S-parameters, and then subtracting the two S_{21} phases so obtained. The operating bandwidth (QE<±6.4°) at the three frequencies was measured to be 0.43 GHz, 0.47 GHz and 0.45 GHz respectively. The LNA consumed 16 mA, while the Cartesian phase shifter block (all unit cells of both I- and Q- PGAs turned on) consumed 14.5 mA from a 1V supply. Due to instrument limitations, the NF of the LNA-VM was not measured. As shown in Figure 5.17(a), the quadrature frequency could be tuned from 25.1 GHz (coarse word='15', fine word='15') to 27.6 GHz (coarse word='0', fine word='0'), with a fine frequency tuning resolution of ~40 MHz. The frequency resolution of the coarse word was ~150 MHz. While this architecture can synthesize all possible 5-bit I/Q complex weights, Figure 5.17(b) shows the constant modulus phase settings at the three frequencies which demonstrates high-resolution phase tuning over the entire 360° range (also see Figure 5.17(c)). The worst-case measured RMS phase and amplitude error was 2.6° and 0.39 dB respectively. Here, RMS phase error quantifies the deviations from ideal phase value resulting
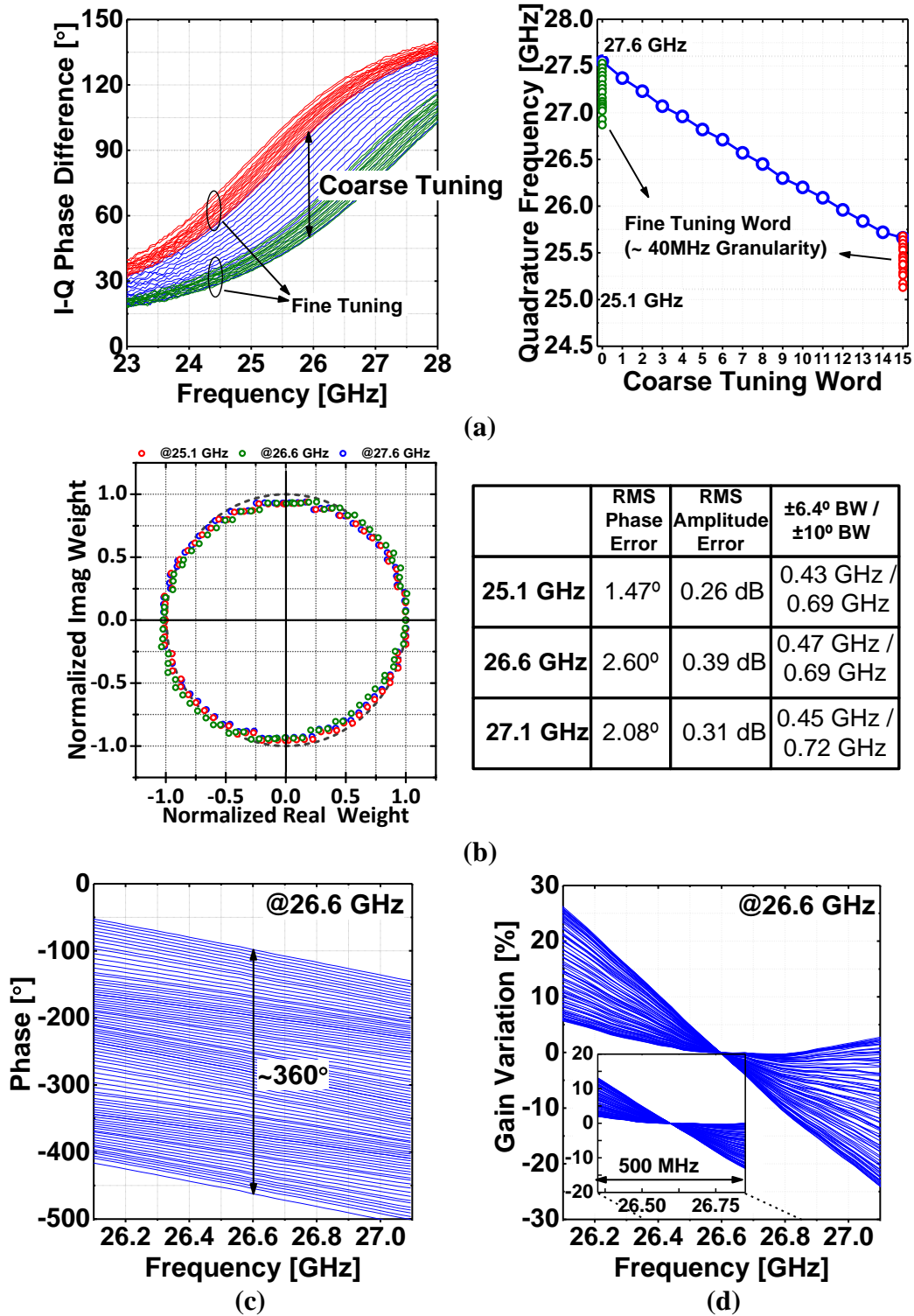
Figure 5.17 (a) Measured phase difference between I- and Q-paths and quadrature frequency for different values of capacitance word. **(b)** Measured constant modulus constellation points on the normalized I/Q channel coordinates. **(c)** Measured phase-response of the LNA-VM at 26.6 GHz demonstrating full-span range. **(d)** Measured gain-variation over 500 MHz bandwidth at 26.6 GHz.
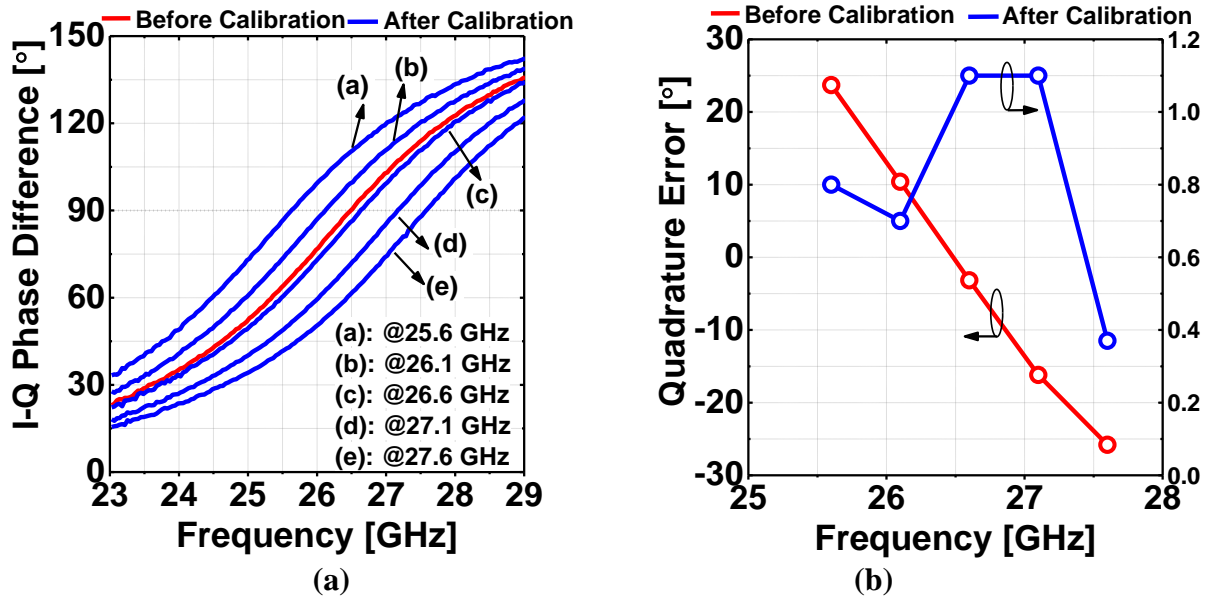
Figure 5.18 (a) I/Q phase difference, and (b) quadrature error before and after calibration.

	Technology	Phase-Shifting Method	Frequency [GHz]	Design Details	Phase Resolution	Phase Tuning Range	RMS Phase Error	Gain [dB]	Power [mW]	Area [mm²]
[127] CICC'15	65 nm CMOS	Vector Modulator	2-24	Passive I/Q +Vector Interpolation	5-bit I, Q	360°	<1.22° [2]	-3.5	84	2.16
[129] MWCL'16	65 nm CMOS	Switched-Filter	27.5-28.35	Phase Shifters	4-bit (22.5°)	360°	<8.98°	-6.36	0	0.23
[130] RFIC'16	45 nm SOI CMOS	Switched-LC	26-28	LNA+VGAs+ Phase Shifters	5-bit (11.25°)	360°	<4°	12	42	1.75
[128] TCAS-II'17	130 nm CMOS	Vector Modulator	24.55-27.4/ 26.55-29.4	PPF+Vector Interpolation	6-bit	360°	<2.6°	-6.1±1.5/ -5±1.5	27	0.284
[122] TMTT'17	65 nm CMOS	RTPS	28	LNA+Phase Shifter	5-bit (11.25°)	360°	0.4°	9.5±0.4	10	0.32
[119] JSSC'17	130 nm SiGe	Dual-Vector	28-32	LNA+Vector Interpolation	4-bit (22.5°)	360°	<5.4°	10.5	136.5	1.08
This Work	65 nm CMOS	Merged Narrowband LNA-VM	25.1-27.6 (Tunable, ≥0.43GHz BW)	LNA+Vector Interpolation	5-bit I, Q (~3-5° [5])	360°	1.47° [1] 2.60° [2] 2.08° [3]	6 [4] 7.75 [4] 8 [4]	30.5	0.318 [6]/ 0.123 [7]

Table 5-1 Measurement results and comparison.

[1]Measured at 25.1 GHz, [2]Measured at 26.6 GHz, [3]Measured at 27.6 GHz ,[4]LNA gain (excludes loss of the Cartesian phase shifter and output buffer), [5]Non-uniform phase steps, [6]LNA-VM+Calibration, [7]LNA-VM only.

from 5-bit I and Q quantized constant-modulus complex-weight settings, and RMS gain error

quantifies the standard deviation from average gain [114]. It is evident that use of phase-invariant

PGAs with constant input capacitance [85], [118] ensured low RMS gain and phase errors.

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Table 5-1 compares the proposed LNA-VM with recent RF phase-shifter front-ends. Amongst the compared work, only [128] is frequency tunable. However, the design is based on the use of lossy current-mode *R-C* poly-phase shifters which are highly susceptible to PVT variations and may require extensive calibration. Figure 5.18 demonstrates the calibration operation: for a desired frequency of operation at 5 different frequencies– 25.6 GHz, 26.1 GHz, 26.6 GHz, 27.1 GHz and 27.6 GHz respectively, the calibration loop approaches the right cap settings from an initial arbitrary cap setting (coarse control word='8'), bringing down the quadrature error to ~1° and below.

5.6 Summary

This work proposes the use of wide tuning range and narrowband compact vector modulators for emerging 5G phased-array receivers. A low-*Q* coupled-resonator load in the LNA is used for quadrature generation, thereby avoiding the need for an explicit quadrature hybrid and facilitating an ultra-compact design. The use of phase-invariant PGAs with constant input capacitance following the LNA ensures low RMS gain and phase errors. An on-chip calibration loop is implemented which adjusts the coupled-resonator's capacitance to generate quadrature I/Q outputs at any desired frequency in the band.

6 Conclusions and Future Work

6.1 Conclusions and Contributions

This research introduced several CMOS-integrated, transformer-based reconfigurable circuit techniques whose effectiveness was validated through measurements of designed transceiver front-end low-noise (LNA) and power amplifier (PA) proof-of-concept prototypes.

The first contribution is the demonstration of an integrated, PC-switch based, dual-band (3/5 GHz) reconfigurable CMOS LNA with transformer source degeneration in a 0.13 µm process. This work was significant because it demonstrated, for the first time, that a phase-change RF switch could be integrated with a parasitic-sensitive RF design block like an LNA, and that the integrated system could be stably and reversibly configured between different frequency bands. A novel and compact LNA design was proposed such that both a power and a noise match could be achieved at two different frequencies. Unlike other dual-bands reported in literature, the integrated LNA achieved identical performance in both bands: this was a result of both a careful design as well as a superior RF switch. The work identified the impact of integration on LNA performance which will motivate the development of alternative integration strategies in the future, such as the homogeneous integration of PC switches with CMOS, for example as reported in [131]. This work will also serve as the foundation for the development of more complex RF systems like transceivers leveraging the demonstrated benefits of an integrated CMOS-PC system. It resulted in the following publications:

- R. Singh, G. Slovin, M. Xu, A. Khairi, S. Kundu, T. E. Schlesinger, J. A. Bain and J. Paramesh, "A 3/5 GHz reconfigurable CMOS low-noise amplifier integrated with a four-terminal phase-change RF switch," in *Proc. IEEE Intl. Electron Devices Meeting*, Dec. 2015, pp. 25.3.1-25.3.4. [5]

– R. Singh, G. Slovin, M. Xu, T. E. Schlesinger, J. A. Bain and J. Paramesh, "A Reconfigurable Dual-Frequency Narrowband CMOS LNA using Phase-Change RF Switches," *IEEE Trans. Microw. Theory Techn*, vol. 65, no. 11, pp. 4689-4702, Nov. 2017. [6]

[7], [20], [39] and [40] are other publications of fellow PhD students who were involved in the development of CMU's CMOS-PC integration project [17]-[19] and [26] report the parallel development of the four-terminal PC RF switch at Northrop Grumman.

After the development of an integrated small-signal CMOS-PC system, we intended to leverage the PC switch's advantages in a large signal system like a power-combining CMOS PA. During our investigations, we proposed a frequency-reconfigurable CMOS transformer combiner that could be reconfigured to have similar efficiencies at widely separated frequency bands. This work was significant because previous transformer combiners in CMOS PAs were always tuned for operation at a single frequency standard: however, this work introduced a way to re-use the same transformer combiner for different frequencies using regular CMOS switches. A switched capacitor design was also introduced with a high C_{ON}/C_{OFF} ratio. A 65-nm CMOS triple-band (2.5/3/3.5 GHz) PA employing the reconfigurable combiner was implemented. While the original intention was to use PC switches, our first prototype was CMOS-only as the design worked equally well with regular low-breakdown CMOS switches. Future work will require a careful study of the power-handling and linearity performance of the PC RF switch, such as reported in [25] and [132], which will consequently pave the way for the development of frequency-reconfigurable large-signal CMOS-PC systems. This work was published in:

– R. Singh and J. Paramesh, "A Digitally-Tuned Triple-Band Transformer Power Combiner for CMOS Power Amplifiers," in *Proc. IEEE Radio Frequency Integr. Circuits Conf.*, pp. 332-335, June 2017.

The interested reader should refer to [48], [49], [54], [56], [58] and [63] for relevant literature concerning this work.

In the final part of this work, the use of transformer coupled-resonators in mm-wave LNA designs for 28 GHz bands was investigated. To cover contiguous and/or widely-separated narrowband channels of the emerging 5G standards, a 65-nm CMOS 24.9-32.7 GHz wideband multi-mode LNA using one-port transformer coupled-resonators was designed. The main contribution of this work was the introduction of design techniques to facilitate the use of the driving point impedance (Z_{11}) of one-port transformer coupled-resonators as wideband loads of millimeter-wave amplifier stages for a 28 GHz receiver front-end. While the use of both the Z_{11} of a one-port and the trans-impedance (Z_{21}) of a two-port coupled-resonator has been previously considered to achieve a wideband response [85], [88]-[90], [94], it was shown that under conditions of low magnetic coupling and constrained network quality factor, the use of Z_{11} results in a higher gain-bandwidth product. The effect of the complex zero in the Z_{11} response on the in-band gain ripple was shown to be alleviated merely by lowering the quality factor of the transformer's secondary coil. This work will be submitted for publication in:

- R. Singh and J. Paramesh, "A 28 GHz Wideband LNA Design Using One-Port Transformer Coupled-Resonators". [To: *IEEE Trans. Microw. Theory Techn*,]

Finally, a 25.1-27.6 GHz tunable-narrowband digitally-calibrated merged LNA-vector modulator design was presented that proposes a compact, differential quadrature generation scheme for phased-array architectures. This work is significant because in contrast to the traditional paradigm of using bulky quadrature hybrids in vector-modulated based phased array architectures, it proposes the use of narrowband, frequency-tunable and compact merged LNA-vector modulators based on the use of coupled-resonators. This work showed that by using a low-Q coupled-resonator

load, differential quadrature signals can be generated from the LNA stage itself, thereby avoiding the need for explicit quadrature hybrids and facilitating an ultra-compact design. The work also proposed a gain and external phase-mismatch tolerant quadrature error detector that was employed in a correction loop to generate accurate quadrature signals at any desired frequency in the band. This work will be published in:

- R. Singh, S. Mondal and J. Paramesh, "A 25.1-27.6 GHz Tunable-Narrowband Digitally-Calibrated Merged LNA-Vector Modulator for 5G Phased Arrays," in *Proc. IEEE Radio Frequency Integr. Circuits Conf.*, June 2018.
- R. Singh, S. Mondal and J. Paramesh, "Narrowband merged LNA vector modualtor phased-array receiver front ends," [To: *IEEE Trans. Microw. Theory Techn*,].

6.2 Future Work

Several different future directions can be outlined based on the work presented in this thesis.

[1] A complete multi-band CMOS Receiver using PC RF switches: This research demonstrated the feasibility of employing PC RF switches in CMOS LNAs, while a concurrent research has explored their use in multi-band VCOs [133]. These ideas can be combined together to implement a multi-band CMOS receiver integrated with a multitude of RF PC switches. Figure 6.1 shows the detailed block diagram of an example quad-band (2.5/5/11/17 GHz) direct-conversion receiver front-end and LO generation/distribution. The receiver comprises two parallel narrowband LNAs, similar to the ones implemented in Chapter 2. The LNA is followed by a wideband balun, which is then followed by current-driven passive mixers. Each of the I/Q mixers drives a low impedance load consisting of the virtual ground of a closed loop two-stage operational amplifier. The two stage op-amp together with the feedback network functions as a transimpedance amplifier (TIA). To generate quadrature LO signals required by the image-reject receiver, a wideband 9-17 GHz quadrature VCO is employed. To enable wideband operation, each of the two VCO cores exploits
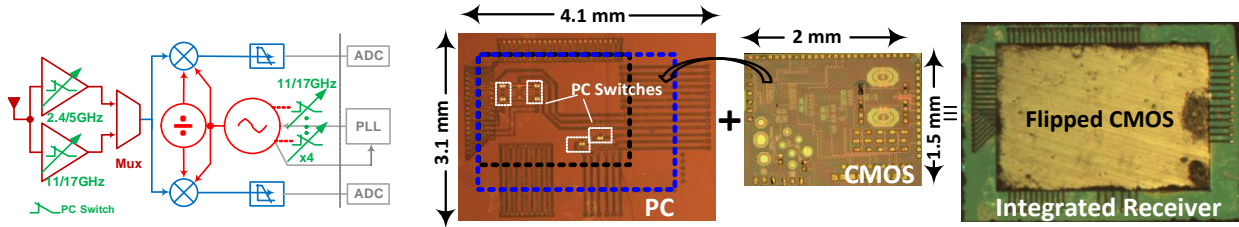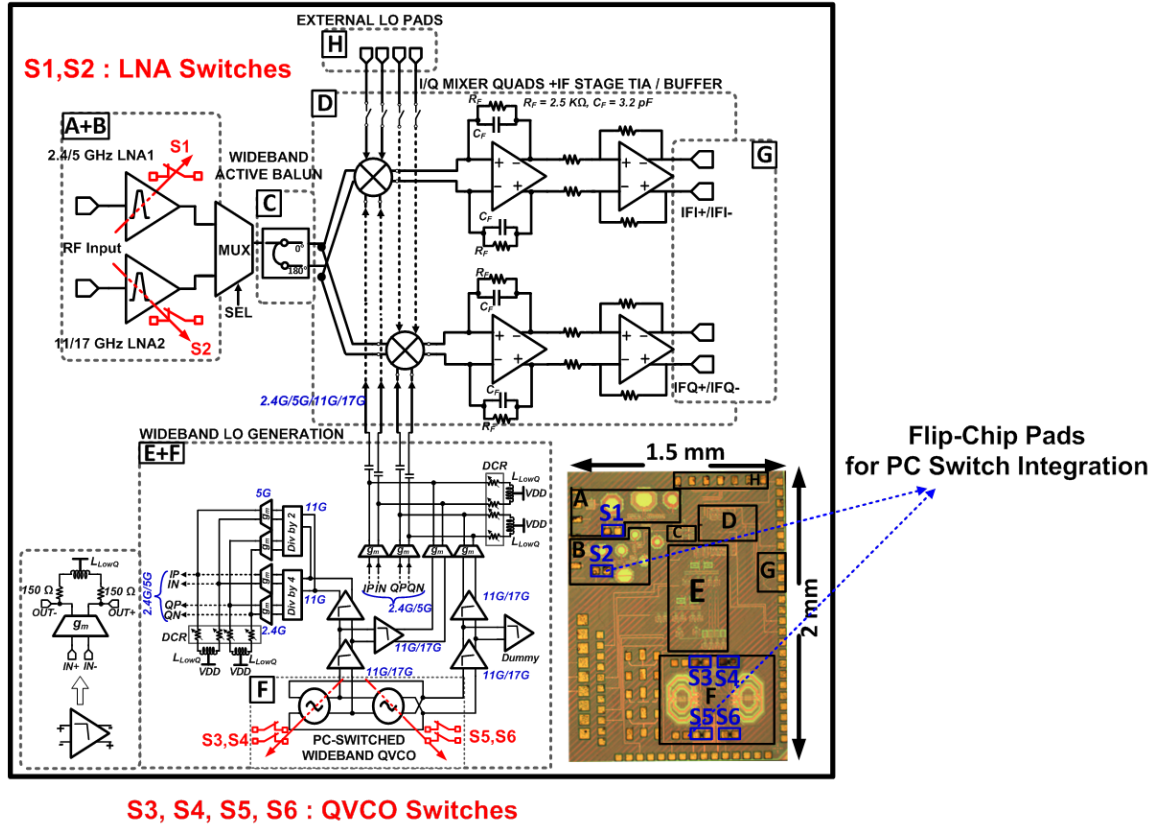
Figure 6.1 (a) Envisioned 2.4/5/11/17 GHz reconfigurable quad-band CMOS receiver with PC-switched LNAs and VCO. (b) Block diagram and layout of the quad-band receiver. S1 to S6 highlights the location of the flip-chip pads that connect to the PC switches on the PC chip. DCR standards for digitally-controlled resistor, implemented through a parallel network of binary weighted pMOS switches controlled by digital code.

dual resonance of coupled-resonator tanks in addition to PC-switched capacitors to achieve a wide tuning range [133]. The QVCO is followed by compact LO buffers (shunt-peaked differential amplifiers) and divider stages. The designed receiver is expected to achieve comparable performance to baseline single-band CMOS receivers in all the four frequency bands. This work

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is currently in development, with plans to demonstrate a complete CMOS-PC receiver prototype. A successful demonstration will pave the way for future implementations of complex, high-performance, field-programmable CMOS-PC transceivers.

[2] PC switch matrices for high power handling: RF measurements on fabricated PC switches has already demonstrated promising power handling capabilities (at least 20 dBm of incident RF power) [39]. However, there is room for improvement, and the PC-switch can be re-engineered to stand-off multi-watt incident power levels without sacrificing RF performance. The fundamental limit of power handling capability of PC switches comes from their tendency to spontaneously switch from OFF-state to ON-state due to a threshold-switching event which in turn leads to memory switching (permanent change in the resistivity state) [134]. Threshold switching is initiated when the voltage across the RF terminals of a PC switch reaches a threshold voltage V_{TH}. Experimental methods need to be determined to accurately determine the DC and RF threshold voltages of PC switches. Admittedly, redesigning the PC switch involves various device design considerations, outside the scope of a circuit designer. Various aspects of the switch design including: (1) the composition ratio of the Ge_xTe_{1-x} alloys and its electrodes, (2) the dimensions of the GeTe switch, (3) the dimensions of the heater element, (4) the choice and thickness of the thermally conductive dielectric layer between the heater and GeTe layer and (5) the choice of the substrate material, will have to optimized to achieve high power-handling functionality. However, these device directions will have to be pursued together with circuit considerations in mind to achieve the right trade-off between RF performance, robustness and the power handling capabilities. Additionally, there are interesting possibilities to be pursued in terms of new switch architectures that can lead to improved power handling. For example, placing switches in series can allow for an increase in V_{TH} by reducing the electric field across an individual switch. The
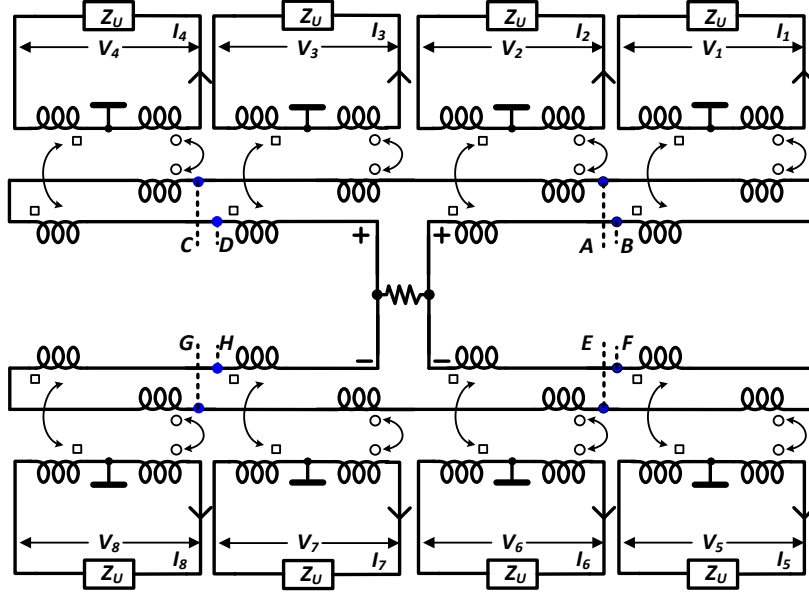
Figure 6.2 Possible implementation of an 8-way voltage-current combining frequency-reconfigurable PA architecture. Z_U represents the output impedance of each unit amplifier.

effective R_{ON} can be brought back to its original value by adding a parallel branch of series-connected switches. Since PC switches have small form factors and limit the addition of parasitic capacitances, N×N switch array can then be employed depending on the insertion loss and power handling requirements of the design. Successful prototypes of large-signal CMOS-PC systems like power amplifiers, and Rx/Tx SPnT switches will further poise CMOS-PC technology for rapid mainstream adoption.

[3] 8-way >1W power-combining CMOS PA: Unlike the single-ended voltage-combining implementation of the combiner's secondary coil in Chapter 3, when the output terminals of the combiner are connected differentially, the phase mismatches between the amplifier ports are expected to reduce due to differential symmetry. Furthermore, current-combining architectures have been shown to be superior in terms of channel symmetry, as discussed in Chapter 3. These observations lead to several interesting possibilities for implementing a very high power 8-way PA with minimal phase/amplitude mismatches between the unit amplifiers. Figure 6.2 shows a

possible implementation of an 8-way PA where both voltage and current combining is used to reduce mismatches between the amplifier ports. Since the design is based on the earlier 4-way reconfigurable PA design, low-swing nodes (A-B, C-D, E-F and G-H) are still available where reconfiguration capacitors can be conveniently inserted. This design will be symmetrical if all unit amplifiers are identical. However, if like the design in Chapter 3, a Doherty-like architecture is adopted, then careful attention should be given to minimizing the phase mismatch between the main and the peaking amplifiers. The application of reconfigurable combiner architecture at mm-wave frequencies is also an unexplored but potentially promising opportunity.

[4] mm-wave LNA designs: This work, together with [85], [90] and [119] has employed coupled-resonators in 28 GHz LNA designs employing both common-source (CS) and common-gate (CG) stages. While the versatility of coupled-resonator design at these frequencies has been established, the design considerations between choosing a CS or CG dominated LNA design are not yet clear. In a seminal paper [135], it was predicted that CG-LNA designs will become more and more attractive at higher frequencies as the low-noise advantage of CS amplifiers rapidly deteriorates with frequency. On the other hand, CG-LNA designs require passive G_m-boosting to break the tight link between input matching and noise figure, and suffer from limited gain. Examples of CS/CG LNA designs at these frequencies do exist in literature; however, a proper evaluation of their advantages, disadvantages and performance is absent. A theoretical and experimental evaluation along these lines is especially important due to the high current interest in the development of 28/37 GHz 5G transceivers.

References

[1] M. Rais-Zadeh, J. Fox, D. Wentzloff, and Y. Gianchandani, "Reconfigurable radios: A possible solution to reduce entry costs in wireless phones," *Proc. IEEE*, vol. 103, no. 3, Mar. 2015.

[2] D. J. Allstot, C. T. Charles, S. Kodali, X. Li, D. Ozis, J. Paramesh, S. Shekhar, J. Walling, "CMOS integrated transformers: coming of age," *IEEE International Conference on Solid-State and Integrated Circuit Technology,* pp. 23-26 Oct. 2006.

[3] Fact sheet: Spectrum frontiers proposal to identify, open up vast amounts of new high-band spectrum for next generation (5G) wireless broadband [Online]. Available: https://apps.fcc.gov/edocs_public/attachmatch /DOC-339990A1.pdf.

[4] T. O. Dickson, M.-A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. P. Voinigescu, "30-100-GHz Inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *IEEE Trans. Microw. Theory Techn*, vol. 53, no. 1, pp. 123-133, Jan. 2005.

[5] R. Singh, G. Slovin, M. Xu, A. Khairi, S. Kundu, T. E. Schlesinger, J. A. Bain and J. Paramesh, "A 3/5 GHz reconfigurable CMOS low-noise amplifier integrated with a four-terminal phase-change RF switch," in *Proc. IEEE Intl. Electron Devices Meeting*, Dec. 2015, pp. 25.3.1-25.3.4.

[6] R. Singh, G. Slovin, M. Xu, T. E. Schlesinger, J. A. Bain and J. Paramesh, "A Reconfigurable Dual-Frequency Narrowband CMOS LNA using Phase-Change RF Switches," *IEEE Trans. Microw. Theory Techn*, vol. 65, no. 11, pp. 4689-4702, Nov. 2017.

[7] G. Slovin, M. Xu, R. Singh, J. Paramesh, T. E. Schlesinger, and J. A. Bain, "Design Criteria in Sizing Phase-Change RF Switches," *IEEE Trans. Microw. Theory Techn*, vol. 65, no. 11, pp. 4531-4540, Nov. 2017.

[8] R. Singh and J. Paramesh, "A Digitally-Tuned Triple-Band Transformer Power Combiner for CMOS Power Amplifiers," in *Proc. IEEE Radio Frequency Integr. Circuits Conf.*, pp. 332-335, June 2017.

[9] R. Singh and J. Paramesh, "A 28 GHz Wideband LNA Design Using One-Port Transformer Coupled-Resonators". [Under Review: *IEEE Trans. Microw. Theory Techn*,]

[10] R. Singh, S. Mondal and J. Paramesh, "A 25.1-27.6 GHz Tunable-Narrowband Digitally-

Calibrated Merged LNA-Vector Modulator for 5G Phased Arrays," in *Proc. IEEE Radio Frequency Integr. Circuits Conf.*, June 2018.

[11] S. Ovshinsky, "Reversible electrical switching phenomenon in disordered structures," Phys. Rev. Lett., vol. 21, no. 20, pp. 1450-1453, 1968.

[12] G. Atwood, "Phase-change materials for electronic memories," *Science*, vol. 321, no. 5886, pp. 210-211, Jul. 2008.

[13] G. W. Burr, M. J. Breitwisch, M. Fanceschini, D. Garetto, K. Gopalakrishnan, B. Jackson, B. Kurdi, C. Lam, L. A. Lastras, A. Padilla, B. Rajendran, S. Raoux, R. S. Shenoy, "Phase change memory technology," *J. Vac. Sci. Technol. B*, vol. 28, no. 2, pp. 223-262, Apr. 2010.

[14] E. K. Chua, L. P. Shi, R. Zhao, K. G. Lim, T. C. Chong, T. E. Schlesinger, and J. A. Bain, "Low resistance, high dynamic range reconfigurable phase change switch for radio frequency applications," *Appl. Phys. Lett.*, vol. 97, 183506, 2010.

[15] H. Lo, E. Chua, J. C. Huang, C. C. Tan, C.-Y. Wen, R. Zhao, L. Shi, C. T. Chong, J. Paramesh, T. E. Schlesinger, and J. A. Bain, "Three-terminal probe reconfigurable phase-change material switches," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 312-320, Jan. 2010.

[16] Y. Shim, G. Hummel, and M. Rais-Zadeh, "RF switches using phase change materials," in *Proc. IEEE Int. Conf. MEMS*, Jan. 2013, pp. 237-240.

[17] N. El-Hinnawy, P. Borodulin, B. P. Wagner, M. R. King, J. S. Mason Jr., E. B. Jones, V. Veliadis, R. S. Howell, R. M. Young, and M. J. Lee, "A four-terminal, inline, chalcogenide phase-change RF Switch using an independent resistive heater for thermal actuation," *IEEE Electron Device Letters*, vol. 34, no. 10, Oct 2013.

[18] N. El-Hinnawy, P. Borodulin, B. P. Wagner, M. R. King, E. B. Jones, R. S. Howell, M. J. Lee, and R. M. Young, "Low-loss latching microwave switch using thermally pulsed nono-volatile chalcogenide phase change materials," *Appl. Phys. Lett.*, vol. 105, 013501, 2014.

[19] N. El-Hinnawy, P. Borodulin, E. B. Jones, B. P. Wagner, M. R. King, J. S. Mason Jr., J. Bain, J. Paramesh, T. E. Schlesinger, R. S. Howell, M. J. Lee, and R. M. Young, "12.5 THz Fco GeTe inline phase-change switch for reconfigurable RF and switching applications," in *Proc. Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2014, pp 1-3.

[20] G. Slovin, M. Xu, J. Paramesh, T. E. Schlesinger, and J. A. Bain, "AlN barriers for capacitance reduction in phase-change RF switches," *IEEE Electron Device Lett.*, vol. 37, no. 5, May 2016.

[21] M. Wang, Y. Shim, and M. Rais-Zadeh, "A low-loss directly heated two-port RF phase change switch," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 491-493, Apr. 2014.

[22] C.-Y.Wen, E. K. Chua, R. Zhao, T. C. Chong, J. A. Bain, T. E. Schlesinger, L. T. Pileggi, and J. Paramesh, "A phase-change via-reconfigurable on-chip inductor," in *Proc. IEEE Intl. Electron Devices Meeting*, Dec. 2010, pp. 10.3.1-10.3.4.

[23] C.-Y. Wen, G. Slovin, J. A. Bain, T. E. Schlesinger, L. T. Pileggi, and J. Paramesh, "A phase-change via-reconfigurable CMOS LC VCO," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 3979-3988, Dec. 2013.

[24] R. Howell, *et al.*, "The Super-Lattice Castellated Field Effect Transistor (SLCFET): a novel high performance transistor topology ideal for RF switching," in *Proc. Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2014, pp 1-4.

[25] M. Wang, F. Lin, and M. Rais-Zadeh, "Performance measurements and non-linearity modeling of GeTe phase change RF switches with direct and indirect heating schemes," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 2015, pp 1-4.

[26] N. El-Hinnawy, P. Borodulin, A. Ezis, C. Furrow, C. Padilla, M. King, E. Jones, B. Wagner, J. Paramesh, J. Bain, D. Nichols, and R. M. Young "Substrate agnostic monolithic integration of the inline phase-change switch technology," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 2016, pp 1-4.

[27] G. M. Rebeiz, K. Entesari, I. Reines, S.-J. Park, M. A. El-Tanani, A. Grichener, and A. R. Brown, "Tuning in to RF MEMS," *IEEE Microw. Mag.*, vol. 10, no. 5, pp. 55-72, Oct. 2009.

[28] A. Jajoo, L. Wang, and T. Mukherjee, "MEMS varactors enabled frequency-reconfigurable LNA and PA in the upper UHF band," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 2009, pp 1121-1124.

[29] Z. Li, R. Quintal, and K. O. Kenneth, "A dual-band CMOS front end with two gain modes for wireless LAN applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2069-2073, Nov. 2004.

[30] S. Hyvonen, K. Bhatia, and E. Rosenbaum, "An ESD-protected, 2.45/5.25-GHz dual-band CMOS LNA with series LC loads and a 0.5-V supply," in *Proc. IEEE Radio Frequency Integr. Circuits Conf.*, 2005, pp. 43-46.

[31] L.-H. Lu, H.-H. Hsieh, and Y.-S. Wang, "A compact 2.4/5.2-GHz CMOS dual-band low-noise amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 10, pp. 685-687, Oct. 2005.

[32] C.-T. Fu, C.-L. Ko, C.-N. Kuo, and Y.-Z. Zhang, "A 2.4-5.4-GHz wide tuning-range CMOS reconfigurable low-noise amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 12, pp. 2754-2763, Dec. 2008.

[33] N. M. Neihart, J. Brown, and X. Yu, "A dual-band 2.45/6 GHz CMOS LNA utilizing a dual-resonant transformer-based matching network," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1743-1751, Aug. 2012.

[34] X. Yu and N. M. Neihart, "Analysis and design of a reconfigurable multimode low-noise amplifier utilizing a multitap transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1236-1246, Mar. 2013.

[35] F.-J. Huang and K. O, "A 0.5-µm CMOS T/R switch for 900-MHz wireless applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 486-492, May 2000.

[36] B.-W. Min and G. M. Rebeiz, "Ka-band low-loss and high-isolation switch design in 0.13-µm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 6, pp. 1364-1371, Jun. 2008.

[37] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin, Y.-T. Chang and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 1, pp. 31-39, Jan. 2006.

[38] S. Raoux, B. Munoz, H.-Y. Cheng, and J. L. Jordan-Sweet, "Phase transitions in Ge-Te phase change materials studied by time-resolved x-ray diffraction," *Appl. Phys. Lett.*, vol. 95, 142118, 2009.

[39] G. Slovin, "Design and Optimization of 4-Terminal RF Phase Change Switch," Ph.D. dissertation, Dept. Elect. And Comp. Eng., Carnegie Mellon Univ., Pittsburgh, PA, 2015.

[40] M. Xu, G. Slovin, J. Paramesh, T. E. Schlesinger, and J. A. Bain, "Thermometry of a high temperature high speed micro heater," *Rev. Sci. Instrum.*, 87, 024904, 2016.

[41] T.-K. Nguyen, C.-H. Kim. G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 5, pp. 1433-1442, May 2004.

[42] B. Razavi, *RF Microelectronics*, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2011.

[43] "Low Noise Amplifier Design Techniques", *IEEE RFIC Virtual Journal*, Issue 4, 2014.

[44] A. M. Niknejad, *Electromagnetics For High-Speed Analog and Digital Communication Circuits*, 1st ed. Cambridge, U. K.: Cambridge Univ. Press, 2007.

[45] S. Kundu and J. Paramesh, "A transformer-neutralized 0.6 V VDD 17-29 GHz LNA and its application to an RF front-end," in *Springer Journal of Analog Integrated Circuits and Signal Processing*, vol. 83, issue 2, pp. 173-186, May 2015.

[46] M. Wang and M. Rais-Zadeh, "Development and evaluation of germanium telluride phase change material based ohmic switches for RF applications," *Journal of Micromechanics and Microengineering*, 27(1), 013001, 2016.

[47] J.-S. Moon, H.-C. Seo, K.-A. Son, K. Lee, D. Zehnder, H. Tai, and D. Le, "Phase-change RF switches with robust switching cycle endurance," in *Proc. Radio and Wireless Symposium (RWS)*, 2018.

[48] G.Liu, T.–J. King, and A. M. Niknejad, "Fully integrated CMOS power amplifier with efficiency enhancement at power back-off," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600-609, Mar. 2008.

[49] P. Haldi, D. Chowdhury, P. Reynaert, G. Liu, and A. M. Niknejad, "A 5.8 GHz linear power amplifier using a novel on-chip transformer power combiner in standard 90 nm CMOS," IEEE *J. Solid-State Circuits*, vol. 43, no. 5, pp. 1054-1062, Mar. 2008.

[50] K.-H. An et.al, "Power combining techniques for fully-integrated CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, May 2008.

[51] Q. J. Gu, Z. Xu, and M.-C. Chang, "Two-way current-combining W-band power amplifier in 65-nm CMOS", *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1365-1374, May. 2012.

[52] A. Afsahi and L.E. Larson, "Monolithic power-combining techniques for watt-level 2.4-GHz CMOS power amplifiers for WLAN applications", *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1247-1260, Mar. 2013.

[53] J. W. Lai and A. Valdes-Garcia, "A 1V 17.9 dBm 60 GHz power amplifier in 65 nm CMOS", in *IEEE Int. Solid-State Circuits Conf.*, Feb. 2010, pp. 424-425.

[54] A. R. Suvarna, V. Bhagvatula, and J. C. Rudell, "Transformer-based tunable matching network design techniques in 40-nm CMOS," *IEEE Trans. Circuits Syst. II*, vol. 60, no. 4, pp. 202-206, Apr. 2013.

[55] V. Bhagavatula, W. C. Wesson, S.-K. Shin, and J. C. Rudell, "A fully integrated, regulatorless CMOS power amplifier for long-range wireless sensor communication," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1225-1236, May 2013.

[56] R. Jegadeesan and Y. -X. Guo, "Topology selection and efficiency improvement of inductive power links," *IEEE Trans. Antennas Propag.*, vol. 60, no. 10, pp. 4846-4854, Oct. 2012.

[57] H. Wang, C. Sideris, and A. Hajimiri, "A CMOS broadband power amplifier with a transformer-based high-order output matching network," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2709-2722, Dec. 2010.

[58] Y. Yoon, H. Kim, Y. Park, M. Ahn, C.-H, Lee, and J. Laskar, "A high-power and highly linear CMOS switched capacitor," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 11, pp. 619-621, Nov. 2010.

[59] M. Ahn, H.-W. Kim, C.-H. Lee, and J. Laskar, "A 1.8-GHz 33-dBm P0.1-dB CMOS T/R switch using stacked FETs with feed-forward capacitors in a floated well structure," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 11, pp. 2661-2670, Nov. 2009.

[60] Cadence Spectre RF Workshop: Power Amplifier design using Spectre RF (MMSIM 11.1).

[61] S. Emami, C. H. Doan, A. M. Niknejad and R. W. Brodersen, "Large-signal millimeter-wave CMOS modeling with BSIM3," in *Proc. IEEE Radio Frequency Integr. Circuits Conf.*, 2004, pp. 163-166.

[62] B.-W. Min and G. M. Rebeiz, "Ka-band low-loss and high-isolation switch design in 0.13-um CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 6, pp. 1364-1371, June 2008.

[63] E. Kaymaksut and P. Reynaert, "Transformer-based uneven Doherty power amplifier in 90 nm CMOS for WLAN applications", *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1659-1671, Jul. 2012.

[64] S. C. Cripps, *RF Power Amplifiers for Wireless Communication*, 2nd ed., Norwood, MA: Artech House, 2006.

[65] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEEE Microw. Mag.*, vol. 7, no. 5, pp. 42-50, Oct. 2006.

[66] K. Kim, D.-H. Lee, and Songcheol Hong, "A quasi-doherty SOI CMOS power amplifier with folded combining transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 8, pp. 2605-2614, June. 2016.

[67] E. Kaymaksut and P. Reynaert, "Dual-mode CMOS Doherty LTE power amplifier with symmetric hybrid transformer," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 1974-1987, Sep. 2015.

[68] D. Chen, C. Zhao, Z. Jiang, K. M. Shum, Q. Xue and K. Kang, "A V-band Doherty power amplifier based on voltage compensation and balance compensation marchand balun," in *IEEE Access*, vol. 6, pp. 10131-10138, 2018.

[69] D. Chowdhury, C. D. Hull, O. B. Degani, Y. Wang, and A. M. Niknejad, "A fully integrated dual-mode highly linear 2.4 GHz CMOS power amplifier for 4G WiMax Applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3393-3402, Dec. 2009.

[70] B. Afshar and A. Niknejad, "X/Ku band CMOS LNA design techniques," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2006, pp. 389-392.

[71] Amplifier Coaxial ZVE-8G+ [Online] https://www.minicircuits.com/pdfs/ZVE-8G+.pdf

[72] L. Nan, K. Mouthaan, Y.-Z. Xiong, J. Shi, S. C. Rustagi, and B.-L. Ooi, "Experimental characterization of the effect of metal dummy fills on spiral inductors," in *Proc. IEEE Radio Frequency Integr. Circuits Conf. (RFIC)*, 2007, pp. 307-310.

[73] A. Tsuchiya and H. Onodera, "Patterned floating dummy fill for on-chip spiral inductor considering the effect of dummy fill," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 12, pp. 3217-3222, Dec. 2008.

[74] D. Zhao and P. Reynaert, "A 60-GHz dual-mode class AB power amplifier in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2323-2337, Oct. 2013.

[75] Y.-T Chang, Y. Ye, H. Xu, C. Domier, N. C. Luhmann Jr, and Q. J. Gu, "An ultra-wideband CMOS PA with dummy filling for reliability," *Solid State Electronics*, vol. 129, pp. 125-133, Mar. 2017.

[76] H. Wang, C. Sideries and A. Hajimiri, "A CMOS broadband power amplifier with a transformer-based high-order output matching network," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2709-2722, Dec. 2010.

[77] D. Wu, "A Doherty power amplifier with extended bandwidth and reconfigurable back-off level," Ph.D. dissertation, Dept. Elec. Comp. Eng, Univ. Waterloo, Waterloo, ON, 2013.

[78] Q. J. Gu and M.-C. F. Chang, "Two-way current-combining W-band power amplifier in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1365-1374, May 2012.

[79] J.-W. Lai, A. Valdes-Garcia, "A 1V 17.9dBm 60GHz power amplifier in standard 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 558-559, Feb. 2008.

[80] R. Darraji, F. M. Ghannouchi, and O. Hammi, "A dual-input digitally driven Doherty amplifier architecture for performance enhancement of Doherty transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, May. 2011.

[81] S. Hu, F. Wang, and H. Wang, "A 28 GHz/37 GHz/ 39 GHz multiband linear Doherty power amplifier for 5G massive MIMO applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 558-559, Feb. 2008.

[82] K. Onizuka, K. Ileuchi, S. Saigusa, and S. Otaka, "A 2.4 GHz CMOS Doherty power amplifier with dynamic biasing scheme," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2012, pp. 93-96.

[83] R. W. Heath Jr., N. Conzalez-Prelcic, S. Rangan, W. Roh, and A. M. Sayeed, "An overview of signal processing techniques for millimeter wave MIMO systems," *IEEE J. Sel. Topics Signal Process.*, vol. 10, no. 3, pp. 436-453, Apr. 2016.

[84] S. Kundu and J. Paramesh, "A compact, supply-voltage scalable 45-66 GHz baseband-combining phased-array receiver," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 527-542, Feb. 2015.

[85] S. Mondal, R. Singh, A. I. Hussein, and J. Paramesh, "A 25-30 GHz 8-antenna 2-stream hybrid beamforming receiver for MIMO communication," in *Proc. IEEE Radio Frequency Integr. Circuits Conf. (RFIC)*, 2017, pp. 112-115.

[86] 5G spectrum recommendations, April 2017 [Online]. http://5gamericas.org/files/9114/9324/1786/5GA_5G_Spectrum_Recommendations_2017_FINAL.pdf

[87] T. S. Rappaport *et. al*, "Millimeter wave mobile communications for 5G Cellular: It will work!" *IEEE Access*, vol. 1, pp. 335-349, 2013.

[88] V. Bhagavatula, T. Zhang, A. R. Suvarna, and J. C. Rudell, "An ultra-wideband IF millimeter-wave receiver with a 20 GHz channel bandwidth using gain-equalized transformers", *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 323-331, Feb. 2016.

[89] M. Vigilante and P. Reynaert, "On the design of wideband transformer-based fourth order matching networks for E-band receivers in 28-nm CMOS", *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 20171-2082, Aug. 2016.

[90] S. Mondal, R. Singh, and J. Paramesh, "A reconfigurable 28/37GHz hybrid-beamforming MIMO receiver with inter-band carrier aggregation and RF-domain LMS weight adaptation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2018, pp. 72-74.

[91] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "Transformer-based dual-mode voltage-controlled oscillators," *IEEE Trans. Circuits and Systems-II: Express Briefs*, vol. 54, no. 4, pp. 293-297, Apr. 2007.

[92] Z. Safarian and H. Hashemi, "Wideband multi-mode CMOS VCO design using coupled inductors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1830-1843, Aug. 2009.

[93] S. V. Thyagarajan, A. M. Niknejad, and C. D. Hull, "A 60 GHz drain-source neutralized wideband linear power amplifier in 28 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 8, pp. 2253-2262, Aug. 2014.

[94] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A millimeter-wave (23-32 GHz) wideband BiCMOS low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 289-299, Sep. 2009.

[95] S. Kundu and J. Paramesh, "A transformer-neutralized 0.6 V VDD 17-29 GHz LNA and its application to a RF front-end," *Springer Journal of Analog Integr. Circuits and Signal Processing*, vol. 83, issue 2, May 2015.

[96] E. Adabi, B. Heydari, M. Bohsali, and A. M. Niknejad, "30 GHz CMOS low noise amplifier," *Proc. IEEE Radio Frequency Integr. Circuits Conf.*, Jun. 2007, pp. 625-628.

[97] H.-K. Chen, Y.-S. Lin, and S.-S. Lu, "Analysis and design of a 1.6-28-GHz compact wideband LNA in 90-nm CMOS using a π-match input network," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 8, Aug. 2010.

[98] Y.-T. Lo and J.-F. Kiang, "Design of wideband LNA using parallel-to-series resonant matching network between common-gate and common-source stages," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 9, pp. 2285-2294, Sep. 2011.

[99] A. M. Niknejad, *Electromagnetics for High-Speed Analog and Digital Communication Circuits*, Cambridge University Press, 2007.

[100] M. Dishal, "Exact design and analysis of double- and triple-tuned band-pass amplifiers," *Proc. of the IRE*, vol. 35, no. 6, pp. 606-626, 1947.

[101] I. Zverev, *Handbook of Filter Synthesis*. New York: Wiley, 1967.

[102] C. Bowick, *RF Circuit Design*, 2nd ed. Oxford, U. K.: Newnes, 2007.

[103] F. F. Kuo, *Network Analysis and Synthesis*. New York: Wiley, 1996.

[104] Kenneth O, "Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technology," *IEEE J. Solid-State Circuits*, vol. 33, no. 8, pp. 1249-1252, Aug. 1998.

[105] V. N. R. Vanukuru, "Millimeter-wave bandpass filter using high-Q conical inductors and MOM capacitors," in *Proc. IEEE Radio Frequency Integr. Circuits Conf. (RFIC)*, May 2016, pp. 39-42.

[106] A. Mazzanti, M. Sosio, M. Repossi, and F. Svelto, "A 24 GHz subharmonic direct conversion receiver in 65 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 88-97, Jan. 2011.

[107] W. Chen, T. Copani, H. Barnaby and S. Kiaei, "A 14-GHz CMOS receiver with local oscillator and bandpass filter for satellite applications," in *Proc. IEEE Radio Frequency Integr. Circuits Conf. (RFIC)*, 2009, pp. 123-126.

[108] S. Kulkarni, D. Zhao, and P. Reynaert, "Design of an optimal layout polyphase filter for millimeter-wave quadrature LO generation," *IEEE Trans. Circuits Syst. II*, vol. 60, no. 4, pp. 202-206, Apr. 2013.

[109] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1996.

[110] B. Sadhu, *et. al*, "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3373-3391, Dec. 2017.

[111] B.-W. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 10, pp. 2239-2250, Oct. 2008.

[112] U. Kodak and G. M. Rebeiz, "A 42mW 26–28 GHz phased-array receive channel with 12 dB gain, 4 dB NF and 0 dBm IIP3 in 45nm CMOS SOI," in *Proc. IEEE Radio Frequency Integr. Circuits Conf. (RFIC)*, 2016, pp. 348-351.

[113] M. Kumar, R. J. Menna, and H. Huang, "Broad-band active phase shifters using dual gate MESFET," *IEEE Trans. Microwave Theory Techn.*, vol. 29, no. 10, pp. 1098-1102, Oct. 1981.

[114] K.-J. Koh and G. M. Rebeiz, "0.13-µm CMOS phase shifters for X-, Ku-, and K-band phased arrays," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2535-2546, Nov. 2007.

[115] A. Asoodeh and M. Atarodi, "A full 360° vector-sum phase shifter with very low RMS phase error over a wide bandwidth," *IEEE Trans. Microwave Theory Techn.*, vol. 60, no. 6, pp. 1626-1634, Jun. 2012.

[116] S. Shahramian, Y. Baeyens, N. Kaneda, and Y. K. Chen, "A 70-100 GHz direct-conversion transmitter and receiver phased array chipset demonstrating 10 Gb/s wireless link," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1113-1125, May. 2013.

[117] J. Paramesh, R. Bishop, K. Soumyanath and D. J. Allstot, "A four-antenna receiver in 90-nm CMOS for beamforming and spatial diversity," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2515-2524, Dec. 2005.

[118] S. Mondal, R. Singh, A. I. Hussein, and J. Paramesh, "A 25-30 GHz fully-connected hybrid beamforming receiver for MIMO communication*," IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp., May 2018.

[119] Y. S. Yeh, B. Walker, E. Balboni and B. A. Floyd, "A 28-GHz phased-array receiver front end with dual-vector distributed beamforming," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1230-1244, May. 2017.

[120] J.-C. Wu, C.-C. Chang, S.-F. Chang, and T.-Y. Chin, "A 24-GHz full-360° CMOS reflection-type phase shifter MMIC with low loss variation," in *Proc. IEEE Radio Frequency Integr. Circuits Conf. (RFIC)*, 2008, pp. 365-368.

[121] M. D. Tsai and A. Natarajan, "60 GHz passive and active RF-path phase shifters in silicon," in *Proc. IEEE Radio Frequency Integr. Circuits Conf. (RFIC)*, 2009, pp. 223-226.

[122] R. Garg and A. Natarajan, "A 28-GHz low-power phased-array receiver front-end with 360° RTPS phase shift range," *IEEE Trans. Microwave Theory Techn.*, vol. 65, no. 11, pp. 4703-4714, Nov. 2017.

[123] 5G spectrum recommendations, April 2017 [Online] http://5gamericas.org/files/9114/9324/1786/5GA_5G_Spectrum_Recommendations_2017_FINAL.pdf.

[124] G. Mangraviti, K. Khalaf, B. Parvais, G. Vandersteen, and P. Wambacq, "Design and Tuning of coupled-LC mm-wave subharmonically injected-locked oscillators," *IEEE Trans. Microwave Theory Techn.*, vol. 63, no. 7, pp. 2301-2312, July 2015.

[125] X. Li, S. Shekhar and D. J. Allstot, "G_m-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-µm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2609-2619, Dec. 2005.

[126] T. Zhang, A. Najifi, M. Taghivand, and J. C. Rudell, "A precision wideband quadrature generation technique with feedback control for millimeter-wave communication system," *IEEE Trans. Microwave Theory Techn.*, vol. 66, no. 1, pp. 215-226, Jan. 2018.

[127] T.-W. Li, J. S. Park, and H. Wang, "A 2-24 GHz 360 full-span differential vector modulator phase rotator with transformer-based poly-phase quadrature network," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2015, pp. 1-4.

[128] F. Akbar and A. Mortazawi, "A frequency tunable 360 analog CMOS phase shifter with an adjustable amplitude," *IEEE Trans. Circuits Syst. II*, vol. 64, no. 12, pp. 1427-1431, Dec. 2017.

[129] G.-S. Shin, J.-S. Kim, H.-M. Oh, S. Choi, C.-W. Byeon, J. H. Son, J. H. Lee, and C.-Y. Kim, "Low insertion loss, compact 4-bit phase shifter in 65 nm CMOS for 5G applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 1, pp. 37-39, Jan. 2016.

[130] U. Kodak and G. M. Rebeiz, "A 42mW 26-28 GHz phased-array receive channel with 12 dB gain, 4 dB NF and 0 dBm IIP3 in 45nm CMOS SOI," in *Proc. IEEE Radio Frequency Integr. Circuits Conf. (RFIC)*, 2016, pp. 348-351.

[131] N. El-Hinnawy, P. Borodulin, M. R. King, C. Furrow, C. R. Padilla, A. Ezis, D. T. Nichols, J. Paramesh, J. A. Bain, and R. M. Young, "Experimental demonstration of AlN heat spreaders for the monolithic integration of inline phase-change switches," *IEEE Electron Device Letters*, vol. 39, no. 4, pp. 610-613, Apr. 2018.

[132] N. El-Hinnawy, P. Borodulin, M. R. King, C. R. Padilla, A. Ezis, D. T. Nichols, J. Paramesh, J. A. Bain, and R. M. Young, "Origin and optimization of RF power handling limirations in inline phase-change switchces," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3934-3942, Sept. 2017.

[133] A. B. Khairi, "Wide-band multi-mode voltage tuning oscillators utilizing phase-change switches," Ph.D. dissertation, Dept. Elect. And Comp. Eng., Carnegie Mellon Univ., Pittsburgh, PA, 2016.

[134] A. Redaelli, A. Pirovano, F. Pellizzer, A. L. Lacaita, D. Ielmini, and R. Bez, "Electronic switching effect and phase-change transition in chalcogenide materials," *IEEE Electron Device Letters*, vol. 25, no. 10, pp. 684-686, Oct 2004.

[135] D. J. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," in *Proc. IEEE Radio Frequency Integr. Circuits Conf.*, pp. 97-100, 2004.

[136] A. Grebennikov and S. Bulja, "High-efficiency Doherty power amplifiers: historical aspect and modern trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190-3219, Dec. 2012.

[137] S.-C Jung, O. Hammi, and F. M. Ghannouchi, "Design optimization and DPD linearization of GaN-based unsymmetrical Doherty power amplifiers for 3G multicarrier applications," *IEEE Trans. Microwave Theory Techn.*, vol. 57, no. 9, pp. 2105-2113, Sept. 2009.