Design Techniques for Low Spur Wide Tuning All-Digital Millimeter-Wave Frequency Synthesizers

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Abstract

With the explosive growth of mobile traffic demand, the contradiction between capacity requirements and spectrum shortage becomes the bottleneck towards high date rate wireless communication systems. The millimeter-wave (mm-wave) frequency bands have recently emerged as a viable option to meet the exploding demand for wireless multimedia content over short ranges. Frequency synthesizers that can tune over wide bandwidths in finely spaced steps are essential components in wireless mm-wave applications. With all the advantages of all-digital frequency synthesizers, they remained restricted to low gigahertz operating frequencies since the design of DCOs, TDCs, and frequency dividers operating at mm-wave frequency poses enormous challenges, and the mitigation of those challenges remains an open problem.

This research explores the feasibility, advantages, implementation, and testing of millimeter-wave fractional-N digital frequency synthesizers. In addition, it proposes several design techniques to overcome the design challenges of the constituent blocks in mm-wave ADPLL's, thereby enhancing performance by reducing spurs, increasing tuning range and frequency resolution. While, the proposed architectures and techniques is suitable for all mm-wave applications below 100 GHz, a 60 GHz frequency synthesizer is implemented in this work as an example to validate the proposed techniques. During the investigation of millimeter-wave Fractional-N digital frequency synthesizers, several solutions are proposed and validated.

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1 Introduction

1.1 Motivation and overview

Capacity for wireless communication depends on spectral efficiency and bandwidth. Currently, almost all wireless communications use spectrum in 300 MHz to 3 GHz band. This band derives benefits from its reliable propagation characteristics over several kilometers in different radio environments. However, with the explosive growth of mobile traffic demand, the contradiction between capacity requirements and spectrum shortage becomes the bottleneck towards high date rate wireless communication systems.

The millimeter-wave (mm-wave) frequency bands have recently emerged as a viable option to meet the exploding demand for wireless multimedia content over short ranges. Historically, collision avoidance radars are the first to exploit this mm-wave spectrum [1]. The US Federal Communication Commission (FCC) opened the spectrum between 59 ~ 64 GHz and 81 ~ 86 GHz for unlicensed wireless and peer to peer communications respectively [1]. In particular, the IEEE802.15.3c WPAN [2] and the IEEE.802.11ad WLAN [3] standards have been finalized in the 57-66 GHz unlicensed band to achieve multi-Gbps data rates over 10 meters. Channel models based on measurements in realistic usage scenarios have been developed for these standards. These models play a key role in evaluating system design options for transceivers for these standards.

Wireless backhaul is another emerging application [4] in the mm-wave bands. The 71-76 GHz and 81-86 GHz bands are being considered for this application due to lower channel attenuation, which in turn enables longer range communication. Based on these successes, the mm-wave

bands are attracting high interest for cellular operation. Until recently, any proposal of mm-wave cellular communication has been met with much skepticism due to the peculiar propagation characteristics in these bands. Recently, however, channel measurements in the 28, 38, and 73 GHz bands have been reported [5] and these reports indicate the conceptual feasibility of mm-wave cellular communication. As a result, the mm-wave bands are increasingly considered to be a viable option for 5G cellular communications [6]–[9]. Millimeter-wave automotive radar system have been implemented also at 77 GHz [10], [11] to detect and track the objects and traffic with speed and distance adjustment.

Semiconductors have been used for millimeter-waves since the 1970s, where the transceiver's blocks have been implemented using Gallium Nitride (GaN) [12] and Gallium Arsenide (GaAs) [13] substrates to achieve high operating frequency with high output power. However, with the revolution in silicon process technology, it was emphasized that CMOS technology represents the cheapest solution for commercial mm-wave applications. The key point of cost reduction is the ability of RF/analog-digital integration in the same chip.

Mm-wave transmitters and receivers have been implemented recently and demonstrate superior performance in CMOS technology [14]–[18]. Frequency synthesizers that can tune over wide bandwidths in finely spaced steps are essential components in such applications. They especially play a crucial role in frequency modulated continuous wave (FMCW) radars when high range resolution is required. Therefore, extensive research works focus on the implementation of low-cost, low power, and wide bandwidth mm-wave frequency synthesizers [19]–[39].

All-digital phase-locked loop (ADPLL) based frequency synthesizers are desirable for several reasons as will be discussed later. Several semi-digital and all-digital frequency synthesizers

[40]–[57] have been reported for several applications but have remained restricted to low gigahertz operating frequencies.

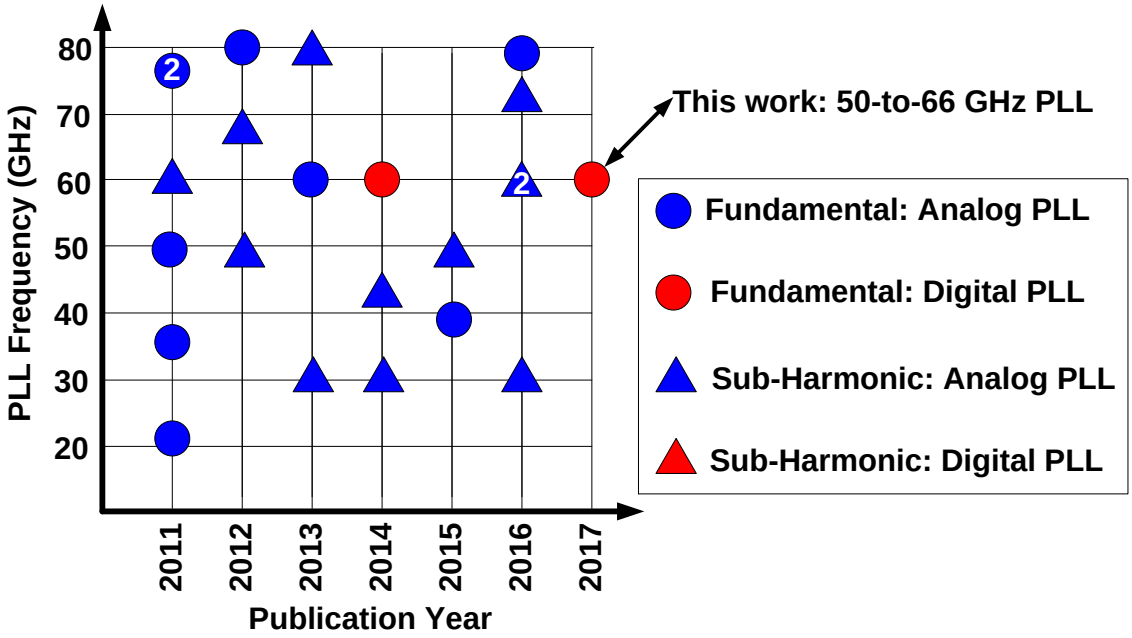


Figure 1.1 Reported mm-wave PLLs VS. publication year

Figure 1.1 shows the reported architectures of mm-wave PLLs last six years, it can be observed that synthesizers in the mm-wave bands still rely on analog PLL's. This is because the design of DCOs, TDCs, and frequency dividers operating at mm-wave frequency poses enormous challenges, the mitigation of which remains an open problem, as will be discussed later.

1.2 Thesis scope and contribution

This research explores the feasibility, advantages, implementation, and testing of millimeter-wave fractional-N digital frequency synthesizers. In addition, it proposes several design techniques to overcome the design challenges of the constituent blocks in mm-wave ADPLL's, thereby enhancing performance by reducing spurs, increasing tuning range and frequency

resolution. While the proposed architectures and techniques are suitable for all mm-wave applications below 100 GHz, a 60 GHz frequency synthesizer is implemented in this work as an example to validate the proposed techniques. During the investigation of millimeter-wave fractional-N digital frequency synthesizers, several solutions are proposed and validated:

1) Wide tuning range mm-wave digitally controlled oscillator (DCO) with very fine frequency tuning granularity [58]: Switched coupled-inductor and switched-capacitor banks are used to provide the coarse tuning to achieve 24% tuning range from 48.1 GHz to 61.3 GHz. A fine frequency tuning resolution of 39 kHz is achieved using capacitive degeneration. This DCO is fabricated in 65 nm CMOS and achieves the highest figure-of-merit (FOM) among recent mm-wave DCO benchmarks.
2) Based on an accurate time-domain analysis of DCML latch, five different design techniques are proposed in [59] to widen the operating frequency range and to increase the locking range of dynamic current-mode latch (DCML) based inductor-less millimeter-wave frequency divider. Three divide-by-4 prototypes incorporating these techniques are designed and fabricated in 65 nm CMOS to cover a frequency range exceeding 16-67 GHz.
3) A background self-calibration technique is introduced to guarantee the frequency locking of DCML dividers over a wide frequency range with low input amplitude and over PVT variations [59]. With this calibration scheme, the DCML dividers operate with input power less than -10 dBm, supply voltage variation of +/- 100 mV and achieve the highest FOM_P reported to date.
4) The first TDC to date that operates at mm-wave range (20-68 GHz) with finest time resolution (450 fs) is implemented. A digital calibration scheme based on “statistical

element selection" [60] is introduced to alleviate TDC nonlinearity results from PVT and random mismatch variation. The measured DNL and INL of 65 nm CMOS two-step TDC are 0.65 LSB and 1.2 LSB, respectively. The 60 GHz TDC consumes only 11 mW which results in best FOM_I over the state of the art.

5) A 60 GHz all-digital phase-domain PLL that covers the widest reported frequency range (50-66 GHz) among 60 GHz PLLs [61]. The PLL incorporates extensive digital calibration of each sub-system to achieve 220 fs jitter, best (worst) phase noise of -83/-93/-126 (-79/-88/-116) dBc/Hz at 0.1/1/10MHz offset, -59 dBc spur and the highest reported FoM_T to date among mm-wave PLL's.
6) Two different techniques are proposed to mitigate phase mismatch effect on ADPLL's performance [61].

1.3 Thesis organization

This thesis is organized as follows:

- Chapter 2 discusses the mm-wave frequency generation approaches and compares briefly between analog and digital frequency synthesizers. In addition, a brief comparison between different architectures of digital PLLs will be presented and design challenges of mm-wave digital PLLs will be discussed.
- Chapter 3 presents the design and implementation of a wide tuning range DCO with fine frequency step. Limitations of mm-wave DCOs will be discussed and state-of-art architectures will be compared briefly. Afterwards, the proposed solutions to achieve the wide tuning range and fine frequency step simultaneously will be presented with measurement results of prototype chip.

- Chapter 4 presents several design techniques to widen the operating frequency range and to increase the locking range of dynamic current-mode latch (DCML) based inductor-less millimeter-wave frequency divider. A comparison between mm-wave frequency dividers will be presented. Then, an accurate time-domain analysis of operation of DCML latch will be presented to highlight the limitations of state-of-art DCML topology. In addition, the locking range sensitivity to PVT variation will be discussed. Three divide-by-4 prototypes incorporating five different techniques are presented and a background self-calibration technique is introduced to guarantee frequency locking over a wide frequency range with low input amplitude and over PVT variations. Finally, measurement results and the effect of technology scaling on proposed techniques will be presented.
- Chapter 5 presents the first TDC operates at mm-wave frequency. The summary of effect of TDC's non-idealities on ADPLL performance will be discussed, then a comparison between state-of-art TDC architectures will be presented. Afterwards, the proposed two-step 16 GHz TDC with sub-sampling interface stage will be presented. A calibration algorithm based on statistical element selection, will be presented to alleviate the TDC non-linearity. Finally, the measurement results of prototype chip will be discussed.
- Chapter 6 presents the design and implementation of 50-to-66 GHz fractional-N ADPLL. The specifications of 60 GHz frequency synthesizer which meets the requirements of IEEE 802.15.33c [2] and IEEE 802.11ad [3] will be discussed. Afterwards, the design of the ADPLL associated with different calibration schemes to

reduce spur level will be presented. Finally, the measurement results of prototype chip will be discussed.

- Finally, chapter 7 concludes this thesis and discusses the future work.

2 MM-Wave Frequency Synthesizers

Frequency synthesizer is used in RF transceiver system to provide a clean, stable and tunable LO signal to the transmitter and receiver. In general, the main specifications of any frequency synthesizers are:

1. Phase noise which affects bit error rate of the communication link, reciprocal mixing in the receiver, modulation accuracy (error vector magnitude) and spectral emissions in the transmitter.
2. Tuning range which must be sufficient to cover the desired bandwidth with additional margin for tolerances due to process, supply voltage, and temperature (PVT) variations.
3. Frequency resolution which is determined by channel and sub-carrier spacing.
4. Settling time which must be sufficiently fast. However, it raises a trade-off with steady state error, spur level, and phase noise.
5. Area and power consumption that should be minimized especially in mobile devices.
6. Reference frequency which raises a trade-off between the feedback division modulus, phase noise and complexity of synthesized digital blocks.
7. Frequency error rotates constellation of received signal periodically therefore, it should be less few ppm.

In addition, complex modulation and coding schemes in mm-wave wireless communication systems require low distortion leading to strict requirements of frequency synthesizer. As an example, IEEE 802.11ad standard requires a TX EVM better than −21 dB for a 16 QAM modulation [3], which sets stringent phase noise (PN) requirement [16], [62].

Wide tuning range (TR) is also necessary to cover the specified frequency bands (e.g., 57–65 GHz) with margin for process and temperature spreads which contradicts with low power consumption requirement. Unfortunately, mm-wave frequency generation in CMOS has typically suffered from poor phase noise, limited tuning range, and high power consumption. Therefore, several design techniques [19], [20], [23], [24], [26], [29], [36], [37] have been reported to implement mm-wave PLLs with the aim of improving the aforementioned specifications.

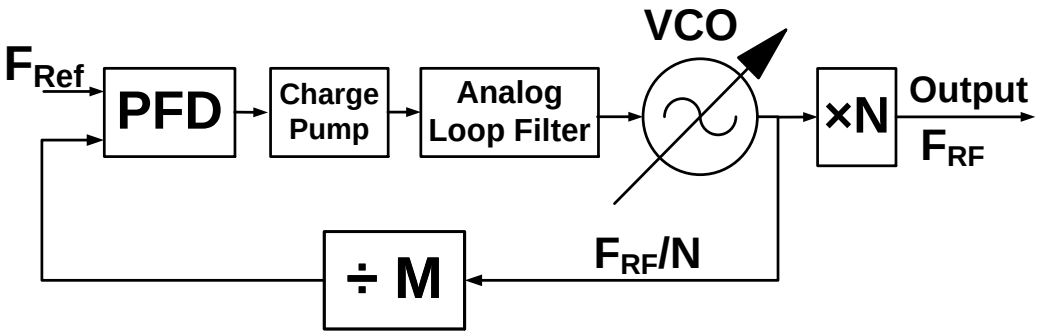
This chapter presents an overview of frequency synthesizer architectures and mm-wave design challenges. This chapter is organized as follows: section 2.1 discusses the difference between mm-wave frequency generation approaches. In section 2.2, the detailed comparison between analog and digital fractional-N PLL and a brief comparison between integral-N and fractional-N frequency synthesizer will be presented. Afterwards, in section 2.3, state-of-art architectures of digital PLLs will be investigated and compared. Finally, section 2.4 discusses the design challenges of mm-wave frequency synthesizers.

2.1 MM-wave frequency generation approaches

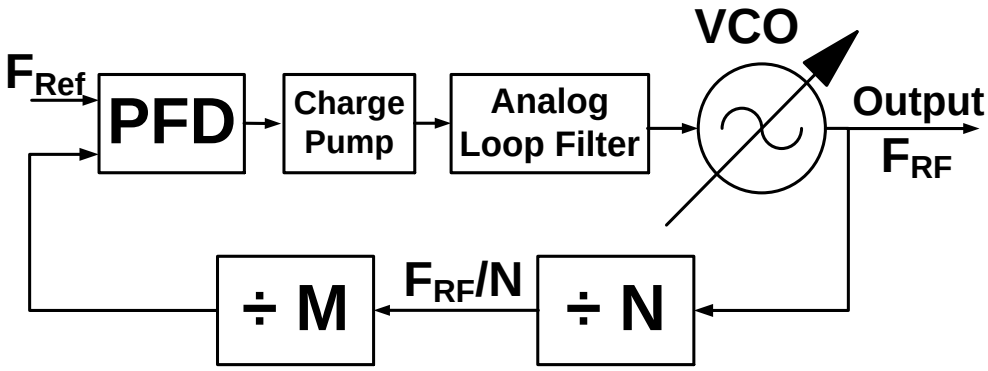
In particular, mm-wave frequency generation approaches can be categorized into three main categories.

2.1.1 Low frequency PLL with frequency multiplier

Popular approach in current mm-wave frequency synthesizers is to design the PLL at a lower frequency and use frequency multiplication [20], [32], [39] to generate the desired output frequency as shown in Figure 2.1 (a).



(a)



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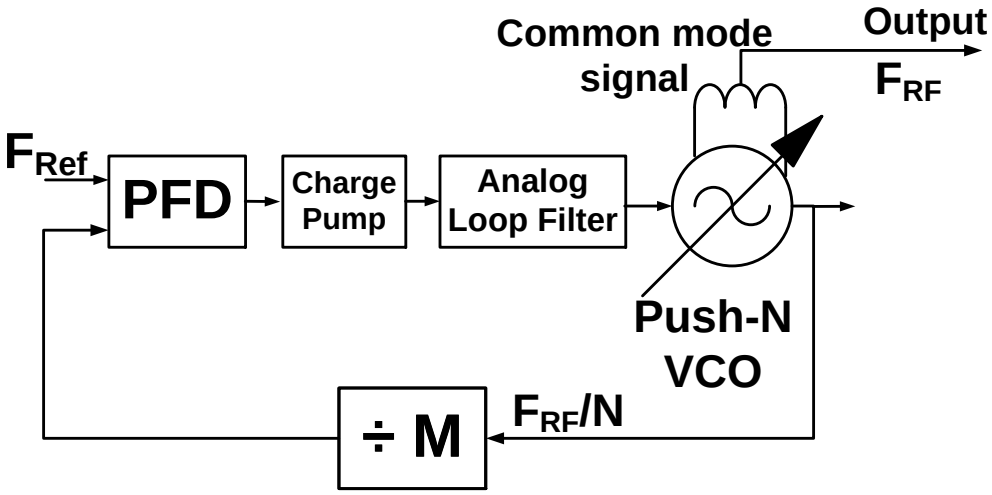


(c)

Figure 2.1 Architectures of mm-wave frequency generation: (a) based on low frequency PLL and frequency multiplier. (b) based on PLL with fundamental oscillator. (c) based on PLL with N-push oscillator

The main advantages of this approach are:

- The reduced tuning range specification allows higher quality factor of the capacitance array and hence of the overall LC tank, which in turn reduces phase noise.
- The divider chain following the VCO operates at lower frequency, which results in lower power consumption and higher the locking range.

Recently, several multiplication techniques have been reported to implement efficient frequency doubler [63]–[65], tripler [66]–[69], and quadrupler [70]–[73] to improve overall performance of Sub-harmonic frequency synthesizers. However, this topology suffers from:

- High spurs power in mixer-type multipliers.
- Limit locking range of injection-locked multipliers.
- Low output power especially with high multiplication ratio [70]–[73].
- Large area due to increasing the number of inductors.
- Single-ended output in case of push-push multipliers which necessitates using of on-chip balun. This, in turn, increases signal losses and chip area.

2.1.2 PLL with a fundamental oscillator

Mm-wave frequency synthesizers based on fundamental frequency VCO's (Figure 2.1 (b)) [23], [31], [36] are less popular, as it suffers from:

- Poor phase noise due to low quality factor of passive element at mm-wave frequency.
- Limited tuning range due to fixed parasitic capacitance.
- Narrow locking range of injection-lock mm-wave frequency divider.

On the other hand, it has several advantages including:

- Avoiding the area overhead, power consumption and non-idealities (e.g., spurs in mixer-type multipliers and limited locking range of injection-locked multipliers) of the frequency multiplier.
- Decreasing the area of VCO due to reduced inductor size.
- Resulting in high IF and wide IF bandwidth in superheterodyne receivers, which eases image-rejection.

2.1.3 PLL with N-push oscillator

In PLLs with N-push oscillators (Figure 2.1(c)), the feedback divider operates at F_{RF}/N and output RF frequency is generated using push-push stage [74]–[76]. Although, frequency multipliers are avoided in this topology, it suffers from:

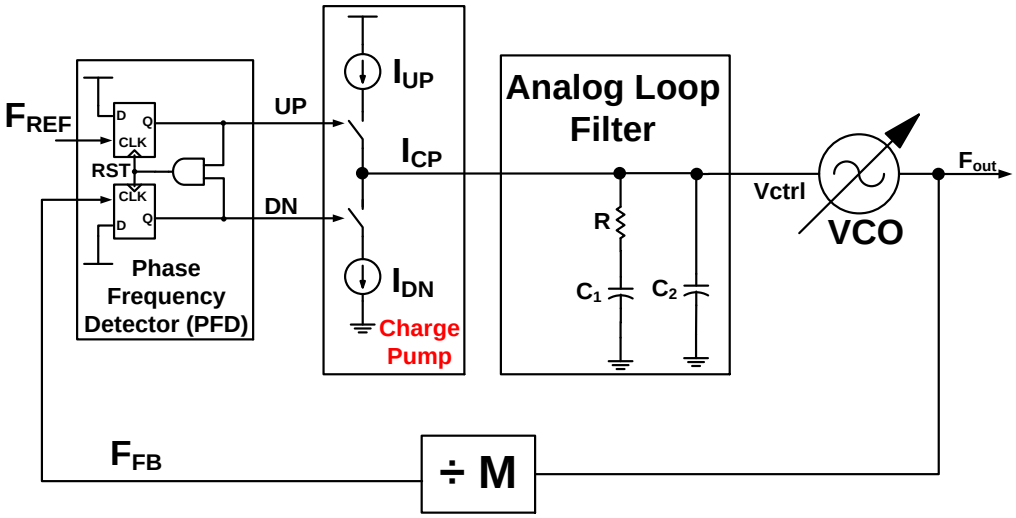
- Low output power and mismatches among the N oscillator (for N > 2).
- Push-push oscillator requires large common mode swing which increases the 1/f noise up conversion [75].
- Conversion from single-ended output to differential outputs which increases chip area, signal losses, and phase error [75].

Table 2-1 Summary of comparison between mm-wave PLL architectures

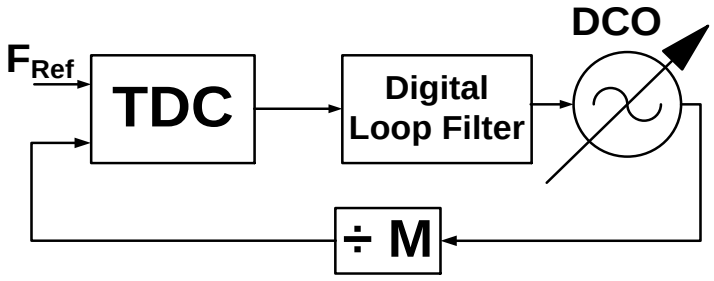
Specification	Fundamental PLL	Sub-harmonic PLL	PLL with N-push VCO
Phase noise	Poor	**Good**	Moderate
Tuning range	Narrow	**Wide**	Moderate
Output power	**High**	Low	Low
Power consumption	**Low**	High	Moderate
Area	**Small**	Large	Large
Quadrature accuracy	**Better**	Moderate	Poor
Image- Rejection	**Better**	Poor	Moderate

Table 2-1 summarize the comparison between mm-wave PLL architectures. In this work, fundamental frequency generation approach is chosen due to its aforementioned advantages. Several techniques are proposed to overcome the limitations of fundamental approach while maintaining the advantages of the sub-harmonic approach.

2.2 Digital versus analog frequency synthesizers



(a)



(b)

Figure 2.2 Block diagram of Integral-N frequency synthesizer (a) Charge-pump analog PLL (b) digital PLL

RF frequency synthesizers have been implemented traditionally using charge-pump PLL (Figure 2.2 (a)). The phase frequency detector (PFD) samples the phase error (Ph_E) between reference

frequency (F_{Ref}) and feedback signal ($F_{FB} = F_{Out}/N$). Based on polarity of $Ph_{E,}$, the PFD generates UP and DN pulses. The charge pump converts these pulses into current pulses I_{UP} and I_{DN}. The net current difference (I_{CP}) is integrated using analog loop filter which generates a filtered control voltage for the voltage control oscillator (VCO).

An important specification of frequency synthesizers for wireless applications is the acquisition or settling time to a new channel frequency. This is determined mainly by the loop bandwidth; wide loop bandwidth enables the fast settling time and reduces the contribution of VCO's phase noise. This, in turn, necessities using a high reference frequency which conflicts with the target frequency resolution requirement.

Fractional-N frequency synthesis is advantageous compared to integer-N synthesis since it breaks the trade-off between target frequency resolution and loop bandwidth. Fractional-N synthesizers can simultaneously achieve fine frequency resolution and wide bandwidth, which helps to achieve fast settling and suppress VCO phase noise. However, loop bandwidth is fixed at narrow value during normal operations of the fractional-N PLL to reduce spur level and the phase noise contribution of charge-pump, phase frequency detector, feedback divider, and reference frequency.

Since the analog loop filter is implemented using passive elements which are sensitive to process, voltage and temperature (PVT) variations, it requires low-leakage devices and a large chip area. In addition, charge pump PLLs suffer from various imperfections results from nonidealities of PFD and charge pump:

- The skew and mismatch between UP and DN pulses.
- Charge injection and clock feedthrough from CMOS switches in the charge pump.
- Static and dynamic mismatch between Up and Down currents in the charge pump.

- Low output impedance of charge pump.

These nonidealities increase spur level and in-band phase noise of PLL.

Moreover, with the continuous scaling of CMOS technology and reduction of supply voltage, the effect of those nonidealities becomes more severe and represents the bottleneck to implementing high performance frequency synthesizers.

During last decade, digital PLLs (Figure 2.2 (b)) have emerged as a feasible solution to overcome the aforementioned drawbacks. In digital PLLs, the PFD and charge pump are replaced by a time-to-digital convert (TDC) which measures the phase error between feedback signal and reference frequency. The phase error is then digitally low-pass filtered to generate the digital tuning word for a digitally controlled oscillator (DCO).

Digital phase-locked loop (DPLL) based frequency synthesizers are desirable for several reasons:

- They allow low voltage implementation by replacing the PFD/charge pump by time-to-digital converter (TDC)
- They help reduce the chip area by replacing the analog loop filter with a digital filter.
- They enable a high degree of programmability or re-configurability to cover the specifications of different applications and communication standards and to accommodate widely varying PVT and loop gain conditions.
- They avoid the nonlinearities associated with the phase-frequency detector (PFD) and charge pump (CP) circuits associated with analog synthesizers, the mitigation of which becomes more challenging with continued technology scaling.
- They avoid introducing noise into the analog control voltage of VCO, therefore achieve greater noise immunity.

- Their implementation results in a small redesign time with process scaling, which is an important consideration in releasing new products.
- Their scaling-friendly nature facilitates the use of digital signal processing to mitigate non-idealities and to enhance the overall DPLL performance.

The main drawback of ADPLL, discussed in more detail later, is the quantization noise of DCO and TDC which increases the in-band and the out-of-band phase noise and leads to undesirable fractional spur.

2.3 Digital PLL Architectures

In a digital PLL, a digitally controlled oscillator (DCO) produces an output frequency based on an input digital word. There are two main digital frequency synthesizer architectures depending on the existence of multi-modulus divider in the feedback path of the PLL, as shown in Figure 2.3.

In the first architecture, henceforth referred to as a semi-digital $\Delta\sum$ Fractional-N PLL (SDPLL), the PFD and charge pump of an analog Fractional-N PLL are replaced by a TDC which converts the phase difference between reference frequency and feedback frequency (F_{Out}/N) to a digital word. The main disadvantage of this architecture arises from the multi-modulus feedback divider which degrades the loop bandwidth and increases in-band phase noise and fractional spur level at the output spectrum. The second architecture, referred to as the phase-domain or ADPLL, avoids the use of a multi-modulus divider by replacing it with a fractional counter (integral counter + TDC) in the feedback path.

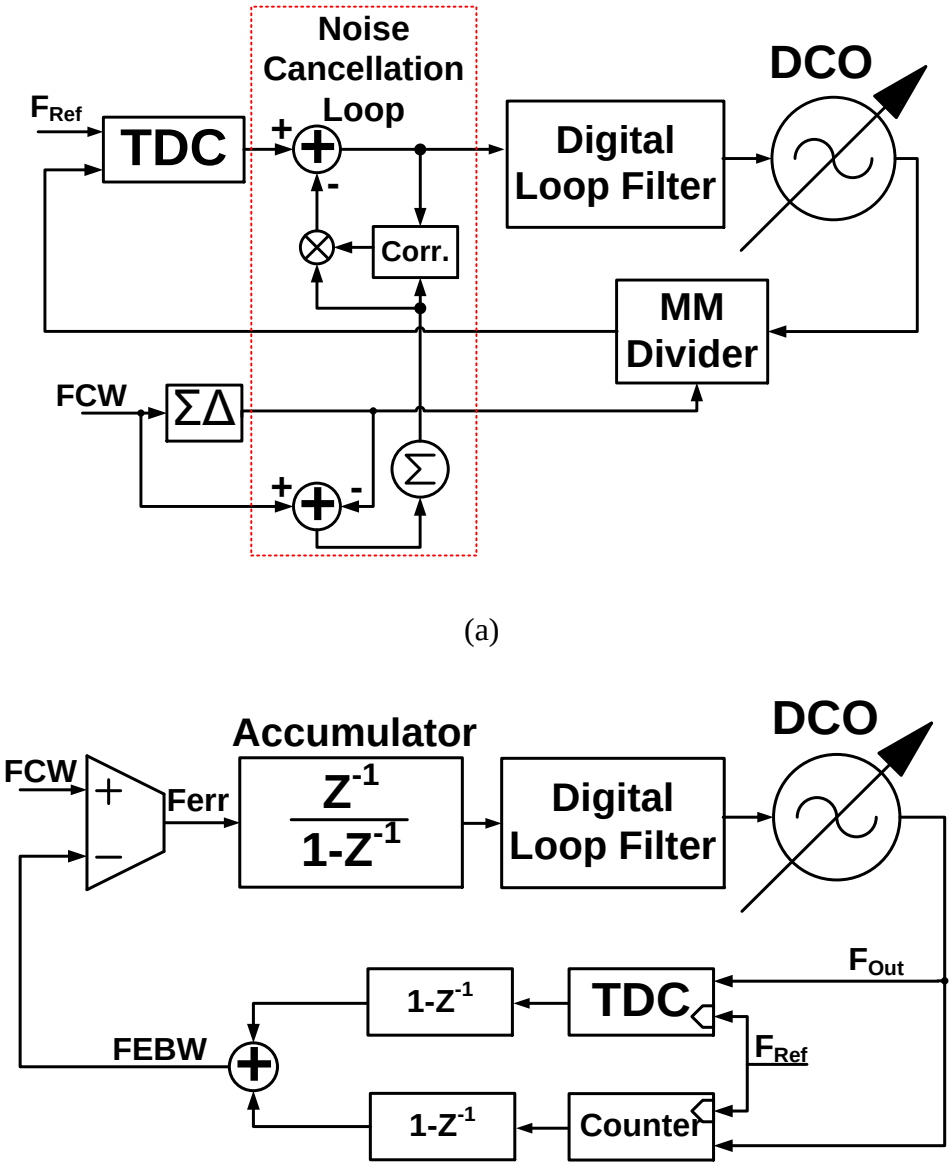


Figure 2.3 Main topologies of Fractional-N digital PLL (a) ∑Δ Fractional-N digital PLL. (b) Divider-less ADPLL

Comparisons between these architectures have been reported in [40], [42], [77]. These comparisons show that the fractional spurs in SDPLL are larger than in the ADPLL due to the large phase error ramp in the former. To equalize the level of phase error ramp (i.e., equalize

spur level), quantization noise cancellation loop can be incorporated into the SDPLL to cancel quantization noise from the TDC output and scaling it by TDC gain as was implemented in 3 GHz ADPLL [77]. However, any error in TDC gain estimation leads to regrowth of spurs. Moreover, SDPLL increases out-of-band phase noise with increasing order of the $\Delta\sum$ modulator; this is not suitable for wideband applications [77]. In addition, the required dynamic range of TDC in SDPLL's is much longer than the counterpart in ADPLL for higher order of $\Delta\sum$ modulator [42], [77]. This means for the same TDC resolution, the power and area consumption of TDC in $\Delta\sum$ Fractional-N PLL is higher than ADPLL.

On the other hand, in an ADPLL, the TDC operates at the DCO output frequency in the feedback path. This necessitates a high performance TDC since it should operate at DCO frequency which results in high power consumption. Moreover, TDC dynamic range should be more than one cycle of the output frequency, along with fine resolution to decrease in-band phase noise and fractional spurs. In addition, the nonlinearity of TDC is the dominant source of fractional spurs [42]. Loop latency is another limiting factor of ADPLL compared to the SDPLL since the TDC is followed directly by digital filter in the latter, while in the former there are digital differentiator, frequency detector, integrator and digital filter. This, in turn, puts some limitations on reference frequency due to speed limitation of the automatic synthesis digital blocks.

Table 2-2 summarizes the comparison between the above two architectures. The ADPLL architecture is selected for the mm-wave frequency synthesizer in this work. A wide dynamic range TDC with fine resolution operating at mm-wave input frequencies is proposed. A digital foreground calibration scheme is proposed to overcome the effects of TDC non-linearity of ADPLL.

Table 2-2 Summary of comparison between digital PLL architectures

Specification	∑Δ Fractional-N DPLL	Divider-less ADPLL
Spur level	Higher	**Lower**
Phase noise	Worse	**Better**
Power consumption	Higher	**Lower**
Loop latency	**Lower**	Higher
TDC dynamic range	Large	**Smaller**
TDC linearity	**Easier**	More challenging

2.4 Design Challenges of mm-wave PLLs

With the continuous scaling of CMOS technology, which increases maximum operating frequency of CMOS circuits, there are enormous challenging issues related to mm-wave frequency synthesizers design.

2.4.1 Transistors

It is important to note that the value of maximum oscillation frequency (F_{Max}) of CMOS transistors operating at mm-wave frequency is significantly reduced due to the interconnect capacitance at the transistor terminals and intrinsic parasitics. Therefore, for a reliable start-up oscillation and output power, transistors should be biased at higher current level and size larger to achieve sufficient $G_{M.}$ This, in turn, reduces the tuning range and increases the overall power consumption of frequency synthesizer.

2.4.2 Tuning range

Figure 2.4 shows the schematic of conventional VCO architecture where the oscillation frequency can be expressed as:

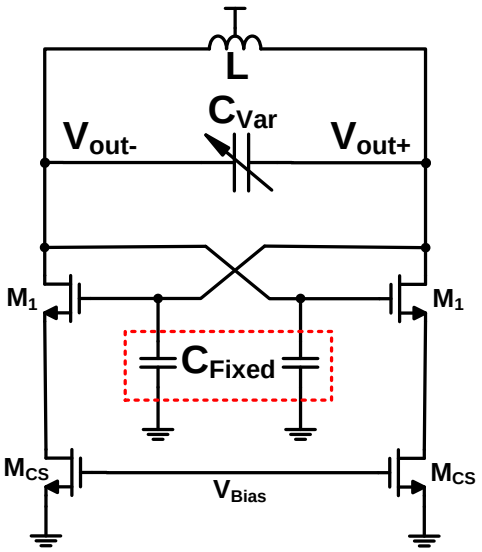


Figure 2.4 Conventional VCO architecture

$$f_{osc} = \frac{1}{2\pi\sqrt{LC_T}} \tag{2-1}$$

Where L and C_T are the effective tank inductance and capacitance, respectively. In addition, the ratio between the maximum and minimum operating frequency can be expressed as:

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{C_{\max}}{C_{\min}}} = \sqrt{\frac{C_{\mathrm{var-max}} + C_{fixed}}{C_{\mathrm{var-min}} + C_{fixed}}} \tag{2-2}$$

Where $C_{var\text{-}max}$, and $C_{var\text{-}min}$ are the maximum and minimum value of varactor. And, C_{fixed} is the fixed capacitance results from interconnect capacitance at the transistor terminals and intrinsic parasitics.

It can be noted from Eq. (2-1), higher oscillation frequency can be achieved by reducing the inductance. However, this approach reduces the tank impedance at resonance which reduces output swing and increases start-up time. Therefore, in order to achieve a reliable output swing

with sufficient start-up margin, the alternative approach is to reduce the absolute value of tank capacitance (C_{var}).

Please, note the fixed capacitance (C_{fixed}) has not been scaled with frequency. Therefore, from Eq. (2-2), it can been note that reducing the absolute value of $C_{var\text{-}max}$, and $C_{var\text{-}min}$ limits the tuning range.

Table 2-3 Comparison between tuning range at 10 GHz and 50 GHz

Parameter	$C_{\mathrm{var-min}}$	C_{fixed}	$\frac{C_{\mathrm{var-max}}}{C_{\mathrm{var-min}}}$	$\frac{f_{\max}}{f_{\min}}$
F_{osc} = 10 GHz	C	$0.4\times C_{\mathrm{var-min}}$	3	1.55
F_{osc} = 50 GHz	$0.2\times C$	$2\times C_{\mathrm{var-min}}$	3	1.28

Table 2-3 provides a numerical comparison between tuning range at oscillation frequencies of 10 GHz and 50 GHz. In the numerical example, two main design points are assumed:

1) The ratio between $C_{var\text{-}max}$, and $C_{var\text{-}min}$ is fixed with frequency.
2) Both inductance and capacitance of LC tank are scaled down five times to increase oscillation frequency from 10 GHz to 50 GHz.

Even with these relaxed assumption, it can be noticed that the tuning range is shrunk down by 50%. Therefore, the implementation of wide tuning mm-wave frequency synthesizer, or VCO is very challenging.

2.4.3 Phase noise and passive elements

Basically, there is a sufficient degradation in quality factor of inductors at mm-wave frequency due to:

- Current crowding in metals which result in skin and proximity effects.
- narrow eddy current loops.
- Strong capacitive and magnetic coupling to substrate.

Moreover, the quality factor of varactors can be below than 10 at mm-wave frequency (beyond 60 GHz). Also, the quality factor of switch capacitors bank is limited by switches' size which raises a trade-off with tuning range. Therefore, the overall quality factor of LC tank degrades at mm-wave frequencies.

In general, the mm-wave frequency suffers from high phase noise due to:

- High oscillation frequency.
- Low quality factor of LC tank as discussed before.
- Low output swing which introduces a trade-off between phase noise and overall power consumption.

2.4.4 Layout and modeling accuracy

The performance of transistors and passive elements (i.e., Inductor, and capacitors) depends mainly on the substrate doping, the oxide and metal stacks, and the transistor's parameters (F_T, F_{Max}). The metal/oxide stack can be simulated, using EM solvers, to develop the models for passive elements. However, even with the improvement in simulators' accuracy, modeling of passive elements suffers from several technical issues:

- The exact geometry of the stack is often unknown to the designer, and most foundries do not provide this information.
- The material parameters, such as the permittivity and loss tangent of the layers, is also not known exactly, especially at mm-wave frequencies.

- Layout complexity increases with the continuous scaling of CMOS technology. This complexity results from the strict process design rules with the purpose of yield maximization. As an example, extra dummy metal layers should be added to meet density rules and wide metal lines should be slotted. This, in turn, increase the complexity of passive elements' modeling as most of EM solvers have difficulty to simulate these complex structures at mm-wave frequency.

Furthermore, the CMOS transistors and passive elements' models provided by most foundries are usually not characterized at mm-wave frequency. It is important to note that the performance of CMOS transistors operating at mm-wave frequency is largely affected by the interconnect at the transistor terminals and intrinsic parasitics which reduce the device (F_T, F_{Max}) significantly from reported values for an intrinsic device. It was observed that RC extraction is not sufficient to model these parasitics.

Since the wavelength of on-chip signals approach circuit dimensions, the interconnect between components becomes crucial part of design. These interconnects must be simulated in EM solvers to incorporate the effect on circuit performance. Depending on the type of interconnect, this step is generally time consuming especially if multiple metal layers and vias are included.

Furthermore, at the layout level, due to close proximity of components the overall layout also needs to be simulated for unwanted coupling and losses. Asymmetric layout of the RF paths at 60 GHz is a potential issue especially in circuits requiring phase accuracy. Layout parasitics are also a major contributor for frequency shift and performance degradation and demand careful RLC extraction.

Therefore, due to modeling inaccuracy, mm-wave frequency synthesizers suffer from large variation in operating frequency, locking range, and tuning range.

2.4.5 State-of-art mm-wave frequency synthesizers

In order to overcome the aforementioned challenging issues, several design techniques for high performance frequency synthesizers have been reported recently. Table 2-4 summarizes the state-of-art 60 GHz frequency synthesizers. Several observations and conclusions can be drawn from this table:

1) The only reported frequency synthesizer based on fundamental PLL which covers the whole 57-to-66 GHz band [78] uses two VCOs which results in high power consumption of 78 mW.
2) Most of synthesizers in the mm-wave bands have been implemented based on integral-N PLL.
3) Synthesizers in the mm-wave bands still rely on analog PLL's for several reasons:
    - Poor tuning resolution of conventional digitally controlled oscillators (DCOs).
    - Quantization noise and non-linearity of the time-to-digital converter (TDC) which replaces the functionality of the PFD/CP in analog PLL's.
    - The design of TDC's and frequency dividers operating at mm-wave frequency poses enormous challenges.
4) The only reported fractional-N ADPLL [79] uses a 32X ILFD/CML divider chain in the DCO-TDC interface which results in high power consumption (> 0.5 of total power), large area, and high in-band phase noise.

Table 2-4 Comparison between state-of-art mm-wave frequency synthesizers

Spec\ Ref #		ISSCC'09 [78]	TCAS'11 [80]	JSSC'11 [19]*	JSSC'14 [81]	JSSC'14 [79]	ISSC'14 [82]	JSSC'16* [34]
Architecture		CP analog PLL	Bang-Bang ADPLL	20GHz analog PLL	CP analog PLL	**TDC-ADPLL**	Sub-sampling PLL	20G Sub-sampling PLL
Type		INT-N	INT-N	INT -N	INT -N	**FRAC-N**	INT-N	INT-N
Output frequency (GHz)		**57-66** (14.6%)**	38.5-41.5 (7.5%)	58-63 (8.3%)	58-68.3 (8.3%)	56.5-63.5 (11.6%)	53.8-63.3 (16.2%)	58.3-64.8 (10.5%)
Ref. frequency (MHz)		100	156.25	36	135	100	40	40
Phase noise (dBc/Hz)	1 MHz	-75	-83.8	**-95**	-91	-90	-88.3	-92
	10 MHz	-	-	-	-	-110	-108	-122
Spurs level (dBc)		-42	-48	-	-45	**-74**	-40	**-73**
Ouput power (dBm)		-24	-	-10	-20.34	**0**+	-20	-18.2
Locking Time (µs)		-	15	-	-	3	-	-
RMS jitter (fs)		-	300.9	-	**238.4**	590.2	220	290
Supply (V)		1.1	1.2	1.2	1.2	1.2	1	1
Power (mW)		78	46	80	24	**52**	42	32
Area (mm2)		0.82 With pads	0.3	1.68	0.192	0.48	0.16	1.09 With pads
Technology (nm)		45	90	65	65	65	40	65

* Use Injection lock oscillator (Third harmonic) to generate output frequency from 20GHz PLL
** Use 2 VCOs to cover the whole output range
+ Use Off-chip buffers

3 Wide Tuning Range Fine Resolution 60 GHz DCO

This chapter presents a wide tuning range mm-wave digitally controlled oscillator (DCO) with very fine frequency tuning granularity. Switched coupled-inductor and switched-capacitor banks provide the coarse tuning to achieve 24% tuning range from 48.1 GHz to 61.3 GHz. A fine frequency tuning resolution of 39 kHz is achieved using capacitive degeneration. The 65 nm CMOS DCO consumes 10mA from 1V supply voltage, and the DCO with output shunt-peaking buffer occupy an active area of 0.0322mm2. The measured max/average/min phase noise at 1 MHz and 10MHz offset are -88.8/-91.9/-95.1dBc/Hz and -114/-116.8/-119.5dBc/Hz respectively. The figure-of-merit varies from -186.4dB to -182.2dB which is better than figure-of-merit of recent mm-wave DCO benchmarks.

3.1 Introduction and motivation

In an ADPLL, the DCO is a critical block as its phase noise, tuning range, and frequency resolution directly affect the PLL performance. The tuning range (TR) of current DCOs at 60 GHz is limited to less than 15% due to significant fixed parasitic capacitance. This is insufficient to meet the requirements of mm-wave communication standards; moreover, additional margin is required to overcome PVT variations. To the best of our knowledge, there is no DCO operating above 50 GHz and achieving tuning range larger than 15%. Furthermore, conventional switched capacitor tuning entails technology-constrained phase-noise (i.e., Q) versus tuning range trade-offs. Multiple VCO's are usually used to overcome the trade-off between phase noise and limit tuning range, which entail other drawbacks including large area and power consumption.

In a DCO, the digital tuning word controls the instantaneous frequency either by directly switching capacitances in the tank, or converting the tuning word to an analog voltage by means of a DAC. In both approaches, frequency can only be changed in discrete steps, and the minimum frequency step is limited by the DAC resolution and the smallest capacitor available in the process, respectively. Since the finite frequency step introduces quantization noise which degrades both in-band and out-of-band phase noise at the synthesizer output [79], it must be made sufficiently small to minimize additional noise over the natural phase noise of the oscillator. For conventional LC-DCO where the output frequency equals $f_{out} = \frac{1}{2\pi\sqrt{LC}}$, the frequency sensitivity to capacitance of LC tank can be expressed as:

$$\frac{\Delta f}{f_{out}} = \frac{-\Delta c}{2C_T} \tag{3-1}$$

where C_T represents total capacitance of LC-tank. Therefore, as an example of 60 GHz DCO with 100 pH inductances and 70 fF capacitance, frequency step of 60 KHz requires capacitance variation less than 0.1 aF which is impractical in CMOS technology due to matching and lithography limitation.

ΣΔ modulation is typically used to achieve fine frequency resolution; however, in a DAC-based DCO, analog filtering is necessary to filter out-of-band quantization noise, while in capacitively dithered DCO, the RF output must be filtered for the same reason [83].

This chapter describes a mm-wave DCO which uses switched capacitor banks and switched coupled inductors [84] to cover a wide tuning range (48.1-61.3 GHz) with a small increase in phase noise degradation. Simultaneously, by using capacitive degeneration [85], it achieves a frequency tuning granularity lower than 40 KHz, thereby reducing or eliminating the need for ΣΔ dithering.

3.2 Design techniques for wide tuning range

Figure 3.1 shows the schematic of the proposed DCO. An NMOS cross-coupled pair with minimum length devices was used to minimize fixed capacitance. The LC tank consists of 2-bits switched coupled inductors, to achieve four different frequency bands, and two capacitors (C_1, C_2) banks to achieve the coarse tuning inside each frequency band. Simultaneously, capacitor banks (C_3, C_4) were used to achieve the fine frequency steps. Moreover, large varactor (C_{big}) was used at the source of cross coupled pair to maintain the desired fine frequency step over the whole operating frequency range.

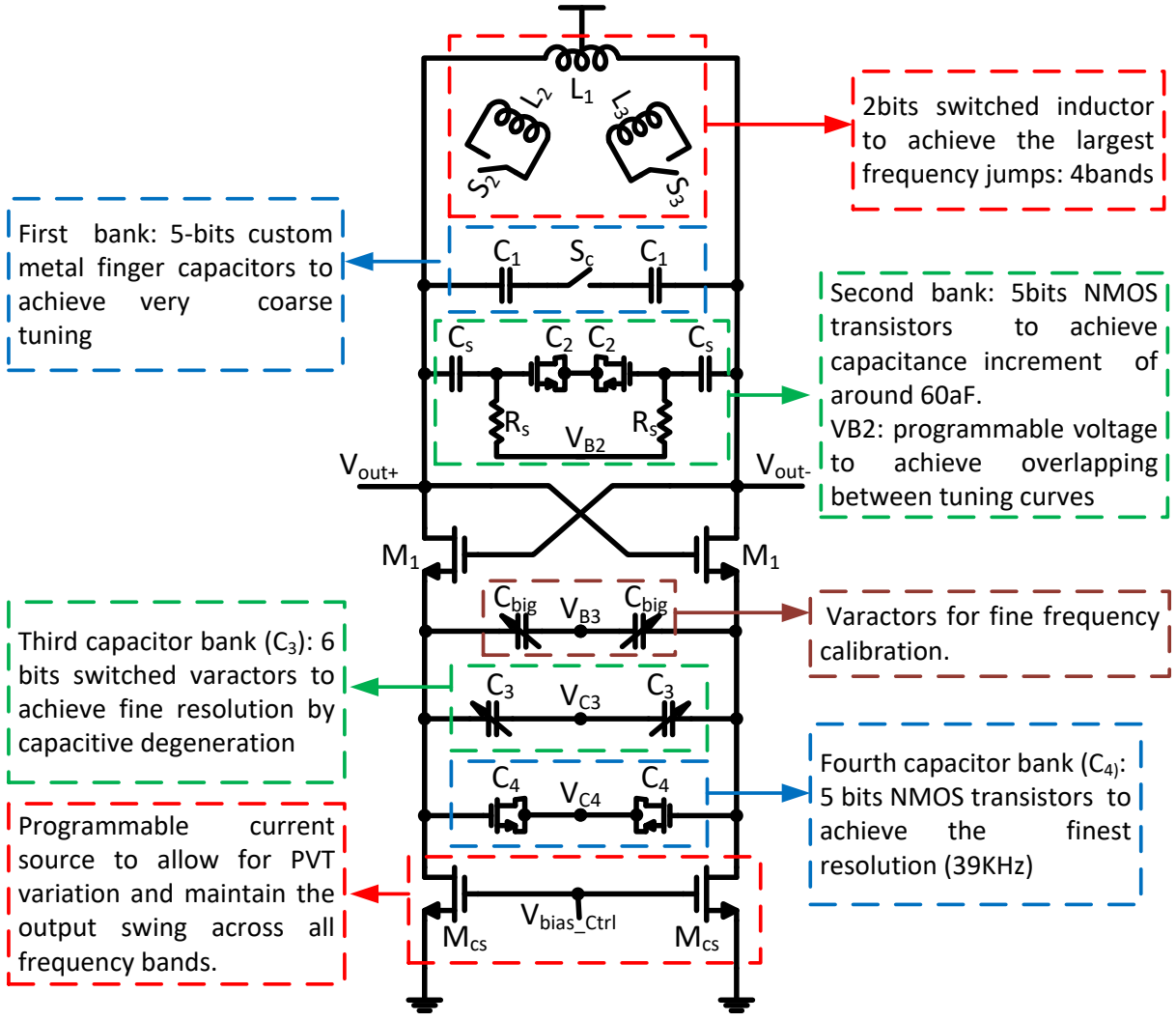
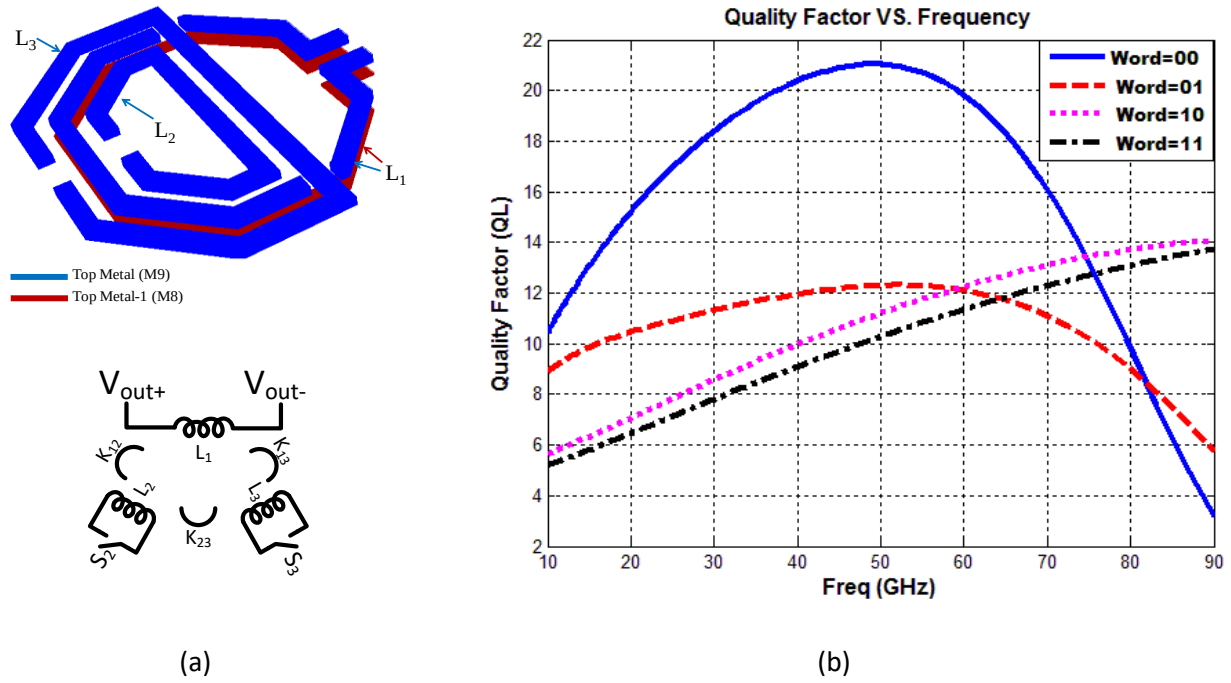


Figure 3.1 Schematic of DCO with four stages of switched capacitor banks and two switched coupled inductors



(a) (b)

Figure 3.2 (a) 3D layout view of proposed transformer. (b) Simulated quality factor (Q_L) for different tuning word of proposed transformer.

Figure 3.2 (a) shows the 3D layout view of the transformer, in which the primary inductor L_1 has one turn in the topmost layer and the layer below it. Two coupled inductors L_2 and L_3 are switched open or short to vary the effective inductance (L_{eff}) seen from the primary side, as shown in Figure 3.1. The variation in the L_{eff} provides wider tuning range than is achievable with switched capacitors alone [84]. Thus, the largest frequency bands are generated by switching L_2 and L_3 using two bits, which form the MSB's of the oscillator tuning word (OTW). Table 3-1 summarizes the parameters of the proposed transformer which was simulated using an electromagnetic field solver (EMX). It can be observed that, the inductance varied from 101.1 pH to 136.5 pH (29.5%) and self-resonance frequency change from 160.6 GHz to 96.4 GHz. Figure 3.2 (b) shows the simulated inductor quality factor (Q_L) versus the frequency for the possible configurations. It can be observed that the highest frequency band which has both switched inductors ON shows the worst-case quality factor of 12 at 65 GHz.

Table 3-1 Summary of transformer parameters for different tuning words

Tuning word	Word = "00"	Word = "01"	Word = "10"	Word = "11"
Inductance (pH)	136.5	123.8	114.5	101.1
Self-resonance frequency (GHz)	96.4	110.2	148.9	160.6
Quality Factor (Q_L)	21.4	15.9	13.9	12.2

Continuously tuned varactors are avoided in the main LC tank due to their low Q at millimeter-wave frequencies; instead, banks of custom switched metal and MOS capacitors are used to achieve the coarse tuning inside each frequency band. Two separate tuning capacitor banks are used as shown in the schematic C_1 and C_2. The frequency resolution provided by each capacitor bank was scaled down with some margin to account for process variation. In the first bank C_1, custom metal finger capacitors were designed with 4 metal layers and wider traces to maximize the quality factor of capacitor bank Q_{C1} at the desired operating frequencies. The switches were sized to guarantee that the worst case Q_{C1} of the bank exceeds 10 over the operating frequency range. The capacitance increment achieved with this binary-weighted capacitor bank was simulated to be around 400 aF.

Minimum length NMOS transistors were used for finer capacitive tuning in capacitor bank C_2, with the drain and the source connected to a control bit. During normal operation, the desired capacitance of each tuning unit can be one of the two distinguishable values at the low gain regions of C-V characteristic [3]. However, the gate is ac-coupled to the inductor and is biased at a programmable voltage V_{B2} to improve frequency resolution. The drawback of using such small NMOS transistors is that the capacitors are more sensitive to variations and mismatch which can lead to high non-linearity in the DCO's tuning characteristic. Post layout simulations show that a capacitance increment of around 60 aF is achieved in capacitor bank C_2 by using a 0.5 μm wide

minimum length finger as the LSB of the capacitor array. The common gate voltage V_{B2} of the capacitor bank C_2 can be programmed by a 4-bit DAC; the tuning range obtained by varying V_{B2} is designed to be larger than the frequency resolution of capacitor array C_1 in order to ensure sufficient overlap between the tuning ranges of these two capacitor banks.

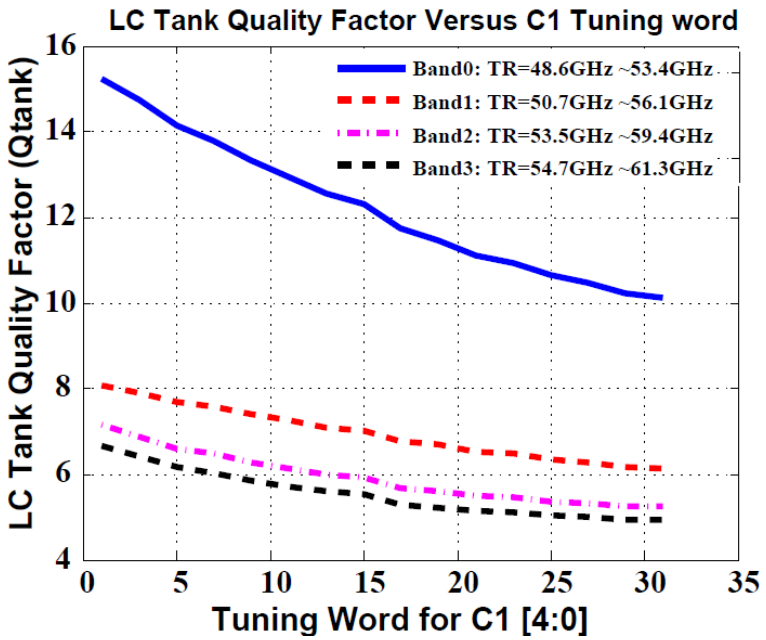


Figure 3.3 Simulated differential quality factor (Q) versus tuning code of capacitor bank C1 for all frequencies bands.

Figure 3.3 shows the simulated differential quality factor Q_{tank} of the complete LC tank versus the C_1 tuning code for the four-possible switched-inductor configurations. The capacitor banks were RC-extracted, and the inductance portion was modeled using an EM field solver tool. As expected, the highest frequency band, in which both switched inductors and switches in C_1 and C_2 banks are ON, has the lowest tank Q of 5.2 across the operating range.

3.3 Fine frequency tuning: Capacitive degeneration

To achieve fine tuning granularity, the DCO employs capacitive degeneration with banks C_3 and C_4 connected between the sources of the cross-coupled pair [2]. The effective capacitance of the degeneration capacitor seen from the tank is negative which allows increasing the inductor

value for the same operating frequency. This, in turn, increase output signal power and reduce phase noise. By defining shrinking factor as:

$$Q_f^2 = \left(\frac{g_m}{2\omega_o C} \right)^2 \tag{3-2}$$

where C is total degeneration capacitor added at the source of NMOS cross pair, g_m is transconductance of the cross-coupled devices and ω_o is the oscillation frequency.

Then, for shrinking factor much lower than one, the effective admittance of cross couple transistors with capacitive degeneration can be expressed as [86]:

$$Y_{eq} = \mathrm{R}_{eq} + j\,\omega_o C_{eq} = -\frac{g_m}{2} - j\,\omega_o C Q_f^2 \tag{3-3}$$

It can be observed that for $Q_f^2 << 1$, adding a small capacitor in order of hundreds atto-Farad at the source of cross coupled transistors results in a very fine oscillation frequency step. However, the shrinking factor changes with transconductance and degeneration capacitor value C as depicted in Figure 3.4. While Figure 3.5 shows the equivalent transconductance and capacitance versus degeneration capacitor.

It can be noted that for $g_m = 10mA/V$, degeneration capacitor should be larger than 150 fF for shrinking factor to be effective. Therefore, a large capacitor C_{big} (Figure 3.1) is added to guarantee that the equivalent capacitor C_{eq} is sufficiently small enough and the variation in the source capacitor banks produces much smaller frequency steps than the main capacitor banks.

An array of switched varactors is used in bank C_3 (L= 500nm), while bank C_4 uses switched MOS transistors with minimum length to implement the finest frequency step. In this design, the capacitance increments in banks C_3 and C_4 are 700 aF and 26 aF respectively, which can be

shrunk to effective increments smaller 2.8 aF and 0.1 aF, respectively; these small increments provide frequency resolution as small as 40 kHz.

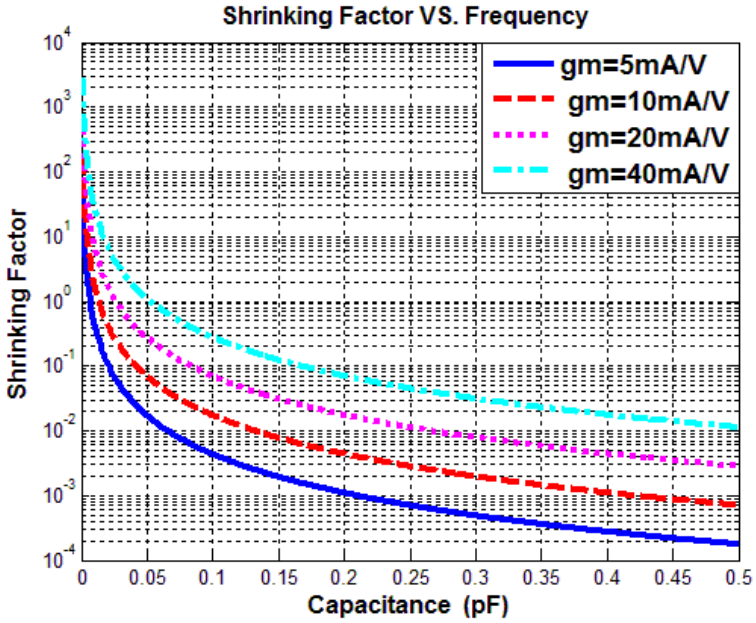
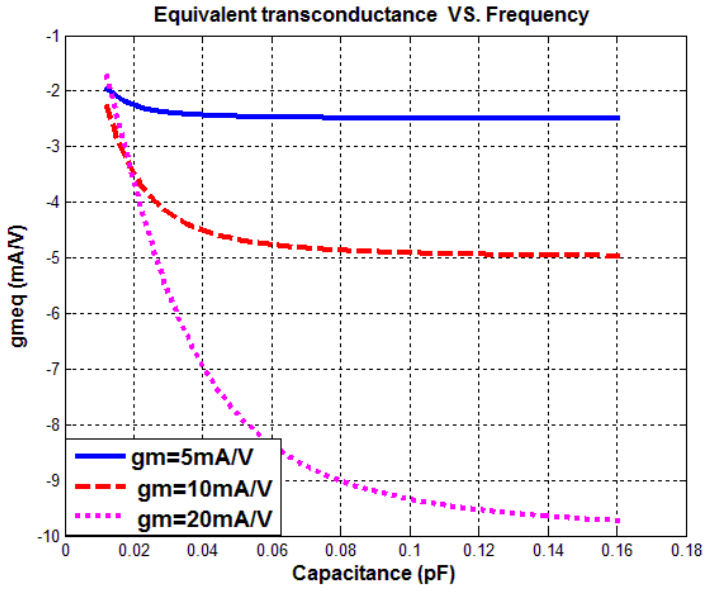
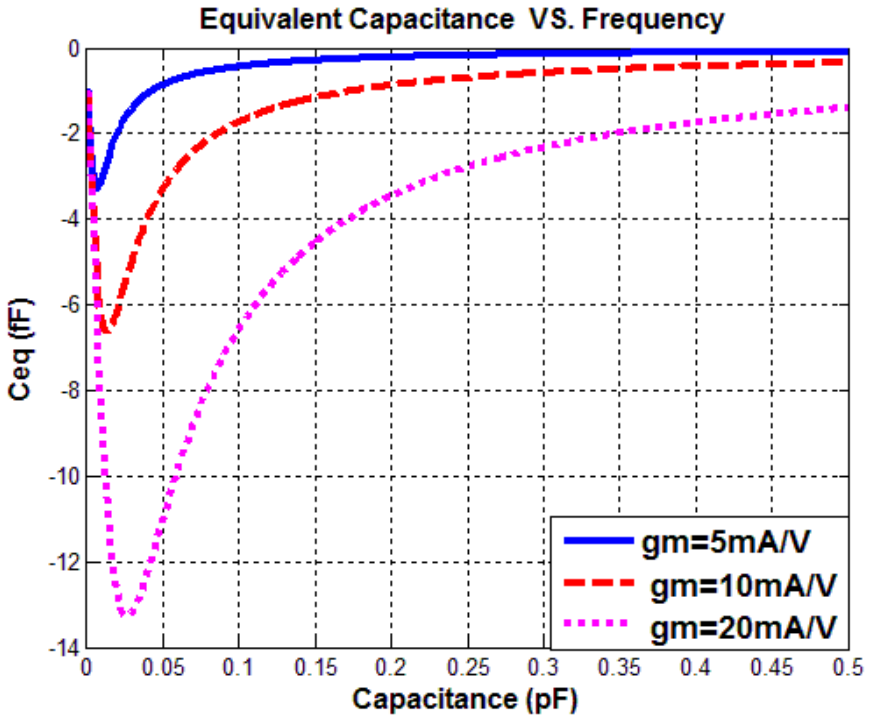


Figure 3.4 Shrinking factor versus degeneration capacitor (f0=60GHz)



$$gm_{eq} = -\frac{g_m}{2}\frac{4C^2\omega_{osc}{}^2}{g_m{}^2 + 4C^2\omega_{osc}{}^2}$$

(a)



$$C_{eq} = -C\frac{g_m{}^2}{g_m{}^2 + 4C^2\omega_{osc}{}^2}$$

(b)

Figure 3.5 (a) Equivalent gm versus degeneration capacitor (f0=60GHz) . (b) Equivalent capacitance versus degeneration capacitor (f0=60GHz)

3.4 Calibration of fine frequency Steps

Since the output swing of DCO changes with oscillation frequency, programmable current source (Figure 3.1) is used to maintain the desired output swing over the whole operating frequency range. However, changing the value of bias leads to a change in the effective transconductance of cross couple transistors which, in turn, changes the shrinking factor and fine resolution step as shown in Figure 3.4.

Moreover, the shrinking factor changes with oscillation frequency and to overcome the above issues with the purpose of maintaining the desired frequency resolution over the operating frequency range, the value of varactor C_{big} is adjusted to change the shrink factor. In other words,

the effective resolution and range of source capacitor banks are changed by changing the bias voltage V_{B3} using a 4-bit DAC. This programmability ensures achieving the fine frequency step and alignment of the tuning range of capacitor bank C_3 with the frequency resolution of capacitor bank C_2 so there would not be a frequency gap between tuning curves.

3.5 Measurement results

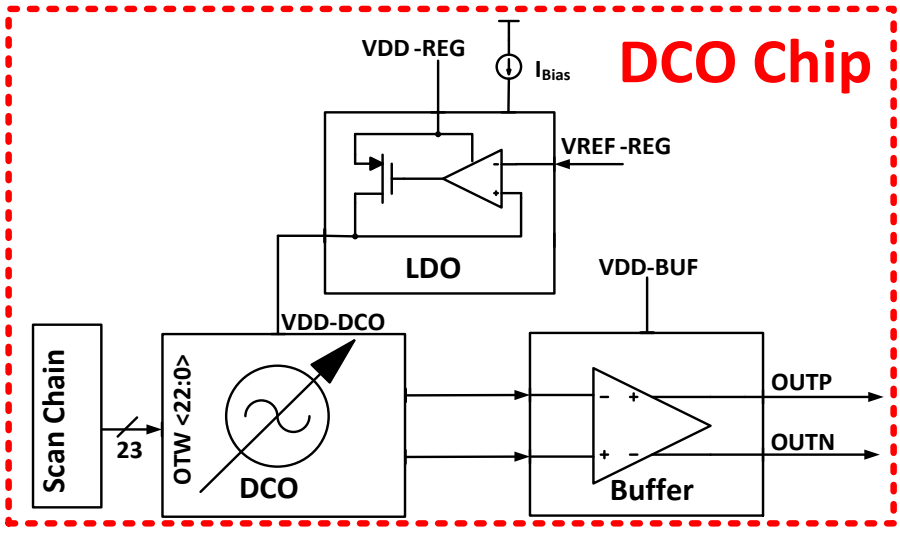
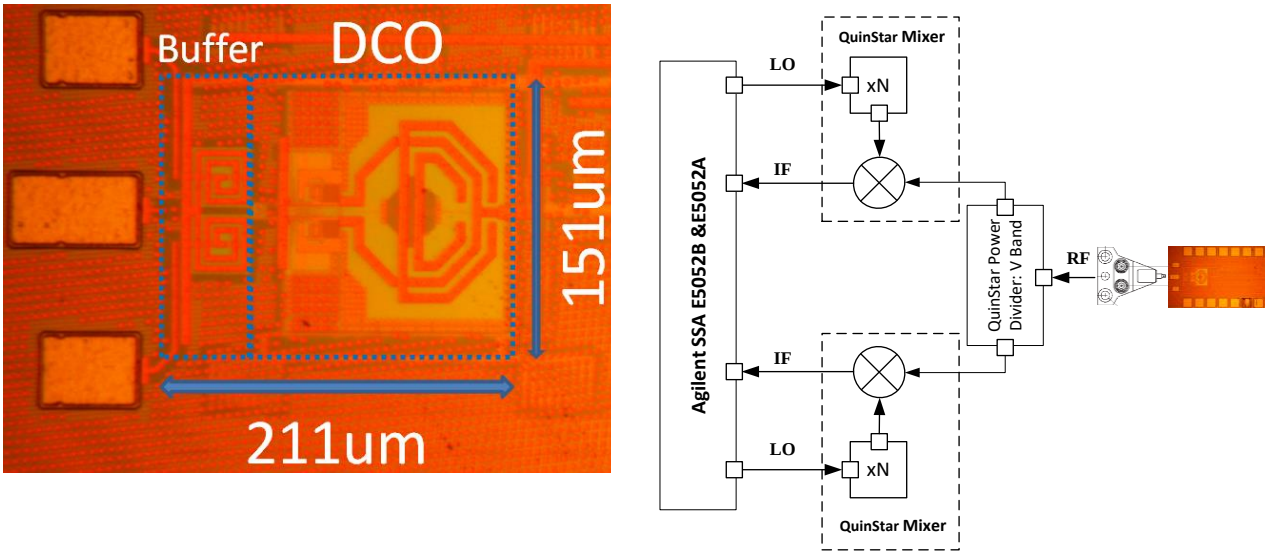


Figure 3.6 Block diagram of DCO chip

Figure 3.6 shows the block diagram of DCO chip which contains the proposed DCO, a differential shunt-peaking buffer to drive 50 Ω measurement loads, and an on-chip low noise LDO to decrease the effect of supply noise on the phase noise. The DCO was fabricated in a 65 nm 9-metal CMOS process. Figure 3.7(a) shows the die photo including the DCO, and output buffer; the bias and control pads (not shown) are located on the top and bottom of the die. As shown in Figure 3.7(a), the core area of proposed DCO and output buffer is 0.0322 mm^2.

The nominal operating point guarantees that sufficient output swing of 500 mVpp is available at the output of the DCO as well as the buffer in all frequency bands. The worst case of output swing happens when all the switches are *ON* and the tank *Q* is at its minimum which corresponds

to the lowest frequency of the fourth band (L_2 and L_3 are both shorted). To maintain 0.5 V swing at this case, DCO and buffer consume 10 mA and 31 mA respectively from a 1 V supply.



(a) (b)

Figure 3.7 a) Die photo of proposed DCO with output buffer. b) Measurement setup for the proposed DCO

The measurement was performed using on-wafer probing using the setup shown in Figure 3.7(b). The DCO output from the probe is split using a Quinstar power divider to generate two RF signals, which are then down-converted by Quinstar V-band mixers. An Agilent E5052B signal source analyzer provides 3.1-6 GHz LO signals to drive the mixers. The IF outputs from the mixers are down-converted again to below 7 GHz using an Agilent E5053A microwave down converter and then input to the E5052B signal source analyzer, which is set up to perform a phase noise and output power measurements.

The oscillator tuning word (OTW) comprises 23 bits: 2 bits for inductor switching and 5/5/6/5 bits for $C_1/C_2/C_3/C_4$ capacitor banks respectively. The two bits for the coupled switched inductors define which frequency band the DCO is operating in. The tuning characteristic of the DCO versus tuning code of the main capacitor banks C_1 and C_2 is plotted in Figure 3.8(a)-(d) with each plot corresponding to four configurations of switched inductors L_2 and L_3.

Figure 3.9 (a) and Table 3-2 summarize the tuning range for all possible configurations of transformer. The overall tuning range of the DCO is 48.1-60.8 GHz; from the measured tuning characteristics, it can be observed that there is sufficient overlap between two consecutive codes of C_1 when sweeping C_2 tuning code.

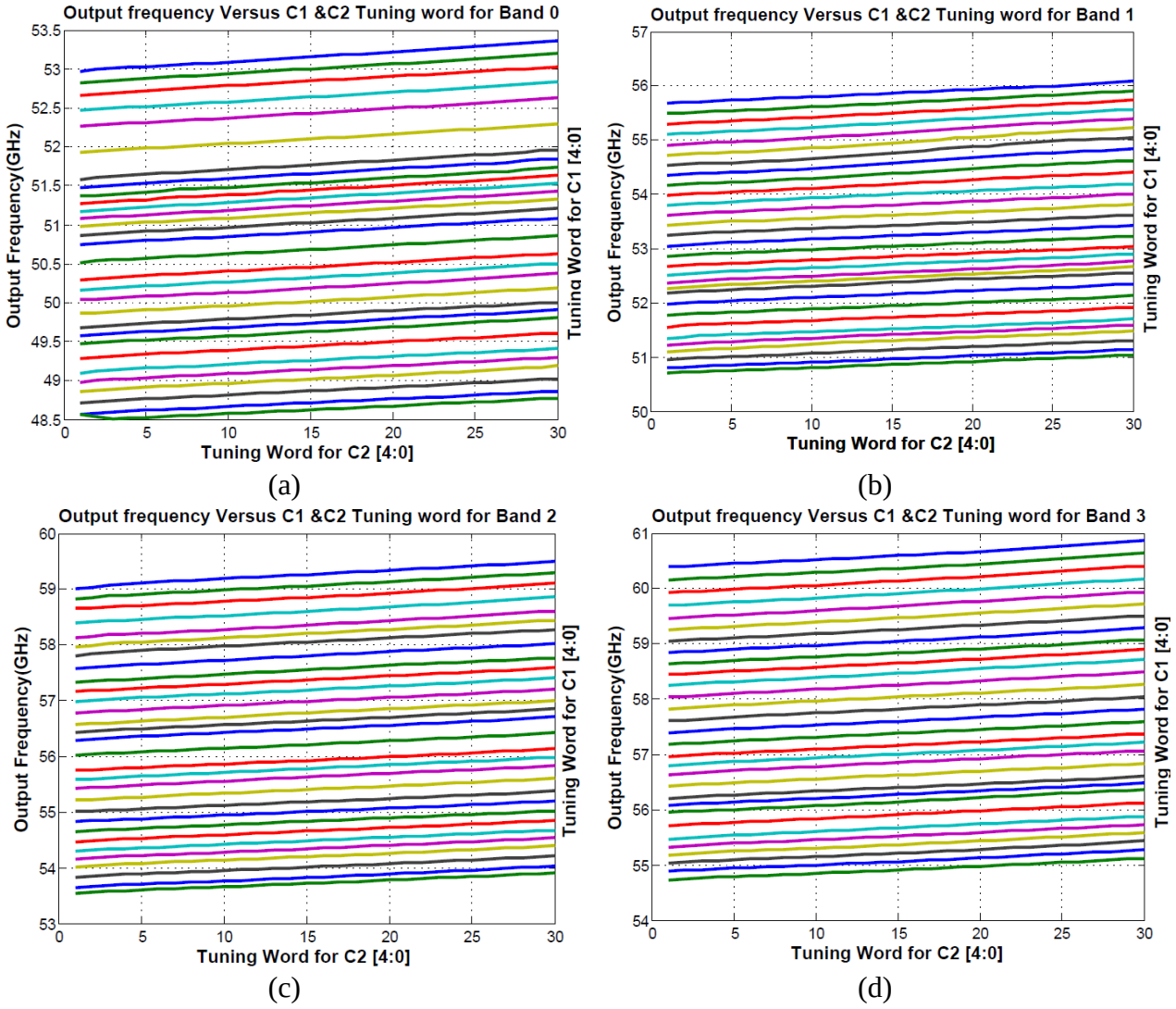
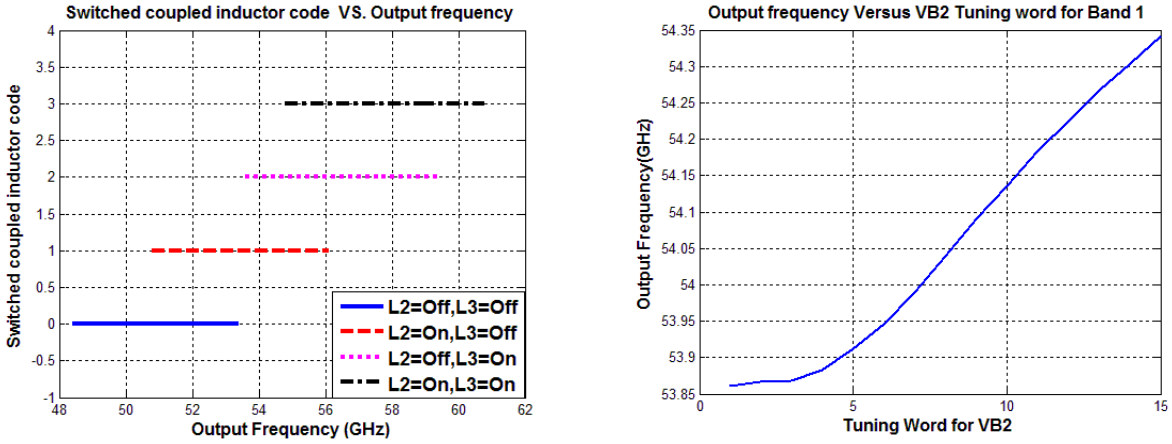


Figure 3.8 Tuning characteristic of DCO versus tuning codes to capacitor bank C1 and C2 a) L2 and L3 switches off b) L2 switch on, L3 switch off c) L2 switch off, L3 switch in d) L2 and L3 switch on

Table 3-2 Summary of tuning range for all possible configurations of transformer

Tuning word	Word = “00”	Word = “01”	Word = “10”	Word = “11”
Covered Range (GHz)	48.1-53.4	50.8-56.1	53.6-59.5	54.8-60.8



(a) (b)

Figure 3.9 (a) Summary of tuning range across possible configurations of proposed transformer (b) Tuning range of capacitor array C2 versus tuning word of VB2

An additional 500 MHz (Figure 3.9 (b)) of tuning range is achieved using the 4-bit DAC that controls the gate bias voltage V_{B2} of bank C_2. The tuning, which extends the upper operating frequency to 61.3 GHz, is larger than the frequency increment (175 MHz) of capacitor array C_1, thereby ensuring sufficient overlap between the tuning curves.

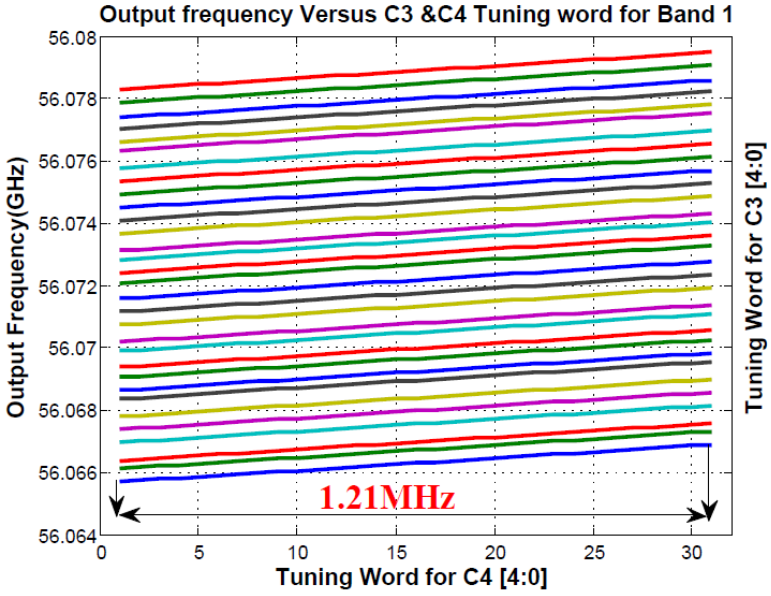


Figure 3.10 Tuning curve of DCO versus tuning codes to cap banks C3 and C4

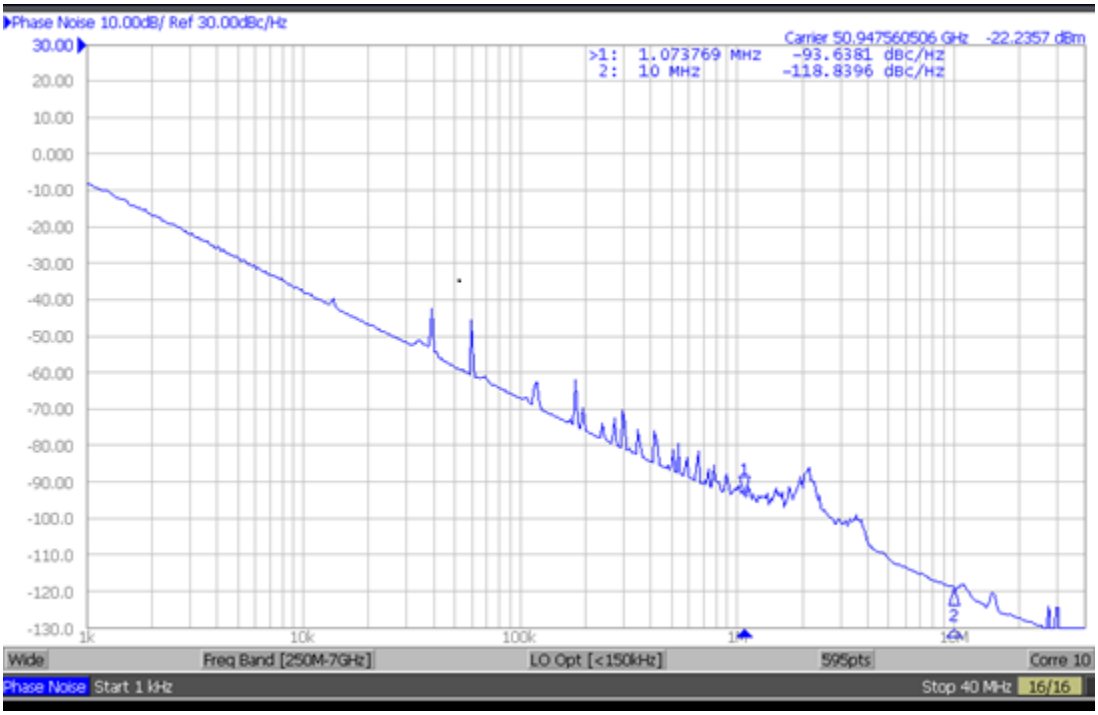
Fine tuning is performed with capacitor banks C_3 and C_4; the varactor C_{big} determines the shrink factor and hence the achievable tuning range. The varactor value is controlled by bias V_{B3} through a 4-bit DAC. Tuning curves of the capacitor banks C_3 and C_4 are plotted in Figure 3.10 when L_2 switch on, L_3 switch off (Band 1). The frequency resolution achieved at each capacitor bank scales down exponentially. Table 3-3 summarize the tuning step of each capacitor bank. It was observed that, from the measurements, capacitor bank C_1 through C_4 on average provide frequency resolution of 174.2 MHz, 12.25 MHz, 450 kHz and 39 kHz respectively.

Table 3-3 Summary of frequency step of capacitor banks

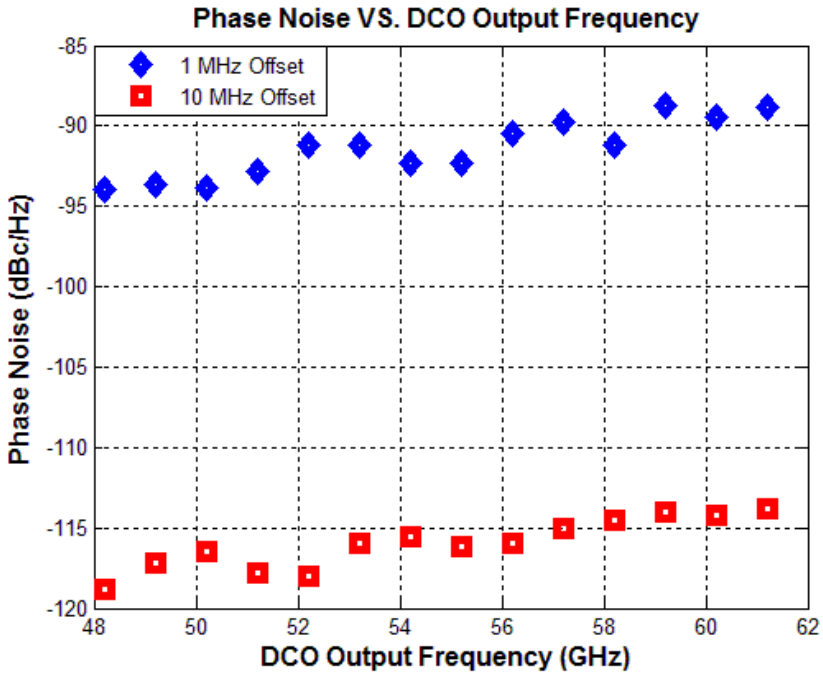
Capacitor bank	C1 (5 bits)	C2 (5 bits)	C3 (6 bits)	C4 (5 bits)
Frequency step	175 MHz	12.25 MHz	450 KHz	39 KHz

The measured phase noise is plotted in Figure 3.11 (a), with the phase noise -93.6 dBc/Hz, which is improved 2 dB using on-chip LDO, at 1 MHz offset from 50.94 GHz and with output power of -22.3 dBm after losses from measurement setup. The phase noise of DCO was also measured at different oscillation frequencies across the tuning range and the result is plotted in Figure 3.11 (b), which shows both phase noise at 1 MHz and 10 MHz offset from the carrier. The highest frequency band which has both switched inductors *ON* shows the worst-case phase noise of -88.8 dBc/Hz, and -114 dBc/Hz at 1 MHz and 10 MHz offset respectively. Table 3-4 provides a performance summary and benchmark comparisons against recent mm-wave DCOs.

With the widest tuning range (24.1%) achieved at these operating frequencies, and with a measured phase noise lower than -88.8 dBc/Hz, at 1MHz offset, the proposed DCO has higher figure-of-merit (-186.4dB ~ -182.2dB) than other recently published DCOs with similar operating frequencies. Moreover, the proposed DCO and output buffer occupy small area compared to the state-of the- art DCOs.



(a)



(b)

Figure 3.11 Measured phase noise a) at carrier frequency of 50.94GHz b) Across the tuning range at 1 MHz offset (blue) and 10 MHz offset (red)

Table 3-4 Comparison between state-of-art mm-wave DCOs

Spec\ Ref #		JSSC'13 [87]	CICC'08 [88]	TCAS'13 [89]	JSSC'14 [79]	**This Work**
Output Freq. (GHz)		56.3-62.1	51.3-53.3	37.6-43.4	56.4-63.4	**48.1-61.3**
TR (%)		10	4	14	11.6	**24.3**
Resolution (Hz)		160K	1.8M	24K*	1.64M	**39K**
Phase noise (dBc/Hz)	1MHz	-95.5~-92.5	-	-	-92	**-95.1~-88.8**
	10MHz	-	-116.5	-109	-	**-119~-114**
Power (mW)		12	2.34	19	11	**10**
Area (mm^2)		0.16	0.09	0.075	-	**0.03**
Output Power (dBm)		-18	-	-10	-16	**-3/-10dBm+**
Technology (nm)		90	90	90	65	**65**
FOM_T (dB)		-177.4~-179	-179.2	-180.6	-178.42	**-186.4~-182**

$$FOM_T = PN(\Delta f) - 20\log\left(\frac{F_{out} * TR}{\Delta f * 10\%}\right) + 10\log\left(\frac{Power(mW)}{1mW}\right)$$

* Using 12 bits dithering controlled by 2nd ∑Δ modulator.

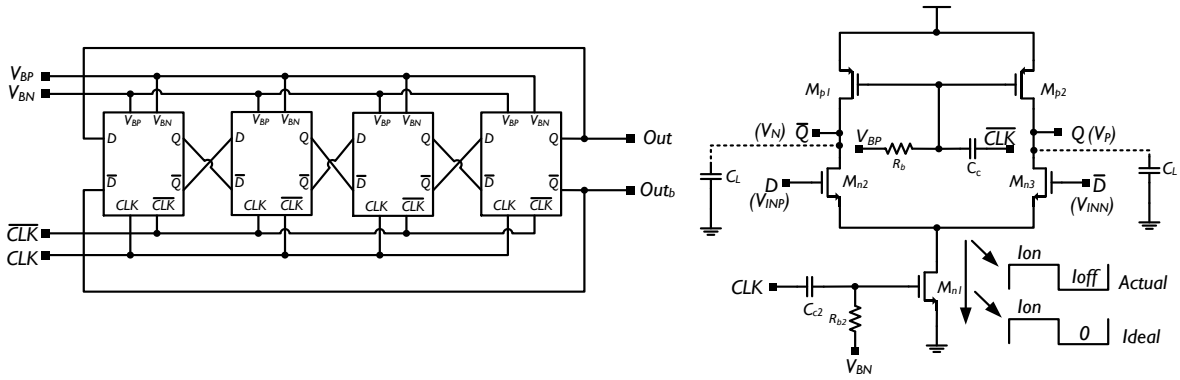
4 Design and Self-Calibration Techniques for Inductor-less mm-wave Frequency Dividers

This chapter presents several design techniques to widen the operating frequency range and increase the locking range of dynamic current-mode latch (DCML) based inductor-less millimeter-wave frequency dividers. A background self-calibration technique is introduced to guarantee frequency locking over a wide frequency range with low input amplitude and over PVT variations, thereby optimizing power consumption and ensuring robustness. Three divide-by-4 prototypes incorporating the aforementioned techniques are designed to cover a frequency range exceeding 16-67 GHz. Fabricated in a 65 nm CMOS technology, the prototypes achieve min-average-max increases of 10%-47.5%-121.4% in fractional bandwidth over the state-of-the-art. The first and third prototypes consume 3.7/6.2 mA (min/max) from a 1 V supply and achieve a figure of merit of 4.1/7.15 GHz/mW (min/max), while the second prototype consumes 3.9/6.7 mA (min/max) from a 1.1 V supply and achieves a figure of merit of 3/6.98 GHz/mW (min/max). The prototypes occupy active areas of 11×42/11×53 μm2 (min/max). Finally, with the self-calibration scheme, the dividers operate with input power less than -10 dBm, supply voltage variation of +/- 100mV and achieve the highest FOM_P reported to date.

4.1 Introduction and motivation

In mm-wave transceivers, common approaches to LO generation include fundamental frequency LO generation [78], [90]–[94] and 2X or 3X frequency multiplication [90], [95]. Also, automotive mm-wave radar transceivers typically use direct frequency modulation using fundamental frequency synthesizers [79].

In all such transceivers, the high-speed frequency divider is a key constituent block that poses serious design challenges in terms of power/area consumption and operating range at mm-wave frequencies. Injection locked frequency dividers (ILFD) [96]–[99] can operate at high frequency with low power consumption, but suffer from large area, limited division ratio, and narrow locking range which is further reduced at higher division ratios [100], [101]. Current mode logic (CML) dividers [102]–[104] are another popular choice, but are very power hungry at mm-wave. The Miller divider [105], [106] is another candidate that can operate at high frequency with low power consumption, but suffers from smaller locking range compared to CML dividers.



(a) (b)

Figure 4.1 (a) Schematic of divider-by-4 circuit. (b) Schematic of the load modulated dynamic CML latches.

In [107], a new class of high speed inductor-less frequency dividers based on dynamic CML (DCML) latches (Figure 4.1(a)) was introduced to achieve wide operating range and low power consumption with small die area. In [108], [109], the load modulation technique was introduced into the DCML latches to improve their locking range and extend the minimum operating frequency (F_{min}). However, both these dividers suffer from several shortcomings. First, the leakage (off-current) of the tail current source (M_{N1}) and finite off-resistances of the load transistors (M_{P1}, M_{P2}) significantly increase F_{min}, thus degrading the locking range. Second, the operating frequency range (F_{max}–F_{min}) is extremely sensitive to parasitic capacitance and

resistance, and to process, voltage, and temperature (PVT) variations. Third, the operating characteristic of the divider is divided into several narrow "sensitivity bands" (e.g., Fig. 8 of [110]); wideband operation is achieved by tuning the bias currents and the loads separately for each band. This adjustment is performed manually in [107]–[110], which is impractical in a mm-wave frequency synthesizer. Fourth, the sensitivity bands in the topology of [107] and [110] become narrower at lower input amplitudes that are typically produced by the LO buffer in a practical mm-wave synthesizer. Nonetheless, it is worth noting that the performance of this divider improves with technology scaling [109], [110].

This chapter introduces several design techniques to increase the operating range under small input amplitude conditions, and demonstrates their effectiveness through three prototype topologies. In section 4.2.2, an accurate time-domain analysis of current DCML dividers [107]–[110] is presented in order to elucidate their limitations. Based on these insights, several new design techniques are proposed and applied to three different topologies, as described in Section 4.3. In the first topology, current bleeding and inter-latch source coupling are introduced to increase F_{max} and decrease F_{min}. The second topology judiciously mixes devices with different threshold voltages to maximize the locking range. The third topology introduces bulk modulation of the tail transistor and adaptive bulk biasing of the load transistors to increase locking range and F_{max}, respectively. Despite these improvements, several bands with individually optimized biases and loads are necessary to cover a wide frequency range. In order to address this issue, a calibration technique is introduced that automatically adjusts bias and load conditions, thereby enabling the divider to lock over an extremely wide frequency range while minimizing power consumption and enhancing robustness over PVT variations. This is described in Section 4.4. Characterization of the three 65 nm CMOS prototypes, presented in Section 4.5, proves robust

self-calibrated operation from 16 GHz to 67 GHz with input amplitude as low as 100 mV (-10 dBm). Section 4.6 compares the proposed divider topologies.

4.2 Limitations of The Conventional Inductor-less Frequency Dividers

4.2.1 Effect of Leakage Current (I_{off}) and Finite Off-Resistance (R_{off})

The load-modulated latch used in the DCML divider [109] is shown in Figure 4.1(b). For a given input amplitude, the bias voltages of the tail current source (V_{BN}) and the PMOS loads (V_{BP}) determine the maximum injection current (I_{on}) and the minimum on-resistance (R_{on}) of the PMOS loads, respectively. The baseline DCML divider using load-modulated latches was analyzed in [109] under the assumption that the tail current source and output PMOS transistors are completely turned off during the hold phase (i.e., $R_{off}=\infty$, $I_{off}=0$). In this section, we present a more accurate time-domain analysis including these effects that provides additional insights necessary to further enhance the operating frequency range.

Waveforms of a load-modulated latch in a locked DCML divider (Figure 4.1(a)) at low input frequency are shown in Figure 4.2(a) by dotted lines for the ideal case, and by solid lines for the case with finite I_{off} and R_{off}. Each latch has two read phases when the tail current source is on and the load capacitances (C_L) (dis)charge causing the outputs to change according to the input data; for the first and third latches in Figure 4.1(a), the read phases are (t_0-t_1) and (t_2-t_3), during which *CLK* is high. During the read phases, assuming that the input differential voltage is sufficiently large to commutate the current in the differential pair completely, the differential output voltage (V_P-V_N) tends towards an amplitude $I_{on}R_{on}$ with time constant $R_{on}C_L$. Each latch also has two hold phases, during which the tail current source and PMOS loads are turned off and the load capacitances maintain their output voltages; for the first and third latches, the hold phases are (t_1-t_2) and (t_3-t_4), during which *CLK* is low.

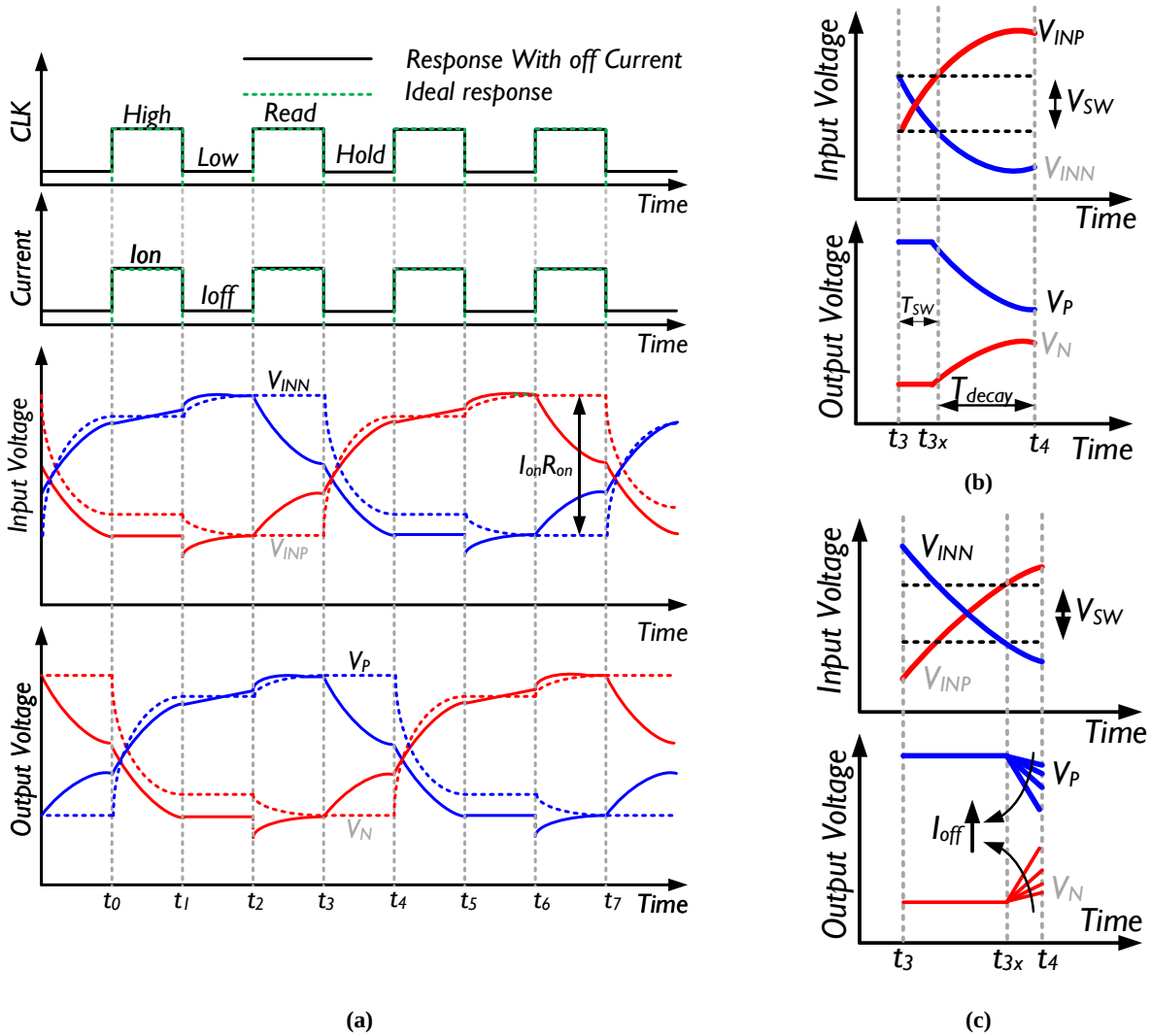


Figure 4.2 (a) Timing diagram of DCML latch when embedded in divide-by-4: ideal response (dotted), and with finite Off current (solid). (b) Second holding phase in case of low input frequency. (c) Second holding phase in case of high input frequency.

To ensure correct operation of the divider, the differential output voltage at the end of each read and hold phase should be higher than the voltage V_{SW} required to switch the following latch. In addition, to achieve lock at high frequency with a practically feasible input amplitude, the bias voltage V_{BN} should be set sufficiently high to increase the injection current during the read phases, while V_{BP} should be small enough to decrease the equivalent resistance of the load transistors. However, for a given input amplitude, this results in a significantly large I_{off} and low R_{off} during the hold phase, which in turn degrades (i.e., increases) F_{min}. It can be observed from

Figure 4.2(a) that the output waveforms with finite I_{off} and R_{off} are similar to the ideal case during the read phases, albeit with different voltage levels. However, during the second hold phase $(t_3$-$t_4)$, when the inputs exchange states, the differential output voltage $(V_P$-$V_N)$ decreases towards -$I_{off}R_{off}$ with time constant $R_{off}C_L$, thus leading to an increase in F_{min}.

4.2.2 Time Domain Analysis of Minimum Operating Frequency

An expression for F_{min} can be derived with reference to Figure 4.2(b), where the second hold phase (t_3, t_4) is divided into two regions: (1) the switching region (t_3,t_{3x}) during which $(V_{INP}$-$V_{INN})$ changes from V_{SW} to -V_{SW} and output voltages (V_P, V_N) remain approximately constant, and (2) the decaying region (t_{3x},t_4) where the $(V_P$-$V_N)$ starts to decay towards -$I_{off}R_{off}$ instead of remaining at $I_{on}R_{on}$ as in the ideal case. F_{min} can be expressed in terms of the switching time T_{SW} and the decaying time T_{decay} as $F_{min} = 0.5/(T_{decay}+T_{SW})$; T_{SW} and T_{decay} can be found using first-order RC equivalent circuit analysis. Assuming that $T_{decay} >> T_{SW}$ in case of low input frequency, and that V_{SW} is between $0.25I_{on}R_{on}$ to $0.75I_{on}R_{on}$ [109] which are both realistic assumptions in the DCML latch.

From Figure 4.1 and Figure 4.2, the latch output voltages V_P and V_N during the read phases (t_0, t_1), and (t_2, t_3) can be expressed as

$$V_P(t) = V_{DD} + (V_{Pi} - V_{DD})e^{-\frac{t-t_i}{R_{on}C_L}}$$
$$V_N(t) = V_{DD} - I_{on}R_{on} + (V_{Ni} - V_{DD} + I_{on}R_{on})e^{-\frac{t-t_i}{R_{on}C_L}} \quad (4\text{-}1)$$

In addition, during the decaying region (t_{3x},t_4), when the differential output voltage $(V_P$-$V_N)$ starts to decay towards -$I_{off}R_{off}$ instead of remaining at $I_{on}R_{on}$ as in the ideal case, the latch outputs can be expressed as:

$$V_P(t) = V_{DD} - I_{off} R_{off} + (V_{P3x} - V_{DD} + I_{off} R_{off}) e^{-\frac{t - t_{3x}}{R_{off} C_L}}$$
$$V_N(t) = V_{DD} + (V_{N3x} - V_{DD}) e^{-\frac{t - t_{3x}}{R_{off} C_L}} \quad (4\text{-}2)$$

In order to maintain frequency lock, the differential output voltage $(V_P\text{-}V_N)$ should be higher than V_{SW} at the end of decaying region. In other words, the following condition should be satisfied

$$V_{SW} \geq -I_{off} R_{off} + \left(I_{on} R_{on} + I_{off} R_{off}\right) e^{-\frac{T_{decay}}{R_{off} C_L}} \quad (4\text{-}3)$$

where T_{decay}, the maximum allowable decaying time to ensure proper operation can be derived as

$$T_{decay} = t_4 - t_{3x} = R_{off} C_L \cdot ln\left(\frac{I_{on} R_{on} + I_{off} R_{off}}{V_{SW} + I_{off} R_{off}}\right) \quad (4\text{-}4)$$

By defining the minimum operating frequency F_{min} as $0.5/(T_{decay}+T_{SW})$, and by deriving $T_{SW} = t_{3x} - t_3$, from (4-1), F_{min} can be expressed as:

$$F_{\min} = \frac{1}{2R_{off} C_L \cdot ln\left(\frac{I_{on} R_{on} + I_{off} R_{off}}{V_{SW} + I_{off} R_{off}}\right) + 4R_{on} C_L \cdot ln\left(\frac{V_{SW}}{I_{on} R_{on}} + 1\right)} \quad (4\text{-}5)$$

An approximate expression for F_{min} can be written as follows:

$$F_{\min} = \frac{V_{SW} + I_{off} R_{off}}{2R_{off} C_L (I_{on} R_{on} - V_{SW})} \quad (4\text{-}6)$$

Equation (4-6) reveals that F_{min} increases approximately linearly with I_{off} of the tail current source. Although I_{off} degrades F_{min}, it improves the F_{max} slightly. Figure 4.2(c) plots the second hold phase in case of high input frequency where the switching time is much longer than decaying time. It can be observed that for given R_{off}, higher I_{off} during the decaying period leads

to smaller differential voltage at the end of second hold phase (t_3-t_4). This, in turn, decreases the time required for differential output voltage to exceed V_{SW} during the next read phase (t_4-t_5) which increases the F_{max}. , Neglecting I_{off} , a simple expression can be derived for F_{max}:

$$F_{\max} = \frac{1}{2R_{on}C_L Cosh^{-1}\left(\frac{I_{on}R_{on}}{I_{on}R_{on} - V_{SW}}\right)} \tag{4-7}$$

Figure 4.3(a) compares the analytical expressions (4-6) against simulations of a divide-by-4 using idealized DCML latches wherein PMOS loads were switched dynamically between explicit resistors R_{on} (during read phase) and R_{off} (during hold phase), the tail current source was switched dynamically between ideal current sources I_{on} (during read phase) and I_{off} (during hold phase), and actual transistors were used for input transistors (M_{n2},M_{n3}). Figure 4.3(b) plots the simulated F_{min} and F_{max} versus I_{off}, and highlights the significant effect of I_{off} on F_{min}. The simulation also reveals a gradual increase in F_{max} as I_{off} increases; in fact, an accurate, but complicated expression for F_{max} can be derived including I_{off}, however, this was not presented here since it offers little insight compared to (4-6).

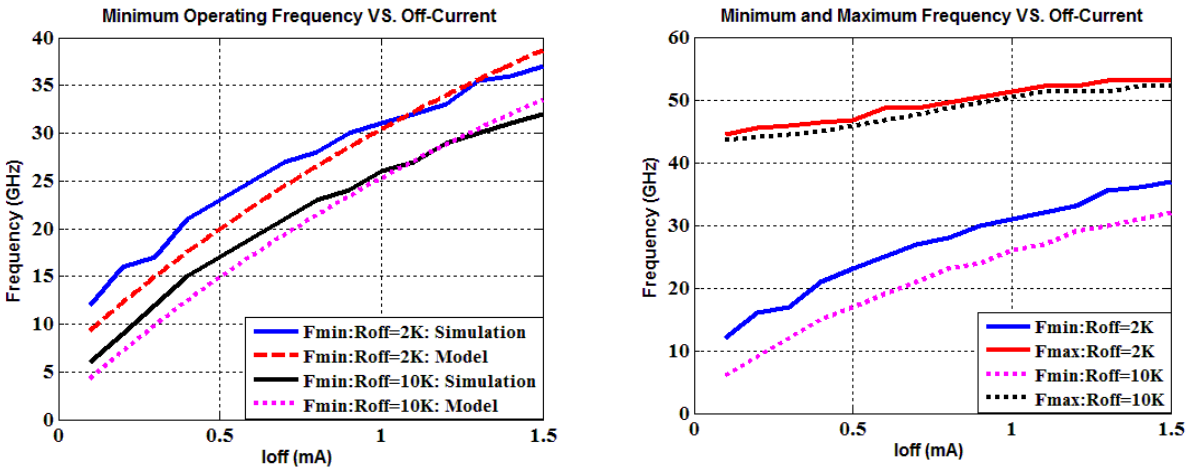
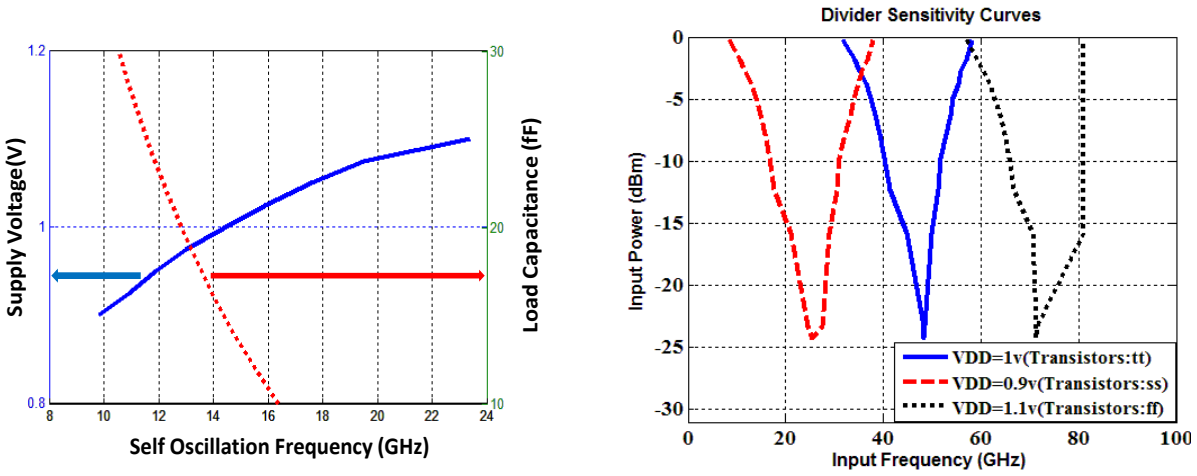


Figure 4.3 (a) Comparison between analytical and simulated Minimum operating frequency versus Off-current (b)Simulated maximum and minimum operating frequency versus Off-current

4.2.3 Effect of PVT Variations

Equations (1) and (2) show that the operating range of the DCML divider is highly sensitive to the parasitic capacitance and resistance of the load transistors. The former is exacerbated from modeling/extraction uncertainties while the latter varies with supply voltage, threshold voltage and process parameters. Figure 4.4(a) shows the simulated variation in self-oscillation frequency (F_{OSC}) of the DCML divider (Figure 4.1) with supply voltage and load capacitance (C_L). The bias voltages of the tail current source (V_{BN}) and the PMOS loads (V_{BP}) are set to 650 mV, and 325 mV respectively. Load capacitance is swept with the supply voltage held at 1 V, and supply voltage is swept with an extra 15 fF added to the 43 fF intrinsic capacitance at the output nodes.



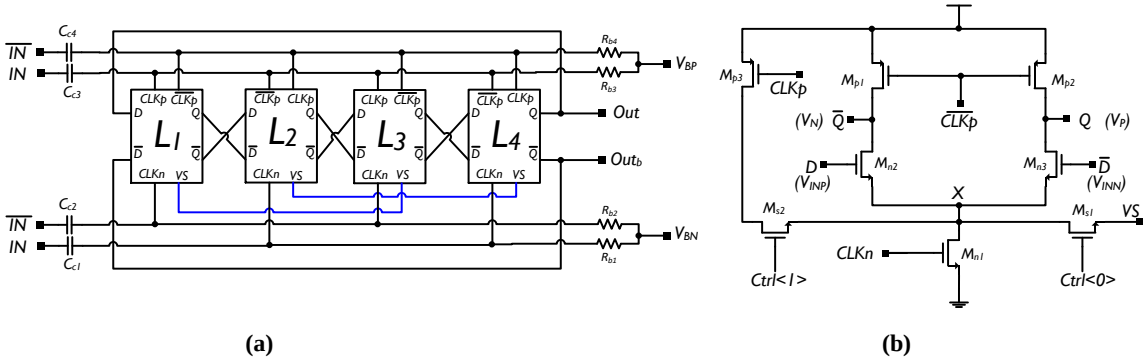
(a) **(b)**

Figure 4.4 (a) Self oscillation frequency variation with supply voltage (solid) and parasitic capacitance (dotted). (b) Simulated sensitivity curve for different supply voltages and process corners.

It can be seen that variations as small as a few millivolts in supply voltage or a few femto-farads in $C_{L,}$ cause shifts of several GHz in $F_{OSC.}$ In addition, for given input amplitude, process and temperature variations affect the threshold voltage, which in turn causes variations in the maximum injection current, the switching threshold V_{SW} of the differential pair, and equivalent resistance of output transistor. Figure 4.4(b) shows that, according to simulations, the sensitivity curve can shift by more than 25 GHz over process and typical supply voltage variations (100

mV). This underscores the need for automatic calibration. Furthermore, it is seen that the operating range becomes narrower at higher V_{DD} and at the fast-fast corner; this is due to: (1) higher I_{off} of the tail current source and load transistors which increase F_{min}, and (2) higher V_{OV} of the differential pair which limits F_{max}. Moreover, PVT and mismatch variations degrade the input duty cycle which in turn degrades both F_{max} and F_{min} due to decreased times available for the read or hold phases.

4.3 Proposed Wide Locking Range Frequency Divider Topologies



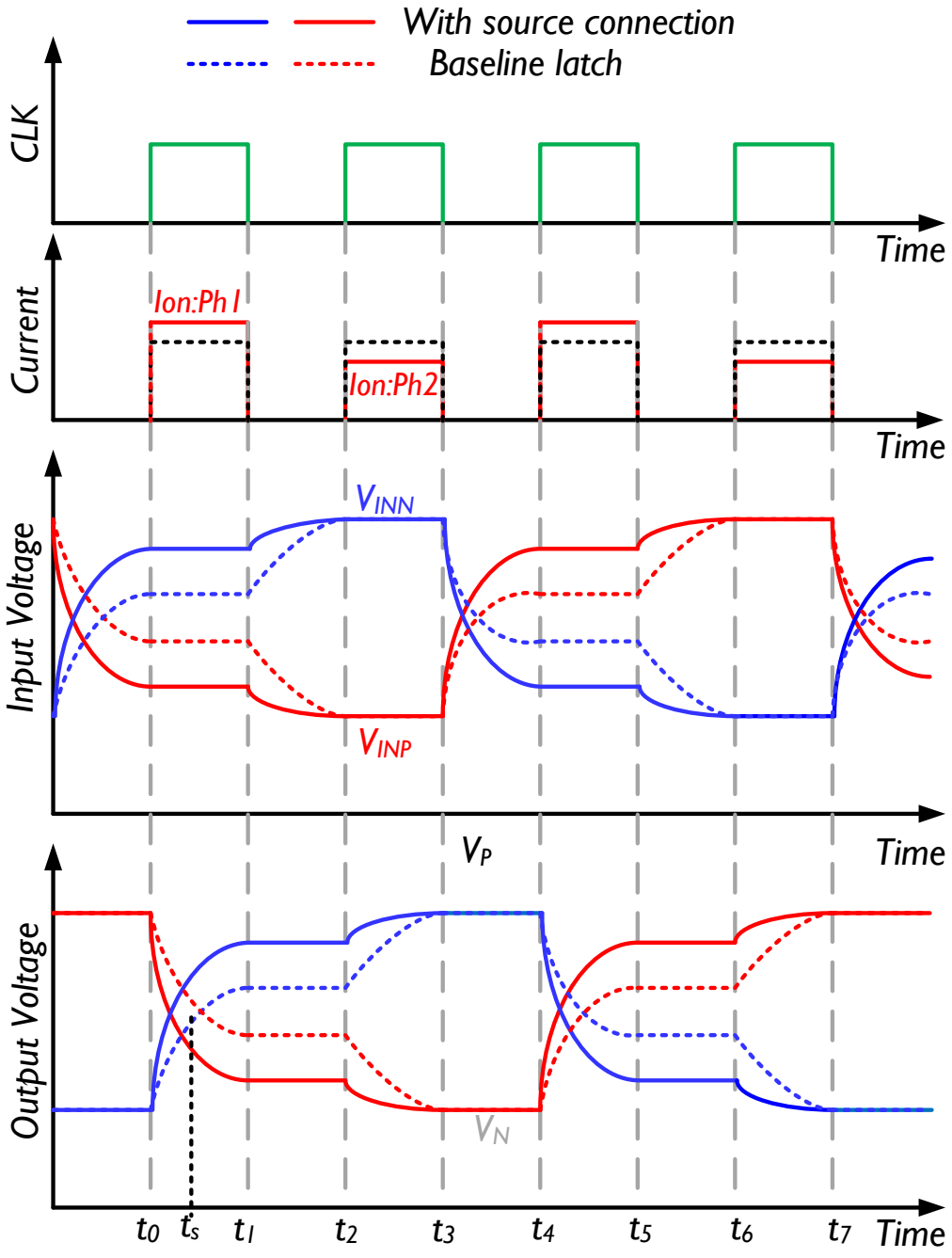
(a) **(b)**

Figure 4.5 DCML divider using source coupling and current bleeding. The configurations DIV1-0, DIV1-SC, DIV1-CB and DIV1-SC+CB can be realized by turning on the switches Ms1 or Ms2.

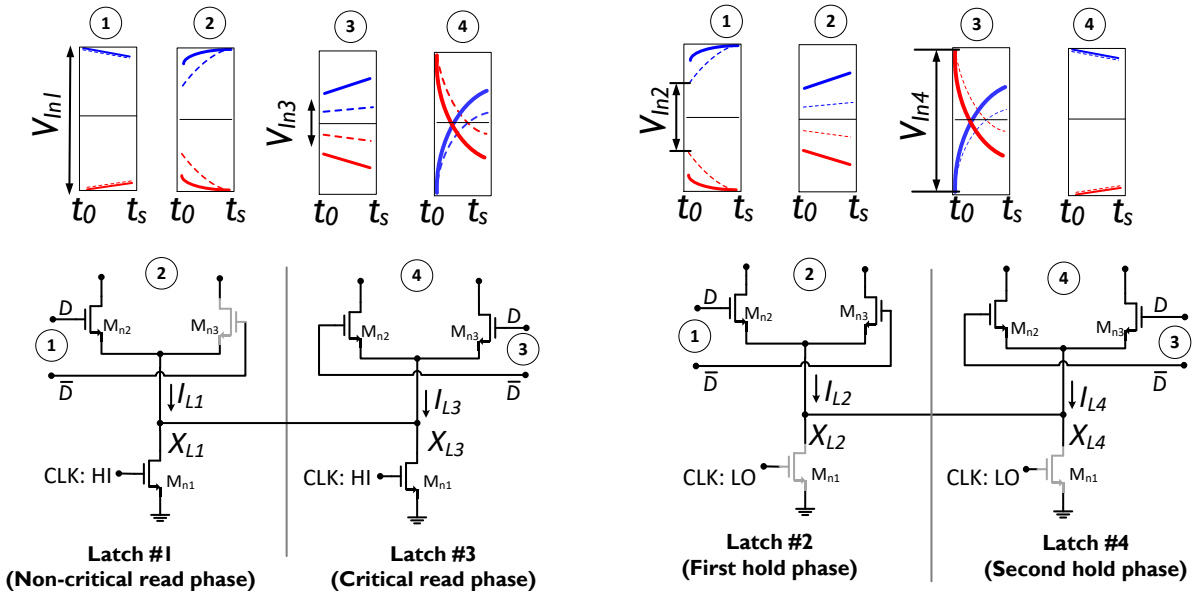
4.3.1 First Topology (DIV1): Current bleeding and source coupling

Figure 4.5(a) shows the schematic of the DCML divide-by-4 circuit employing source coupled DCML latches, each incorporating current bleeding. The input signals (IN, $\overline{IN}$) are ac coupled to the latch cores via common RC networks with appropriate bias levels V_{BN} and V_{BP}. The modified DCML latch (Figure 4.5(b)) can be configured in one of four modes: (1) Baseline mode (DIV1-0) with both MS1 and MS2 off (2) Source-coupled mode (DIV1-SC) with MS1 on and MS2 off, (3) Current bleeding mode (DIV1-CB) with MS1 off and MS2 on, and (4) Combined current bleeding and source coupled mode (DIV1-CB+SC) with both MS1 and MS2 on. The baseline DIV1-0 latch and the resulting divider provide a reference to compare the proposed dividers in the same technology node. DIV1-0 has been designed to maximize locking

range for a given power consumption; the methodology described in [109], [110] is used to size the output loads, tail current source, and input differential pair.



(a)



(b) (c)

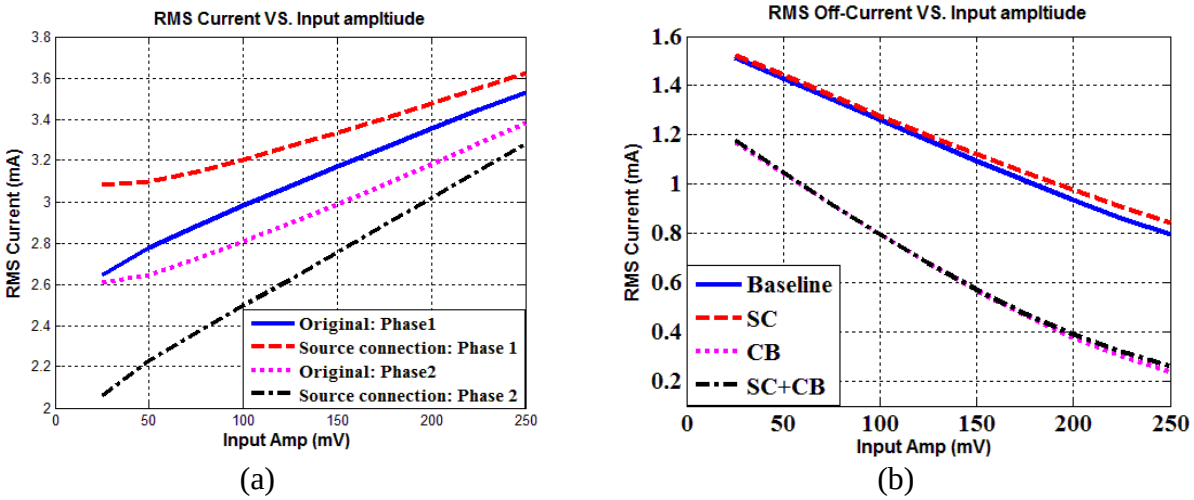
Figure 4.6 (a)Timing diagram of DCML latch (L3) when embedded in divider by 4: ideal response with Roff=∞, Ioff=0 (dotted), and with source connection (solid). (b) Current flow between L1 and L3 during first read phase (c) Current flow between L2 and L4 during first read phase. Note: In (b) and (c), all bounding boxes for the waveforms represent the same scale

As noted in the previous section, the time required for the differential output voltage to exceed V_{SW} during the read phase (t_0-t_1) should be reduced in order to increase the operating frequency. This can be done by increasing the injection current (I_{on}), but in order to do so without increasing the overall current consumption, the sources of the differential pairs of alternate latches driven by the same clock (i.e., L_1-L_3 and L_2-L_4) are coupled as shown in Figure 4.5(a). The operation of this technique can be understood by examining the idealized waveforms of latch L_3 during L_3*'s* critical read phase (t_0-t_1), as shown in Figure 4.6(a). During this period, L_1 is in its non-critical read phase, while L_2 and L_4 are in their hold phases. In essence, source coupling results in using a fraction of the tail current of L_1 to provide the injection current in L_3 during L_3*'s* critical read phase (t_0-t_1). This is achieved at the expense of less injection current in L_3 during its non-critical read phase (t_2-t_3).

Conceptually, there are two reasons why source coupling increases injection current and therefore F_{max}, as described next. To understand the first reason, refer to Figure 4.6(b) which shows the input pairs and voltages of L_1 and L_3 during (t_0-t_1) before the instant t_s when the outputs of L_3 switch states. Before the instant t_s, the differential input voltage of L_1 (V_{IN1}) is higher than the differential input voltage of L_3 (V_{IN3}). Therefore, in the baseline divider where the sources are not coupled, the voltage at node X_{L1} is higher than that at node $X_{L3.}$ Hence, the injection current in L_1 is higher than that in L_3. However, this simply increases power consumption without increasing F_{max} since L_1 is in its *non-critical* read phase while L_3 is in its *critical* read phase. On the other hand, in DIV1-SC where the source nodes X_{L1} and X_{L3} are coupled to each other, the voltage at the coupled node attains a level between the levels of X_{L1} and X_{L3} in the un-coupled case. Therefore, for the same power consumption, higher injection current is available to L_3 compared to the baseline case. This, in turn, increases F_{max}.

To understand the second reason, refer to Figure 4.6(c) which shows the input pairs and voltages of L_2 and L_4 during (t_0-t_1) before the instant t_s when the outputs of L_3 switch states. The latches L_2 and L_4 are in their hold phases during this interval. Due to the non-zero tail current, the differential output of L_2 increases during (t_0-t_1), whereas the differential outputs of L_4 decrease slowly since its inputs – L_3*'s* outputs – are switching states. Before switching instant t_s, the differential input voltage of L_4 (V_{IN4}) is higher than differential input voltage of L_2 (V_{IN2}). Therefore, in the baseline divider, node X_{L4} is at a higher voltage than X_{L2}. When X_{L2} and X_{L4} are coupled as in DIV1-SC, the voltage at the coupled node is lower than the voltage at X_{L4} in the baseline divider. Therefore, the average current flowing into L_4 (which is in its second hold phase) during (t_0-t_1) is lower than the baseline case, while the average current flowing into L_2 (which is in its first hold phase) is higher than the baseline case. Therefore, the differential output

of L_2 (differential input of L_3) increases faster than in the baseline case, which increases the source voltage of input pairs of L_3. This, in turn, leads to higher injection current in L_3 due to channel length modulation of the tail transistor in L_3. The insights gained above are verified by simulation. Figure 4.7(a) compares the RMS on-current I_{L3} during first and second read phases of DIV1-0 and DIV1-SC when the tail current source is biased at 600mV and driven by 66GHz signal. As predicted by the above analysis, the source coupled case achieves higher injection current in the critical read phase, and lower injection current in the non-critical read phase, thereby leading to an increase in F_{max} without increasing overall power consumption.



(a) (b)

Figure 4.7 Comparison between RMS On-Current of DCML latch without and with source connection. (b) Comparison between RMS Off-Current of first architecture in all possible configuration

The source coupling technique nonetheless suffers from a drawback for low input frequency. Due to faster switching in the first read phase, the differential output voltage at the end of this phase is higher in DIV1-SC than in DIV1-0, as shown in Figure 4.6(a). Since this is the second hold phase of the following latch (L_4 in this discussion), it exacerbates the effect of I_{off} for the following latch (Figure 4.2). However, as discussed in the previous paragraph, the off-current that flows through the source of the input pairs of any latch in DIV1-SC (i.e., L_4 in this discussion) decreases during the second hold phase; this partially alleviates the impact of source

coupling on F_{min}. The combined effect of these two effects is a small increase in F_{min} in DIV1-SC.

In order to extend downwards the operating frequency range, a current bleeding transistor M_{P3} is introduced next (DIV1-CB). During the read phase, with CLK_n low and CLK_p high, M_{P3} is turned off and the latch operates as before. During the hold phase, M_{P3} is turned on and absorbs most of I_{off}. This helps maintain the correct output state, thereby decreasing F_{min}. The size of M_{P3} has an important effect on the operating frequency range. Increasing the size of M_{P3} helps to absorb a larger I_{off} which enhances F_{min}. However, this increases leakage current through M_{P3} during the read phase and adds capacitance at the source of the input pair, which absorbs a part of the injection current during the read phase. Post-layout simulations of DIV1-CB conducted with different sizes for M_{P3} resulted in an optimum device size of 4μm/60nm transistor.

In order to improve both F_{max} and F_{min}, source coupling and current bleeding were combined, resulting in DIV1-CB+SC. Figure 4.7(b) compares the simulated average RMS current flowing in the input pair during the hold phases of the four DIV1 configurations. It can be observed that the current bleeding technique reduces I_{off} significantly and this reduction increases with increasing input amplitude. This in turn decreases F_{min}. For example, examination of Figure 4.7(b) together with Figure 4.3(a) reveals that at 100mV input amplitude, current bleeding decreases I_{off} from 1.22mA to 800uA, resulting in a decrease in F_{min} of more than 8 GHz.

4.3.2 Second Topology (DIV2): Mixed V_t Design

The second proposed latch topology, shown in Figure 4.8, uses devices with different threshold voltages. Low-V_t (LVT) devices are used in (1) the tail current source to increase the injection current, and (2) the input differential pair to commutate current completely faster than

regular-V_t (RVT) devices. From Equation (2), this increases F_{max} for a given input amplitude and input capacitance.

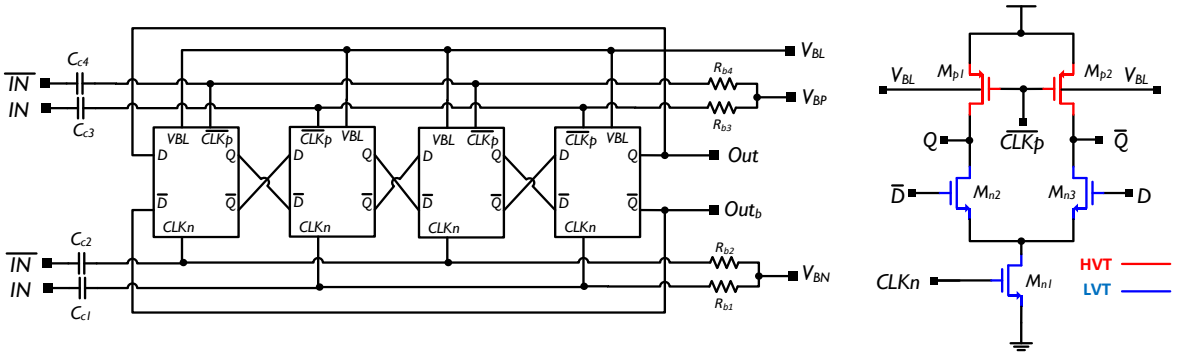
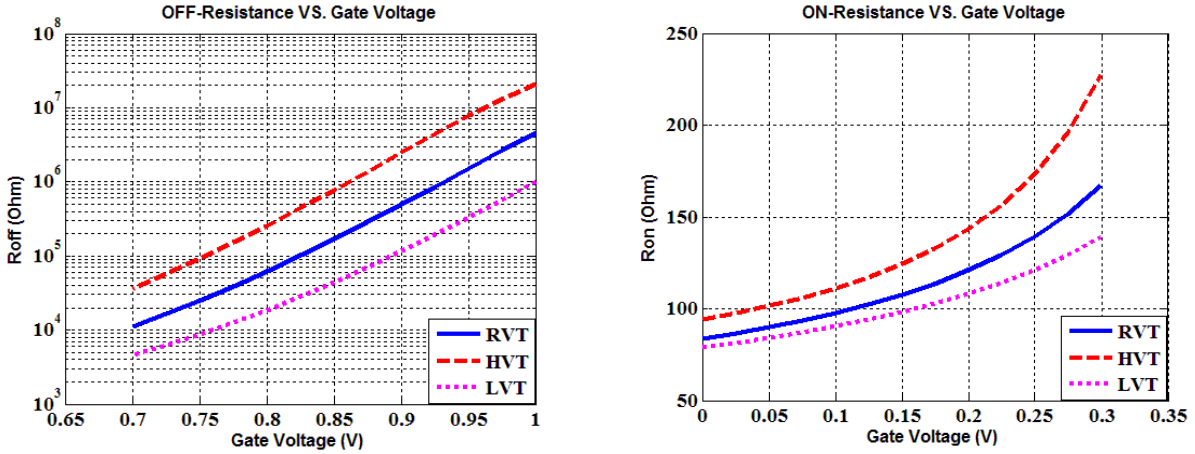


Figure 4.8 Second architecture of DCML divider based on HVT and LVT devices

In a mm-wave divider, the bias voltage V_{BP} of the PMOS loads is usually made small (e.g., < 300mV) to decrease the load time constant. However, for practical input amplitudes, the PMOS loads do not turn completely off resulting in a relatively small equivalent resistance during the hold phase. This degrades F_{min} and results in narrow locking range. To mitigate this degradation, high-V_t (HVT) devices are used for the PMOS loads.

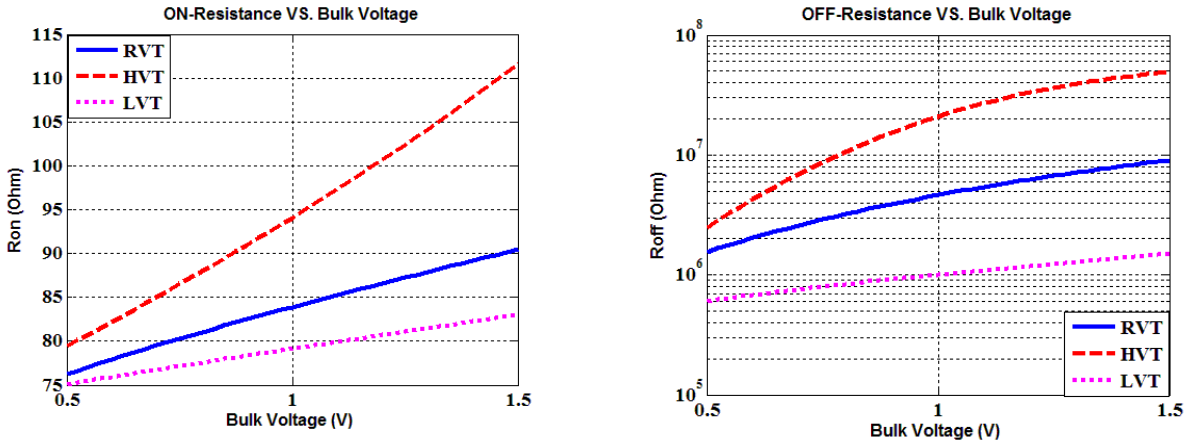


(a) (b)

Figure 4.9 Comparison between on and off-resistances versus gate voltage for different PMOS devices: RVT(solid), HVT(dashed), and LVT(dotted)

Figure 4.9 compares simulated off and on resistances of different V_t devices versus gate voltage; the off and on resistances are calculated with V_{DS} of 1 V and 150 mV, respectively. For

the same gate voltage, it can be seen that the off resistance of HVT devices is much higher, at the expense of slightly higher on resistance. Thus, using HVT loads, F_{min} decreases significantly while F_{max} decreases slightly. To compensate the degradation in F_{max}, higher injection current or higher supply voltage can be used at the expense of power consumption. Alternatively, as shown in Figure 4.8, PMOS bulk adaptation (V_{BL}) is proposed to change the effective R_{on} and R_{off} of the PMOS loads. Figure 4.10 compares the simulated off and on resistances of different V_t devices versus their bulk voltage. The off and on resistances are calculated with (V_{DS} = 1 V, V_{GS}=0) and (V_{DS} = 150 mV, V_{GS}=1 V), respectively. Clearly, decreasing the bulk voltage slightly results in smaller R_{on} of HVT device which in turn increases F_{max}. For example, in order to have the same F_{max} (i.e., R_{on}) using RVT device with bulk voltage (V_{BLR}) of 1.1 V, the bulk voltage of HVT transistors (V_{BLH}) should be connected to 0.7 V.

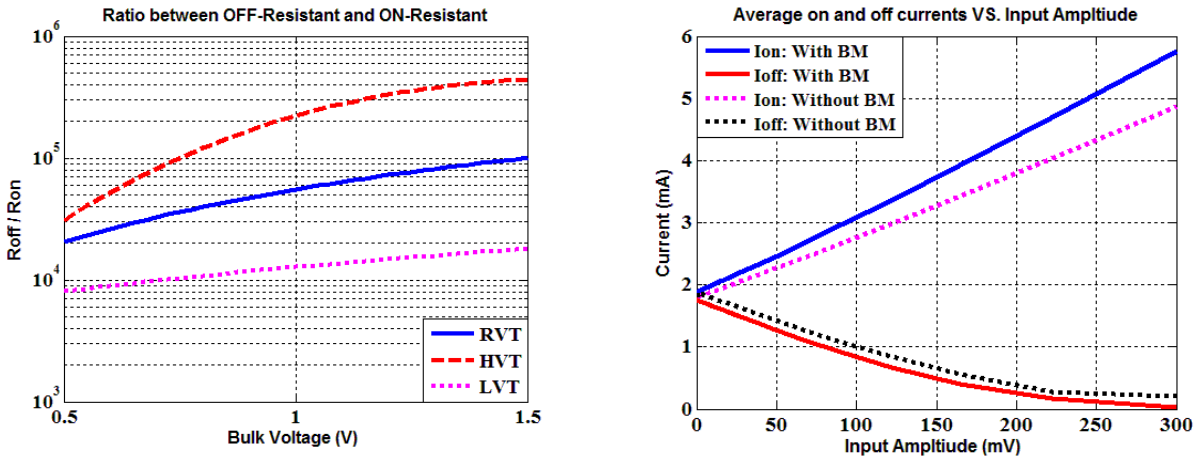


(a) (b)

Figure 4.10 Comparison between on and off resistances versus bulk voltage for different PMOS devices: RVT (solid), HVT(dashed), and LVT(dotted)

It can be seen from (4-6) and (4-7) that the ratio F_{max}/F_{min} is proportional to the ratio by R_{off} /R_{on} of the PMOS loads [109]. Figure 4.11(a) compares R_{off} /R_{on} of different V_t devices versus their bulk voltages. It can be seen that HVT devices have higher R_{off}/R_{on} ratio for the same F_{max}. For example, with V_{BLR} =1.1 V and V_{BLH} = 0.7 V, the R_{off}/R_{on} of a HVT device is 1.27X that of an RVT device, which results in wider locking range. Figure 4.10 and Figure 4.11(a) show that, for

a divider with any of the aforementioned latch topologies and for given power budget, bulk biasing can be used to increase the F_{max} at the expense of narrower locking range, or to widen the locking range for lower operating frequencies.



(a) (b)

Figure 4.11 (a)Ratio between off and on-resistances versus bulk voltage for different PMOS devices: RVT (solid), HVT (dashed), and LVT (dotted). (b) Comparison between average on-current and off-current of tail current source with BM (solid), without BM (dotted)

4.3.3 Third Topology (DIV3): Bulk modulation and bulk control

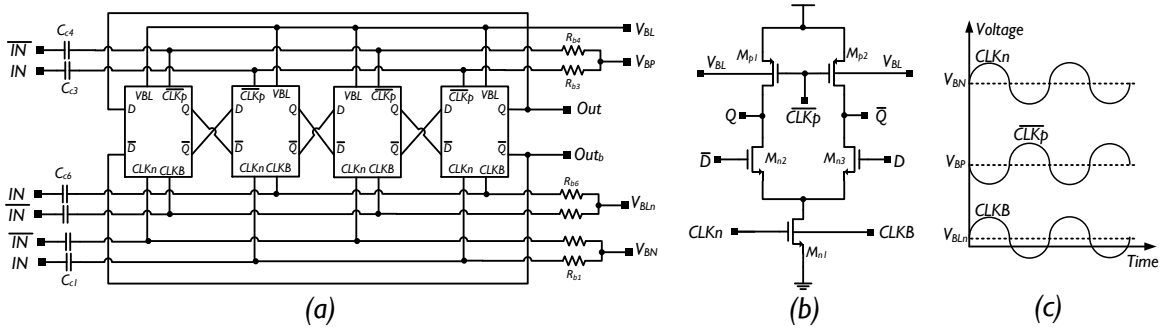


Figure 4.12 Third architecture of DCML divider based on bulk modulation

As discussed in the previous section, for a given tail transistor size and bias, using an LVT device increases F_{max}. On other hand, F_{min} also increases due to large leakage current during the hold phase. To overcome this trade-off, bulk modulation is introduced in the tail current source, as shown in Figure 4.12. Here, the clock is applied to the bulk of the tail transistor with a bias voltage V_{BLn}, which is different from the gate bias V_{BN} as shown in Figure 4.12(c). During the

read phase, with *CLKn* high, the bulk voltage of tail current increases which decreases the threshold voltage and in turn increases the maximum injection current. During the hold phase, with *CLKn* low, threshold voltage increases, thus reducing the minimum leakage current. The post-layout simulated threshold voltage variation was found to be -200 mV/V.

The bulk modulation technique improves both F_{min} and F_{max}. Figure 4.11(b) compares the average on and off current of the tail current source (10 μm/60 nm), biased in saturation, with and without bulk modulation when it is driven by 40GHz clock. For example, as shown in Figure 4.11(b), with 150 mV input amplitude, bulk modulation increases the average I_{on} from 3.23 mA to 3.79 mA, and decreases the average I_{off} from 690 uA to 495 uA. From (2) and (1), this improves F_{max} and F_{min} by 8 GHz and 4.2 GHz, respectively. Note that the average power consumption of the divider with and without bulk modulation is approximately the same. Additionally, the designed *DIV3* incorporates bulk control (V_{BL}) of the PMOS loads, as discussed in the previous section.

4.4 Background Self-Calibration and Current Minimization

Despite the enhancement achieved by the aforementioned techniques in the frequency range covered by each sensitivity band, setting an appropriate bias current and load bias voltage is necessary to enable ultra-wideband coverage. Moreover, as discussed in Section 4.2.3, the operating frequency and locking ranges of all proposed divider topologies are extremely sensitive to PVT variations which necessitate different optimal bias settings depending on PVT conditions. These challenges are exacerbated when the input amplitude to the divider is small; in practice, this amplitude – produced by a VCO buffer – will also vary with PVT. In order to facilitate practical applicability of the divider in a wide variety of usage scenarios, a self-

calibration scheme that sets optimal bias conditions regardless of input frequency and PVT conditions is proposed in this section.

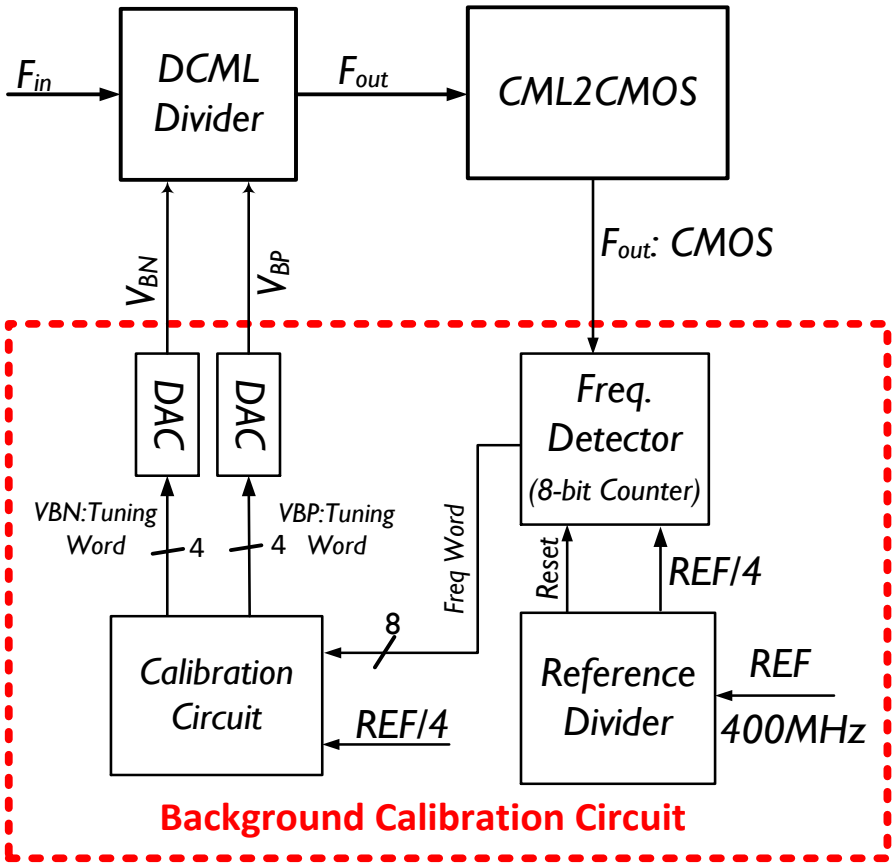
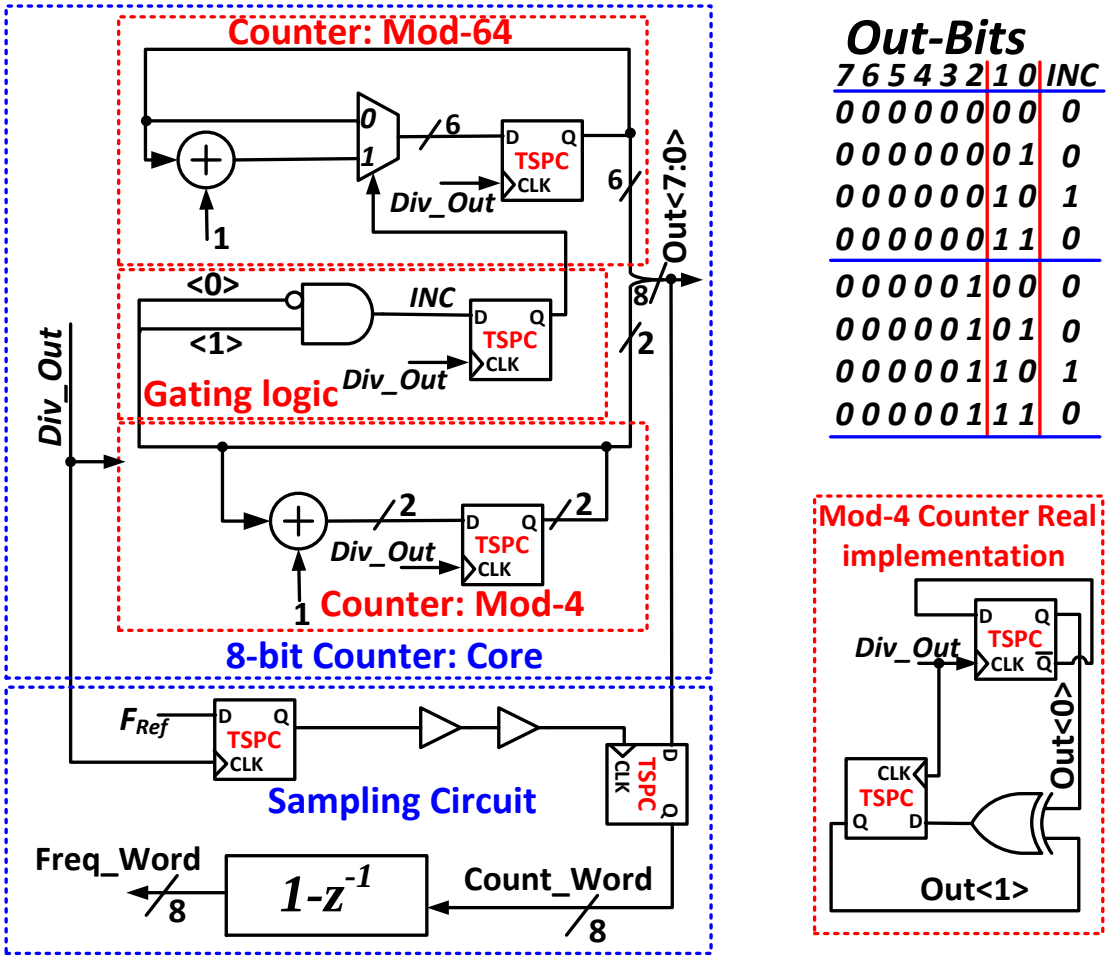
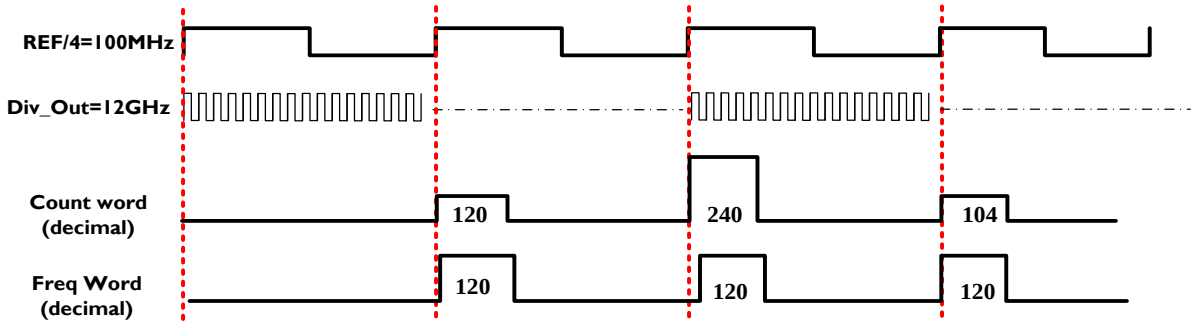


Figure 4.13 Block diagram of proposed background calibration engine

The calibration circuit, shown in Figure 4.13, implements two algorithms – frequency calibration and current minimization, and comprises a high-speed frequency detector, reference frequency divider, resistive DAC's and a fully synthesized digital controller. Frequency detection is realized using an 8-bit synchronous counter which generates an 8-bit digital word representing the ratio of the divider output frequency and the reference frequency (F_{Ref}). Figure 4.14(a) and (b) show the implementation of the 8-bit counter and its timing diagram, respectively. The 8-bit high speed counter is based on a binary ripple carry incrementer.



(a)



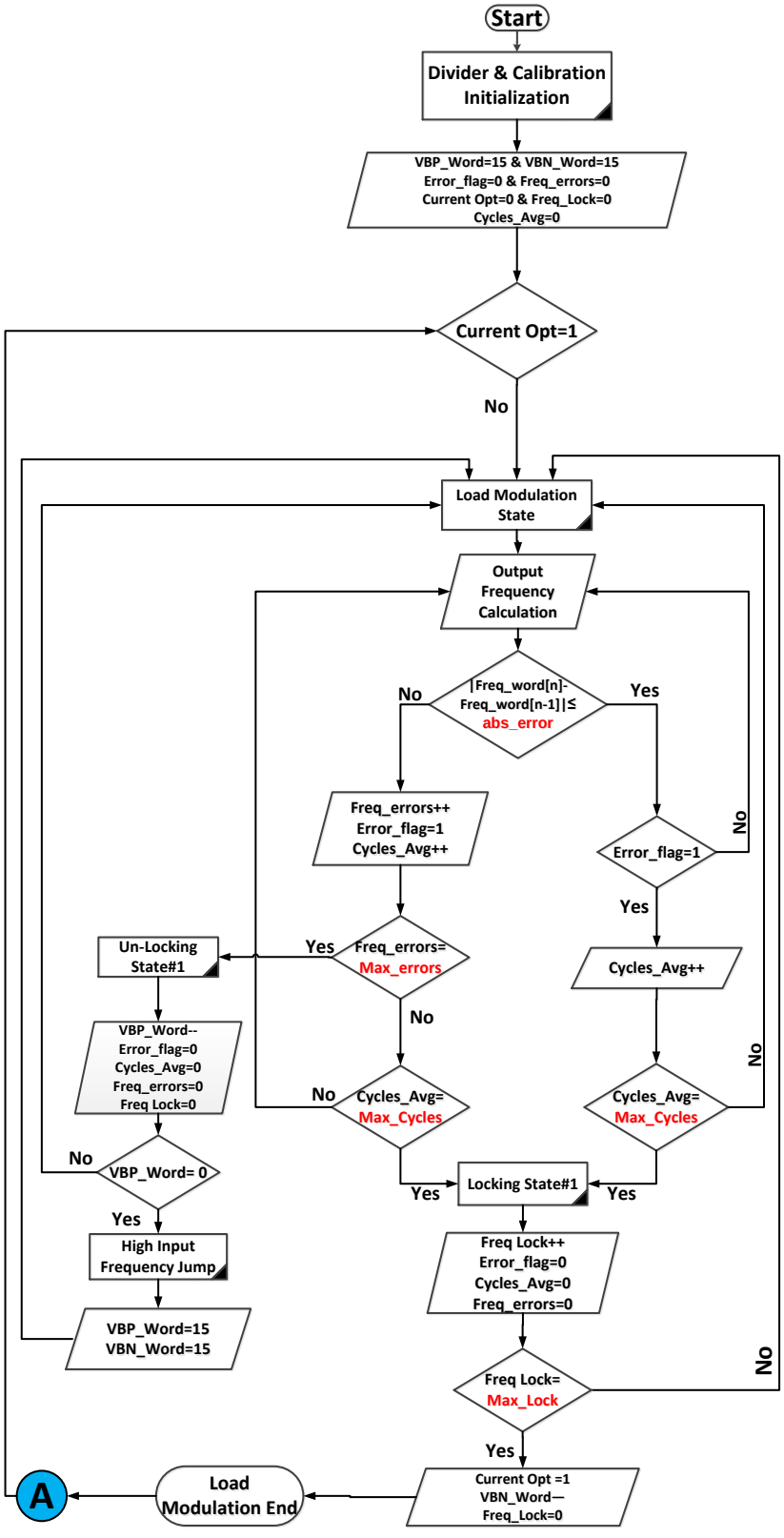
(b)

Figure 4.14 (a) Detailed block diagram of high speed counter with sampling circuit. (b) timing diagram of high speed counter.

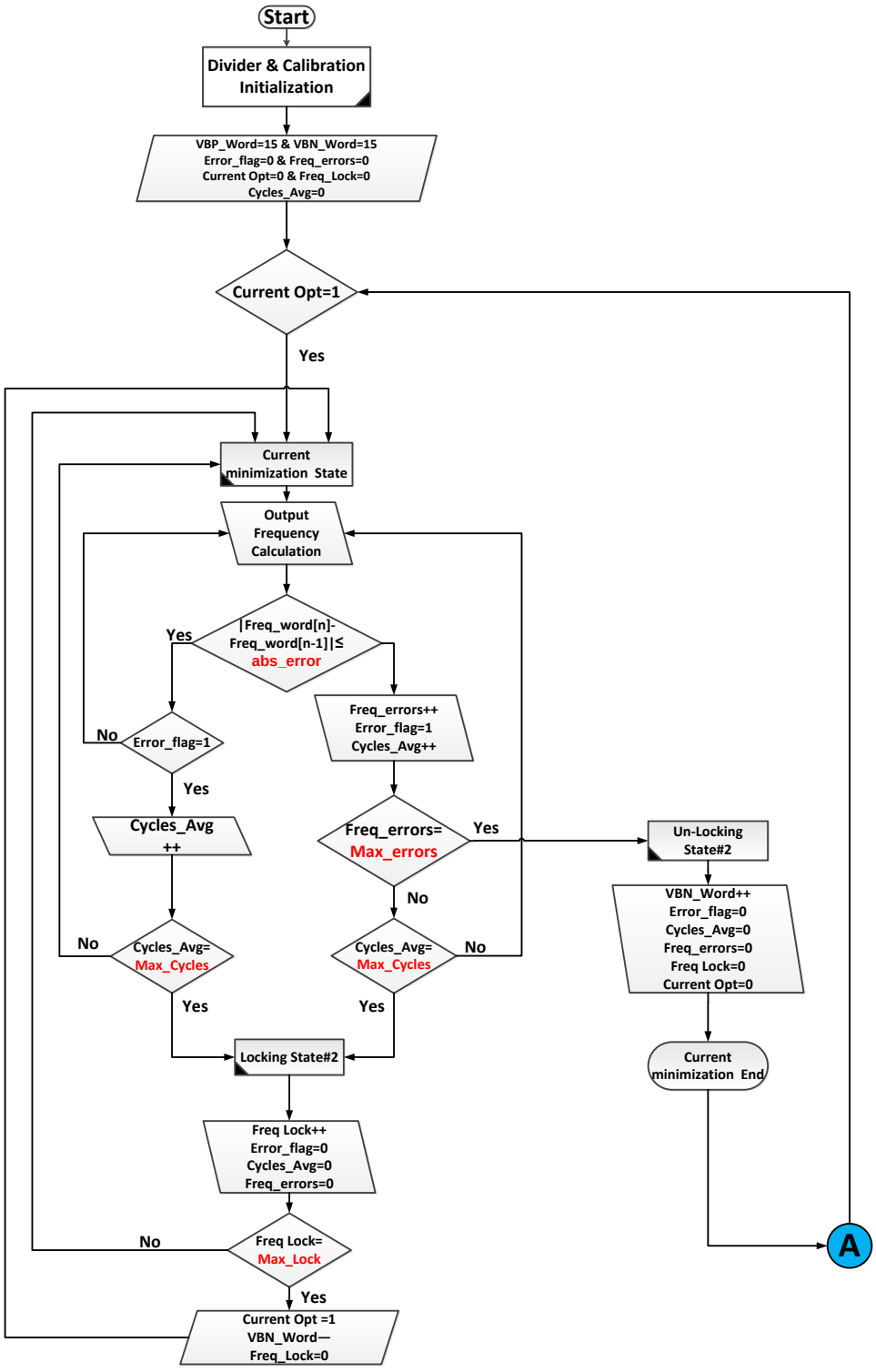
The incrementer is spilt to two smaller incrementers (mod-4 and mod-64) to achieve sufficient timing margin over PVT variations [111]. The first incrementer generates the trigger of the higher incrementer once its count reaches "10" as shown in truth table (Figure 4.14) to add extra timing margin [111] for counter's critical path (i.e., gating logic in Figure 4.14). The TSPC flip-flops in the counter are periodically reset by a signal generated by the reference divider, which also generates the reference signal F_{Ref} for the counter from a 400 MHz source. The counter outputs are sampled by re-timed version of F_{Ref} as shown in Figure 4.14. The frequency detector has been verified to function robustly up to an input frequency of 18 GHz over all PVT corners. The high-speed counter and reference divider consume 2.6 mA from a 1 V supply.

4.4.1 Frequency Calibration and Current Minimization Algorithms

The frequency calibration and current minimization algorithms are illustrated in the flowcharts shown in Figure 4.15(a) and (b). Initially, the digital words controlling the bias voltages V_{BP} and V_{BN} of the PMOS loads and tail current sources (Figure 4.5) are preset to their highest value, thereby setting V_{BP} and V_{BN} to their minimum and maximum value, respectively. This initializes the divider to operate in the sensitivity curve with highest frequency and maximum injection current. For frequency calibration (load modulation state), the difference between current and previous frequency words generated by the high-speed counter is compared with a programmable value (*Abs_error*) to detect the change in output frequency. The frequency change is averaged over a large programmable number (*Max_cycles*) of reference cycles. The calibration engine detects the state of frequency unlocking if the averaged frequency change exceeds a certain level (*Max_Errors*). If unlocked, the digital word controlling V_{BP} is decreased and other calibration state variables are reset.


Start
Divider & Calibration Initialization
VBP_Word=15 & VBN_Word=15
Error_flag=0 & Freq_errors=0
Current Opt=0 & Freq_Lock=0
Cycles_Avg=0
Current Opt=1
No
Load Modulation State
Output Frequency Calculation
|Freq_word[n]-Freq_word[n-1]|≤ abs_error
No
Yes
Freq_errors++
Error_flag=1
Cycles_Avg++
Error_flag=1
No
Yes
Cycles_Avg++
Freq_errors= Max_errors
Yes
Un-Locking State#1
No
VBP_Word--
Error_flag=0
Cycles_Avg=0
Freq_errors=0
Freq Lock=0
Cycles_Avg= Max_Cycles
No
Cycles_Avg= Max_Cycles
No
VBP_Word= 0
No
Yes
Locking State#1
Yes
Yes
High Input Frequency Jump
VBP_Word=15
VBN_Word=15
Freq Lock++
Error_flag=0
Cycles_Avg=0
Freq_errors=0
Freq Lock= Max_Lock
No
Yes
A
Load Modulation End
Current Opt =1
VBN_Word—
Freq_Lock=0

(a)



(b)

Figure 4.15 Flow chart of self-calibration scheme (a) Frequency calibration via load modulation and (b) Current minimization algorithm

The above procedure is repeated until the divider locks to the right sensitivity curve and the frequency change become negligible (i.e., less than reference frequency). Then, before switching to the current minimization algorithm, the frequency comparison is repeated for *Max_lock* reference cycles to ensure locking.

In the current minimization phase, the digital word corresponding to V_{BN} is decreased and frequency lock detection is repeated. If the divider still remains in lock after (*Max_lock* × *Max_cycles*) reference cycles, V_{BN} is again decreased until a frequency unlocked state is detected. Finally, to return to the locked state with minimum current consumption, the digital word controlling V_{BN} is increased by one step, where after the calibration engine resets and resumes monitoring the output frequency variation. The operation of the self-calibration is described in detail below for two cases under different PVT conditions.

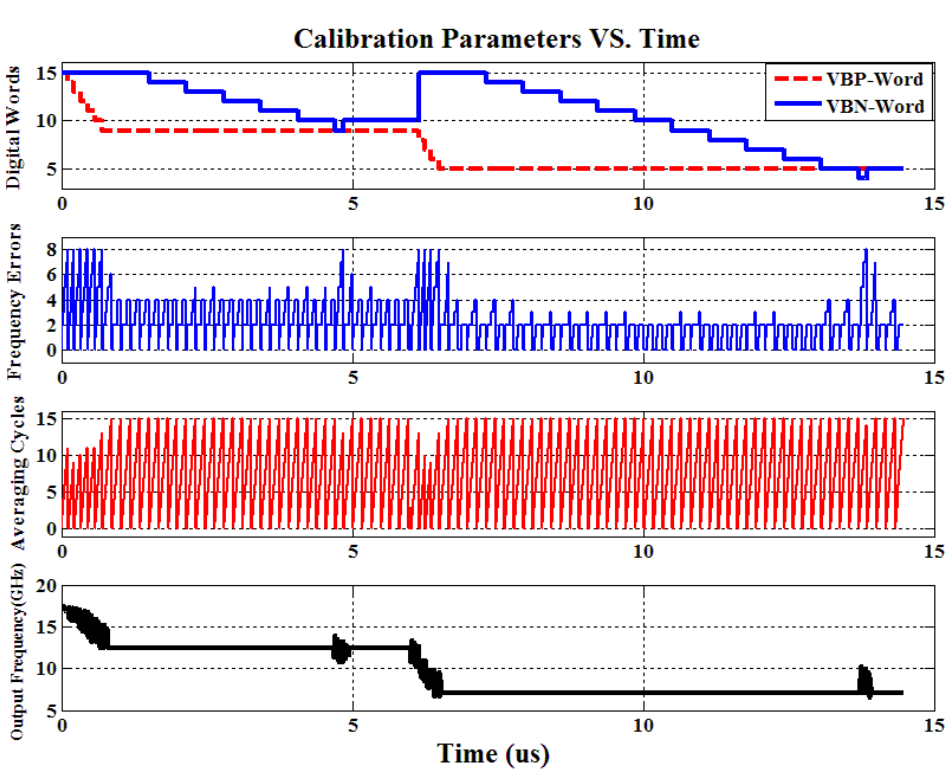


Figure 4.16 Simulation results of background calibration scheme for Case1: DIV-CB at (typical process corner, Temp=27oc, and VDD=1V)

Case 1– Abrupt Frequency Decrease: Figure 4.16 shows the simulation results of the calibration scheme when a 50 GHz, 100 mV input signal is applied initially to DIV1-CB with supply voltage of 1 V, temperature of 27ºC, and typical process corner.

Table 4-1 Simulation parameter of background calibration scheme

Parameter	Abs_error	Max_cycles	Max_errors	Max_lock
Value (Case1)	1	15	8	4
Value (Case2)	2	15	4	4

Table 4-1 shows the nominal values of the programmable calibration parameters. The calibration operation can be divided into several regions as shown in Figure 4.17.

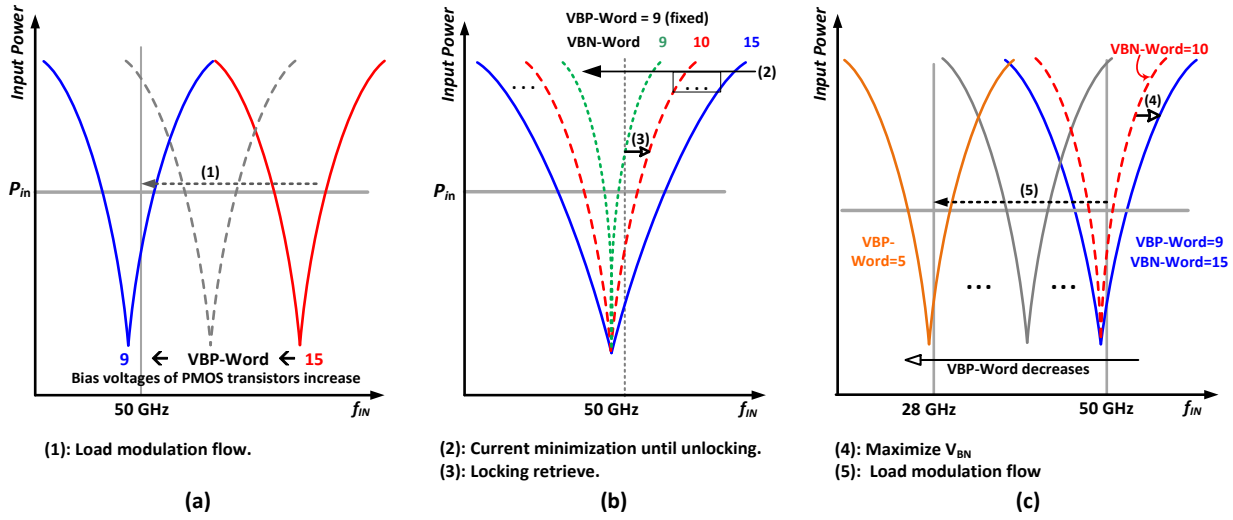
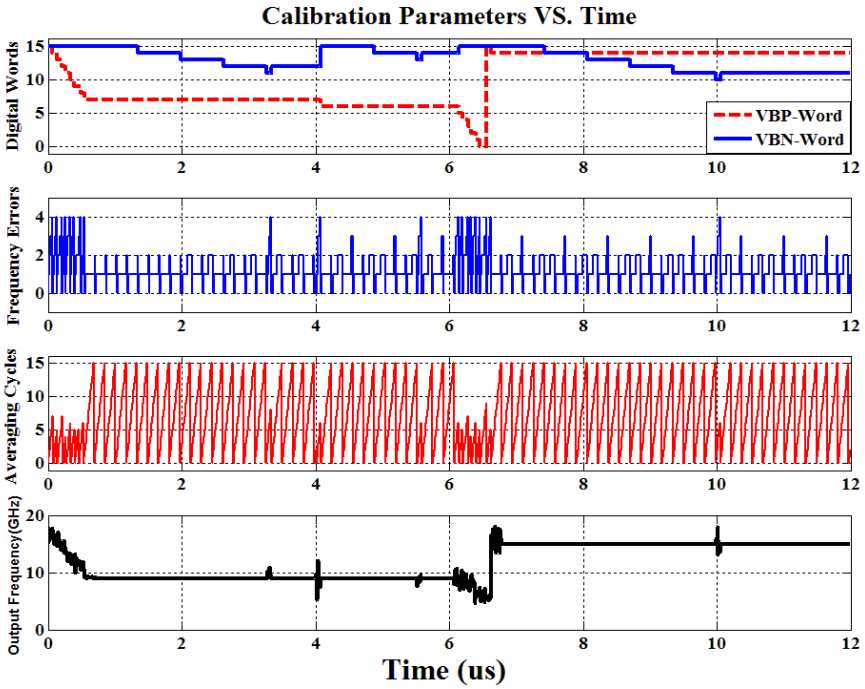


Figure 4.17 Illustration of calibration shown movement across sensitivity curves (Case 1). (a) Load Modulation flow. (b) Current minimization flow. (c) Input frequency change to lower value (28 GHz).

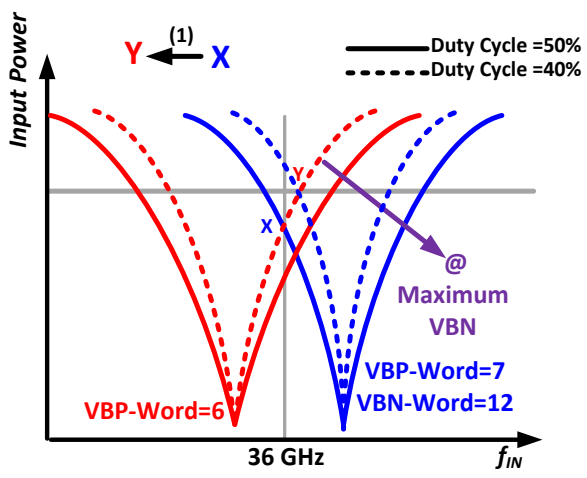
Initially, the divider operates at the highest sensitivity curve and calibration begins in the load modulation mode. The calibration engine modulates the output load by decreasing bias voltage V_{BP} to move across the sensitivity curves, as shown by (1) in Figure 4.17(a). Once locking is achieved, the calibration engine switches to the current minimization mode. In this mode, shown by (2) in Figure 4.17(b), the bias voltage V_{BN} is progressively decreased thereby decreasing the

injection current in the divider and effectively narrowing the sensitivity curve. Eventually, divider loses lock, whereupon the calibration engine switches V_{BN} to back its previous value causing lock to be achieved once again, as shown by (3) in Figure 4.17(b). This results in minimum power consumption at 50 GHz under the specific PVT condition. Next, the input frequency is switched to 28 GHz which causes the divider to lose lock. The calibration engine responds by setting the injection current to its highest value and updating V_{BP} to modulate the load until the lock is achieved once again ((4) and (5) in Figure 4.17(c)). Thereafter, the calibration engine switches to the current minimization mode as described previously.

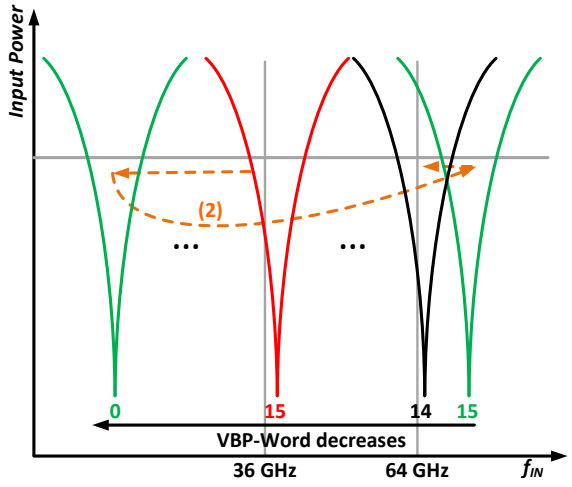
Case 2−Duty cycle variation and abrupt frequency decrease: In this case, the duty cycle of the input waveform is reduced to below 50% followed by an abrupt increase in frequency. The operation of the calibration is illustrated for divider DIV3 which is assumed to operate initially with a 36 GHz, 150 mV input at 85ºC in the fast-fast process corner with a supply voltage of 0.9V. Simulation results are shown in Figure 4.18. The divider is assumed to have initially settled into an "optimally" locked condition with digital words V_{BP}=7 and V_{BN}=12 (i.e., Point X in Figure 4.18(b)). When the duty cycle of input signals is switched from 50% to 40%, the sensitivity curves become narrower and the divider becomes unlocked. The calibration engine responds by setting the bias current to its maximum value (by changing V_{BN}) and then updates V_{BP} and V_{BN} until lock is achieved once again ((1) in Figure 4.18(b)). When the input frequency is switched abruptly to 60 GHz (region (2) in Figure 4.18(b)), the calibration engine searches for the optimal sensitivity curve by first decreasing the digital word controlling V_{BP} down to its lowest value and then resetting to its maximum value.



(a)



(b)



(c)

Figure 4.18 (a) Simulation results of background calibration scheme for Case 2: DIV-3 at (fast-fast process corner, Temp=85ºC, and VDD=0.9 V). Illustration of calibration shown movement across sensitivity curves (Case 2). (b) Duty cycle changes to 40% (c) Input frequency change to higher value (64 GHz)

4.4.2 Calibration Parameters

Calibration accuracy depends on the parameters *Abs_error* and *Max_Errors*. Ideally, when divider is locked, these values should converge to zero. In practice, due to PVT variations and supply voltage noise of frequency detector, the counter output toggles about the correct value. Therefore, programmable parameters *Abs_error* and *Max_Errors* are used to increase margin for PVT variation. Extensive post-layout simulations of the divider with a semi-behavioral model of the calibration loop (where only the high-speed counter is replaced with an extracted circuit) under PVT variations have been used to set the values of *Abs_error* and *Max_Errors*; the calibration has been verified to operate correctly for settings of 1/8, 2/4 and 4/2.

In addition, to improve calibration operation and reduce the effect of parameters on calibration performance, the impact of supply variation can be alleviated by using on-chip supply regulator for frequency detection circuit and by increasing averaging time (*Max_cycles*). The calibration time can be reduced by decreasing the number of averaging cycles and locking cycles, or by increasing the reference frequency. However, this reduction will be achieved at the expense of calibration accuracy, higher power consumption and complexity of the fully synthesized digital controller. Calibration performance can also be improved by adapting *Max_Errors* after locking is detected (i.e., decreasing the value of *Max_Errors* during locking to improve calibration accuracy). Finally, it is noted that this calibration scheme can be scaled to accommodate dividers with moduli greater than four by changing the number of bits in the high-speed counter. The minimum number of bits for frequency detector can be expressed as $K_{min} > log_2(F_{in}/N \cdot F_{Ref})$ where F_{in} and N are input frequency of divider and division ratio, respectively.

4.5 Characterization and Discussion

A chip (Figure 4.19) with three prototypes using the proposed techniques was fabricated in a 65 nm CMOS process.

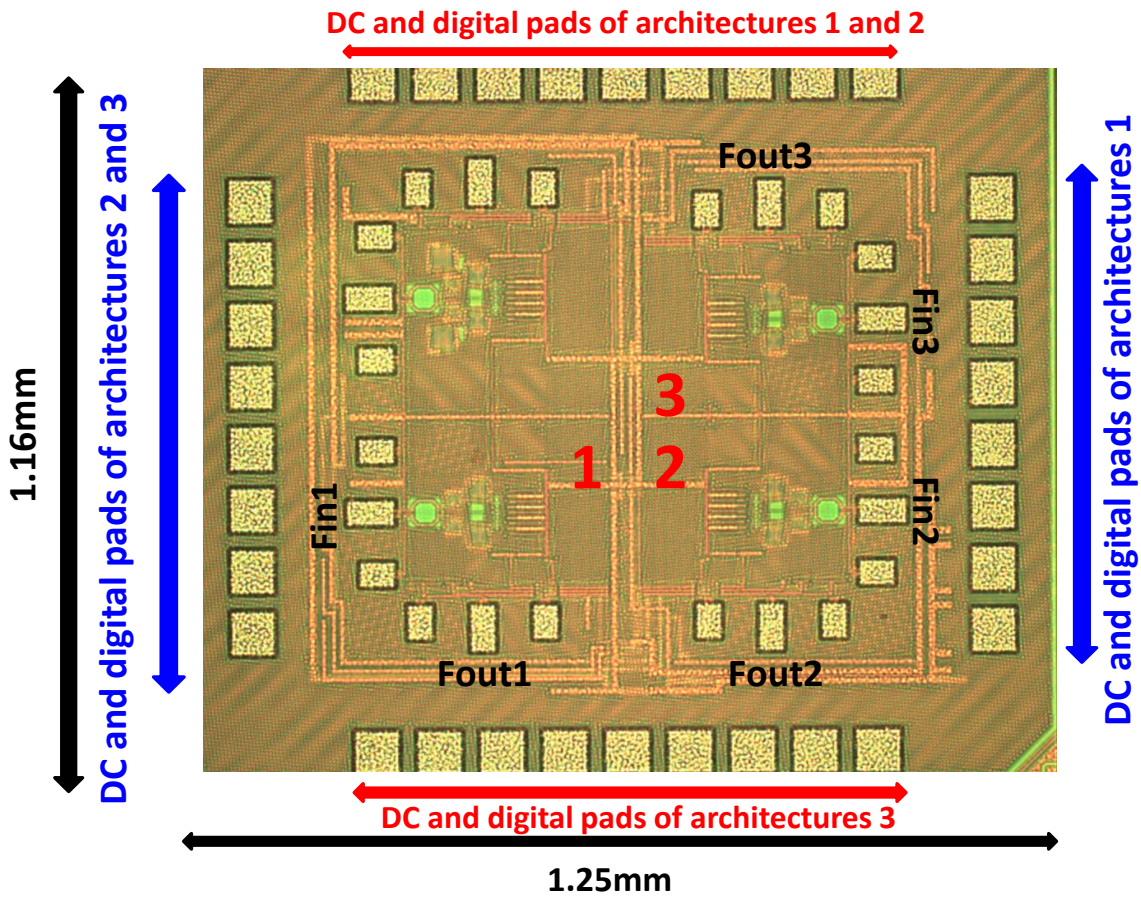


Figure 4.19 Die photo of fabricated chip.

The core of each divider has dimensions of 11 µm×43 µm. A top level schematic representative of all three prototypes is shown in Figure 4.20. The input is provided externally via an on-chip balun. The divider outputs are converted to CMOS levels by a two-stage CML-to-CMOS converter which comprises a differential amplifier followed by CMOS inverters that are coupled using back-to-back inverters to maintain 50% duty cycle. A buffer chain is used to drive 50 Ω measurement loads. The supply voltage for the divider core is provided by an on-chip LDO

regulator, while the supply voltage for digital circuits is provided from an external DC source. All measurements were performed using on-wafer probing.

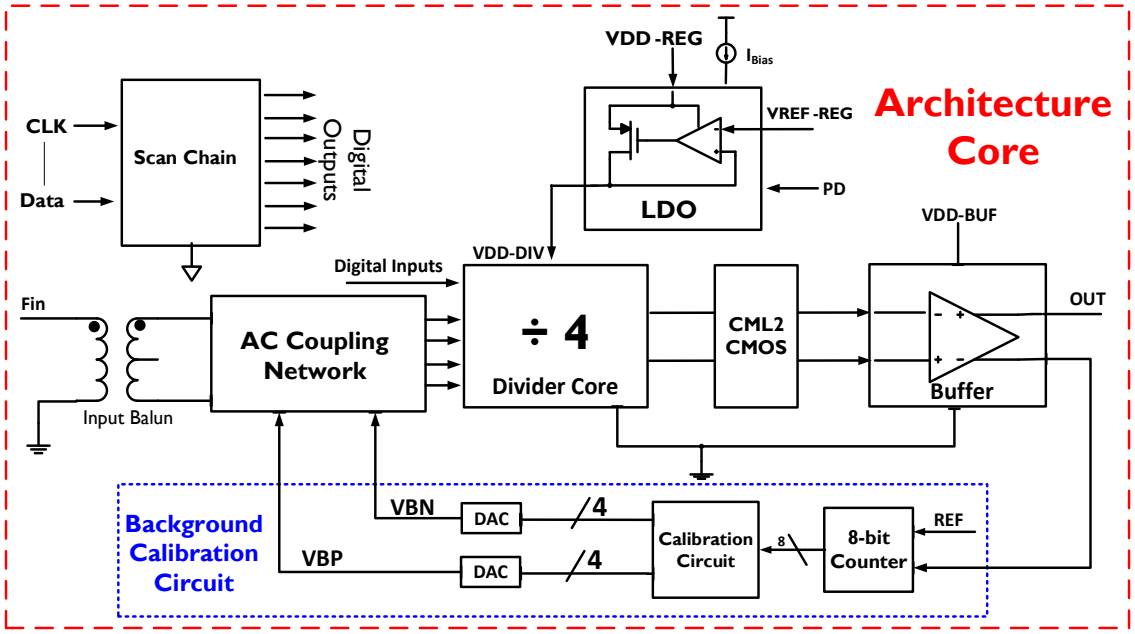
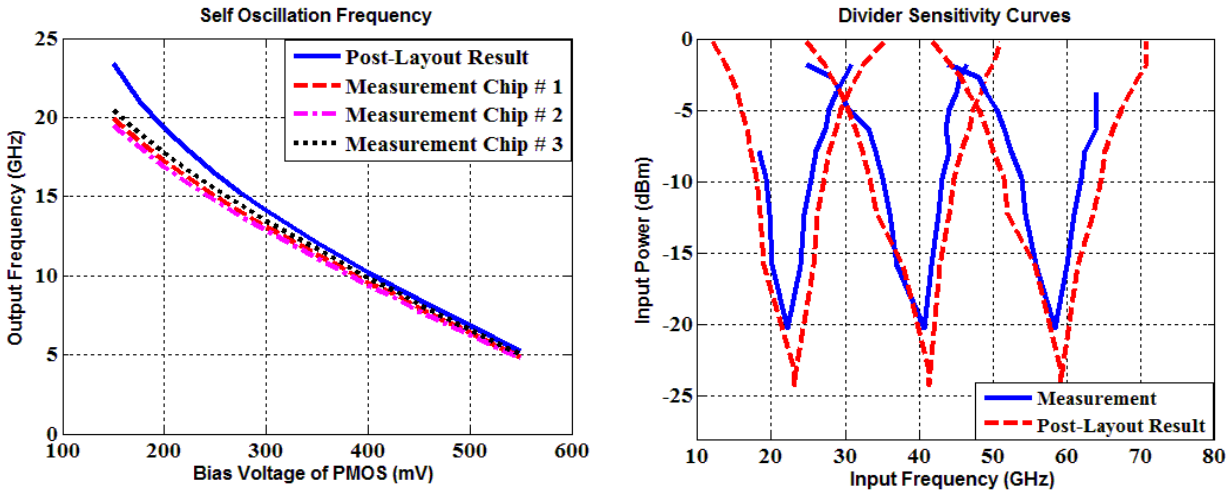


Figure 4.20 Block diagram of prototype divider chip

It is noted that a separate "conventional" divider (Figure 4.1) with devices M_{S1}, M_{S2}, and M_{P3} removed from the layout was not implemented on the test chip in order to save silicon area. However, in order to verify that DIV1-0 provides a fair reference for comparison, the locking ranges of DIV1-0 and the conventional DCML divider were compared using post-layout simulation. The input capacitance and capacitance at node X (Figure 4.5(b)) of DIV1-0 were estimated to be 80 fF and 156 fF, compared to their respective values of 77 fF, and 151 fF for a conventional divider. The locking ranges of DIV1-0 and the conventional divider were estimated from post layout simulation as (41.75 - 71GHz) and (41.5 - 71.25GHz) at 0 dBm input power. Their lock ranges at -10dBm input power were (51.5 - 64.5GHz), and (51.4 - 64.8 GHz).

Figure 4.21(a) compares measurements and post-layout simulations of the self-oscillation frequency F_{osc} of three samples of the baseline topology DIV1-0. The simulations – conducted

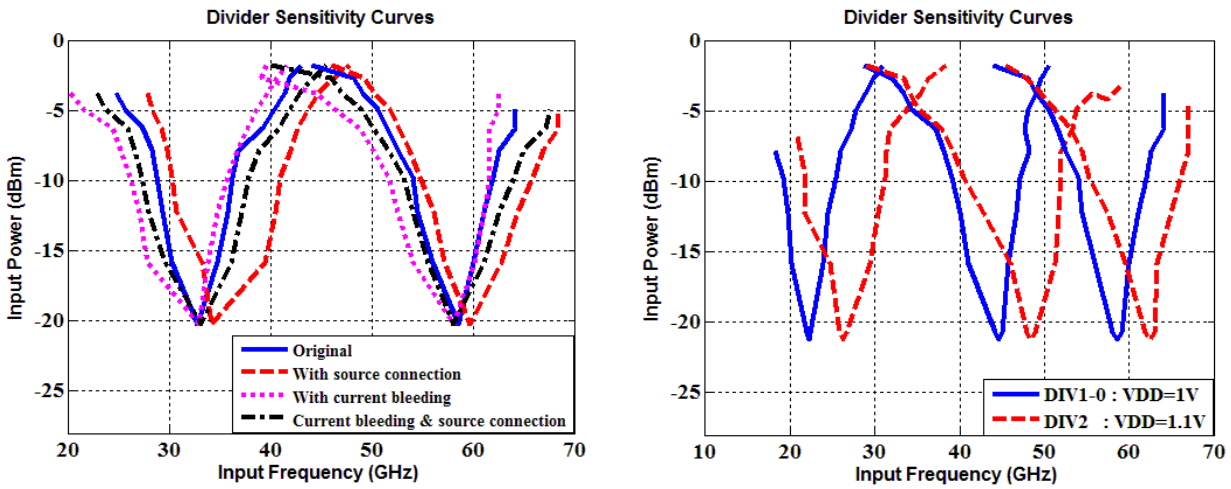
on an RC-extracted divider core with EM-modeled supply, ground and output signal paths – indicate that by changing the PMOS bias voltage V_{BP}, the F_{osc} can vary from 5 GHz to 20 GHz, which indicates an F_{max} of 80 GHz. Figure 4.21(b) compares the measured and post-layout simulated sensitivity curves of DIV1-0 for different bias voltages V_{BP}.



(a) (b)

Figure 4.21 (a) Measured and simulated self-oscillation frequency of first architecture divider versus bias voltage of PMOS output load. (b) Measured (solid line) versus simulated (dashed line) sensitivity curves for first architecture (control word =00) with different bias voltage VBP (525mV: lower frequency band, 400mV: middle frequency band, 275mV: higher frequency band)

A standalone on-chip balun was characterized for the purpose of de-embedding test setup losses. Maximum/minimum losses of the overall test setup were measured to be 24/18.2 dB at 16/45 GHz and they have been de-embedded. The measured sensitivity curves, which are in good agreement with simulations, span 18 GHz to 64.2 GHz with fractional bandwidths of 51.7%, 56.1%, and 35.6%, respectively. At the low end, the measurement is limited by the band-pass nature of the on-chip balun. At the high end, although the divider was not characterized beyond 67 GHz due to signal generator limitations, the good agreement between the simulated and measured F_{osc} indicates that the divider is capable of operation beyond 67 GHz.



(a) (b)

Figure 4.22 Measured sensitivity curves of first architecture with different bias voltage levels and control words. Note that only two sensitivity curves are reported due to figure's clarity (b) Measured sensitivity curves of conventional DCML divider (solid line) versus measured sensitivity curves of second architecture (dashed line) with combination of HVT and LVT devices with different bias voltage levels (Note: For clarity, only a few sensitivity curves are shown here).

Figure 4.22(a) compares two measured sensitivity bands of the four configurations of DIV1 with V_{BP} set to 425 mV and 275 mV. Table 4-2 compares the locking range and fractional bandwidth of DIV1 for the sensitivity curves reported in Figure 4.22(a).

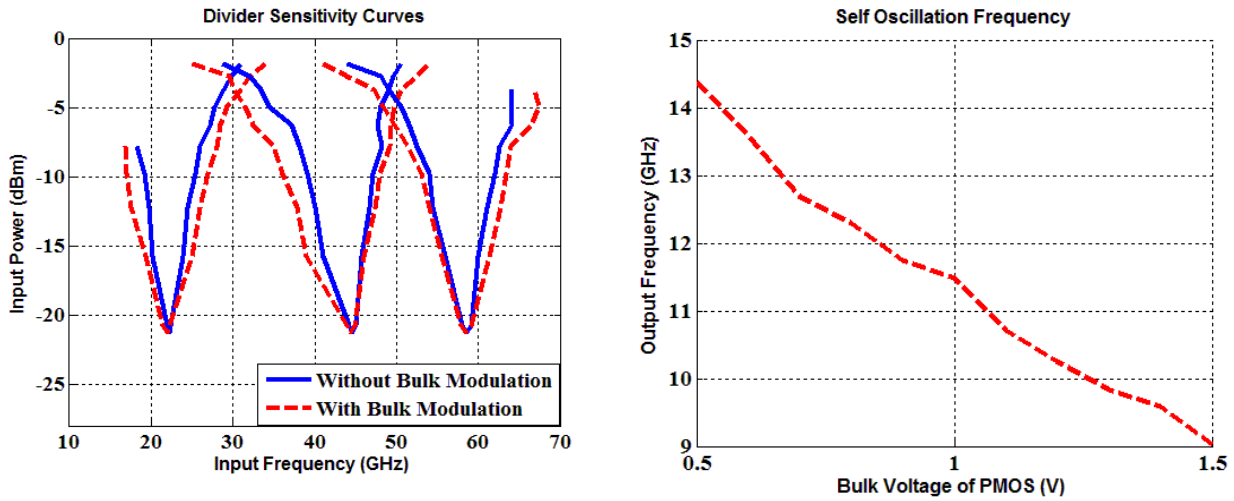
Table 4-2 Comparison between all possible configuration of DIV1

Configuration	Original	Source coupled	Current bleeding	Both
LR: low band (GHz)	24.75-42.5	24-46.75	19-43	19-44.75
FBW: low band (%)	52.5	63.84	76.98	80.7
LR: High band(GHz)	45-63.25	45.75-67	39.5-61.5	40-66.5
FBW: High band (%)	35.6	38.58	44.71	51.1

It can be observed that the locking range is improved by more than 5 GHz when the current bleeding or source coupling techniques are used separately. Examination of Table 4-2 reveals that current bleeding along (DIV1-CB), F_{min} decreases significantly, while F_{max} is not affected significantly. On the other hand, source coupling alone (DIV1-SC) enables a significant increase in F_{max} while affecting F_{min} slightly. These observations are consistent with the analysis in

Section 4.2. Combining current bleeding and source coupling (DIV1-CB+SC) improves the locking range by 4.75 GHz and 3.25 GHz at input power of -5 dBm and -10 dBm, respectively. The measured locking range improvement of the DIV1-CB+SC configuration is observed to be less than the analytical prediction of sections 4.2.2 and 4.3.1; this is due to unaccounted capacitance at node X in Figure 4.5 resulting from devices M_{n1}, M_{S1} and M_{S2}. This capacitance absorbs a fraction of the injection current and hence decreases the operating range.

Figure 4.22(b) compares DIV2 with DIV1-0 for different bias voltages V_{BP}. A 1.1 V V_{DD} is used in DIV2, so that it operates in roughly the same frequency bands as DIV1-0 for given V_{BP}; this increases the power consumption of DIV2 from 6.2mW to 7mW. In the low/mid/high sensitivity bands, DIV2 extends the locking range by 4.75/8.25/2.75 GHz and achieves fractional bandwidth of 59.4/68.2/39.1% compared to 51.7/54.1/35.6% for DIV1-0. Note that the improvements in the highest and lowest curves in Figure 4.22(b) are limited by signal generator and on-chip balun limitations, respectively.



(a) (b)

Figure 4.23 Measured sensitivity curves of conventional DCML divider (solid line) versus measured sensitivity curves of third architecture (dashed line) with bulk modulation for different bias voltage levels (b) Measured self-oscillation frequency of third architecture versus bulk of PMOS load

Figure 4.23(a) compares the measured sensitivity curves of DIV3 and DIV1-0 for different bias voltages V_{BP}. It is seen that bulk modulation improves both F_{min} and F_{max}, as discussed in Section 4.3.3, and extends the locking range by 4.5/5.75/6.25GHz at low/medium/high curve; correspondingly, the fractional bandwidth has been improved from 51.7/55.1/35.6% to 67.9/70/47.1% in the three bands. The measured locking range and fractional bandwidth of DIV1-0, DIV2 and DIV3 are summarized in Table 4-3; examination of this table highlights the large improvements that are enabled by the proposed circuit design techniques.

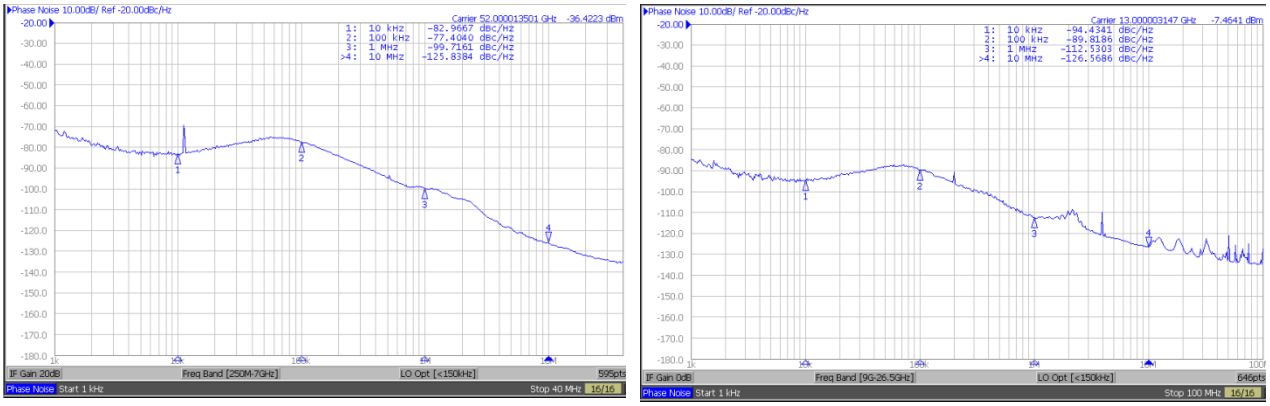
Table 4-3 Comparison between DIV1-0, DIV-2, and DIV-3

Architecture	DIV1-0	DIV2 (VDD=1.1V)	DIV3
LR(GHz): Lower band (VBP=525mV)	18.25-31	20.75-38.25	16.75-34
FBW: Lower band (%)	51.7	59.4	67.9
LR(GHz): Middle band (VBP=350mV)	28.5-50.25	29-59	25.5-53
FBW: Middle band (%)	55.1	68.2	70
LR(GHz): Higher band (VBP=275mV)	44.75-64	45-67	41.5-67
FBW: Higher band (%)	35.6	39.1	47.1

Figure 4.23(b) shows the variation in F_{OSC} of DIV3 with the bulk bias voltage V_{BL} for V_{BP} =350mV. The sensitivity of F_{OSC} to V_{BL} is -5.3GHz/V; this provides another method to shift the sensitivity curve by more than 20GHz for a given current consumption.

The phase noise at the input and the output of the divider (DIV2) are measured using a Keysight E5052B signal source analyzer, and are shown in Figure 4.24(a) and Figure 4.24(b), respectively for 52 GHz input frequency. Figure 4.25 and Table 4-4 compare the measured phase noise of proposed architectures with input frequency of 44 GHz. Since DCML divider is a synchronous divide-by-4, it does not suffer from jitter accumulation. The output phase noise is reduced by roughly 12 dB compared to the input. This reduction extends to about 2 MHz offset

from the carrier frequency beyond which amplitude noise from the buffers starts to dominate. As expected, the phase noise of proposed DIV2, DIV3 is better than DIV1-0, since the phase noise of a DCML latch is proportional to $\frac{C_L}{I_{On}^{\ 2}}$ [109].



(a) (b)

Figure 4.24 Phase noise measurement a) input signal (Fin=52GHz) b) output signal (Fout=13GHz)

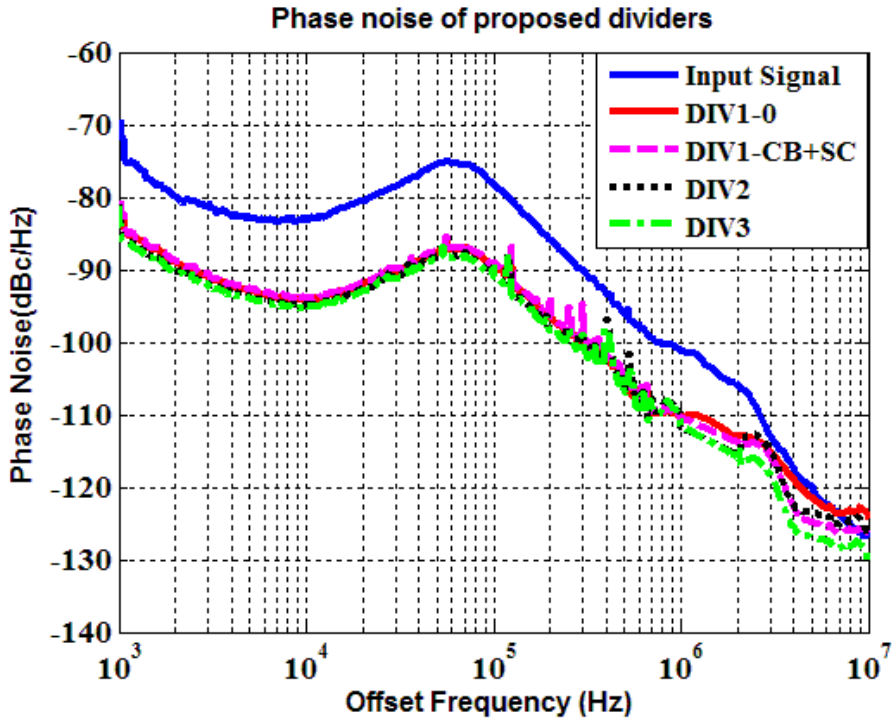


Figure 4.25 Comparison between measured phase noise of proposed dividers with input signal of 44GHz

Table 4-4 Comparison between phase noise of proposed architectures

	Frequency Offset (Hz)	1K	10K	100K	1M	2M	10M
Phase noise (dBc/Hz)	Input signal (44GHz)	-69.34	-82.93	-78.14	-101.1	-105.8	-126.1
	DIV1-0	-80.72	-94.13	-89.5	-110.3	-113.1	-124.5
	DIV1+ CB+SC	-80.63	-94.39	-89.27	-110.81	-113.25	-126.3
	DIV2	-81.05	-94.62	-89.4	-110.52	-113.72	-127
	DIV3	-80.61	-94.2	-89.38	-111.2	-112.9	-127.7

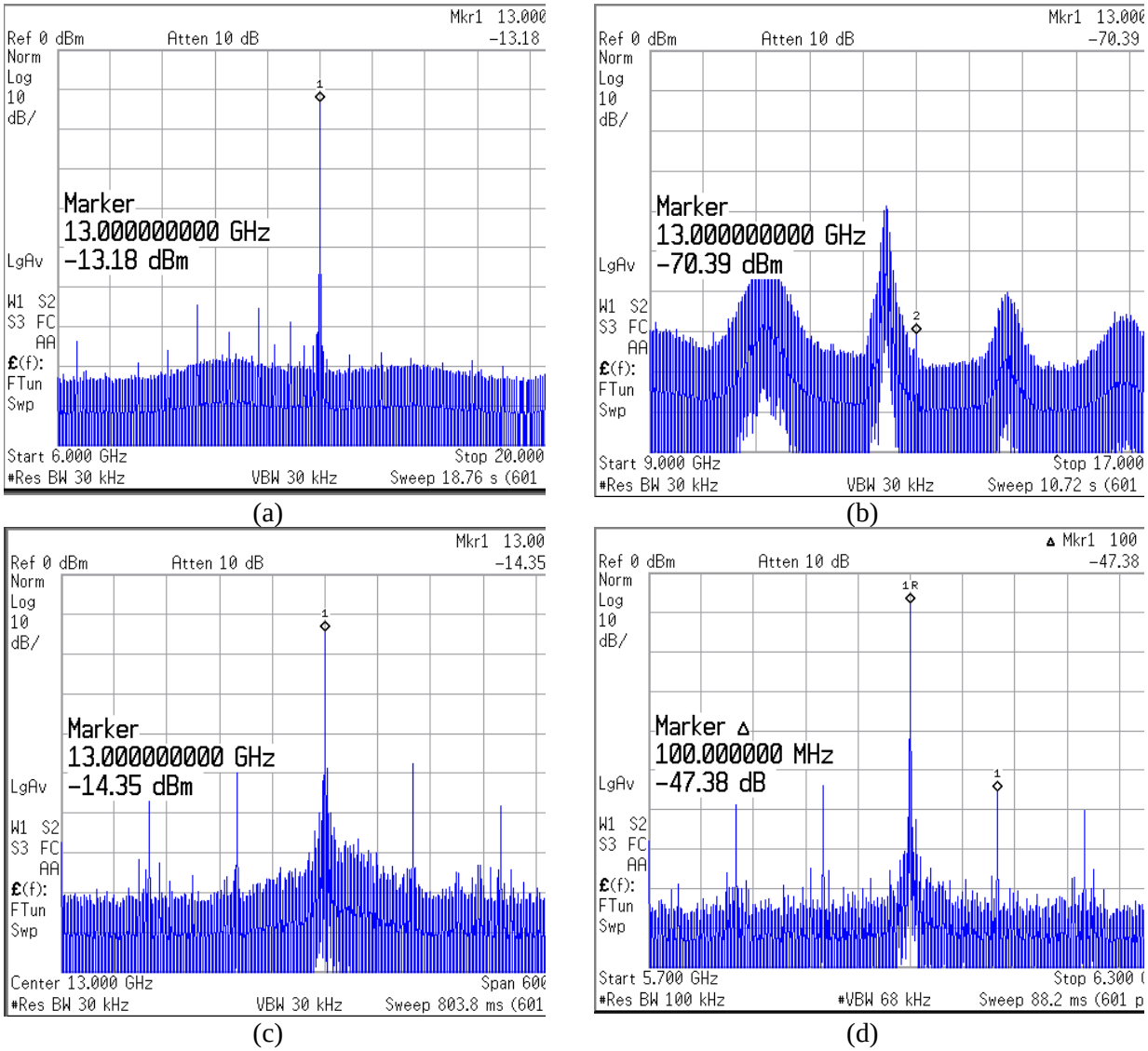


Figure 4.26 Output spectrum of DIV1-0 with self-calibration scheme (a) Fin=52GHz, VDD=1 V,Cal_EN=0 (Locked) (b) Fin=52GHz, VDD=0.9V, Cal_EN=0 (Unlocked) c) Fin=52GHz, VDD=0.9V, Cal_EN=1 (Locked) d)Fin=24GHz,VDD=0.9v, Cal_EN=1(Locked)

Figure 4.26 shows the operation of the calibration engine. Calibration was characterized for all divider topologies, and behaves as expected; however, characterization results are presented herein only for DIV1-CB+SC. Figure 4.26(a) shows the locked output spectrum at 1 V V_{DD} for a 52 GHz, -10 dBm input. When the V_{DD} is decreased by 100 mV, the divider loses lock, as shown in Figure 4.26(b). The calibration circuit is then enabled, whereupon the divider regains lock by changing the bias voltage V_{BP} and moving to a different sensitivity curve; this is shown in Figure 4.26(c). The input frequency is then changed abruptly to 24 GHz; Figure 4.26(d) shows the output spectrum as the calibration engine enables the divider to regain lock. It can be observed that spurs appear at $F_{out} \pm nF_{Ref}$ after calibration; these are caused by clock feedthrough from the calibration engine that generates the digital word that controls (through a DAC) the bias voltages V_{BP} in the latches. Simulations with carefully extracted parasitics show that these spurs can be eliminated by either gating the clock of these latches after calibration or by buffering them prior to the DAC controlling V_{BP}.

Measurement results and benchmarks are summarized in Table 4-5. For the dividers with multiple sensitivity curves, *FOM* and *FBW* of each curve are calculated at maximum reported input power of each benchmark. In order to make a fair comparison with dividers with moduli other than 4, and to explicitly account for the fact that achieving a target locking range becomes harder at low input amplitude, it was necessary to define a new figure-of-merit as follows:

$$FOM_P\left(GHz/\mu W^2\right) = \frac{F_{\max}(GHz) - F_{\min}(GHz)}{P_{diss}(mW)P_{in}(mW)} X \frac{F_{in}}{F_{out}} \tag{4-7}$$

Three main conclusions are drawn from Table 4-5: (1) The proposed techniques significantly enhance performance and robustness in practical applications. (2) In contrast to previous designs, the proposed designs demonstrate little locking range degradation at low input amplitude

compared to the maximum achievable locking range at high input amplitude. (3) Using the calibration scheme, the proposed dividers cover widest locking range reported to date (16-67 GHz) without any manual tuning which results in highest FOM_P to date.

It is worth noting that the divide-by-2 ILFD in [99] features the highest FOM in Table 4-5. This is due to the combined advantage of injection locking to a resonant circuit using a strong second harmonic rather than a weak fourth harmonic in divide-by-4. However, this advantage vanishes when FOM_P is used for comparison, as seen in Table 4-5.

Table 4-5 also underscores the scaling-friendly nature of the DCML approach, as evidenced by the fact that the divide-by-4 designs [109], [110] with superior FOM are designed in more advanced CMOS technologies. Note, however, that advanced technologies (especially 32 nm and below) vary widely in terms of process type and flavor. Such considerations, as well as the availability of process features chosen for a particular application can heavily influence design choices. Therefore, the circuit techniques proposed herein (or combinations thereof), and the self-calibration scheme are highly relevant even in more advanced technologies.

4.6 Comparison and Extensions of Divider Topologies

In this section, the proposed divider topologies are compared based on the analysis and measurements presented in previous sections. Several observations and conclusions can be drawn:

1. In low-cost CMOS designs without additional process options such as multiple Vt devices or triple well, source coupling alone can be used to increase F_{max}, while current bleeding alone can be used to decrease F_{min}. Combining the two techniques improves F_{max} and F_{min} despite a small increase in the input capacitance.

2. In designs using technologies where devices with different V_t and/or triple well are available, DIV2 and DIV3 can improve locking range at the expense of slightly higher power consumption and input capacitance, respectively.

3. Certain combinations of the proposed techniques can be used to further improve the locking range. For example, source coupling can be combined with HVT loads to improve both F_{max} and F_{min} with approximately the same input capacitance and power consumption. Bulk modulation and current bleeding can be combined to further reduce F_{min}.

4. Combining all of the above techniques can further improve locking range; however, a price is paid in terms of higher input capacitance and power consumption. In other words, overall performance improvement can be achieved if the input amplitude is low, but such improvement is diminished when higher input amplitude can be delivered. For example, the effectiveness of combining current bleeding, HVT loads and bulk modulation in reducing I_{off} is diminished when the input amplitude is increased. Similarly, the effectiveness of combining source coupling, LVT tail transistor and bulk modulation in increasing I_{on} is diminished at higher input amplitude. Nevertheless, the improvements offered by combining all techniques can result in a reduction of overall system power, especially at high mm-wave frequencies, since the swing at the output of the LO buffer can now be smaller, thereby reducing its current consumption.

Table 4-5 Measurement summary and comparison with the state-of-the-art

Ref.	$\frac{F_{in}}{F_{out}}$	F_{min}-F_{max} (GHz)	FBW [(a)] (%)	FBW [(b)] (%)	Power (mW)	Supply(V)	Area (μm2)	Tech (nm)	FOM[(c)] (Min/Max)	FOMP[(d)] (Min/Max)
[96]*	4	62.9-71.6	2.2	1.13	2.8	0.5	110x130	90	0.21/0.57	4.3/11.4
[97]	4	79.7-81.6	2.4	0.87	12	0.56	106x330	65	0.16	2.34
[98]	2	82.5-89	7.6	5.1	3	0.5	220x290	90	2.17	28.67
[99]	2	53.4-79.4	39.2	8.4	2.9	0.8	420x300	65	8.97	37.93
[100]*	3	48.8-54.6	3.5	3.1	3	0.9	300x300	65	0.27/0.57	6/16
[101]	4	58.5-72.9	21.9	6.8	2.2	0.6	260x160	65	6.54	81.8
[102]	2	31-47	41.1	20.3	24	1.2	260x350	90	0.67	7.083
[107] *	4	20-70	9.7	4.52	6.5	1	15x30	65	0.46/1	6.15/15.4
[109] *	4	14-70	90	63.4	1.3/4.8	1	18x55	32	6.7/17.5	83.3/399
[110] *	4	25-102	42.2	16.67	2.8/5.6	0.9	25.6x25	28	0.71/8.57	28.4/142
[112]	3	58.6-67.2	13.7	6.25	5.2	1	170x220	65	1.65	23.1
[113]	4	67-72.4	7.7	0.3	15.5	1.2	870x760	90	0.35	0.516
[114]*	2	35-59.5	32	8.8	3.9	1.1	630x90	130	2.4/4.2	23.1/24.6
This Work*: DIV1-0	**4**	**18-65****	**55.1**	**23.3**	**3.7-6.2**	**1**	**11x52**	**65**	**3/5.8**	**51.6/67**
This Work*: DIV1-CB+SC	**4**	**16-67****	**81.2**	**49.8**	**3.7-6.2**	**1**	**11x52**	**65**	**4.4/7.03**	**66.4/113**
This Work*: DIV2	**4**	**16-67****	**68.2**	**38.7**	**4.3-7.4**	**1.1**	**11x43**	**65**	**3/6.98**	**56.8/105**
This Work*: DIV3	**4**	**16-67****	**70**	**45.4**	**3.85-6.25**	**1**	**11x43**	**65**	**4.1/7.15**	**67.2/104**
This Work: DIV1-CB+SC Calibration	**4**	**16-67****	**122**	**110.5**	**6.2-8.7**	**1**	**52x60**	**65**	**5.87**	**202.3/283.8**
This Work: DIV2-Calibration	**4**	**16-67****	**122**	**104.2**	**6.75-9.65**	**1.1**	**52x60**	**65**	**5.285**	**188.6/269.7**
This Work: DIV3-Calibration	**4**	**16-67****	**122**	**114.8**	**6.42-8.82**	**1**	**52x60**	**65**	**5.782**	**199.5/274.14**
$FBW\ (\%) = \frac{2(F_{max} - F_{min})}{(F_{max} + F_{min})}$			$FOM\ (GHz/mW) = \frac{F_{max}(GHz) - F_{min}(GHz)}{P_{diss}(mW)}$				$FOM_P\ (GHz/\mu W^2) = \frac{F_{max}(GHz) - F_{min}(GHz)}{P_{diss}(mW) P_{in}(mW)} X \frac{F_{in}}{F_{out}}$			

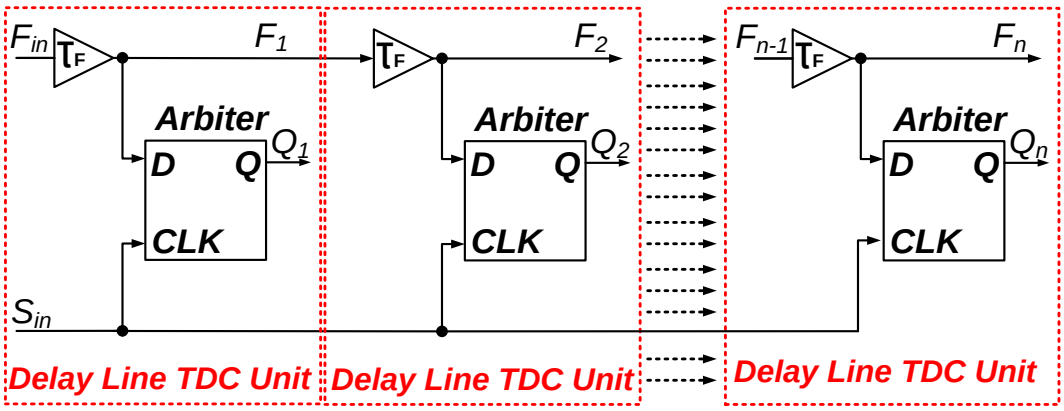
(a) Reported locking range at maximum reported input power. (For all cases except the last row, in which calibration is enabled, the FBW is defined as the best amongst the FBW's of all sensitivity curves).
(b) Best FBW, among all reported sensitivity curves, at input power of -10dBm.
(c) Best/Worst FOM among all reported sensitivity curves. Locking range is calculated at maximum reported input power of each sensitivity curves.
(d) Best/Worst FOMP, among all reported sensitivity curves, at input power of -10dBm.
* Covers the whole locking range (Fmin-Fmax) by multiple sensitivity curves.
** Limited by on-chip balun and available equipment

5 Wide dynamic range fine resolution time-to- digital converter (TDC)

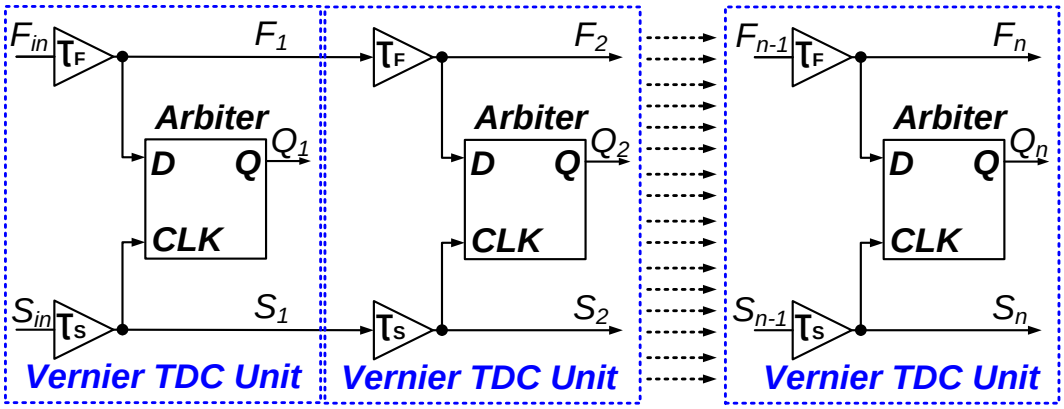
5.1 Introduction and motivation

Time-to-digital converters (TDCs) have been implemented previously in different applications such as laser range finders [115], time-of-flight and timing jitter measurements [116], [117]. Recently, high-resolution TDCs have been used in digital PLLs [40], [42], [44] to serve as a digital replacement for the phase-frequency detector and charge pump. The time resolution, linearity, and conversion range of time-to-digital converter (TDC) represent the main bottleneck to achieving low in-band phase noise in fractional-N frequency synthesizers [40], [42], [44]. Therefore, numerous TDC architectures and calibration techniques have been reported recently to improve TDC resolution and its linearity [118]–[135].

The resolution of a conventional delay line TDC (Figure 5.1 (a)) depends primarily on process technology since the minimum resolvable time quantity is proportional to the delay time of one inverter. The Vernier delay line (Figure 5.1 (b)) has been demonstrated as a circuit technique to achieve sub-gate time resolution. The time resolution (T_Q) is determined by the time difference between two delay cells, ($T_Q = T_F - T_S$), where T_S is the propagation time of a slow delay cell and T_F is that of a fast delay cell. However, since the time resolution is determined by the difference between two delay units, an large number of inverter stages are required to cover a large dynamic range, resulting in high power consumption and silicon area. Moreover, as will be discussed later, cascading a large number of inverters increases TDC non-linearity due to PVT and mismatch variation, and thus limits the effective resolution of TDC.



(a)



(b)

Figure 5.1 Schematic of conventional TDCs (a) Delay line TDC (b) Vernier TDC

Recently, several approaches have been proposed to achieve the fine resolution with low power consumption. One example is the 2-D Vernier delay line [128], [132], [135], where the Vernier plane is implemented by calculating all possible delay differences between the delay lines' taps rather than calculating the time differences between corresponding taps only as in 1-D Vernier delay line. This, in turn, achieves large dynamic range with fewer stages compared to a conventional Vernier delay line (Figure 5.1 (b)). However, this technique suffers from complexity and large parasitics at the internal nodes due to routing complexity, which limit the conversion rate of TDC.

Alternatively, the two step TDC architecture can be used to simultaneously achieve wide dynamic range and fine resolution. This architecture comprises a coarse TDC to cover the desired input range and a fine TDC with fewer stages (compared to Vernier delay line for same dynamic range) to measure the residual time following coarse measurement. The main challenge in this architecture is the interface between coarse and fine TDCs and storage of the residual time from the coarse measurement. Two-step TDC's based on time amplifier [123], [126] have been demonstrated to relax the resolution requirement of fine TDC by amplifying the residual time. Time amplification is implemented by using a cross-coupled structure in the metastable region or through the input dependent time delay of an SR latch. However, the linear input range of time amplifiers is small which results in low amplification. In addition, the time amplifier gain is very sensitive to PVT and mismatch variation which limits the effective TDC resolution.

In [136] time-domain successive-approximation approach have been used to achieve high resolution but it consumes large area and power, (9.6 mW at 80 MHz input frequency), to accurately implement the tunable delay cells.

The gated ring oscillator [137] and switched ring oscillator [120] topologies can achieve fine resolution, large dynamic range, and low power consumption. In gated ring oscillators, the delay cells are connected together to form a ring oscillator. The multiple phases in the ring are used to trigger a counter while holding the clock phases between the measurement cycles to allow an accurate time measurement with first-order quantization noise cancellation. These techniques shape the quantization noise and mismatch nonlinearity of TDC to high-frequency and allow for reducing them with a low pass filter. This, in turn, results in fine effective resolution while eliminating the need to further calibration of the nonlinearity due to mismatch or PVT variation.

However, these techniques are suitable only at low input frequency (750 MHz in [120]) due to the trade-off between oversampling ratio and power consumption.

All these aforementioned techniques operate at low input frequency (< 2 GHz). A survey of state-of-art TDCs shows that a TDC that operates at mm-wave frequency range and achieves the target resolution and linearity has not been demonstrated. This represents the main bottleneck in implementing wide-band fractional-N ADPLL's at mm-wave frequencies. In the only reported fractional-N ADPLL [79], 32X ILFD/CML divider chain has been used in the DCO-TDC interface to reduce the input frequency of TDC to 2 GHz. This results in high power consumption (> 0.5 of total power), large area, and high in-band phase noise.

In this work, we demonstrate the first TDC that operates at mm-wave input frequency (20-68 GHz) with finest time resolution (450 fs) reported to date. A two-step architecture is used to simultaneously achieve the wide dynamic range (programmable from 128ps to 300ps) and fine time resolution (programmable from 500fs to 1.2ps). A synthesized digital calibration engine based on statistical element selection (SES) [60] is used to alleviate the TDC nonlinearity that results from PVT and random mismatch variations. The measured DNL and INL of a 65 nm CMOS two-step TDC prototype are 0.65 LSB and 1.2 LSB, respectively. The 60 GHz TDC consumes only 11mW which results in best FOM_I compared to the state of the art.

This chapter is organized as follows: the specifications of TDC for 60 GHz ADPLL are derived in section 5.2. In section 5.3, the design and implementation of two-step TDC that operates up to 17 GHz will be discussed. Section 0 discusses the main sources of TDC non-linearity. In section 5.5, the calibration technique based on SES is proposed to improve TDC non-linearity.

Section 5.6 presents the detailed calibration algorithm and the verification methodology. Measurement results of a 65 nm CMOS TDC prototype are presented in Section 5.7.

5.2 Specification of TDC for 60 GHz ADPLL

The performance of the TDC represents the main bottleneck to implement a wide-band digital frequency synthesizer since its quantization noise dominates the overall in-band phase noise [138]. The in-band phase noise of ADPLL due to quantization noise can be expressed as [138]:

$$\ell\left(\sigma_{\varphi}\right)_{TDC} = \frac{\left(2\pi\right)^2}{12}\left(\frac{T_{LSB}}{T_{DCO}}\right)^2 * \frac{1}{F_{\mathrm{Re}\,f}} \tag{5-1}$$

Figure 5.2 shows the in-band phase noise of mm-wave ADPLL versus output frequency for different TDC resolution step. The above equation and Figure 5.2 indicate that the resolution of TDC should be better than 600 fs to achieve in-band phase noise less than -100 dBc/Hz for output and reference frequency of 66 GHz, and 100 MHz. In addition, due to the repetitive behavior of the error signal in the ADPLL, finite TDC resolution leads to in-band fractional spurs at multiples of fractional frequency of desired channel [40], [42], [139]. In ADPLL, in-band fractional spurs due to finite resolution of TDC can be expressed as [139]:

$$\ell = \left(\frac{T_{LSB}}{T_{Div}}\right)^2 \tag{5-2}$$

The above equation indicates that the resolution of TDC should be better than 400 fs to achieve fractional spurs less -45 dBc for output frequency of 66 GHz.

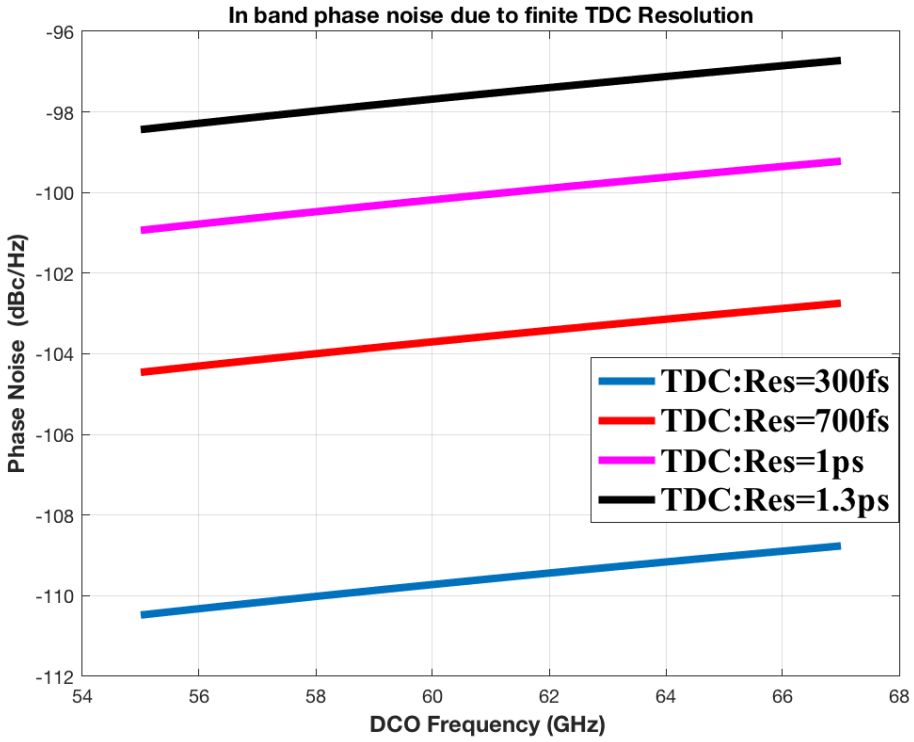


Figure 5.2 In-band phase noise of mm-wave ADPLL VS. output frequency for different TDC resolution

Moreover, it was proven that increasing the TDC resolution beyond a certain limit by increasing number of bits for the same input range will not reduce fractional spurs due to nonlinearities that result from local mismatches between delay elements and PVT variations. In [139], it was shown that TDC non-idealities lead to spur regrowth and any error in its cancellation exaggerates spurs level. In ADPLL, in-band fractional spurs due to INL of TDC can be expressed as [139]

$$\ell = 10\log\left[\frac{\pi^2}{4}\left(\frac{INL(LSB)\times TDC_{res}}{T_{Div}}\right)^2\right] \tag{5-3}$$

The above equation indicates that resolution of TDC (LSB) should be better than 400 fs with INL < 1 LSB to achieve fractional spurs less -45 dBc for output frequency of 66 GHz.

Therefore, the design of fine resolution TDC's and associated calibration/linearization schemes have recently evoked high interest.

In a typical mm-wave divider-less frequency synthesizer, the TDC should ideally operate at the DCO output frequency (57 GHz-66 GHz) and cover one cycle of the input frequency; however, this is infeasible due to the extremely high frequency of the DCO. Therefore, an inductor-less DCML divider is used in this work to divide the DCO frequency by 4 to provide a reasonable operating frequency range for the following stages.

Table 5-1 Basic specifications of proposed TDC for 60 GHz ADPLL

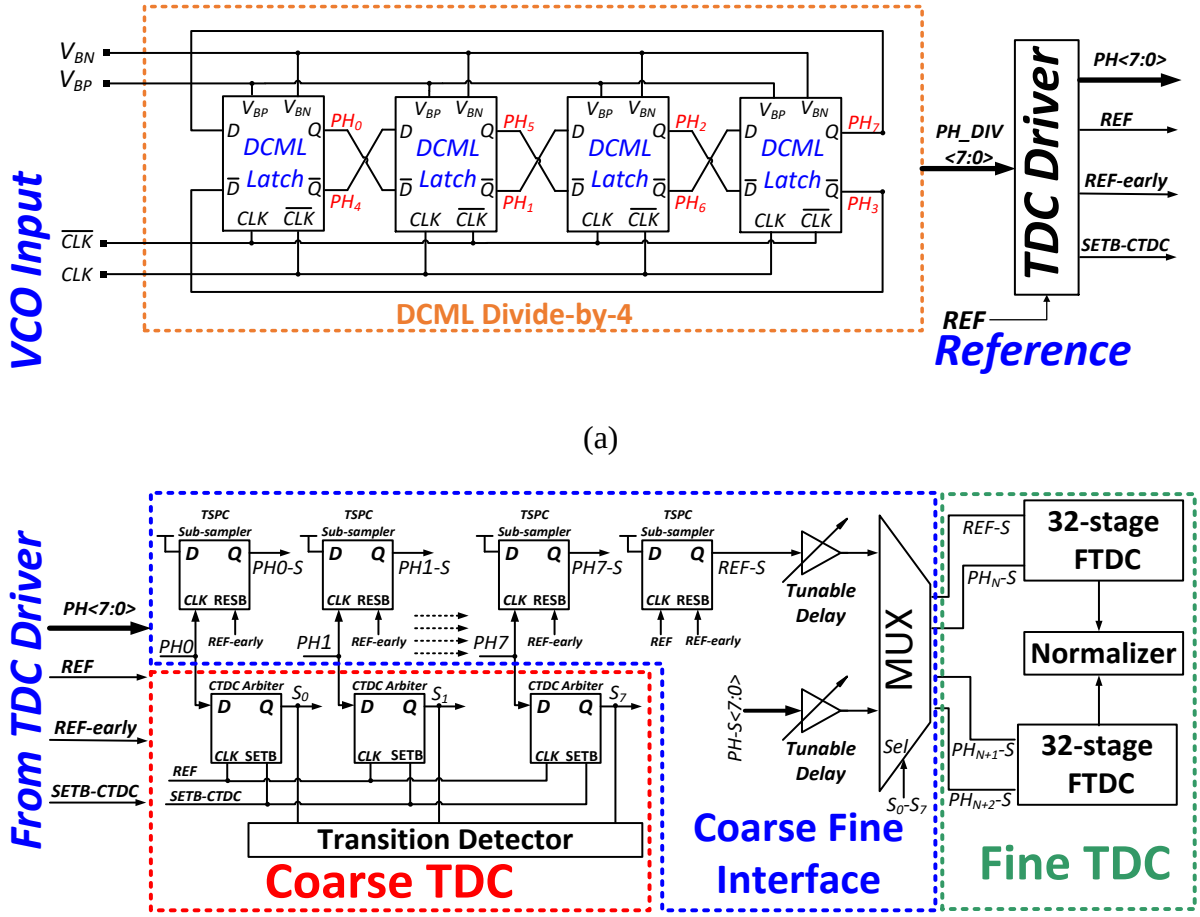
Specification	Input Frequency	Dynamic Range	Resolution	INL	Conversion Rate
Value	12.5GHz-17GHz	80ps	< 400fs	< LSB	F_{Ref} (100MS/s)

From the above discussion, a basic set of specifications can be derived for the TDC, as summarized in Table 5-1, to suppress fractional spurs to below -45 dBc at 66 GHz output frequency and with in-band phase noise less than -100 dBc/Hz.

5.3 Proposed two-step 17 GHz TDC

Figure 5.3 shows the block diagram of the proposed 60 GHz TDC which comprises:

1) A dynamic CML (DCML) divider that divides the input frequency by 4 and produces eight phases *PH_DIV<7:0>*, with uniform spacing of 45^{o}, at 5-17 GHz from a 20-68 GHz input. The source coupling + current bleeding topology (Figure 4.5) have been used to implement the DCML latch to widen locking range of divider with low power consumption.
2) A two-step 8-bit TDC comprising a coarse stage (CTDC), a sub-sampling coarse fine interface (CFI) and a pair of fine TDC's (FTDC).



(a)

(b)

Figure 5.3 Simplified block diagram of proposed mm-wave two-step TDC. (a) DCML divider-by-4 and TDC Driver. (b) 17 GHz two-step TDC

As discussed previously, the main advantage of two-step TDC architecture is breaking the trade-off between the dynamic range requirement and number of stages in Vernier delay line. However, there are three main challenging issues related to implementing two-step TDC inside the mm-wave ADPLL:

- Storing and delivering the time residual from coarse measurement to fine TDC.
- Due to ADPLL operation [138], the output of TDC should be normalized to the input period which requires additional circuits.
- High power consumption of overall TDC due to high input frequency.

In order to overcome these challenging issues, 17 GHz two-step was originally conceptualized in [140] and implemented in this work with new circuit implementations of the driving stage, the interface stage, CTDC and the FTDC stage.

The TDC driver converts the eight phases, produced by the DCML divider (*PH_DIV<7:0>*) to CMOS level and passes these eight phases (*PH <7:0>*) and the reference signal (*REF*) to the CTDC and interface stage. It also generates the desired set and reset signals of the CTDC and interface stage with the appropriate delays (not shown in Figure for drawing simplicity). The design and layout of driver should be done carefully to ensure equal delays between the 8 phases and reference signal which are connected to interface stage, and CTDC.

The CTDC uses these eight phases as delay versions of input signal (*PH<0>*). The main purpose of CTDC stage is find the location of rising edge of reference signal (*REF*) with respect to rising edges of *PH <7:0>* as shown in Figure 5.4. The core of CTDC comprises 8 arbiters (time comparators) which determine how many phases arrive earlier than the reference signal (Figure 5.3 (b)). The transition detector converts the output of the CTDC to a one-hot code which is encoded as a 3-bit word which represents the three MSB's bit of the TDC word. It can be noticed that the three bits output of CTDC are pre-normalized.

The interface stage in the proposed two-step TDC plays a crucial role in TDC. Its main functions are:

1) Accurately store and pass the time residue from the coarse stage to the fine stage as shown in Figure 5.4.
2) Reducing the switching frequency of *PH<7:0>* in order to reduce power consumption of FTDC. Therefore, the interface stage (*CFI*) comprises a sub-sampling circuit which samples the eight phases generated by the TDC driver (*PH <7:0>*) using the early

version of reference signal (*Ref_early*). In order to maintain the same delay difference between reference signal and the eight phases generated from subsampling circuit (*PH<7:0>-S*), the reference signal (*Ref*) is also retimed using the early version of reference signal (*Ref_early*) as shown in Figure 5.3 (b) and Figure 5.4. This, in turn, reduces the switching rate of the eight phases from 17 GHz to 100 MHz which reduces power consumption in the following stages and the FTDC.

Following the subsampling stage, the eight signals (S_0-S_7) that are generated from transition detector of CTDC are used by the multiplexer (*MUX*) in the interface stage to pass on to the FTDC stage the time residue between the reference signal (*REF-S*) and the phase that immediately leads it (PH_N-*S*) as shown in Figure 5.4. It should be mentioned that, the reference signal (*REF-S*) passes through a dummy multiplexer which is included in the interface stage in order to equalize the delays between selected signal phase (PH_N-*S*) and reference signal. Additionally, *CFI* passes to the second FTDC the two phases (PH_{N+1}-*S*, PH_{N+2}-*S*) which lag reference signal for normalization purpose.

The coarse-fine interface also includes an input multiplexer (*MUX Cal*) and tunable delay elements for CFI calibration, as will be discussed in next sections.

Each FTDC employs a Vernier delay line and it consists of 32 stage to cover one quantization step of CTDC (7.4ps - 10ps) with the desired time resolution of 400 fs. The first FTDC measures the time residual of coarse measurement and generates 32 output signals that are converted to a one-hot code using a transition detector, then this code is encoded as 5-bits word ($FTDC_1$<4:0>).

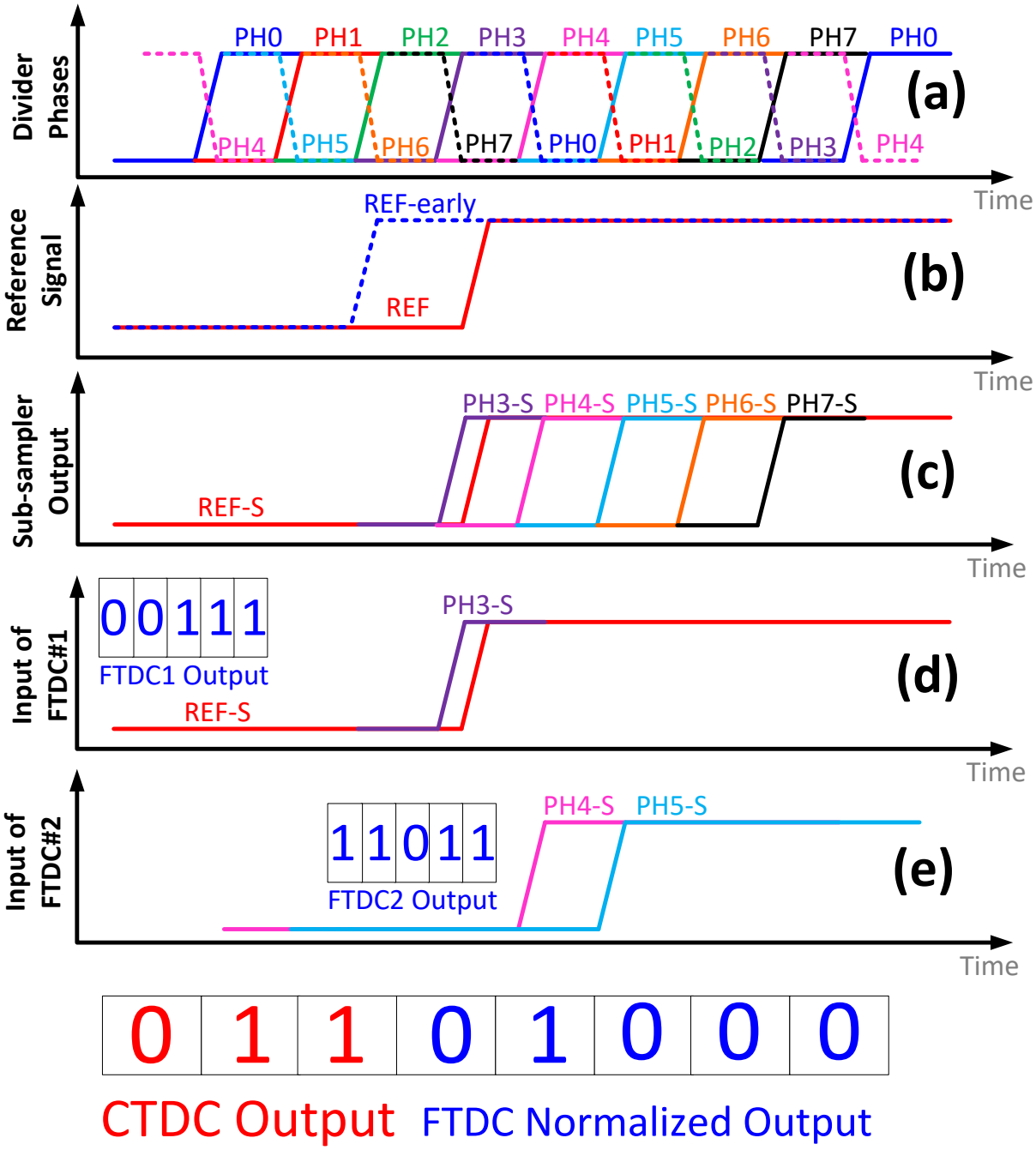


Figure 5.4 Time waveforms of TDC (a) Eight phases from DCML divider (16 GHz). (b) Reference signal (100 MHz). (c) sub-sampler outputs (100 MHz). (d) Input of first FTDC. (e) Input of second FTDC.

The second FTDC measures the delay difference between two consecutive phases (i.e., one quantization period of CTDC) to estimate the input period of TDC, to use afterwards in output normalization. The 32 output signals of second FTDC are converted to a one-hot code using a transition detector, then this code s encoded 5-bits word($FTDC_2<4:0>$).

In the normalization operation, $FTDC_1<4:0>$ and $FTDC_2<4:0>$ form the numerator and the denominator, respectively. The division operation is implemented with a look-up-table (LUT) and provides a 5-bit output which along with pre-normalized 3-bits of CTDC will generate 8-bit TDC word.

Table 5-2 Basic specifications of coarse TDC (CTDC)

Specification	Input Frequency	Dynamic Range	Resolution	Conversion Rate	Normalization
Value	12.5GHz-17GHz	58-80 ps	7.4 - 10 ps	F_{Ref} (100MS/s)	Pre-normalized

Based on the above discussion, the basic specifications of CTDC and FTDC can be summarized in Table 5-2 and Table 5-3, respectively.

Table 5-3 Basic specifications of fine TDC (FTDC)

Specification	Input Frequency	Dynamic Range	Resolution	Conversion Rate	Normalization
Value	F_{Ref} (100 MHz)	10ps	< 400fs	F_{Ref} (100MS/s)	Using LUT

5.3.1 Coarse TDC (CTDC)

As mentioned in last section, the coarse TDC stage (CTDC) consists of 8 arbiters (time comparators) which determine how many phases arrive earlier than the reference signal. D-flip flops are avoided since it creates a mismatch between clock and data path which results in large blackout time, the unresolvable time difference between arbiter inputs, compared to target resolution.

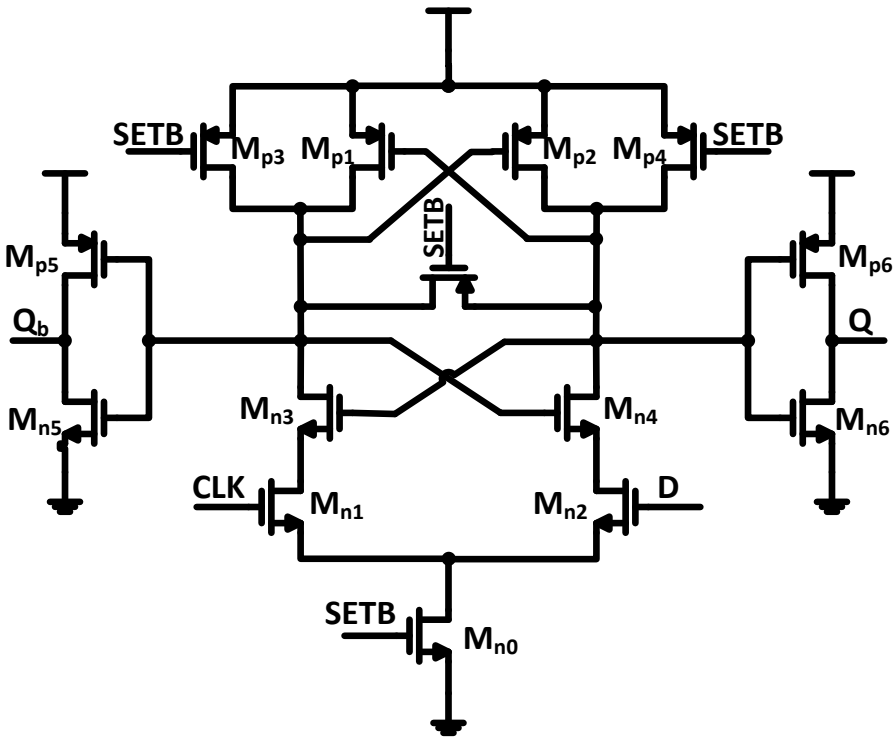


Figure 5.5 Schematic of coarse TDC arbiter

Alternatively, a differential fully symmetric sense amplifier (Figure 5.5) is used as CTDC's arbiter to guarantee equal delay in data and clock paths to minimize time offset in CTDC core.

Initially, the arbiter outputs are pulled high through SETB signal and PMOS transistors (M_{p3}-M_{p4}). When, the SETB becomes high, input transistors senses the leading edge and The cross-coupled NMOS (M_{n3}-M_{n4}) and PMOS (M_{p1}-M_{p2}) pair will then regenerate the input difference and latch the output in the direction of the leading edge [140]. The input transistors (M_{n1}-M_{n2}) are sized large enough to reduce the mismatch variation, increases arbiter gain, and to reduce blackout time. Post-layout simulation shows that blackout time is less than 25fs.

Moreover, to reduce switching current due to high frequency of *PH<7:0>*, NMOS switch (M_{n0}) is used to disconnect the current path from ground with SETB (early version of REF) when the arbiter is inactive.

5.3.2 Coarse-Fine Interface (CFI)

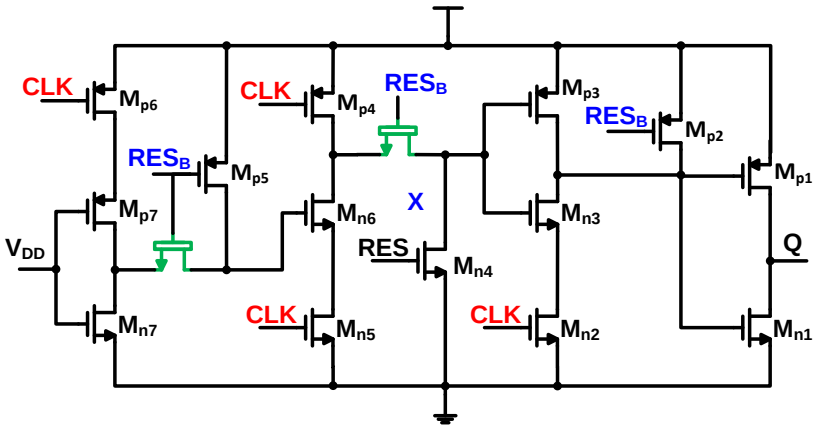


Figure 5.6 Schematic of Sub-sampler TSPC flip-flop. Green transistors are not used in the actual implementation (short circuit)

As mentioned previously, the first block in CFI stage is sub-sampler circuit which accurately maintains the delay between the eight phases and reference signal and reduces the switching rate of the eight phases from 17 GHz to 100 MHz in order to reduce power consumption. The sub-sampling operation has been implemented using TSPC flip-flop (Figure 5.6) where the input is tied to supply and high speed phases are connected to *CLK* terminal. Early version of reference signal (*REF-early*) and its inverted version are connected to *RES* and RES_B, respectively, as shown in Figure 5.6 to reset the flop's output. At the rising edge of *REF-early* the internal reset devices (M_{n4}, M_{p5}, M_{p2}) of TSPC flip-flop are released and the flop is activated.

Afterwards, the output of the DFF will go high at the first rising edge of the input clock (high speed signal), and remains high until the next reset signal. In other words, the rising edge is synchronized with the input signal while the falling edge is synchronized with an early reference. Post-layout simulation shows that the static current of each sub-sampler stage is 92 uA at 16 GHz input frequency (*PH<7:0>*) and 100 MHz reference frequency (*Ref_early*). Please note the

static current can be eliminated by using the NMOS transistors controlled by RES_B in path of static current (Green transistors in Figure 5.6) on the expense of larger CLK-to-Q delay.

Obviously, the frequency of sub-samplers is reduced while the time difference between rising edges of input phases and reference signal is kept the same. Since the output code of the CTDC should be ready at the input of interface multiplexers (MUX in Figure 5.3) before the arrival of the sub-sampler outputs, LVT devices were used in the CTDC path (i.e., core, transition detector, and CTDC buffer), HVT devices were used in the interface stage, and LVT devices were used in the sampling circuit to accommodate 17GHz input signals.

5.3.3 Fine TDC (FTDC)

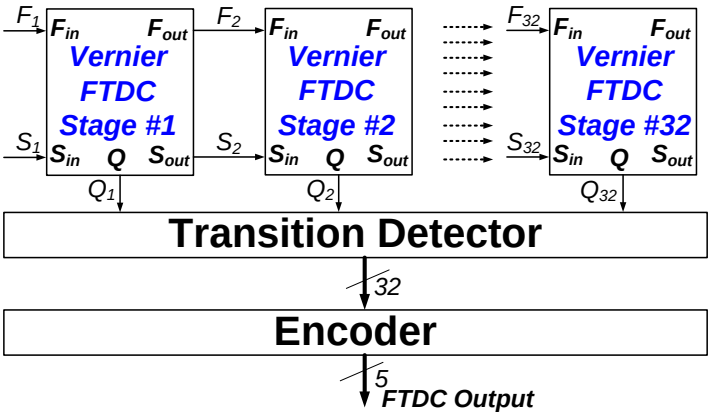


Figure 5.7 Schematic of fine TDC (FTDC)

Figure 5.7 shows the schematic of Vernier delay line FTDC which consist of 32 stage to cover the quantization period of CTDC with the desired resolution as discussed in section 5.2. However, as will be discussed in next section, cascading large number of delay unit increases TDC non-linearity due to PVT and mismatch variation which limits the effective resolution of TDC. In order to alleviate TDC non-linearity, due to mismatch variation, two main designs are considered for FTDC unit. Figure 5.8(a) shows the schematic of first design which depends on statistical element selection (SES) delay unit.

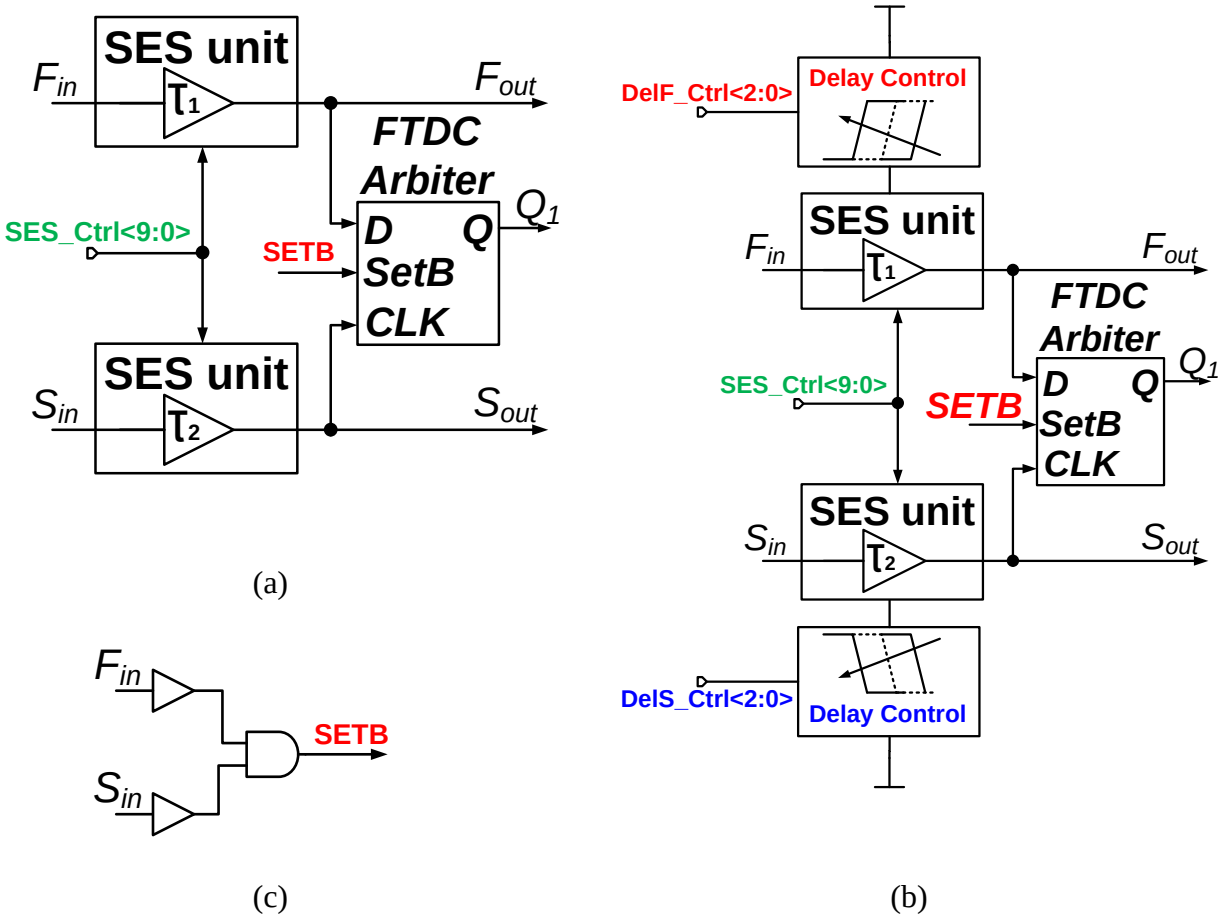


Figure 5.8 (a) Schematic of FTDC stage based on SES. (b) Schematic of FTDC stage based on SES with mean adaption. (c) Generation of reset signal of FTDC arbiter

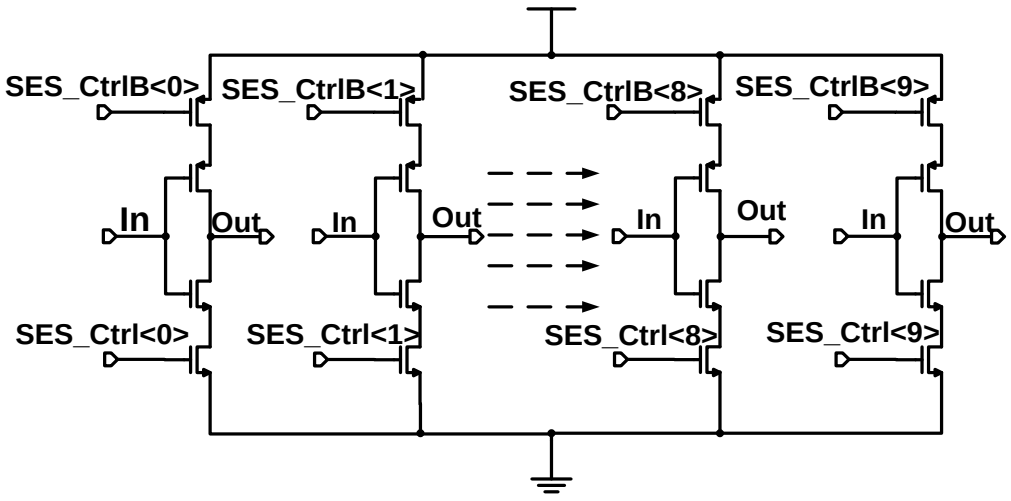


Figure 5.9 Schematic of SES delay unit of FTDC stage

Each SES delay unit consists of two inverter stages, and each inverter is comprised of 10 switched branches of smaller inverters controlled by digital word as shown in Figure 5.9. These small inverters are enabled/disabled, to perform SES, using calibration engine as will be discussed in next section.

Implementing a Vernier delay difference between the input signals using different explicit capacitance, parasitic capacitance, or different loading at output of delay element leads to large dependency on input amplitude (i.e., since load capacitance changes with input amplitude) which exacerbates TDC non-linearity. In this work, the Vernier delay difference is achieved using a 3-bit current-starved cell [141], [142] to guarantee monotonic relative delay difference versus control word and to implement the coarse tuning of SES calibration technique, as discussed later. Behavioral simulations show that the mean delay difference per stage is programmable over the range of 0.2 ps ~ 1.4 ps. This, in turn, implies that the whole TDC can work with input frequency range from 2.8 GHz to 19.5 GHz with resolution less 300 fs.

FTDC unit uses the same CTDC's time arbiter where the reset signal of time arbiter is generated using AND gating between input signals as shown in Figure 5.8 (c). Post-layout simulations show that the delay of reset signal generation's structure (Figure 5.8 (c)) is less than 15 ps while the delay of SES unit is around 75 ps which provides the sufficient time margins for time arbiter to sample input signals accurately.

Similar to CTDC stage, a transition detector finds the stage at which the sampled output changes from 1 to 0 and provides a one hot code which is later decoded into a 5- bit binary output. To avoid bubble errors a three input AND with Q_{N-1}, Q, QB_{N+1} is used in the transition detector [140].

5.4 TDC nonlinearity

Mismatches and PVT variations dramatically degrade the linearity of the FTDC transfer function. Random and systematic mismatches in the delay units or time arbiters can easily cause deviation from an ideal TDC transfer function. Moreover, with the continuous scaling of CMOS technology, the effect of process variation and random mismatches on TDC nonlinearity increases adversely.

In the Vernier delay line, the delay variation of each stage accumulates along the delay line. Figure 5.10 (a) shows the Monte Carlo simulation of first stage in FTDC with target delay difference of 300 fs. In this simulation, the mismatch effects of delay control unit, time arbiter, and SES unit with middle control word are included. It can be noticed that the standard deviation of the delay difference of one stage is more than two times desired resolution. Basically, the standard variations of one stage of Vernier TDC delay line can be expressed as [140]:

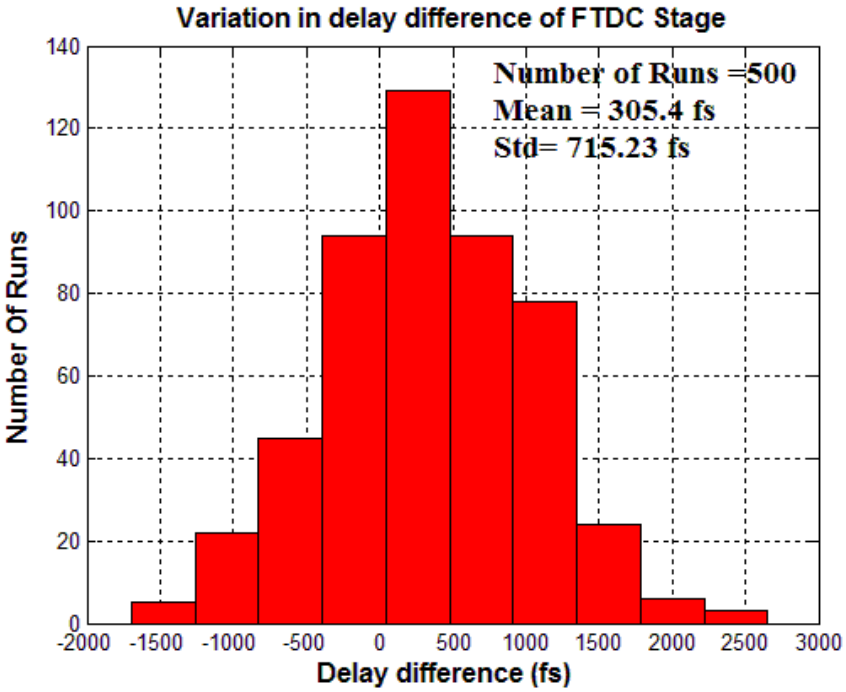
$$\sigma_{stage} = \sqrt{\sigma^2{}_s + \sigma^2{}_f + 2\sigma^2{}_r} \tag{5-4}$$

Where σ_s, σ_f, and σ_r are the standard variation of slow delay line, fast delay line and time arbiter, respectively. Extensive Monte Carlo simulation proves that the delay variation of FTDC stage is dominated by mismatch in delay elements and since the delay variation accumulates along the line, the standard deviation of total delay difference at each step of FTDC transfer function can be expressed as:

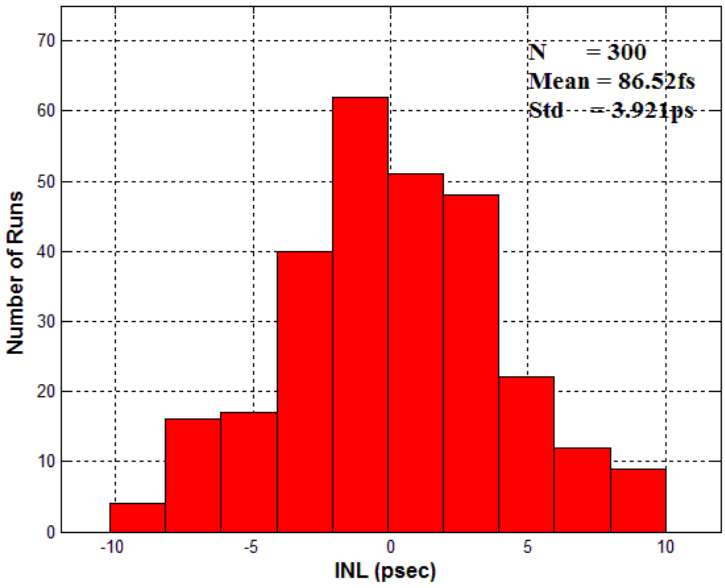
$$\sigma_{n,TDC} = \sqrt{n} \times \sigma_{stage} \tag{5-5}$$

Where n is the stage number and σ_{stage} is the standard variation of single stage. Figure 5.10 (b) shows the Monte Carlo simulation of delay variation of final stage of FTDC. It can be noticed

the standard deviation, which follows the above equation is 13 times target LSB since nonlinearity grows along the line.



(a)



(b)

Figure 5.10 Mismatch variation of (a) First FTDC stage. (b) Final FTDC stage (Stage # 32)

Moreover, the FTDC resolution is very sensitive to supply and temperature variations. Even with a separate voltage regulator for FTDC, glitches on the supply line affect the INL of FTDC; post-layout simulations indicated glitches of 50mV degrade the INL by more than 3 LSB.

5.5 FTDC calibration technique

Several calibration techniques have been reported recently to alleviate the effect of mismatch between delay lines. In [42], a random sequence is added at the input of TDC with the purpose of dithering the error at each step by the random noise. This technique reduces the power of fractional spurs at the output of ADPLL on the expense on increasing in band phase noise [42]. Another calibration method depends on measuring the output code of TDC and creating a histogram of TDC output [143], [144]. Afterwards, the output of each stage is mapped and corrected [144]. In this work, we investigate using statistical element selection (SES) [145], [60] to calibrate the FTDC.

5.5.1 Statistical element selection (SES)

Statistical element selection (SES) was proposed in [146] to mitigate the effect of random transistor mismatches in analog circuits. It was shown in [146] that given N identical elements, a subset of k elements can be chosen such that their combination minimizes the standard deviation of a particular parameter. By using SES, the input offset voltage of latch type comparator is reduced by orders of magnitude [145]. It was shown in [145] that SES reduces the overall area required to meet a specific matching specification between input pairs of latch type comparator.

Calibration techniques based on SES have been applied in different RF and analog circuits and demonstrated large performance improvement. For example:

1) 8-bit 1.5GS/s flash ADC [147]: SES was used to reduce the input offset voltage of latch type comparators to implement 8-bit flash ADC. Measurement results show that, by

applying SES, the standard deviation of input offset of comparator is reduced from 11.2 mV to 0.35 mV which results in yield improvement from 15% to 99.5%.

2) 6-bit flash ADC based on self-referenced comparator [60]: Coarse tuning was applied in [60] in order to increase the calibration range of SES. This method depends on shifting the mean value of the entire offset distribution of a self-referenced comparator to cover a large calibration range compared to SES with fixed mean. It was shown in [60], by applying coarse tuning with SES, the full scale range of self-referenced comparator can be increased by 2.5 times compared to the achievable range using SES only. The goal of using SES in latch type comparators [146], [147] is to minimize the input offset of comparator, while the goal SES with coarse tuning in [60] is to calibrate each self-referenced comparator at different voltage level to cover the whole reference range of flash ADC.
3) 14-bit current steering DAC [148] : SES was used to relax the matching requirements for current source array to reduce overhead cost and to calibrate the amplitude errors which improves the static linearity of current steering DAC. The concept was demonstrated by implementing 14-bit current steering DAC. Measurement results shows that the INL of current steering DAC is improved from 6.28 LSB to less than 0.6 LSB by applying SES.
4) 6-bit 5GS/s flash ADC [149]: SES was used to calibrate the input offset voltage of self-referenced comparators to implement 6-bit flash ADC in 32 nm.

It was shown in [150] that, the SES has limited calibration range and it is effective only if there is only one dominant variation source in the circuit being calibrated. Extended statistical element selection (ESES) [150] was proposed to increase the calibration range of conventional SES and to compensate the other sources of mismatches in the target circuit. The ESES design

methodology depends on having a N non-uniformly sized elements to widen the distribution range even without random variation. It was shown in [150], that the ESES achieves wider calibration range and reduces the area overhead and power consumption compared to SES. However, it leads to a trade-off between the high distribution density at the center of nominal design value and the calibration range. The concept of calibration circuit based on ESES was proposed for:

1) Current steering DAC [151]: Similar to [148], ESES was applied to implement current source array with main target of calibrating the amplitude errors. Simulation results show that, compared to SES, the ESES calibrates the timing errors and achieves better static linearity over Nyquist band of current steering DAC [151].
2) Phase mismatch calibration [152]: The ESES was used in [152] to calibrate the phase/delay mismatch between two signals. The concept of delay calibration depends on breaking the NMOS and PMOS transistors of single inverter (in the path of desired signal) into parallel branches of small inverters. Theses inverters were sized non-uniformly in an arithmetic sequence. These branches were enabled or disabled by controlling switches at the source of NMOS and PMOS transistors of these small inverters.
3) Wideband RF Receiver [152]: ESES was used to calibrate the gain mismatch in harmonic rejection receiver by tuning the bias current of GM stages. Measurement results show that, by applying ESES, the second and third harmonic rejection ratio are improved by more than 24 dB and 37dB, respectively.

5.5.2 FTDC calibration using statistical element selection (SES)

In this work, we apply the concept of statistical element selection (SES) in the implementation of Vernier FTDC to reduce the standard deviation of the delay difference between the two delay lines.

A. SES with Fixed Mean

Assuming the Vernier delay difference between the two delay lines is achieved using different explicit capacitors at their output nodes. The SES can be used to alleviate the transistors mismatch between the delay units inside each delay line to reduce the standard deviation from ideal time difference of each FTDC stage. Figure 5.9 shows the implementation of proposed delay element used in FTDC stage, it consists of ten identical inverter branches (*N=10*) which can be enabled/disabled by digital calibration engine.

If the delay of each inverter is modeled by a Gaussian distribution $\boldsymbol{N}(\mu_i, \sigma_i)$, the standard deviation of *k* selected subset elements (σ_k) can be expressed as:

$$\sigma_k = \frac{\sigma_i}{\sqrt{\sum_{i=1}^{N} k_i}} \tag{5-4}$$

The objective of the calibration engine is to find the 10-bit control word to select the best *k*-element which achieves the desired time difference of each stage.

As was discussed in section 5.2, for proper TDC operation, DNL and INL should be less than one LSB with three sigma variation. Therefore, by assuming a target resolution of 300 fs, the sigma variation of each stage should be less than 7 fs. While, as shown from Figure 5.10, the sigma variation is more than 700 fs.

In [145], the failure probability, defined as the statistical frequency of having a particular specification exceeding a target value, is adopted as a measure of success of the SES technique.

$$P_{failure} = 1 - erf\left(\frac{spec}{\sqrt{2}\sigma_{stage}}\right) \quad (5\text{-}5)$$

Where spec is the target delay variation (i.e., the offset from the ideal time difference of each stage), erf is Gauss error function, and σ_{stage} is the standard variation of single FTDC stage.

Figure 5.12 shows the simulated $P_{faliure}$ of a single FTDC stage based on SES delay unit (Figure 5.8 (a)) for different numbers of element *N* and selected subset elements *k*. Each contour represents a different N value while x-axis represents the number of selected elements (*k*). This figure is generated using 1 x 10^5 Monte Carlo sample in MATLAB. The target deviation (spec) of FTDC stage is 7 fs. Table 5-4 summarizes the simulation conditions used to simulate the $P_{faliure.}$ The standard variation of single FTDC stage (σ_{stage}) is calculated from post-layout simulation of FTDC stage.

Table 5-4 Summary of simulation parameters for failure probability

Parameter	σ_{Stage}	Spec (Stage)	Target LSB	Target INL
Value	679 fs	7 fs	300 fs	< 1 LSB

We use the simulated failure probability of FTDC stage to estimate the required number of combinations (i.e., N and K) to achieve a target yield of whole FTDC. It can be observed that to achieve a stage yield better than 90%, *N* should be higher than 12 with *k* between 4 and 6. This means there is more than 924 possible combinations to achieve the target specification for only one stage.

However, it should be noted that the yield of a cascade of stage with SES implementation reduces exponentially with number of stages. The yield on n stage delay line can be expressed as:

$$Yield = \left(1 - P_{faliure}\right)^{n} \tag{5-6}$$

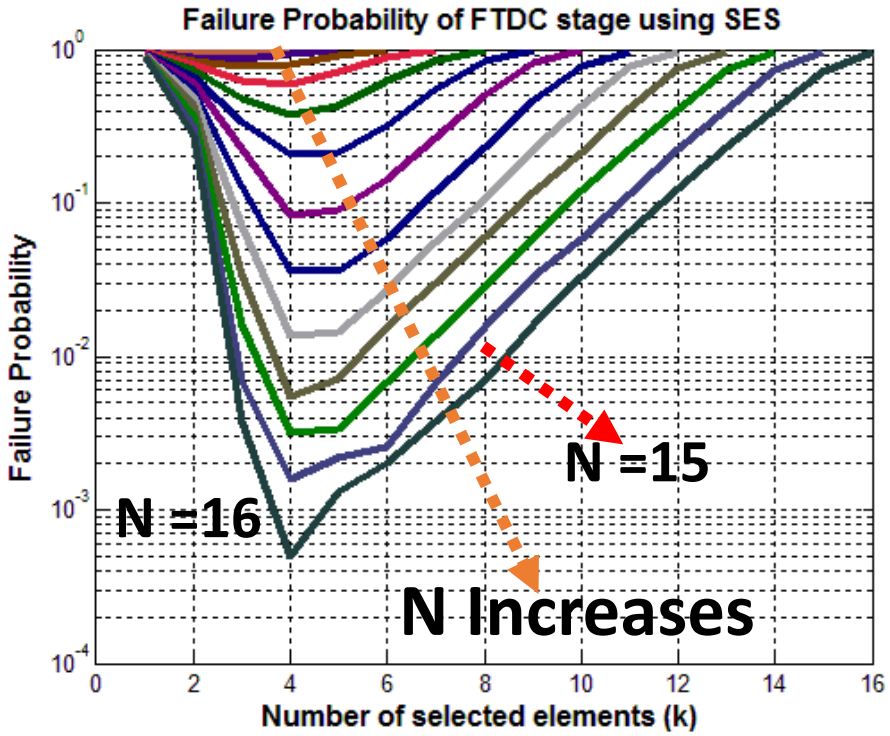


Figure 5.11 Failure probability versus number of selected delay elements for target variation < σ/100 using SES

Therefore, to achieve overall yield more than 90 %, it can be shown that N should be higher than 16 with *k* of 4. This means there is more than 1820 possible combinations. Table 5-5 summarize the required number of combinations of each SES-FTDC stage to achieve yield of 99% and 99.9%.

Table 5-5 Required number of N and K for different yields of FTDC based on SES

N_{Min}	K	${}^{N}C_{K}$	Yield of 1-stage	Yield of 32-stage
13	5	1287	99%	70.6%
16	4	1820	99.9%	96.1 %

B. SES with Mean Adaptation

SES can be used to utilize the process variation to achieve the target resolution of each FTDC stage without explicit output capacitors. In this case, the mismatch variation between the delay units is used to tune each stage for target resolution. The same idea was used to implement a Flash ADC with self-reference [60], [153]. However, in this case, the FTDC stage resolution is limited by the amount of mismatch variations (i.e., 3 σ_{stage}) which limits the dynamic range of TDC.

From Figure 5.12 and Table 5-5, it can be noticed that increasing the population size *N* enhances the probability of finding the best matched *k*-element subset elements, but this also increases the die area and power consumption. Furthermore, it dramatically increases the calibration time and complexity of on-chip calibration engine.

In this work, to overcome the above limitations, the SES is simultaneously used with mean adaption of the target resolution (delay difference in the case of the FTDC). The main target of mean adaption is to shift the variation distribution of stage delay in order to cover large calibration range with fewer combinations. Current starved tunable delay cells [141], [142] are used to adapt the mean of delay difference between the two input paths as shown in Figure 5.8 (b). The mean value of each delay line can be shifted from 0.2ps to 1.4 ps (0.28 σ_{Stage} to 2 σ_{Stage}) with 3-bit control.

This concept was proposed in [60] to increase the calibration range of SES. The whole offset disturbation of comparator is shifted by $\pm 1.5\ \sigma$ to increase the full scaled range of flash ADC based on self-referenced comparator [60]. In this work, the delay distribution of FTDC stage can be shifted by a fractional of σ_{Stage} to reduce required number of combinataions (i.e., N and K) for

giving yield spec. In addtion, the delay distribution can be shifted up to 2 σ_{Stage} to widen the dynamic range of FTDC.

Figure 5.12 (b) shows the simulated $P_{faliure}$ of a single FTDC stage based on SES with mean adaption (Figure 5.8 (b)) for different number of element *N* and selected subset elements *k* with the same simulation conditions summarized in Table 5-4. The calibration algorithm depends on adapting the mean value of delay distribution first then uses the SES searching to find the best subset elements *k* which meets the target delay difference of each FTDC stage.

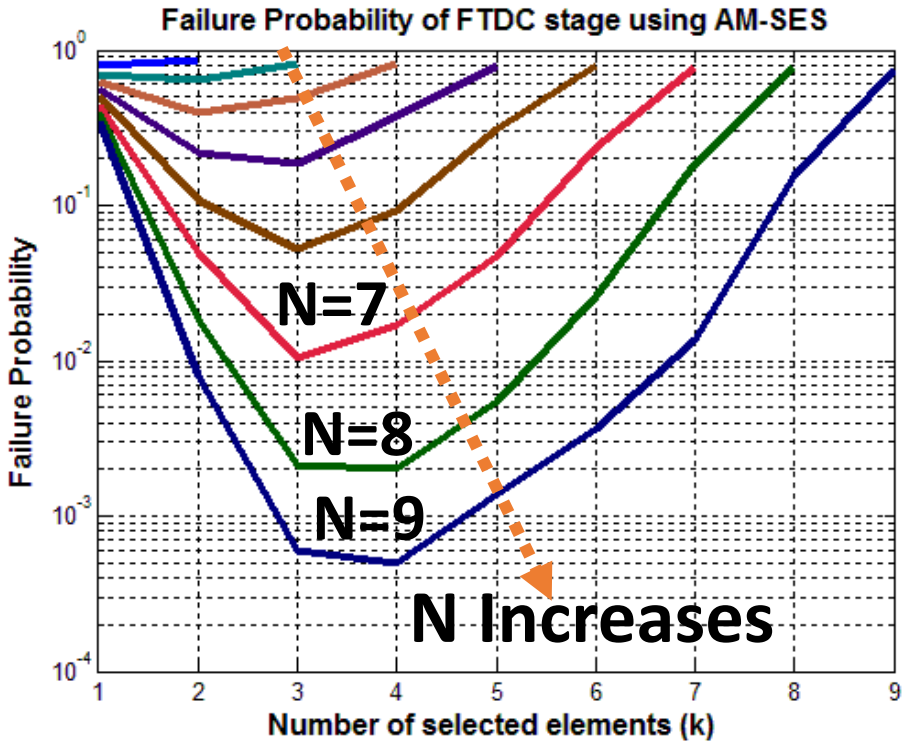


Figure 5.12 Failure probability versus number of selected delay elements for target variation < σ/100 using SES with mean adaption.

It can be observed that to achieve FTDC yield higher than 90%, *N* should be higher than 9 with *k* between 3 and 4. This can be achieved by only 126 combinations. Table 5-6 summarize the required number of combinations of each FTDC stage, based on SES with mean adaption, to achieve yield of 99% and 99.9%.

Table 5-6 Required number of N and K for different yields of FTDC based on SES with mean adaption

N_{Min}	K	${}^{N}C_{K}$	Yield of 1-stage	Yield of 32-stage
7	3	35	99%	70.9 %
9	3-4	84-126	99.9%	96.1 %

Clearly, by using mean adaption with SES, the calibration time, area and power consumption cane be reduced significantly. Moreover, a large improvement in area and complexity of the on-chip calibration engine can be achieved as the number of possible subsets of selected elements decreases. In addition, SES with mean adaption helps to improve calibration robustness if there is a large difference between the target TDC resolution and center of delay distribution.

5.6 TDC calibration algorithm

Two main parts in 17 GHz two-step TDC (Figure 5.3 (b)) should be calibrated accurately to guarantee proper TDC operation and to achieve the desired specifications (Section 5.2).

1. First and second FTDC for accurate time residual and CTDC's quantization period measurement, respectively.
2. Coarse-fine interface (CFI) stage.

In the following sub-sections, the detailed calibration algorithms of FTDC and CFI stages will be illustrated.

5.6.1 FTDC calibration algorithm

As was discussed previously, each FTDC stage consists of one SES delay unit which consists of two inverter stages, and each inverter is comprised of 10 switched branches of smaller inverters. These two inverters are controlled by same 10-bit digital word, while the absolute delay of fast and slow lines is controlled by two different 3-bit control words. In conclusion, each FTDC stage is controlled by 16-bit control word generated from on-chip foreground calibration

engine and stored in (32x16) register file. The main goal of calibration engine is to find the 16-bit control word of each stage which reduces the nonlinearity and to keep the time resolution of each stage around the desired spec.

For calibration purpose, two multiplexers are inserted before each FTDC to select either the signals coming from the coarse-fine interface (during normal operation), or two test signals which are applied externally (during calibration mode). The main idea of calibration engine is to measure the FTDC resolution of each stage with all the available combinations and select the best one with minimum nonlinearity. This process is repeated sequentially for all the 32 stages to minimize the error from previous stages, thereby minimizing the overall DNL/INL.

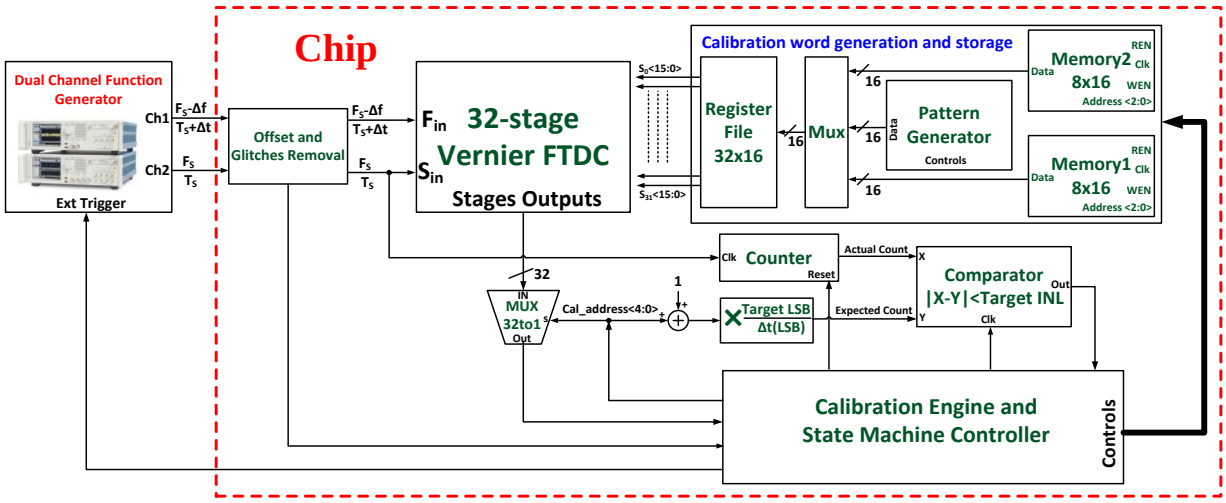


Figure 5.13 Simplified block diagram of on-chip TDC calibration engine

Figure 5.13 shows a simplified schematic of the SES calibration engine. During the FTDC calibration, the dual channel function generator produces two signals with a small frequency difference (Δf) to achieve small incremental time step each rising edge (Δt) between FTDC inputs. The frequency difference (Δf) between input signals is selected such as:

$$\Delta t = \frac{LSB_T}{N} \tag{5-7}$$

Where LSB_T is target resolution of FTDC and N is programmable calibration parameter which controls calibration time and accuracy as will be discussed later. Ideally, the output of M^{th} stage of FTDC will toggle after M*N rising edges. However, due to mismatch variation, this transition might occur at difference rising edge. The main goal of calibration engine is to guarantee that the transition of each stage, starting from initial point of calibration, occurs at rising edge T_r expressed as:

$$T_r = M * N - \frac{LSB_T}{K} \tag{5-8}$$

Where K is a programmable calibration parameter which determine the acceptable error of each FTDC stage.

The core of FTDC calibration algorithm can be explained briefly using two scenarios as shown in Figure 5.14 and Figure 5.15, respectively. Table 5-7 summarizes the calibration parameters used in these two scenarios. The calibration engine operates in two states: monitoring state and running state.

Table 5-7 Summary of FTDC calibration parameter

Parameter	Target LSB (LSB_T)	Calibration address (Stage # 1)	Δt	Excepted count (N)	Target error (K=2)
Value	400 fs	0 (M=1)	100 fs	4	< LSB/2

Monitoring state:

As shown in Figure 5.13 and Figure 5.14, assuming the input signals start initially with zero phase difference, based on address of current calibrated stage (*Cal_address<4:0>*) the transition

of the corresponding stage is monitored using 32-to-1 multiplexer. 16-bit digital controlled of current calibrated stage is generated from on-chip pattern word generator (Figure 5.13) and stored in the corresponding location in the (32x16) register file. Furthermore, a replica of input signal is used to trigger a digital synthesized counter to calculate number of clock cycles (*Actual count*) between start point of calibration and transition moment. Once the transC occurs, the *Actual count* is compared with *expected count (*M*N) as follows:

$$Out = \begin{cases} 1 \quad if \quad |Actual\_count - Expected\_count| < \dfrac{LSB_T}{K} \\ \\ 0 \qquad\qquad otherwise \end{cases} \qquad \textbf{(5-9)}$$

For example, as shown in Figure 5.14, output of first stage is monitored and once the transition occurs, the *Actual count* (4 in this example) is sampled and compared with *expected count.* Based on Equation (5-12), the result of comparison (1 in this example) is feed to calibration engine to move to the algorithm of success state (Figure 5.16 (a)). On the other hand, as shown in Figure 5.15, the transition occurs while the difference between *Actual count* and *expected count* is 2 which violates the target accuracy spec. Therefore, calibration engine moves to the algorithm of failure state (Figure 5.16 (b)).

Running state:

Based on the comparison result, the calibration engine moves to one of two states:

1- **Success state**: Figure 5.16 (a) shows a simplified flow chart of calibration algorithm during success state, when the comparison result indicates that current calibrated FTDC stage meets the desired spec. The main idea, during this state, is to find the best 8

calibration words of current calibrated stage, rank and sort them in First memory (Figure 5.13). Once this memory is full, its contents are moved to second memory and the first memory is erased and calibration address is updated.

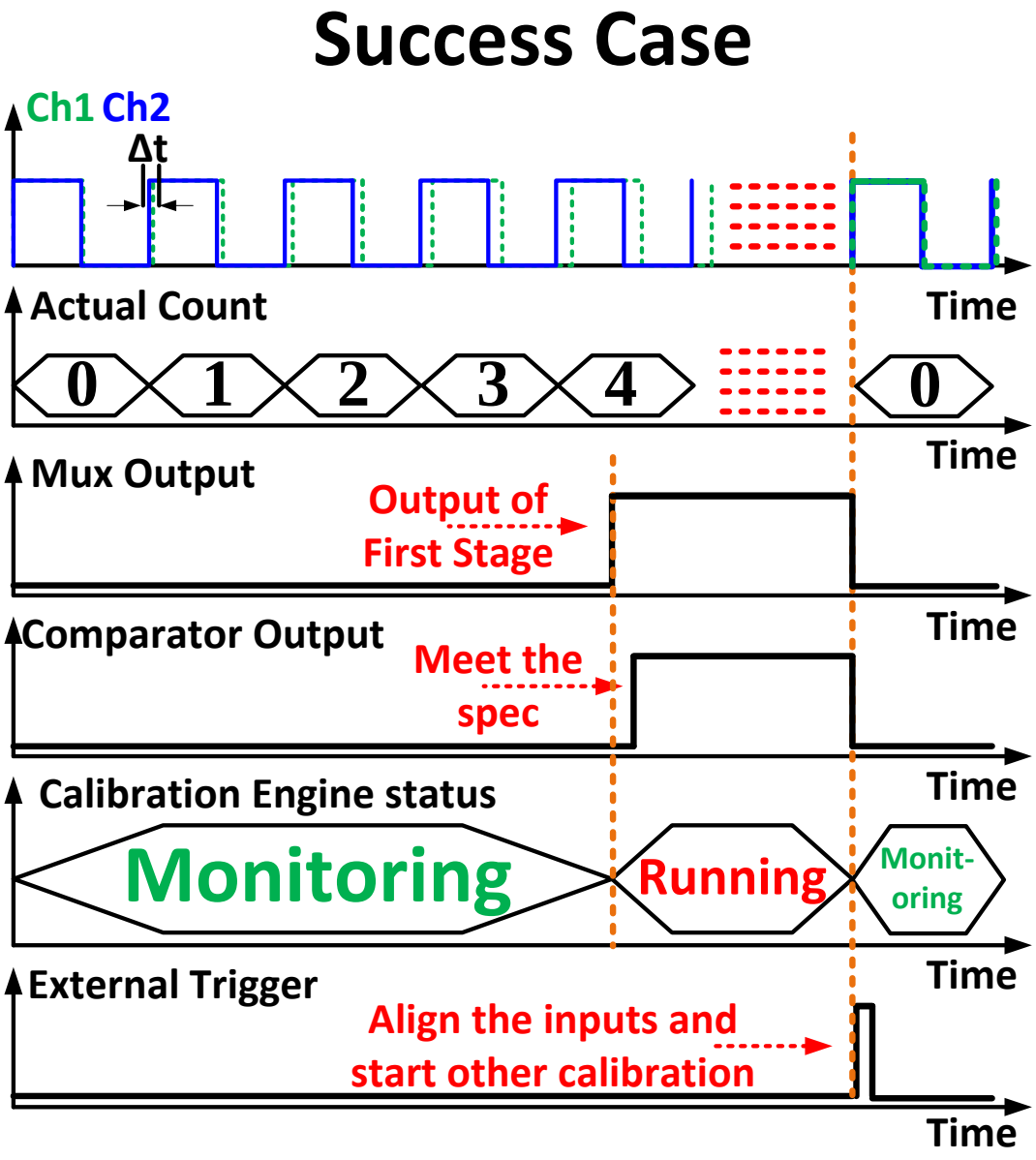


Figure 5.14 Simplified timing waveforms for FTDC stage calibration for case of success (achieve the desired step)

Calibration of next stage is initialized again by sending external trigger to dual channel function generator to align its input again (i.e., reset phase difference to zero)

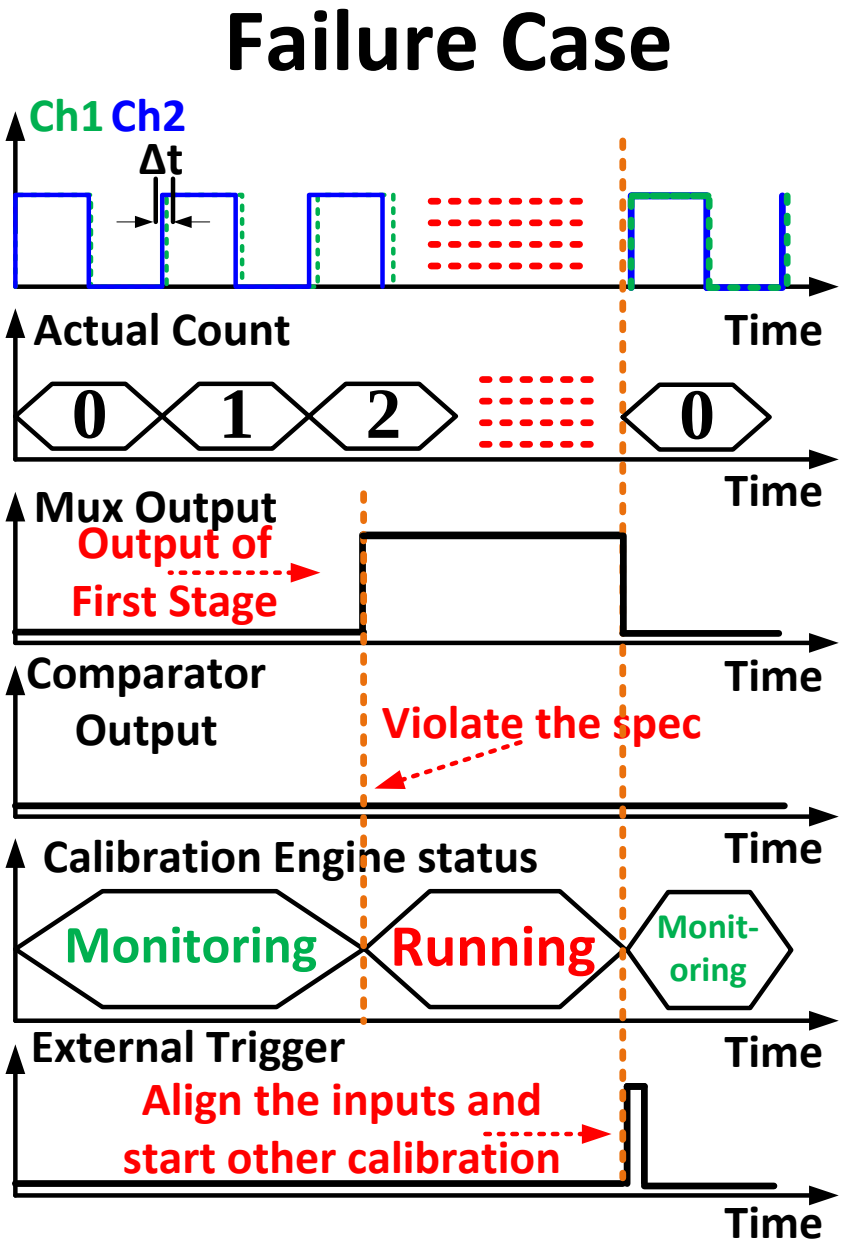


Figure 5.15 Simplified timing waveforms for FTDC stage calibration for cases of failure

1- **Failure state:** Figure 5.16 (b) shows a simplified flow chart of calibration algorithm during failure state, when the comparison result indicates that current calibrated FTDC stage violates the desired spec. In this case, calibration address is fixed and pattern word generator produces the next 16-bit calibration word. Calibration of current stage is repeated again by sending external trigger to dual channel function generator to align its input again (i.e., reset phase difference to zero) and calibration again moves to monitoring state.

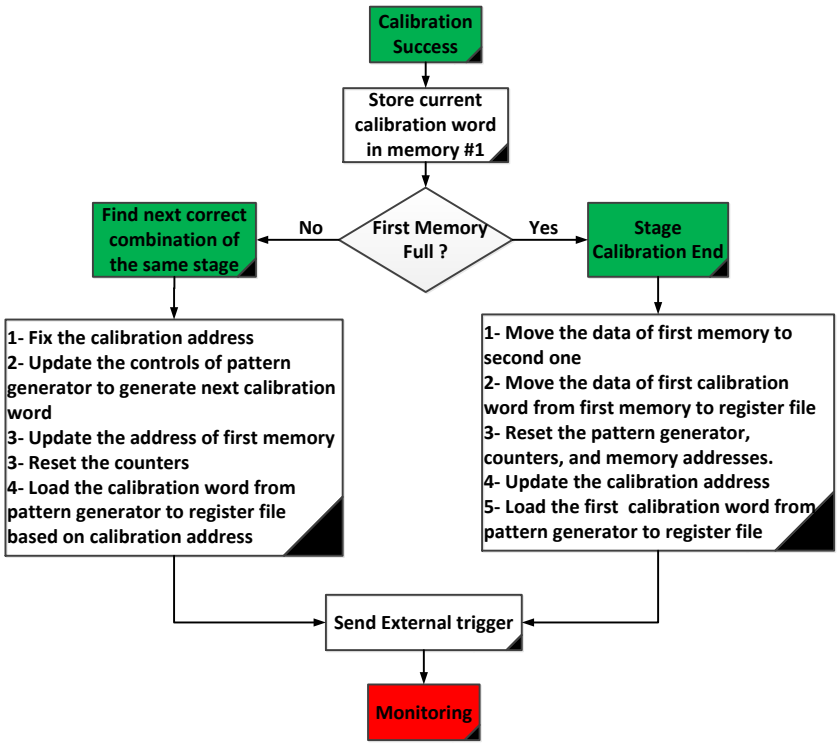
For a given stage if no combination is found to meet the desired spec, the calibration engine updates the calibration address to previous stage and select other calibration word from second memory to load it in register file. Afterwards, the calibration address is set again to the desired stage and its calibration is repeated gain.

5.6.2 Special issues in FTDC calibration

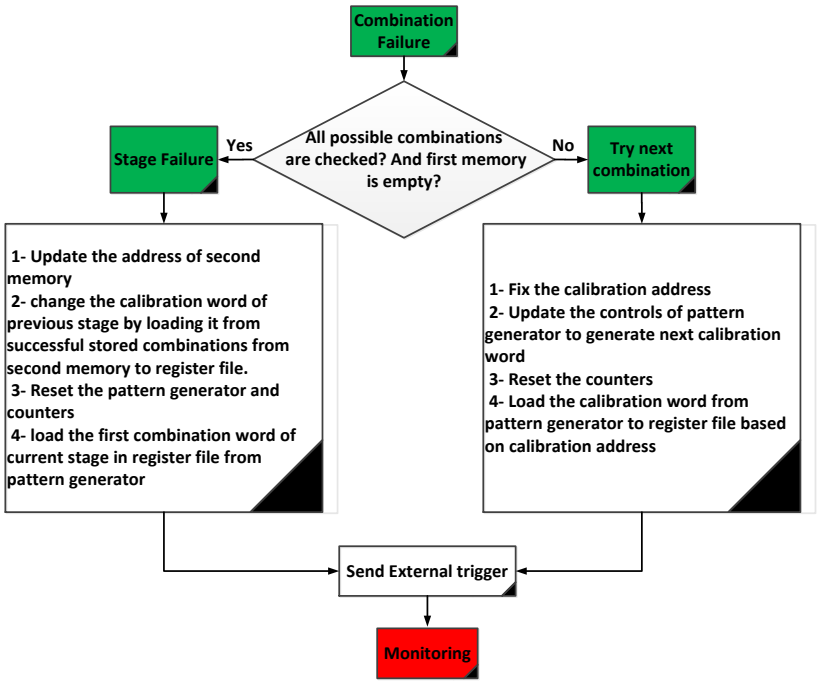
There are enormous issues which can affect the accuracy of calibration scheme such as:

- **Random noise:**

  Random noise of supply voltage, CMOS devices and input clocks which can affect the accuracy of FTDC delay line. Therefore, the behavioral of FTDC delay line during calibration might not replicate the actual delay during the operating conditions. This effect can be reduced by repeating the calibration and averaging the delay as will be discussed in next section.



(a)



(b)

Figure 5.16 Simplified flow chart of FTDC stage calibration for cases of (a) success and (b) failure.

- **Glitches on FTDC output due to high frequency jitter:**

  Ideally, FTDC output toggles when the lag edge crosses lead edge. However, due to high frequency jitter (> 10 MHz), lag and lead edges move in the order of 1ps with respect to each other. Therefore, there will be some glitches at the output of the FTDC which affects the calibration count and hence the Calibration accuracy. Calibration circuitry should be designed so that the calibration count is immune to these glitches.

- **Static Delay Offset between two paths in FTDC:**

  Static delay between lag and lead clocks might exist due to the clock generator connectors, mismatch in the routes, static mismatch in the multiplexing circuit. This might lead to calibration failure. The solution is to remove the effect of static delay offset in the calibration. Initially, static delay offset at the inputs to the FTDC stage is measured using dummy FTDC stage. During the calibration of the each FTDC stage, above offset is subtracted. Current implementation can cancel the delay offsets up to 1 ns.

- **Supply Modulation:**

  the FTDC resolution is very sensitive to supply voltage variation. Previous glitches on the supply voltage can impact the time resolution of FTDC stage in the current cycle. The effect of supply variation is reduced by using the separate regulator for FTDC as shown in Figure 5.19. This supply regulator is designed with a high bandwidth of 50 MHz to eliminate the effect of previous glitches on the supply voltage.

- **Temperature variation effect.**

  The delay of inverters is very sensitive to temperature variation which affects calibration accuracy. Therefore, to minimize the effect of temperature variation, The

FTDC is calibrated while the huge power consuming blocks like DCO, buffers, dividers are powered up.

5.6.3 Hardware requirements and calibration features

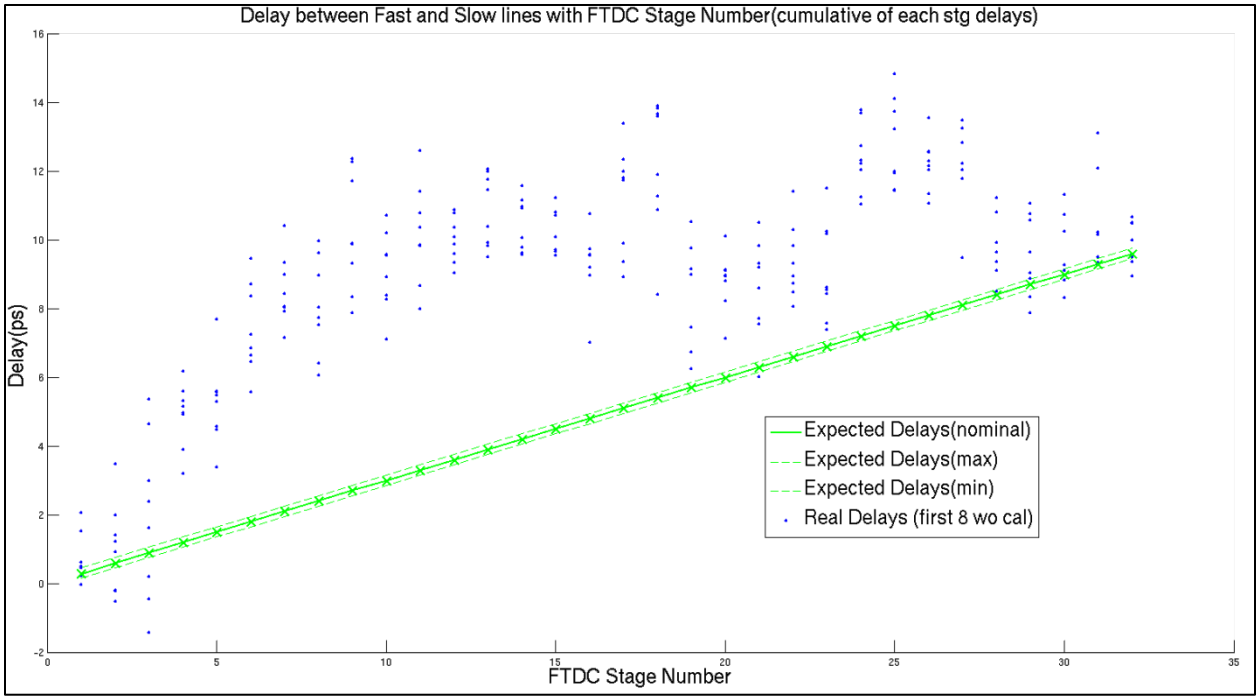
Different solutions for the above issues are addressed in calibration scheme and verified by behavioral simulation using Modelsim and AMS simulation. The calibration has the following features to guarantee proper calibration:

- **Averaging feature**: Calibration of each stage is averaged up to 8192 times to mitigate the effect of jitter and time offset of the test signals. Extensive behavioral simulations show that < 4 ps jitter in the test signals is sufficient to achieve INL< 300fs.
- **First recovery feature** from failure of single stage by relax the step of previous stage. When there is not any possible combination for current calibrated stage to meet the desired resolution, the calibration engine relaxes the spec of current and previous stages and repeat their calibration.
- **Second recovery feature** from failure of whole TDC to meet the specification of INL. In this case, the programmable spec of target error (K) is relaxed automatically and the calibration process is reset and repeated again.
- **Debug feature:** In addition, as a precaution solution, there is an option to overwrite the On-chip calibration and to do the calibration externally. If the calibration scheme fails, manual debugging is implemented by sending two external test signal with the same frequency but with controlled phase difference. In this mode, Clock generator outputs should have programmable constant phase difference between them with the resolution less than 500 fs.

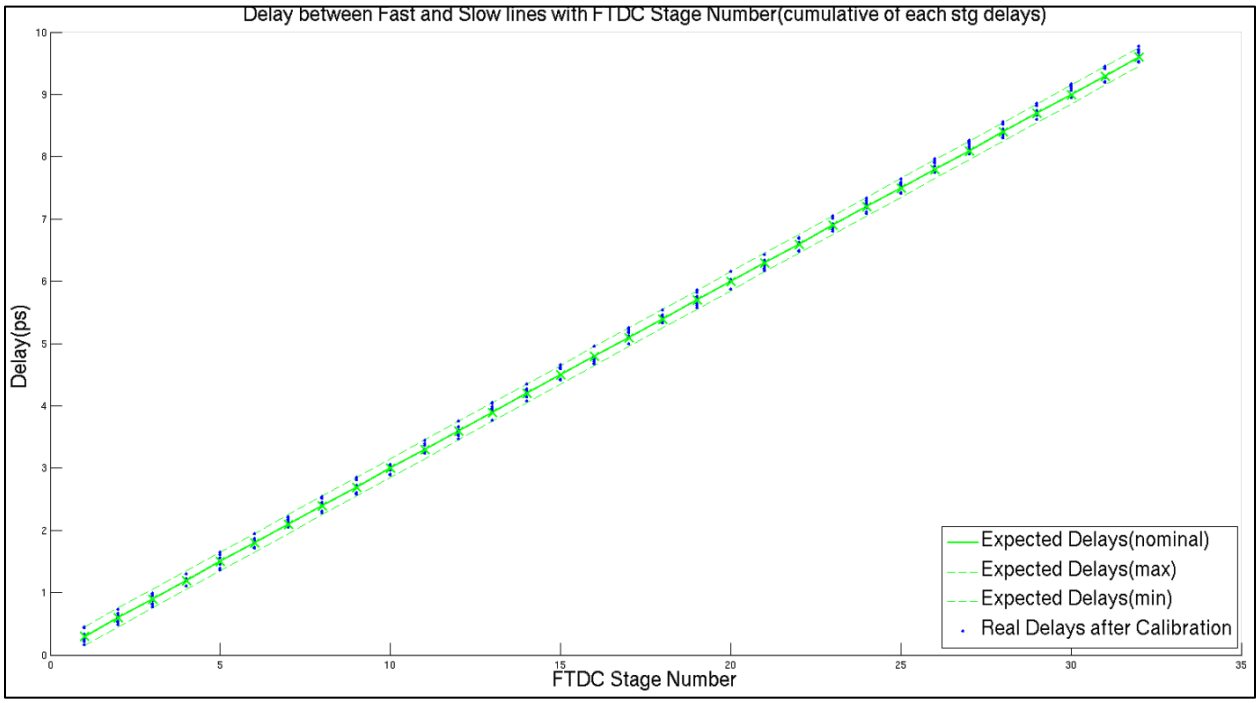
- **Calibration word generation:** There are two main methods to generate all the possible combination digital words: (1) External or internal memory with stored calibration words which increases number of pads and silicon area, respectively. (2) pseudo-random pattern generator based on LFSR. The second method is applied in proposed calibration scheme to minimize the silicon area. The pattern generator is verified using extensive MATLAB and Verilog simulations to guarantee that it generates all possible combinations.

Extensive MATLAB simulations have been used to find the appropriate number of AM_SES control word's combinations to achieve the desired resolution. From these simulations, it was observed that each stage requires 1680 combination to achieve overall INL less than 200 fs. However, as was discussed in previous section, the calibration of any stage is terminated once the best 8 digital controlled words are found and stored in first memory. This, in turn, implies that the calibration time varies and depends on internal calibration parameters, FTDC mismatch variation, and desired TDC resolution.

In order to accurately verify the calibration scheme, the calibration engine for FTDC is auto-synthesized and FTDC stages are modeled with their actual mismatch variations. Then, extensive Verilog/Verilog-A AMS simulations are used to check the calibration behavioral under different simulation conditions. From these simulations, it was observed that (with input frequency of 100 MHz, Δt of 100 fs, and target TDC resolution of 400 fs) the best and worst case of calibration time are 0.2 s and 85 s, respectively. Figure 5.17 shows a sample of Verilog/Verilog-A AMS simulation of cumulative delay of FTDC stages before and after the calibration.



(a)



(b)

Figure 5.17 Simulated cumulative delay of FTDC stages versus stage number: (a) Before the calibration. (b) After the calibration where solid green line is the ideal delay value, dotted green lines are the expected delay boundaries with error of LSB/2, and blue points are the real delay value.

5.6.4 CFI calibration algorithm

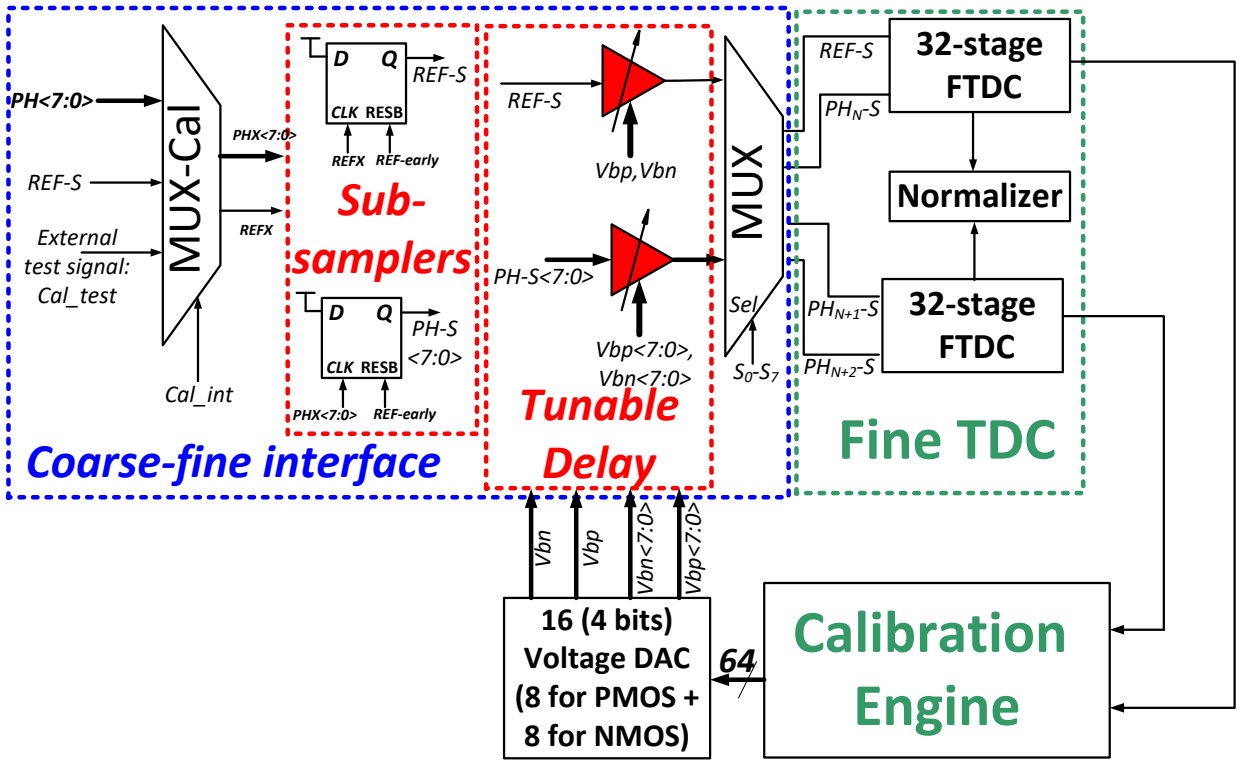


Figure 5.18 Simplified block diagram of on-chip CFI calibration engine

As shown in Figure 5.3 (b), Interface stage includes nine paths for eight phases (*PH_Int<7:0>*) and reference signal (*REF_Int*) and any mismatch in these paths affects the accuracy of FTDC and lead to nonlinearity regrowth. Since FTDC has been calibrated, it is possible to measure any time offsets in different paths of the interface stage very accurately.

To calibrate the mismatch between these paths, current starved tunable delay elements are inserted at the end of interface stage as shown in Figure 5.18 and a common external signal (*Cal_test*) is applied to all paths of interface stage through input multiplexer (*MUX Cal*). Ideally, the FTDC will measure the same delay difference between all delay paths and output of FTDC should be Zero.

Therefore, the output of FTDC is monitored by on-chip calibration engine which adapts the tunable delay elements sequentially, by changing the bias voltage of PMOS and NMOS transistors through voltage DACs, till the output of FTDC is zero for any two consecutive paths.

5.7 Characterization and discussion

Figure 5.19 shows the simplified block diagram of porotype mm-wave TDC chip. The input is provided externally via an on-chip balun. The divider outputs are converted to CMOS levels by a two-stage CML-to-CMOS converter which comprises a differential amplifier followed by CMOS inverters that are coupled using back-to-back inverters to maintain 50% duty cycle. The supply voltages for the divider core and TDC are provided by two on-chip LDO regulators, while the supply voltage for digital circuits is provided from an external DC source. The calibration engines for FTDCs and CFI are auto-synthesized. The TDC chip was fabricated in 65 nm CMOS (Figure 5.20). Two-step TDC occupies active area of $0.0505mm^2$ excluding pads.

Figure 5.21 shows a simplified diagram of the measurement setup of TDC chip. All the measurements were performed using on-wafer probing. Network analyzer (N5247A-X) is used to generate input signal up to 67 GHz. While arbitrary waveform generator (AWG7002A) is used to generator external test signals for FTDC calibration. Mixed signal scope (MSO) is used to measure and store digital outputs. The divider and the TDC consume 7.3 mA and 3.9 mA from a 1 V supply, respectively. The calibration of FTDC and CFI is performed with 100 MHz frequency.

Figure 5.22 shows the transfer function of two-step TDC before and after the calibration of FTDC and CFI. A 33.33 GHz input and an 83.334 MHz reference are applied to the TDC to achieve a time-domain ramp input with 100 fs time step.

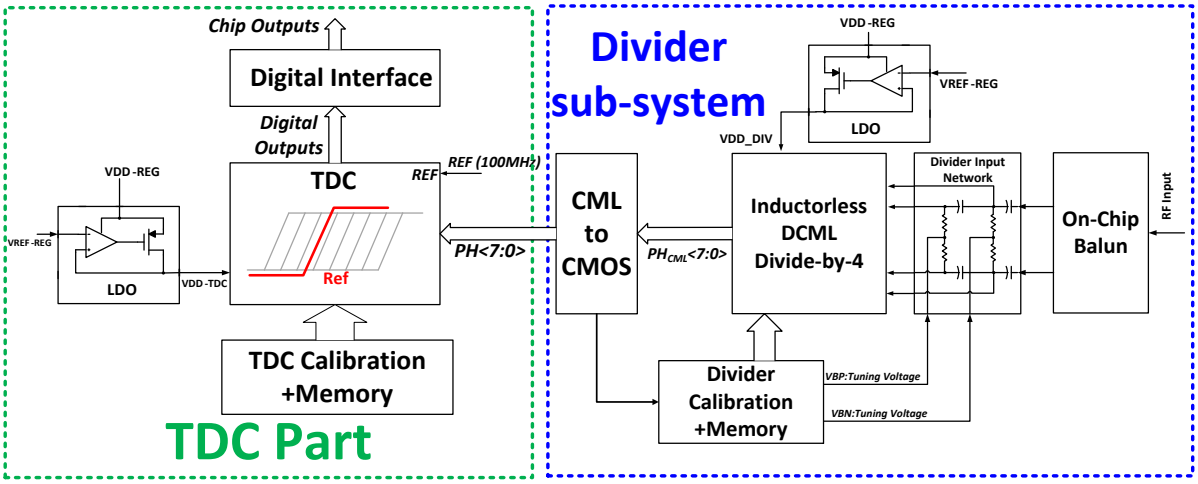


Figure 5.19 Simplified block diagram of TDC chip

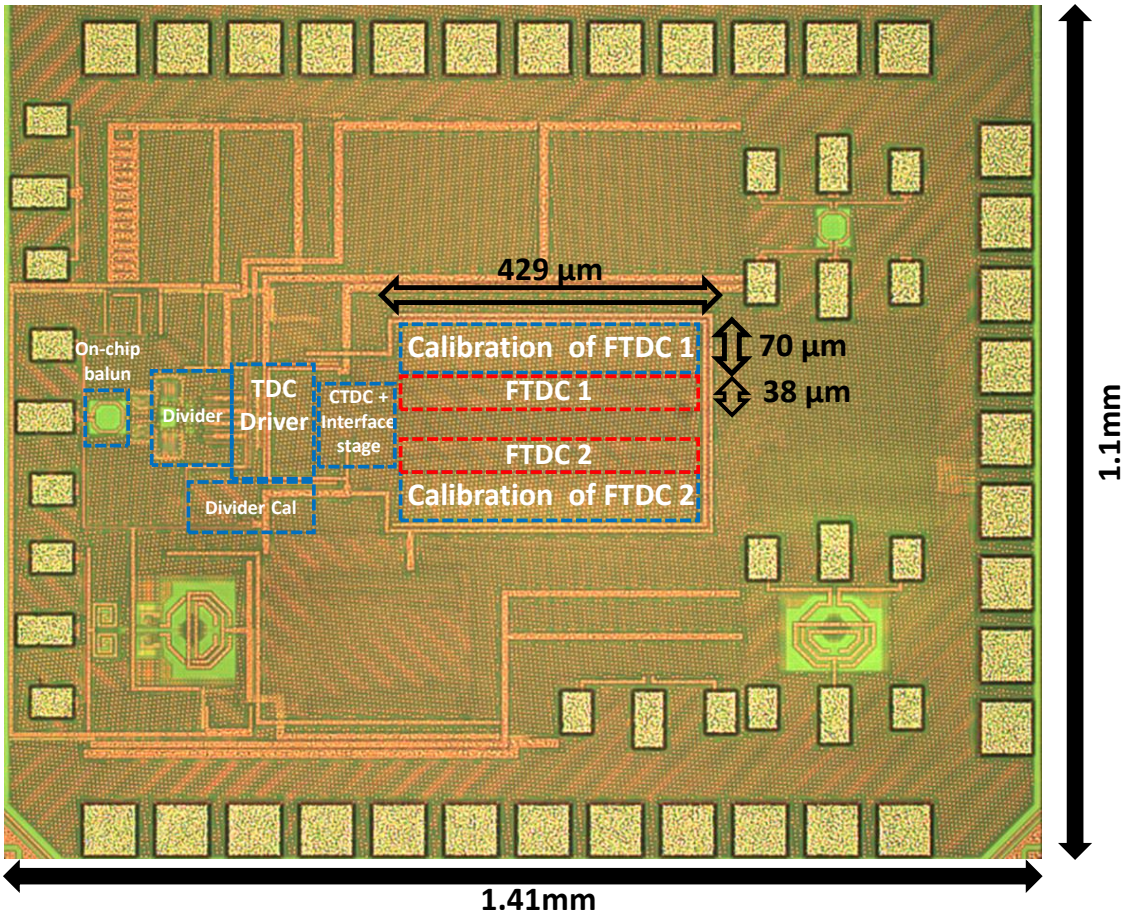


Figure 5.20 Die photo of prototype TDC chip

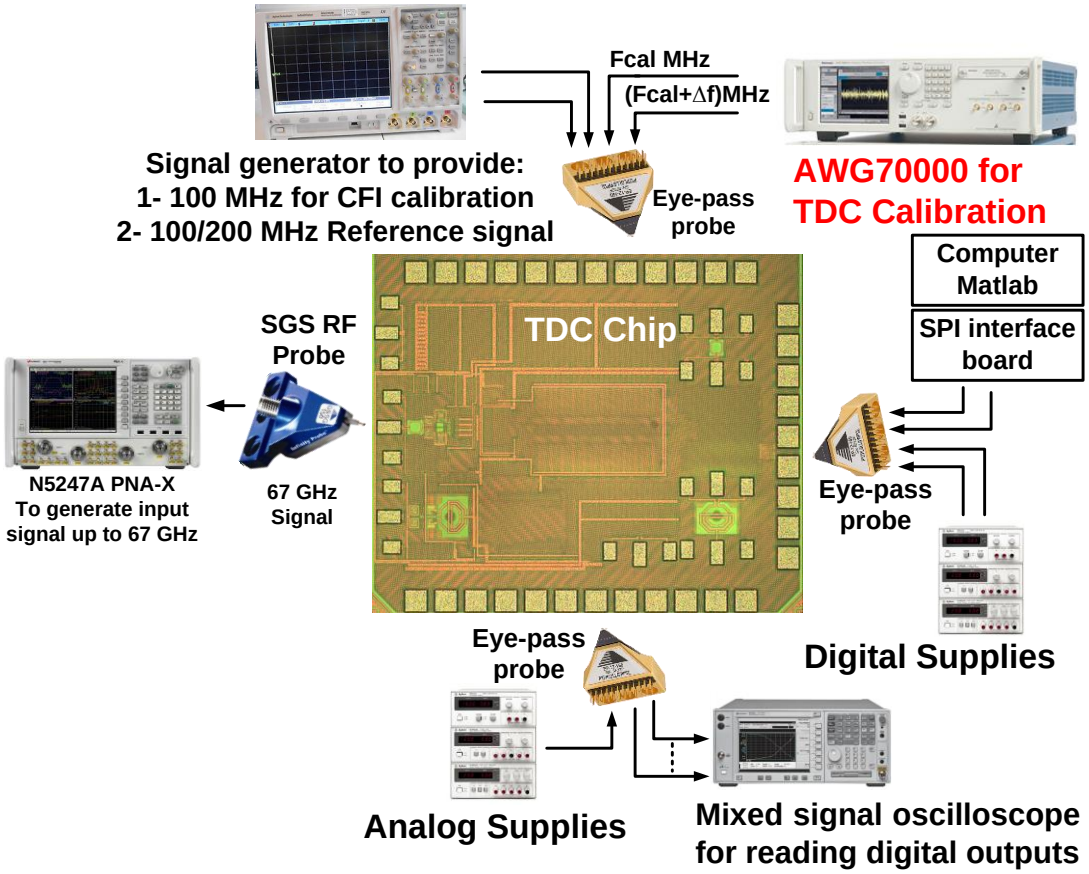


Figure 5.21 Measurement setup of TDC chip

Cumulative code count with 128K samples is used to overcome the effect of external signal jitter on the TDC output code and to average out the TDC noise. By changing the desired resolution of FTDC stage, the two-step TDC achieves programmable resolution of (450 fs - 1.2 ps) with up to 200 ps dynamic range. Please note that the dynamic range is limited by the minimum input frequency which is limited by the operating range of the divider.

Figure 5.23 shows the measured DNL and INL of the TDC before and after the calibration. It can be observed that the calibration reduces maximum value of the DNL from 6.2 LSB to less than 0.65 LSB and reduces the INL from 9 LSB to 1.25 LSB. It can be noticed also that the

highest DNL variations results at the transition between two consecutive phases of DCML outputs due to unresolvable phase mismatch between these phases.

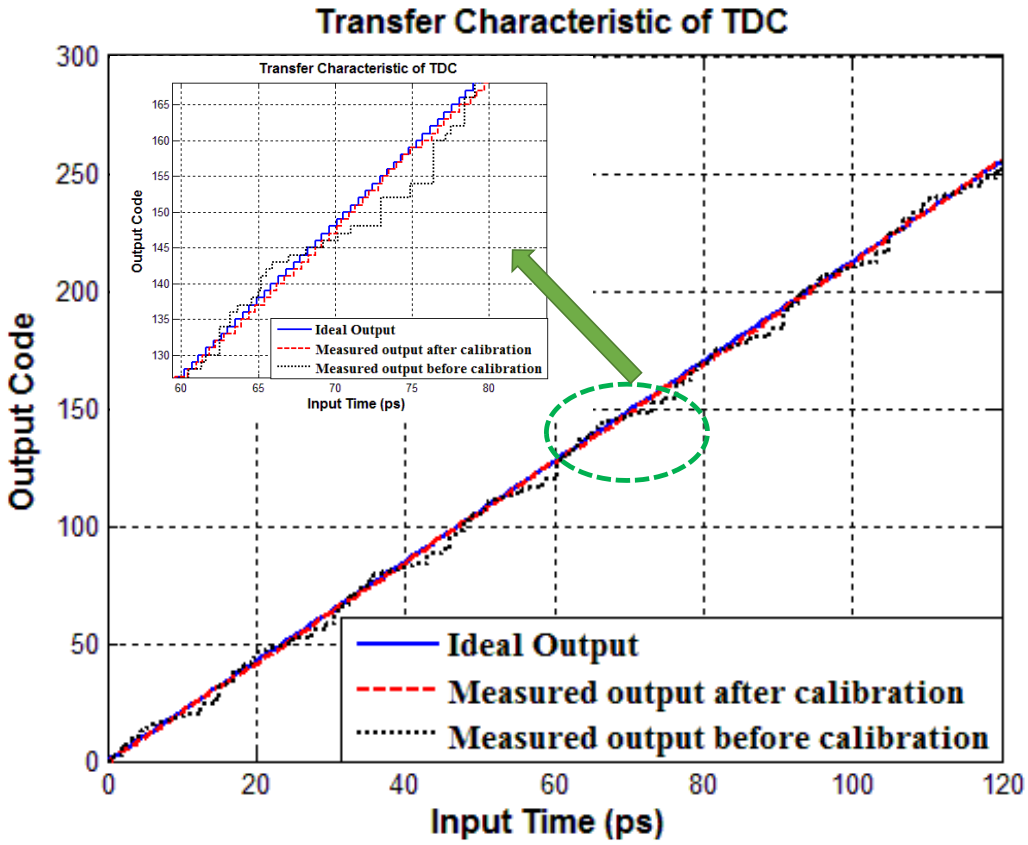
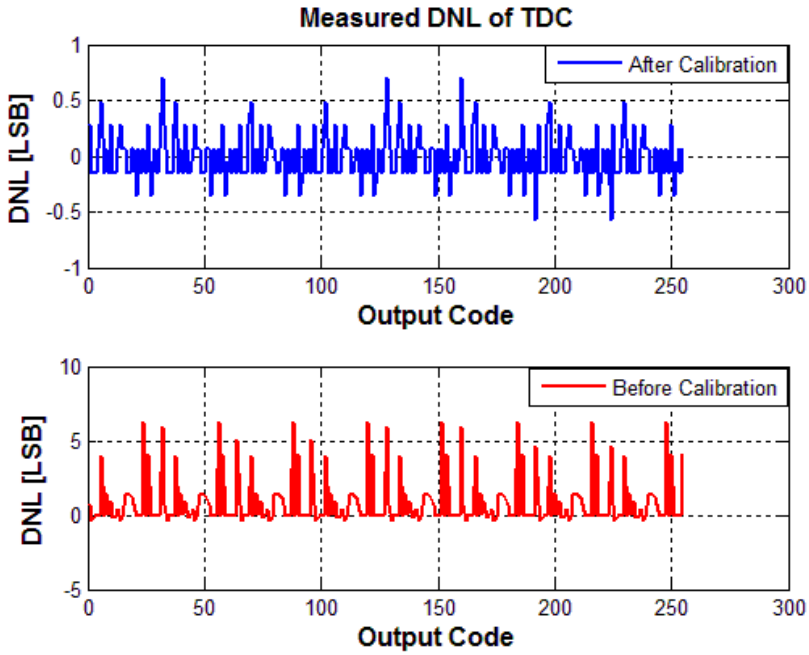
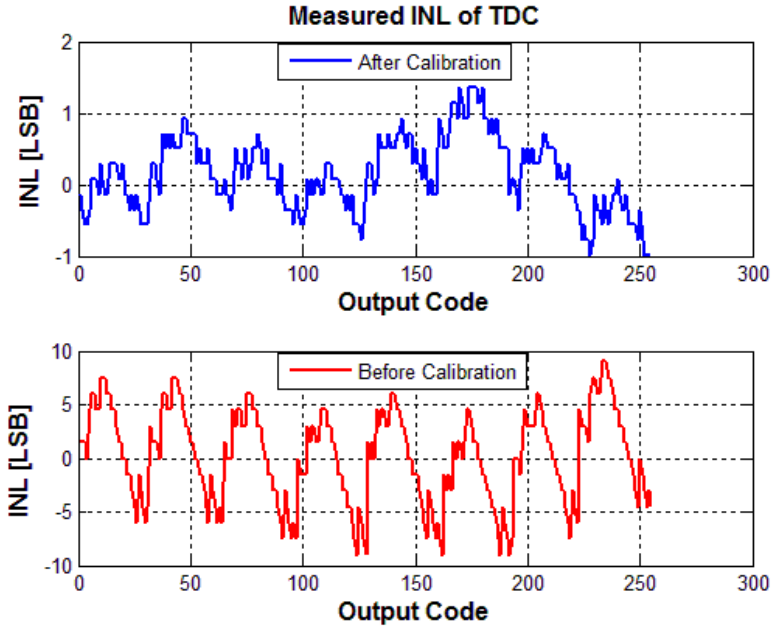


Figure 5.22 Output code of proposed TDC with input frequencies of (33.33GHz and 83.334MHz)

In order to see the noise contribution in the TDC, two consecutive phases (PH<2>, and PH<3>) are applied to second FTDC and 800K output samples are collected and analyzed using MSO. This setup eliminates the input jitter contribution in the noise measurement because the two inputs to the FTDC are from the same signal source. Figure 5.25 (a) and (b) shows the output code distribution for second FTDC without and with LDO, respectively. Obviously, the LDO reduce the supply noise effect on output code of FTDC. As the standard deviation reduces from 0.856 to 0.167 with LDO. It can be noticed that, the mean value of output code is changed with LDO due to a small variation in supply voltage of FTDC.

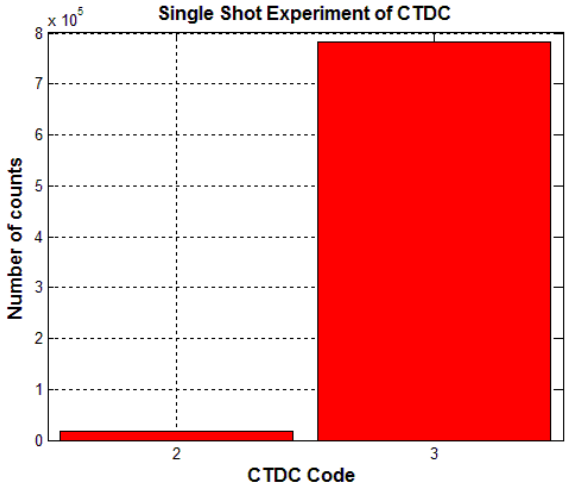


(a)

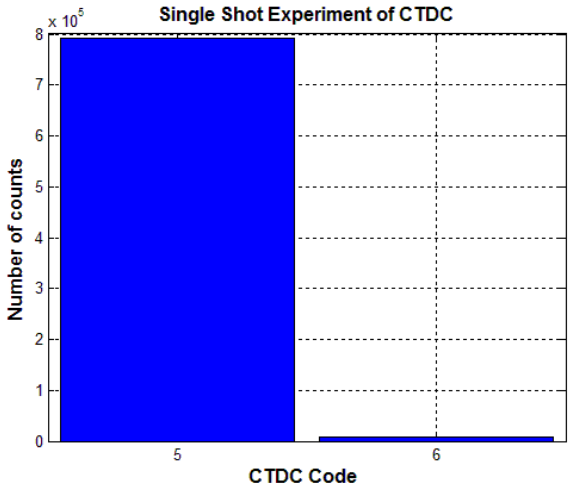


(b)

Figure 5.23 Measured (a) DNL and (b) INL of proposed TDC with input frequencies of (33.33GHz and 83.334MHz)

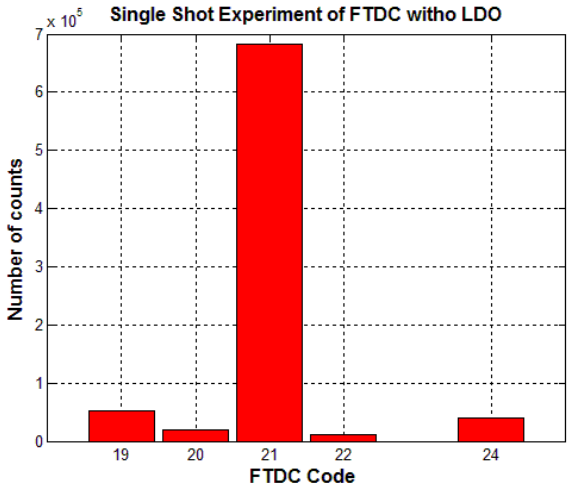


(a)

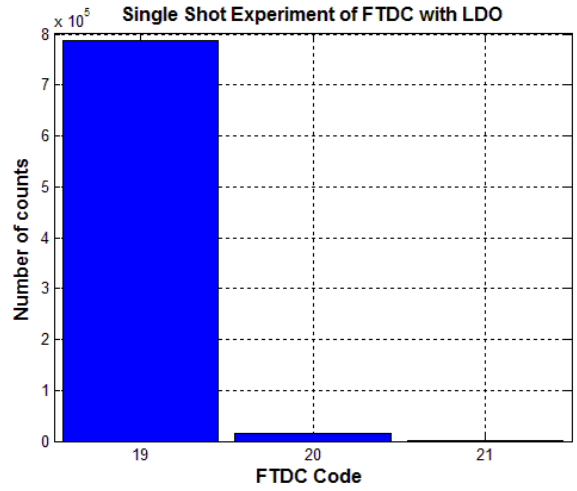


(b)

Figure 5.24 Single shot experiment of CTDC: (a) Code = 3 (b) Code = 5



(a)



(b)

Figure 5.25 Single shot experiment of FTDC: (a) without LDO. (b) with LDO

The TDC operation is verified at input frequency up to 64 GHz. Experimental results are benchmarked against recent TDCs and are summarized in Table 5-8. The SES calibrated TDC has the highest operation frequency and finest time resolution reported to date and achieves the best FOM among state-of-the-art CMOS TDC.

Table 5-8 Performance summary and comparison with state-of-art TDCs.

Spec\ Ref #		JSSC [132]	JSSC [129]	VLSIC [123]	JSSC [122]	JSSC [124]	JSSC [120]	RFIC [133]	This Work
Architecture		2D Vernier	Cyclic	Two Step	Async. Pipeline	True Pipeline	SRO	Flash $\Delta\sum$	Two Step
Resolution (ps)		4.8	1.25	3.75	1.76	1.12	0.32	1.6	0.45
Number of Bits		7	8	7	10	9	13	7	8
Conv. rate (MS/s)		50	50	200	300	250	50	50	200
Input frequency (GHz)		0.05	0.1	0.2	0.3	0.25	0.25	<0.25	17* 64**
Range (ps)		610	320	480	1800	573.4	2000	320	200ps
Linearity (LSB)	DNL	1	0.7	0.9	0.6	0.6	-	-	0.65
	INL	3.3	3	2.3	1.9	1.7	-	0.875	1.25
Single-Shot (LSB)		-	-	-	0.7	0.69	-	-	1.7
ENOB		4.9	6	5.28	8.46	7.57	-	6.1	6.89
FOM		1.139	1.34	0.463	1.086	0.325	-	0.386	0.167* 0.47**
Calibration		Yes	Yes	No	Yes	No	No	No	Yes
Supply (V)		1.2	1.2	1.2	-	1.2	1	1.1	1
Power (mw)		3	4.3	3.6	115	15.4	1.5	1.32	3.9* 11**
Area (mm2)		0.07	0.07	0.02	0.88	0.14	0.02	0.08	0.02
Tech. (nm)		65	130	65	130	65	90	40	65
$FOM = \frac{Power}{2^{ENOB} x F_S} (pJ / conv.step)$					$ENOB = Bits - \log_2(INL + 1)$				

*Without DCML divider

** With DCML divider

6 A 50-to-66 GHz All-Digital Fractional-N PLL in 65 nm CMOS

Digital PLL frequency synthesizers for wireless applications have become popular in the sub-10 GHz range. However, mm-wave synthesizers still rely on analog PLLs, predominantly of the integer-N type. This is due to limited DCO tuning resolution and challenges in phase digitization including limited resolution, linearity, and input frequency of the TDC. The 60GHz ADPLL in [79] uses a 32X ILFD/CML divider chain in the DCO-TDC interface which results in high power consumption (>0.5 of total power), large area, and high in-band phase noise.

This chapter discusses the design and implementation of 60 GHz all-digital phase-domain PLL that uses a 50-66 GHz capacitively degenerated DCO with 40 kHz frequency step and a two-step SES TDC with 450 fs resolution. The PLL incorporates extensive digital calibration of each of its sub-system to achieve 220 fs jitter, best (worst) phase noise of -83/-93/-126 (-79/-88/-116) dBc/Hz at 0.1/1/10MHz offset, -59 dBc spur and the highest reported FoM_T to date among mm-wave PLL's.

This chapter is organized as follows: In section 6.1, the frequency synthesizer's specifications which meet the requirements of *IEEE 802.15.3c, IEEE 802.11ad, and IEEE 802.11ac* will be discussed. Section 6.2 presents the mm-wave frequency synthesizer based on divider less fractional-N digital PLL. In section 6.3, the effect of phase mismatch on output spectrum of ADPLL will be highlighted then two proposed solutions will be discussed to alleviate this effect. Section 6.5 presents the design of digital loop where the main requirements of digital loop filter will be highlighted, then design methodology of loop filter's coefficients will be discussed.

In addition, the effect of non-linearity in DCO transfer function on ADPLL settling will be highlighted then effective and simple solution will be proposed. In section 6.6, the modeling and verification methodologies of ADPLL using Verilog-A and Verilog will be highlighted and verification results at different conditions will be presented. Finally, in section 5.7, the measurement results of 65 nm CMOS 60 ADPLL will be discussed.

6.1 Specification of 60 GHz ADPLL

Phase noise requirement is mainly dependent on modulation scheme defined in communication standard. For Wireless Personal Area Networks (WPANs) *IEEE 802.15.3c*, simulation results for single carrier (SC) modulation in [14] shows that for phase noise better than -84 dBc/Hz, -90 dBc/Hz, and -92 dBc/Hz at 1 MHz offset frequency there is not degradation in BER for QPSK, 8 PSK, and 16-QAM respectively. While, for wireless local area network (WLAN) *IEEE 802.11ad* and *IEEE 802.11ac*, it was proven in [34] that phase noise should be less -115 dBc/Hz at 10MHz offset to alleviate the BER degradation for 16-QAM in case of single carrier (SC) modulation or OFDM. These phase noise requirements restrict DCO phase noise and resolution (for out-of-band phase noise) and TDC resolution (for in-band phase noise) as has been discussed in Chapter 3 and Chapter 5, respectively.

Tuning range of 60 GHz mm-wave frequency synthesizer should be around 20 % to cover the whole 9 GHz available bandwidth (57 GHz - 66 GHz) and to provide additional margin for PVT variation and modeling uncertainties. The main limitation of covering the whole range is the tuning range of DCO and locking range of feedback divider. To best of our knowledge, there is not any reported 60 GHz frequency synthesizer or DCO achieves tuning range more than 15%.

IEEE 802.15.3c, *IEEE 802.11ad*, and *IEEE 802.11ac* specify a sub-carrier spacing of 1.2 MHz, 5.1 MHz and 312.5 KHz respectively, which determines the frequency resolution specification of frequency synthesizer and DCO.

Table 6-1 Basic specifications of 60GHz frequency synthesizer and corresponding specifications of system blocks

System Specification	Requirement	Limitation	Block Specification
In-band phase noise	-85 dBc/Hz	TDC resolution	1 ps
Out-band phase noise	- 115 dBc/Hz at 10 MHz	DCO resolution	100 KHz
		DCO phase noise	- 120 dBc/Hz
Tuning range	57-66 GHz	DCO tuning range	55 GHz - 68 GHz
		Divider locking range	55 GHz - 68 GHz
Frequency resolution	312.5 KHz	DCO resolution	100 KHz
Settling time	< 2 μs	Loop bandwidth	1 MHz
Steady state error	0	PLL type	Type-II
Reference frequency	-	Digital Blocks	100 MHz -200 MHz
Spurs level	-45 dBc	TDC resolution	400 fs
		TDC INL	1 LSB

From the above discussion and based on DCO analysis (Chapter 3) and TDC (Chapter 5), basic specifications of 60 GHz frequency synthesizer and corresponding specifications of system blocks can be summarized in Table 6-1. In the above calculations, it is assumed that the phase noise due to quantization noise of TDC and DCO are less the target system specification by 15 dB to eliminate their effect of PLL's output spectrum compared to their intrinsic phase noise contribution. As has been discussed in Chapter 3 and Chapter 5, increasing reference frequency reduces the effect of DCO and TDC quantization noise. However, to reduce loop latency of auto-synthesized digital loop and to maintain the desired phase margin of ADPLL, reference frequency of 100 MHz is chosen for overall system.

6.2 Proposed architecture of 60 GHz ADPLL

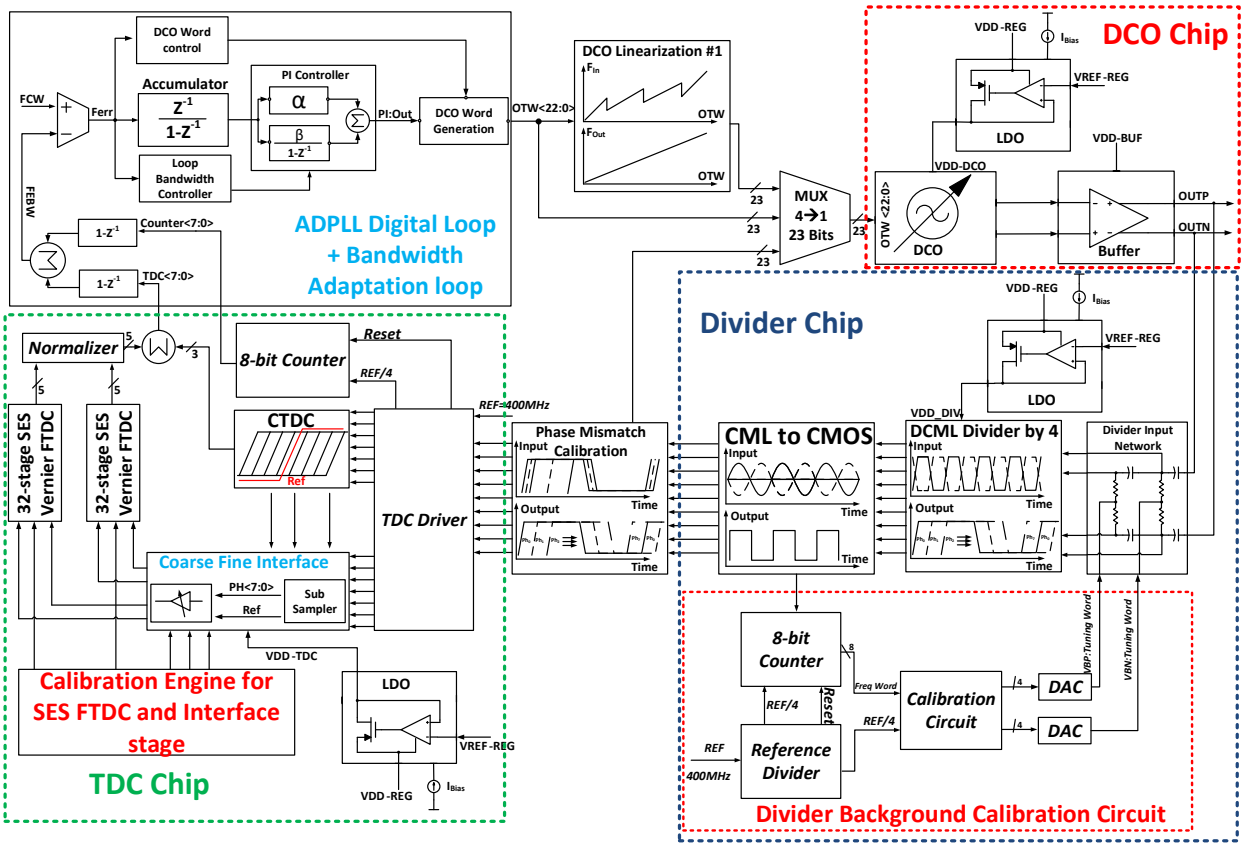


Figure 6.1 Detailed block diagram of proposed mm-wave digital frequency synthesizer

Figure 6.1 shows the detailed block diagram of proposed mm-wave frequency synthesizer based on divider less fractional-N digital PLL (Figure 2.3 (b)). A dither-less wide tuning range fundamental frequency DCO (Chapter 3) is followed by a shunt peaking buffer to drive the dynamic common-mode logic (DCML) divider (Chapter 4) which divides the DCO frequency by 4 in order to provide a reasonable operating frequency range for the following stages. The DCML divider generates 8 phases with uniform 45^{o} spacing.

A CML-to-CMOS converter is used to convert the voltage level of these phases to CMOS level. A background calibration technique (Chapter 4) is used to improve robustness of divider

operation across PVT and mismatch variation, and to facilitate practical applicability of the divider during the acquisition phase of a PLL, wherein the DCO's output frequency can vary widely. A phase mismatch calibration technique (Section 6.3.3) is proposed to mitigate the effect of phases mismatch at the output of CML-to-CMOS converter.

A synchronous counter and a coarse-fine TDC (Chapter 5) are introduced to estimate the integral and fractional ratio between output and reference frequencies. Adaptive mean statistical element selection technical (Section 55.5) is used to mitigate the adverse effects of element mismatch and PVT variation on TDC linearity. The 8-bit output of the synchronous counter and the 8-bit output of the TDC, which together represent a digital estimate of the phase error, are converted using a digital differentiator to a frequency feedback word FEBW; this is then subtracted from frequency control word (FCW) to generate a digital estimate of the frequency error. The ADPLL digital loop filter, which determines the loop response generates a 23-bit oscillator tuning word (OTW) to control the DCO's output frequency, and to realize additional functions as will be discussed in next section.

The OTW is processed using a digital engine which implements DCO linearization technique to alleviate the non-monotonicity in DCO transfer function. Separate supply regular (LDOs) are used for sensitive blocks inside the ADPLL, such as the DCO, the DCML divider, and the fine TDC, in order to isolate them from supply modulation effects. All digital blocks and calibration blocks are clocked with a re-timed version of reference frequency which is synchronized with output of DCML phases. The reference frequency is chosen to be 100 ~ 200 MHz to allow automatic synthesis and layout of the digital blocks, while achieving low loop latency. The prototype ADPLL (Figure 6.1) is designed for operation in the 60 GHz band using 65 nm CMOS technology.

6.2.1 50-to 66 GHz DCO

The same DCO architecture, proposed in Chapter 3, is implemented inside the 60 ADPLL (Figure 6.1). However, based on measurement of several standalone passive inductors and transformers, the DCO's transformer is redesign with two main purposes:

1. Compensate the frequency shift in the previous DCO to meet the operating ranges of IEEE *802.15.3c, IEEE 802.11ad, and IEEE 802.11ac.*
2. Increase the tuning range by decreasing the overlapping between the four frequency bands generated from transformer bits.

6.2.2 Divider

Figure 6.2 shows the schematic of proposed DCML divide-by-4 which incorporates several design techniques, that were proposed in Chapter 4 to widen locking range for small input amplitude, such as:

1. Source coupling (Section 4.3.1) to increase maximum operating frequency.
2. Current bleeding (Section 4.3.1) to decrease minimum operating frequency.
3. Bulk modulation (Section 4.3.3) to improve fractional bandwidth.
4. Bulk adaption (Section 4.3.3) to adapt self-oscillation frequency

Figure 6.3 (a) shows the block diagram of CML-to-CMOS converter which consists from one DCML stage amplifier (Figure 6.3 (b)), to increase the swing of divider outputs, and CMOS buffer stage (Figure 6.3 (c)) to convert the signals to rail-to-rail. The back-to-back inverters are used in CMOS buffer stage to maintain the duty cycle of input signals over PVT variations.

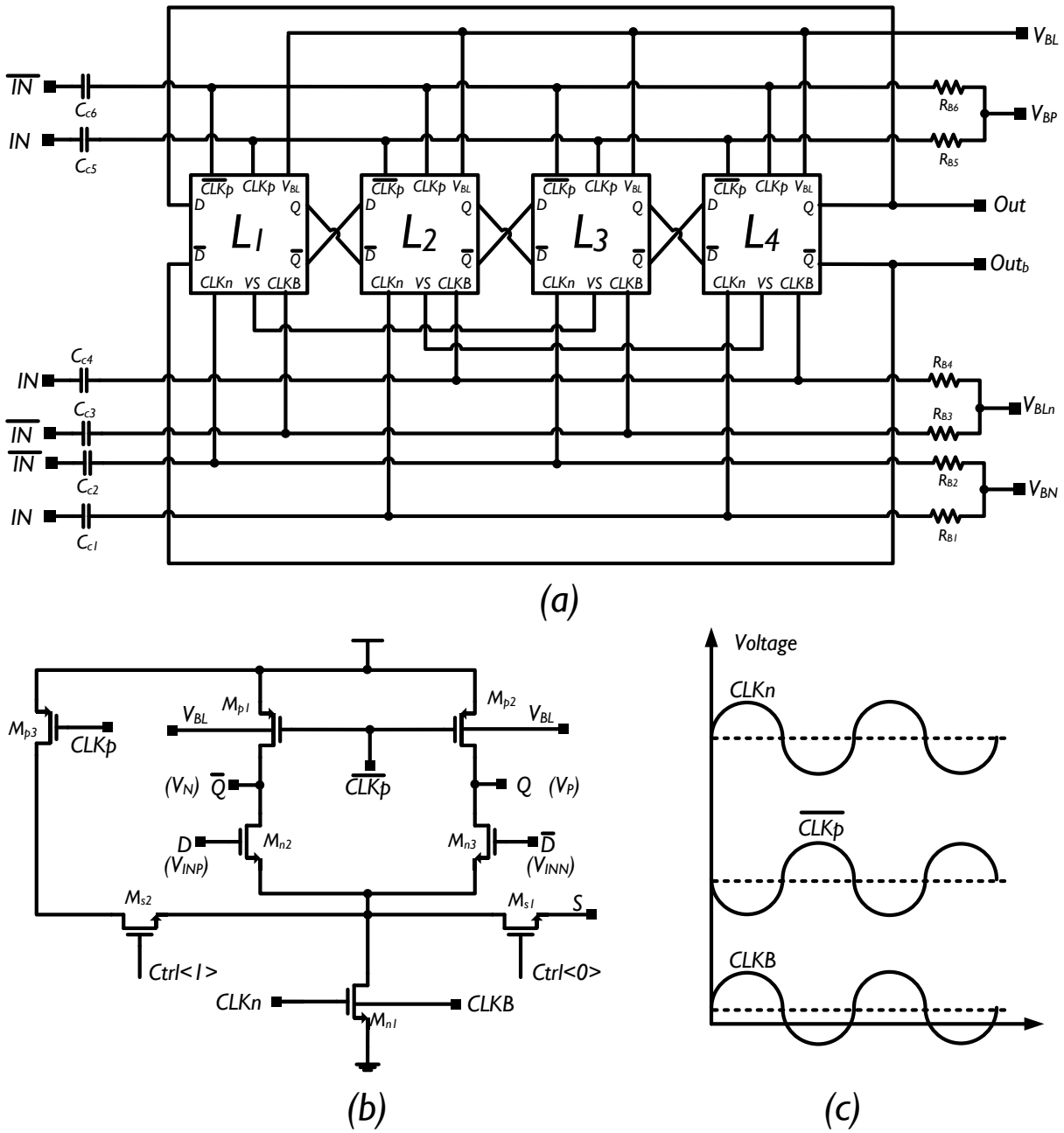


Figure 6.2 DCML divider using source coupling (SC), current bleeding (CB), NMOS bulk modulation (BM), and bulk adaption. The configurations DIV1-BM, DIV1-SC+BM, DIV1-CB+BM and DIV1-SC+CB+BM can be realized by turning on the switches Ms1 or Ms2.

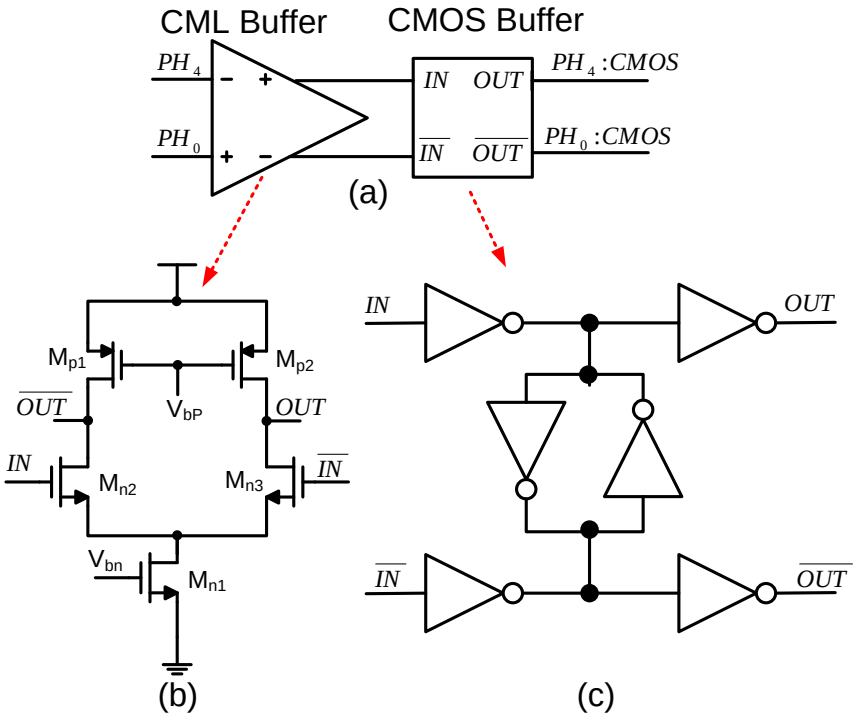


Figure 6.3 (a) block diagram of CML-to-CMOS (b) CML buffer (c) CMOS buffers with back-to-back inverters

6.3 Calibration techniques of Phase mismatch of divider outputs

6.3.1 Motivation to phase mismatch calibration

As depicted in Figure 6.1, the TDC exploits the availability of multiple phases from the divider in many places:

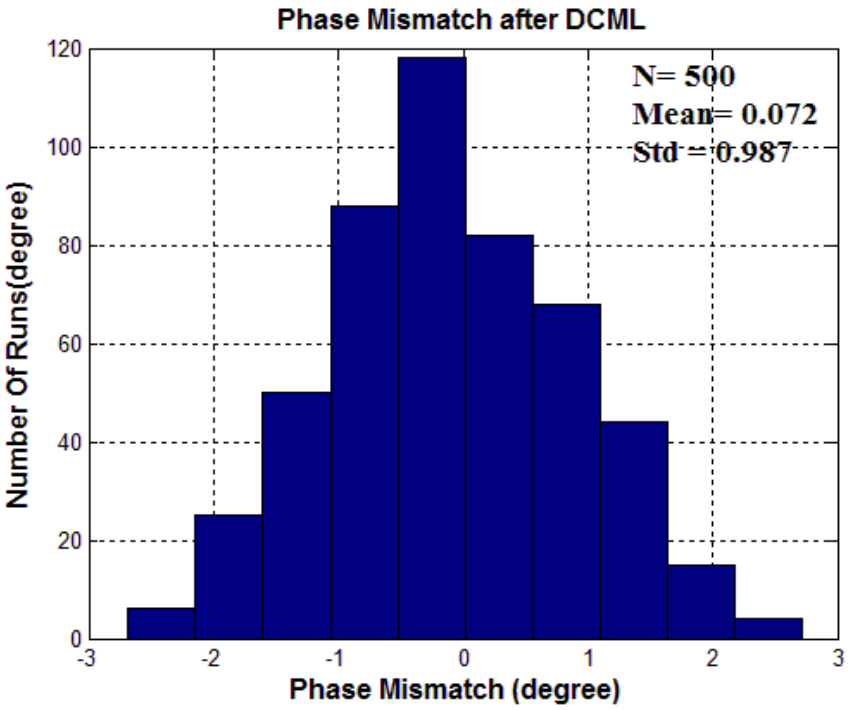
1) In the CTDC to extract the three MSB's of the phase word and to avoid the need for explicit period normalization.
2) In the first FTDC to find the edge that lags the reference signal.
3) In the second FTDC for period normalization purpose.

Ideally, the phase differences between the eight phases from a DCML divider are precisely equal. However, in practice, the edges of these phases are not uniformly spaced. Phase mismatches arise due to several sources including threshold mismatch, device size mismatch, layout parasitic, and coupling mismatches. The phase mismatch between any two consecutive phases can be expressed as:

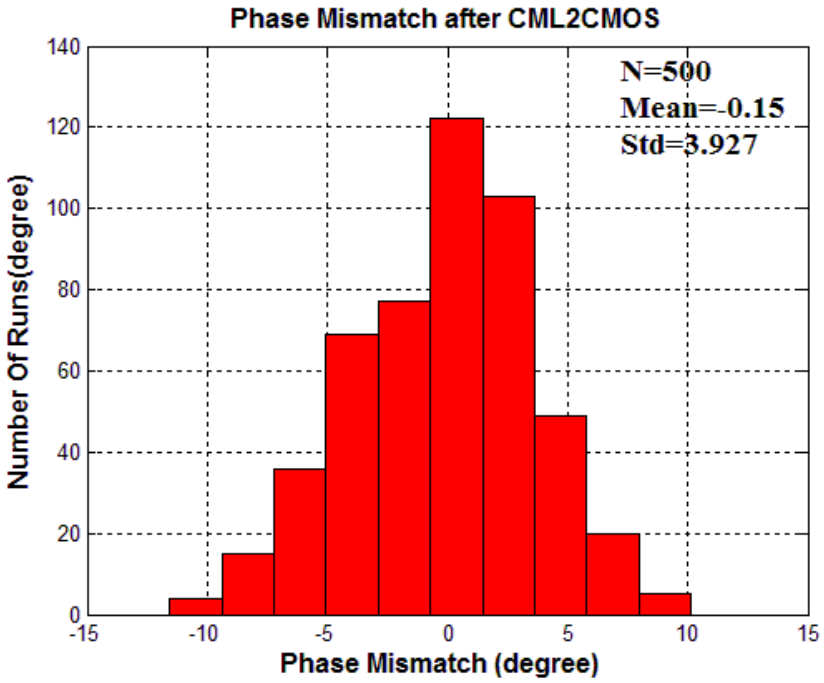
$$PH-MIS(\deg)=\frac{\Delta PH\left(N,N+1\right)}{T_{Div}}\times 360^{o}-45^{o} \qquad 6\text{-}1)$$

Where T_{Div} is the period of divider output, and $\Delta PH\left(N,N+1\right)$ is the delay difference between any two consecutive phases. Figure 6.4 (a) and (b) show the worst-case phase mismatch variation, results from Monte-Carlo simulation for DCO frequency of 60 GHz, between output phases after DCML divider and after CML-to-CMOS stage. As expected, mismatch grows along the chain and the standard deviation at the input of TDC is more than 3.9º. This mismatch at TDC input can be treated likes non-linearity in TDC which introduces periodic phase error, when ADPLL is locked, and generates in-band spurs at frequency offset of multiple of fractional frequency.

Behavioral simulations show that 3º mismatch in the TDC input phases PH<7:0> increases spur levels by 11.8 dB at 60 GHz. Moreover, it can be noticed that the standard deviation of phase mismatch at input of TDC is 2.5 times desired LSB (300 fs). To maintain the desired TDC resolution to achieve the phase noise and spur level specifications, the input phases should be uniformly spaced with mismatch less than LSB/2, which is translated to phase mismatch less than one degree at the maximum DCO output frequency (66 GHz).



(a)



(b)

Figure 6.4 Worst case of phase mismatch variation after (a) DCML divider and (b) CML-to-CMOS converter

6.3.2 Proposed calibration technique based on analog delay elements

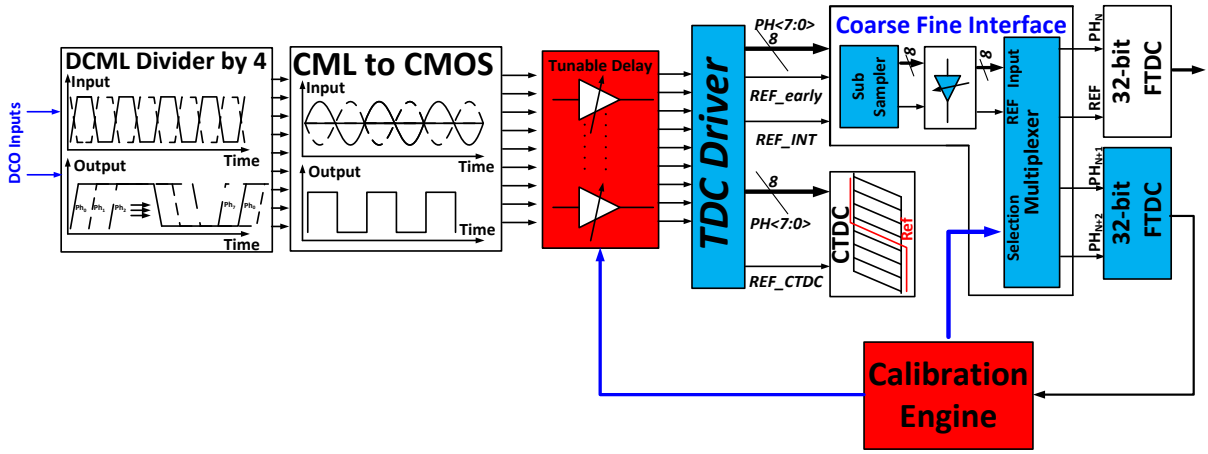


Figure 6.5 Simplified phase mismatch calibration engine that uses tunable delay elements and the calibrated TDC

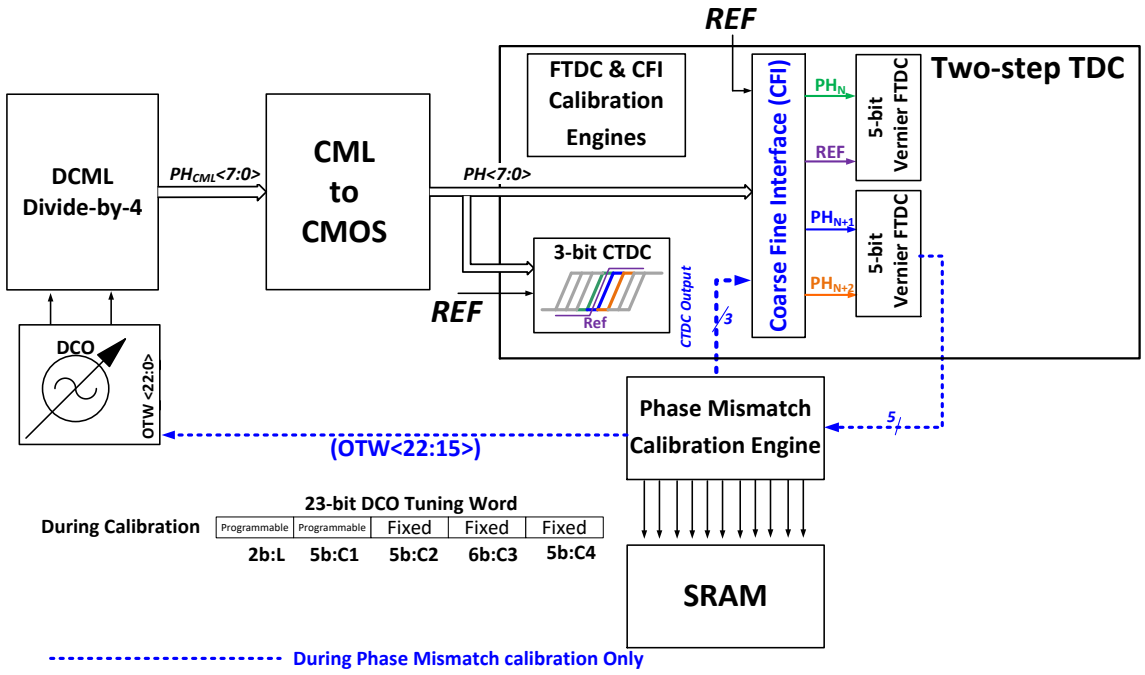
Calibration techniques were demonstrated in [154], [155] to mitigate phase mismatch between fractional frequency divider outputs at low GHz frequencies (i.e., < 4 GHz). These techniques measure the delay between each two consecutive phases and apply a calibration algorithm to update the tunable delay elements until phase mismatch is sufficiently reduced. However, the implementation of these techniques is not feasible at mm-wave frequency. In particular, the phase cloning technique [154] was investigated for the proposed ADPLL, however it requires a 9-bit TDC with resolution of 150 fs and a large number of tunable delay elements. The estimated power consumption of this this technique is 40 mA for output frequency of 60 GHz.

Two techniques are proposed to mitigate phase mismatch effect. Both methods assume that the FTDC and the interface stage are calibrated properly. Figure 6.5 shows the block diagram of the first technique where tunable delay elements are inserted after the CML-to-CMOS converter to align the phases to correct positions. Each two consecutive phases are sub-sampled in interface stage, then the delay difference between their rising edges are measured using pre-calibrated FTDC stage. The calibration algorithm proposed in [155] is used to adapt the tunable

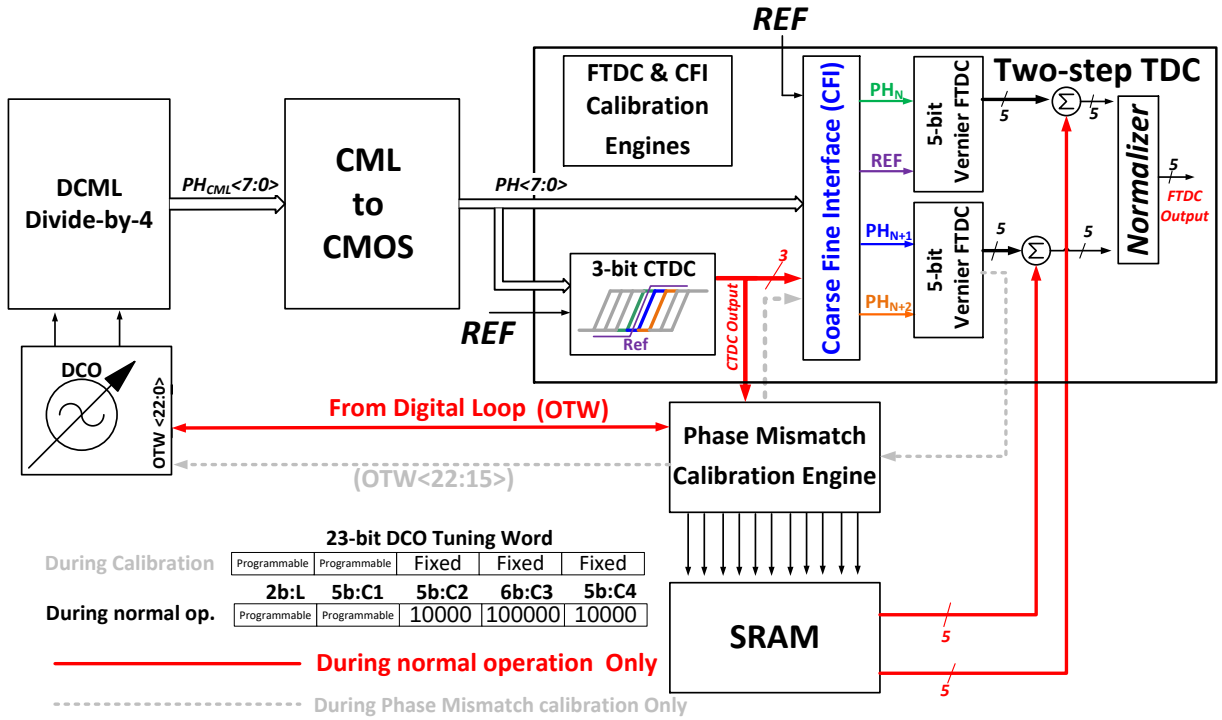
delay elements. This technique largely reuses existing blocks within the TDC (blue blocks in Figure 6.5) which reduces the area consumption. However, tunable delay elements are power hungry and their monotonicity is hard to guarantee at mm-wave frequencies. Moreover, post-layout simulations indicate that the phase mismatch is frequency dependent, therefore mismatch cannot be calibrated at all output frequencies using the first method.

6.3.3 Proposed digital calibration technique

The second proposed technique is simple but effective and power efficient as it eliminates the need for tunable delay elements. In this technique, the delay difference between each two consecutive phases is measured at different DCO frequencies. Figure 6.6 (a) shows the simplified block diagram of digital phase mismatch calibration technique during calibration mode where the DCO frequency is set via the MSB's OTW-L<22:16> and delay differences between each pair of consecutive phases in PH_{CMOS}<7:0> are measured using the CFI and FTDC's (bypassing the CTDC). Mismatches between pairs of phases are calculated from the FTDC outputs and stored in on-chip SRAM which is implemented using memory complier. Please note that the dynamic range of FTDC will be the same as it should measure the delay difference between just two consecutive phases during calibration mode. During normal operation, as shown in Figure 6.6 (b), OTW-L and output of CTDC stage are fed to the calibration engine to determine the corresponding address of SRAM memory. Then, the output of FTDCs are corrected by subtracting the stored phase mismatch from the FTDC outputs before normalization Obviously, the second technique is simpler than the first since it has smaller area and power consumption, and achieves the mismatch calibration at different frequencies. Second method is implemented and integrated in ADPLL loop as shown in Figure 6.1. Behavioral AMS simulation is used to check the effectiveness of proposed scheme inside the ADPLL loop.



(a)



(b)

Figure 6.6 Simplified digital phase mismatch calibration engine that uses the calibrated TDC: (a) During phase mismatch calibration only. (b) During normal operation only.

6.4 Temperature effect on phase extraction path

It should be noticed that the proposed calibration schemes of phase extraction path (i.e., TDC and phase mismatch) are foreground techniques. These techniques mitigate the performance degradation due to process variation, random transistors mismatch, and supply variation. However, they cannot resolve temperature variation effects. Therefore, to minimize the effect of temperature variation, the TDC and phase mismatch between outputs of CML-to-CMOS converter are calibrated while the huge power consuming blocks like DCO, buffers, dividers are powered up. In addition, the calibration of phase extraction path (i.e., TDC and phase mismatch) can be repeated periodically, till the chip temperature is stabilized.

In order to estimate the degradation due to temperature variation, the operations of FTDC and divider sub-system are checked while temperature was swept from 0^{o} to 100^{o}. Although, the absolute delay of inverters is sensitive to temperature variation, the FTDC is implemented based on Vernier architecture where the target resolution is achieved by subtracting the absolute delay of two lines which alleviates the effect of temperature variation. Moreover, to minimize the sensitivity of FTDC resolution to temperature variation, two identical delay lines with same output impedance are used and current starved tunable delay cells with is used to generate the target delay difference. Furthermore, by decreasing the current difference between the two delay lines (the case in the implemented FTDC to improve the resolution), the sensitivity to temperature variation become smaller.

Figure 6.7 (a) shows the average FTDC resolution versus temperature, where the resolution varies from 418 fs to 451 fs over 100^{o}. Based on (5-7), this variation results in only +/- 0.3 dB in-band phase noise variation. Similarly, pre-layout simulation of the divider sub-system shows a

negligible variation in phase difference between any two consecutive phases of CML-to-CMOS converter due to temperature variation.

Figure **6.8** shows the FTDC transfer function at two different temperature corners when the FTDC resolution is 400 fs. Two input signals with a small frequency difference are applied to achieve an input time ramp of 50 fs temperature. Figure 6.9 shows the simulated DNL and INL versus output code of FTDC at two difference temperatures. The maximum INL of FTDC is 0.4 LSB and 0.5 LSB at 100^{o} and Zero degree, respectively. Clearly, the temperature variation has a small effect on TDC linearity which results in a negligible degradation in spur power.

In conclusion, the basic verification of phase extraction path shows a small degradation due to temperature variation. The ADPLL measurements can be repeated with temperature variation to investigate the actual degradation in more powerful methodology.

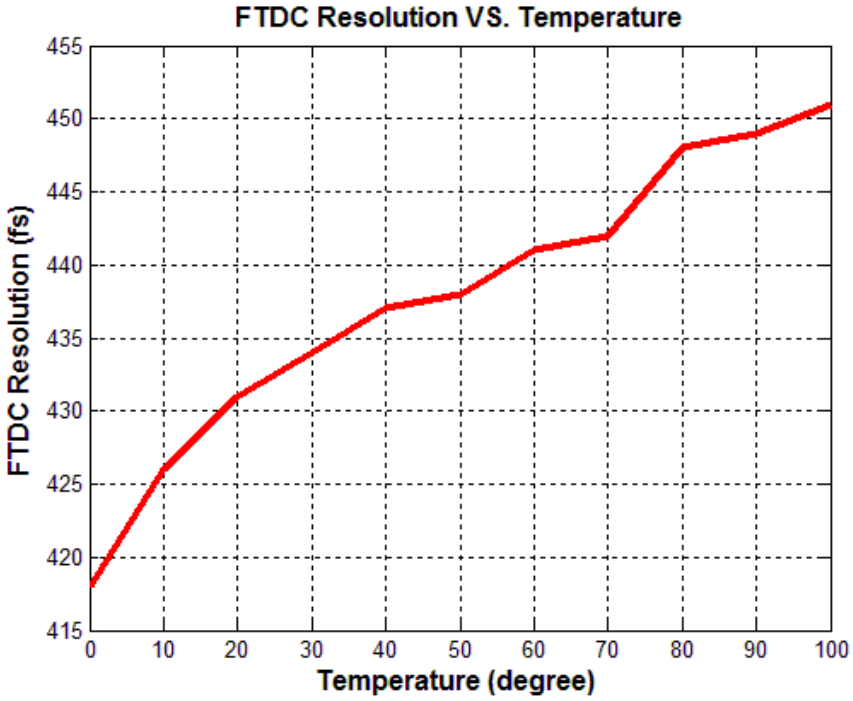
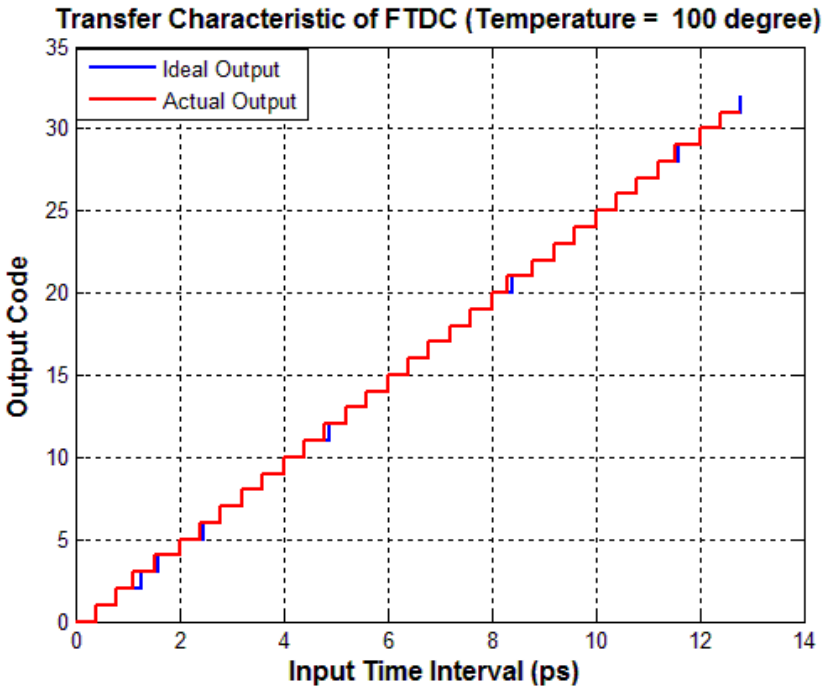
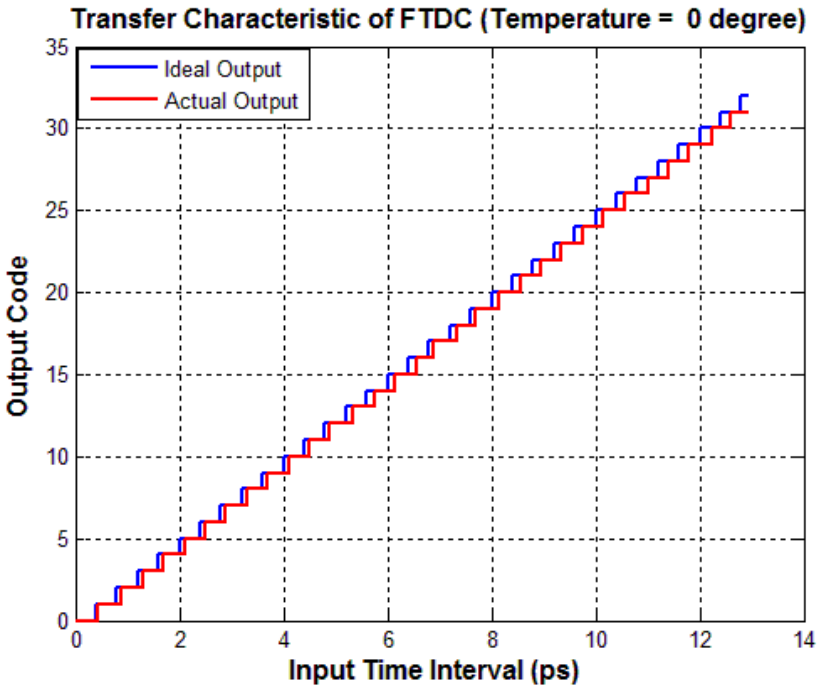


Figure 6.7 Temperature Variation effect of (a) FTDC resolution.

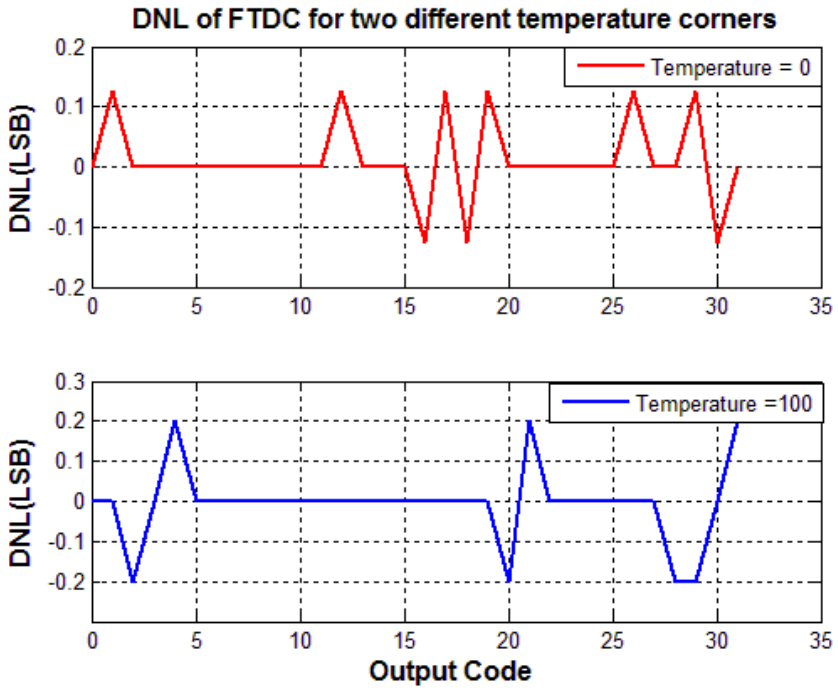


(a)

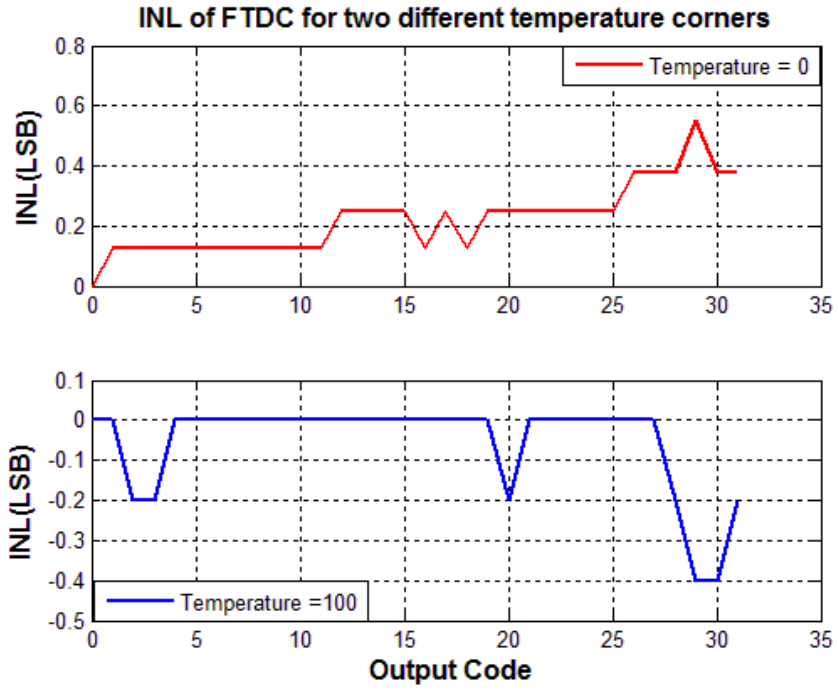


(b)

Figure 6.8 FTDC performance at two different temperature corners (a) Temperature = 100^{o} (b) Temperature = 0^{o}



(a)



(b)

Figure 6.9 FTDC linearity performance at two different temperature corners (a) DNL (b) INL

6.5 Digital loop design of ADPLL

In frequency synthesizer based on PLL, the loop bandwidth is a crucial parameter which directly affects phase noise, spurs level, and the settling time of the frequency synthesizers. The output noise transfer function from the reference, TDC, feedback divider has low-pass response, therefore these noise sources only contribute to the in-band phase noise. In contrast, the noise transfer function from DCO to the output has a high-pass response and which contributes to out-of-band Phase noise. Therefore, the design of optimum loop bandwidth is challenging to minimize overall phase noise. In addition, there are many other considerations related to digital loop design as will be discussed in the following sub-sections.

6.5.1 Main requirements of digital loop

The main considerations in the design of the digital loop filter are:

1) Achieving ultra-fast locking (i.e., < 5μs) during the acquisition mode, which necessitates wide bandwidth.
2) Eliminating the steady state phase error for frequency input step which requires second-order loop filter which in turn leads to slow response.
3) Optimization of loop response to minimize the total phase noise.
4) Re-configurability to meet the specifications of narrow and wide band applications.
5) Guarantee loop stability and mitigation of non-linearity in the DCO transfer function.

However, these considerations pose several trade-offs. For example, phase noise reduction of TDC and reference requires narrow loop bandwidth which increases settling time. Increasing reference frequency and loop bandwidth helps suppress DCO phase noise but degrades the

stability, in-band phase noise, spurs level and requires high-speed digital blocks which may require custom digital design.

6.5.2 Proposed digital loop

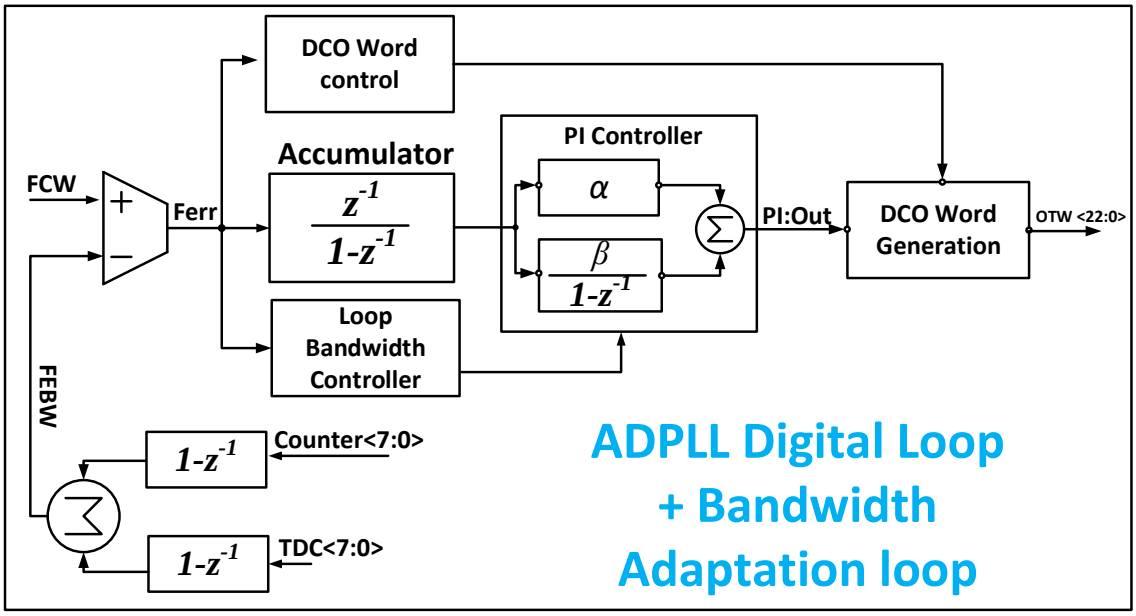
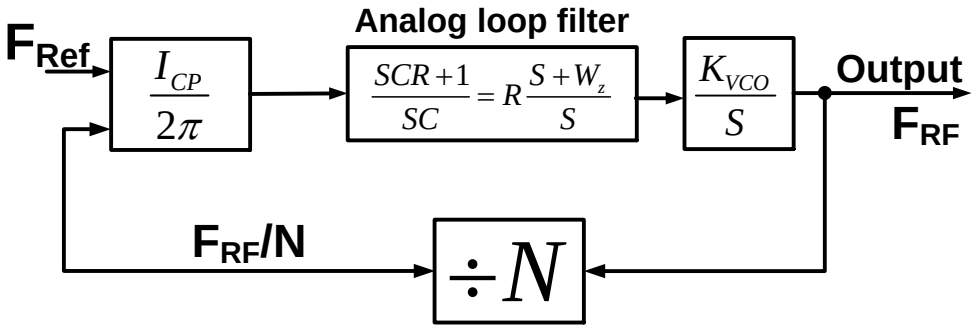


Figure 6.10 Proposed digital loop of 60 GHz ADPLL

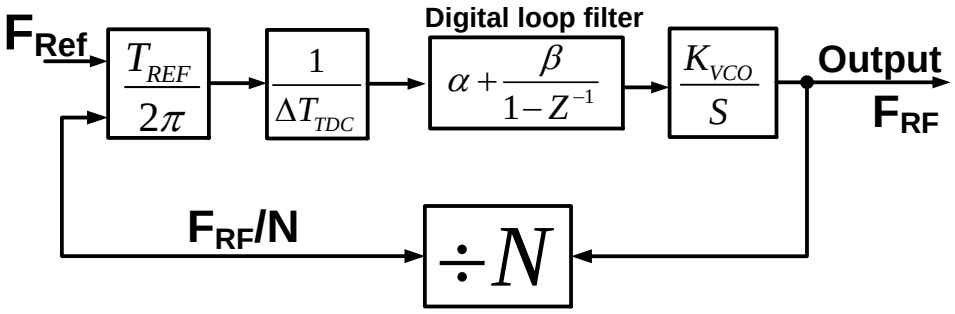
Figure 6.10 shows the block diagram of proposed digital loop, where the integral-plus-fractional frequency feedback word (*FEBW*) is subtracted from the desired frequency control word (*FCW*) and frequency error signal is used in three different paths.

1) First path is the main path of digital loop where the frequency error is accumulated then attenuated by PI controller before generating the OTW.
2) Second path is loop bandwidth controller/adaption. The main goal of this path is to adapt loop filter coefficients to achieve ultra-fast locking with zero steady state error.
3) Third path is responsible on generation of DCO's tuning word to overcome non-monotonic behavioral of DCO.

6.5.3 Design methodology of main path



(a)



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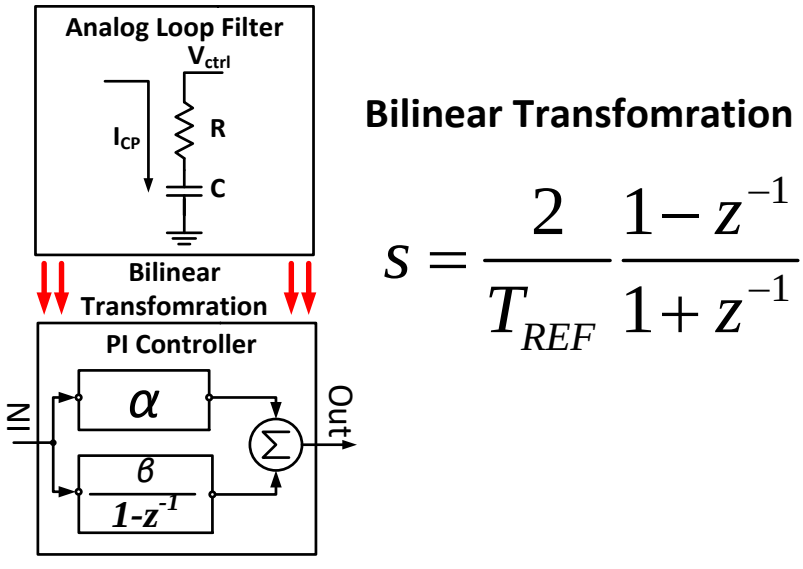


(c)

Figure 6.11 S-domain approximation of charge pump PLL (b) Block domain of digital PLL. (c) Bilinear transformation from analog to digital loop filter

In particular, the operation of both analog and digital PLL happen in discrete time steps rather than continuous time, and during the acquisition mode their operation is nonlinear. On the other hand, during tracking mode when the phase error is small, the analog PLL can be linearized and accurately modeled as a linear time-invariant (LTI) system. Figure 6.11 (a) shows the block diagram of charge pump analog PLL with continuous-time s-domain transfer functions. This model is valid as long as the loop bandwidth is much narrower than the reference frequency. The open loop gain of charge pump PLL can be expressed as:

$$\frac{I_{CP}}{2\pi}\frac{K_{VCO}}{s}\times\frac{s+w_z}{s}R \qquad (6\text{-}2)$$

Where ICP is the charge pump current, and KVCO is VCO sensitivity to its control voltage. From this transfer faction, the phase margin of PLL can be expressed as:

$$PM=\tan^{-1}\left(\frac{w_{GBW}}{w_z}\right) \qquad (6\text{-}3)$$

Where W_{GBW} is gain-bandwidth product of PLL and W_z is the zero of analog loop filter (i.e., $W_z=\frac{1}{RC}$).

From the above equations, and for giving specifications of phase margin and unity gain bandwidth, the values of analog loop filter components can be derived as follows [156]:

$$R=\frac{2\pi N}{K_{DCO}}\frac{\Delta TDC}{T_{REF}}\frac{w^2{}_{GBW}}{\sqrt{w^2{}_{GBW}+w^2{}_z}} \qquad (6\text{-}4)$$

$$C=\frac{\tan(PM)}{R*w_{GBW}} \qquad (6\text{-}5)$$

An S-domain approximation for the second-order ADPLL [156] is shown in Figure 6.11 (b), where the open loop gain can be expressed as:

$$\frac{T_{REF}}{2\pi \times \Delta T_{TDC}} \frac{K_{DCO}}{s}\left(\alpha + \frac{\beta}{1-z^{-1}}\right) \tag{6-6}$$

Where α, β are the coefficients of the digital loop filter. K_{DCO} is DCO sensitivity to its digital tuning word. T_{REF} is period of reference signal and ΔT_{TDC} is TDC resolution.

It can be noticed that there is high similarity between analog charge pump PLL and second order ADPLL. The above similarity is used to design the coefficients (α, β) of digital loop filter.

First, values of analog loop filter components are derived for the desired phase margin and unity gain bandwidth, the equivalent transfer functions [156] and bilinear transformation (Figure 6.11 (c)) are used to design loop filter coefficients for giving specifications of phase margin, unity gain bandwidth, reference frequency, and TDC resolution. The coefficients (α, β) can be expressed as:

$$\alpha = R - \frac{T_{REF}}{2C} \qquad \beta = \frac{T_{REF}}{C} \tag{6-7}$$

For practical implementation, filter coefficients are ceil/floored/rounded to be represented in 2^n format. In order to verify the accuracy of modeling methodology, a MATLAB model is implemented and extensive MATLAB simulations have been performed to check the accuracy modeling and to determine the range of digital filter coefficients. Figure 6.12 (a)-(d) show the closed loop response (Magnitude, and phase) for two simulation cases. Table 6-2 summarizes the simulation conditions of these two cases. It can be observed that, in both cases the closed loop response of analog PLL and ADPLL are in excellent agreement since the unity gain band width

is much smaller than reference frequency. It can be noticed that, there is a large difference at higher frequencies sine the s-domain modeling is inaccurate near Nyquist frequency. Table 6-3 and Table 6-4 summarize the achievable results of modeling using round and floor functions of these two cases. It can be noticed that the peaking in transfer function (Figure 6.12 (a) and (c)) results from low phase margin due to the coefficient's rounding.

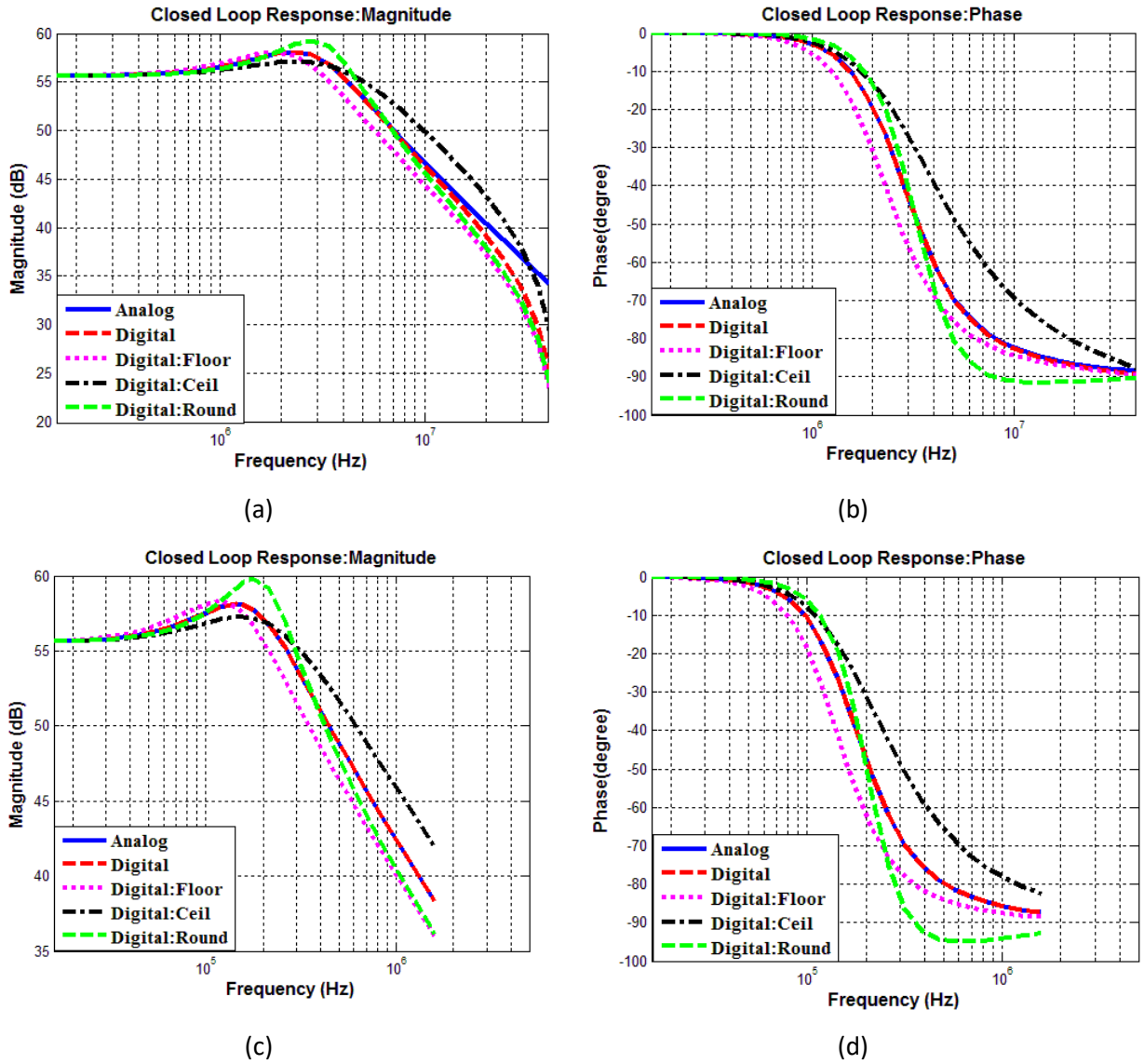


Figure 6.12 Simulated closed loop response: (a) Loop magnitude with (GBW = 4 MHz). (b) Loop phase with (GBW = 4 MHz). (c) Loop magnitude with (GBW = 0.25 MHz). (b) Loop phase with (GBW = 0.25 MHz)

Table 6-2 Simulation conditions of design loop verification

Parameter	K_{DCO} (MHz)	ΔT_{TDC} (fs)	F_{Ref} (MHz)	Phase Margin	BW (MHz)
Case # 1	100	500	100	60	4
Case # 2	100	500	100	60	0.25

Table 6-3 Verification results of digital loop design with bandwidth of 4 MHz

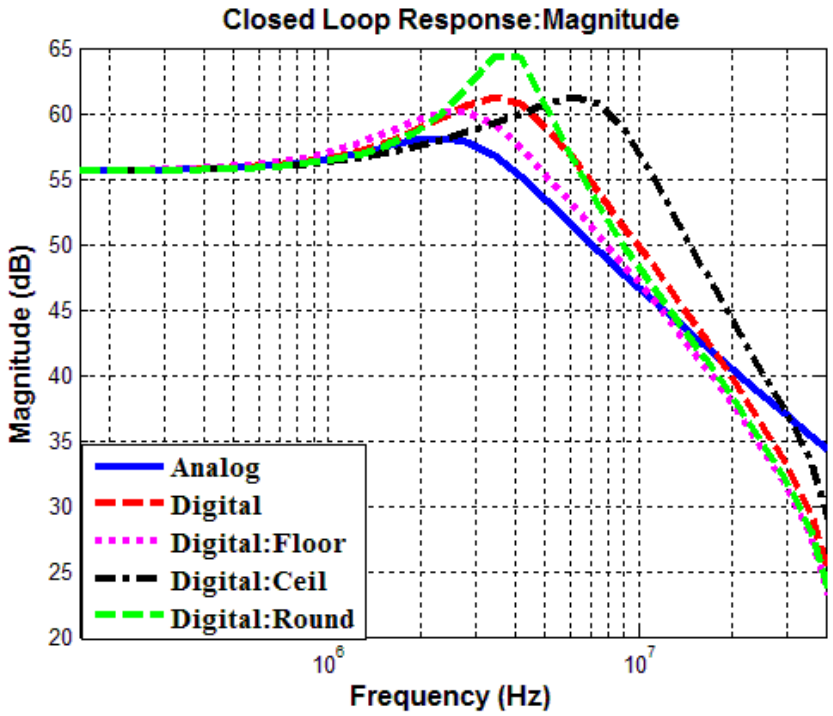
Parameter	α	β	Phase Margin	BW (MHz)
Bilinear transformation	0.038	0.005953	60	3.9791
With round	2^{-5}	2^{-7}	48	3.9541
With Floor	2^{-5}	2^{-8}	60	3.227

Table 6-4 Verification results of digital loop design with bandwidth of 0.25 MHz

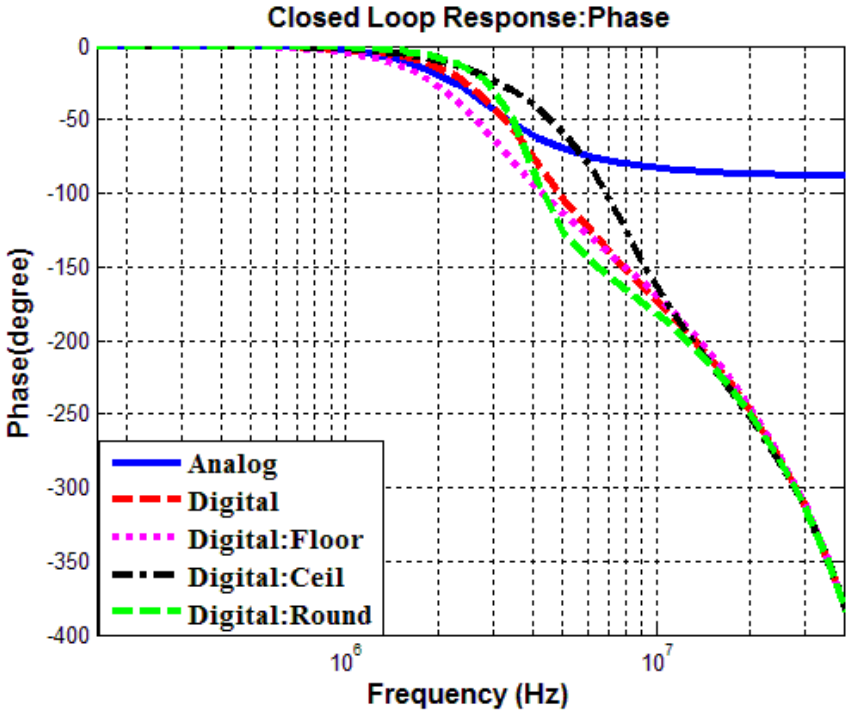
Parameter	α	β	Phase Margin	BW (MHz)
Bilinear transformation	0.00255	2.325×10^{-5}	60	0.25
With round	2^{-9}	2^{-15}	44	0.238
With Floor	2^{-9}	2^{-16}	58	0.1985

Table 6-5 Summary of loop performance after parameters adaption in case of loop latency by Z^{-1}

Parameter	α	β	Phase Margin	BW (MHz)
With round (before adaption)	2^{-5}	2^{-7}	20	3.954
With round (after adaption)	2^{-4}	2^{-10}	49	5.2723
With Floor (before adaption)	2^{-5}	2^{-8}	37	3.22
With Floor (after adaption)	2^{-5}	2^{-10}	60	2.7162



(a)



(b)

Figure 6.13 Simulated closed loop response when loop latency increases by Z^{-1}: (a) Loop magnitude. (b) Loop phase.

As has been discussed in chapter 2, loop latency degrades phase margin and PLL loop stability. Figure 6.13 shows the closed loop response of ADPLL, with simulation parameters of first case in Table 6-2, when loop latency increases by one cycle. From Figure 6.12 (a)-(b) and Figure 6.13, it can be observed that the phase margin degrades with more than 23^{o} in both rounding and flooring approaches due to loop latency increasing. However, with the adaption of the loop filter coefficients as shown in Table 6-5, the phase margin can be increased on the expense of a little degradation on unity gain bandwidth.

From the extensive MATLAB verifications and to meet the desired loop requirements that are discussed in previous section, it was proven that the loop filter coefficients should be programmable as shown in Table 6-6. Since the filter coefficients are represented in 2^{n} format, their adaption can be easily implemented based on shift left/right operations.

Table 6-6 Range of loop filter coefficients

Parameter	Lower value	Higher value	Resolution step
α	2^{-9}	2^{-3}	2^{-1}
β	2^{-16}	2^{-5}	2^{-1}

6.5.4 Loop bandwidth adaption

The main goal of loop bandwidth adaption is to achieve fast settling by operating in Type-I PLL during acquisition mode and switching to Type-II PLL during tracking mode [48], [157]–[159]. In this work, we applied the same concept as shown in Figure 6.10. Initially, the loop starts with Type-I PLL by turning-off the integral path. Once the frequency error becomes less than certain programmable threshold, gear shifting process [159] is enabled and proportional part is adapted to narrow the bandwidth. Then when the frequency error decreases below certain

programmable threshold, the integral part is enabled to convert the loop in Type-II PLL to eliminate steady state error. There are many issues [159] related to switching between each state but all of them are addressed and verified using Verilog/Verilog-A AMS simulation

6.5.5 DCO linearization

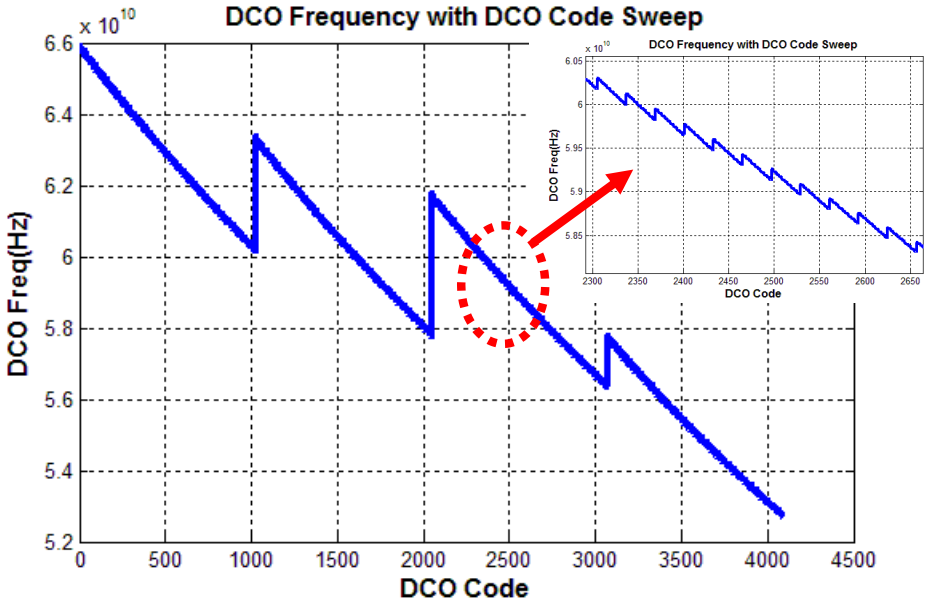


Figure 6.14 DCO transfer function versus tuning code

In order to cover the required tuning range (i.e., > 10 GHz) with frequency resolution better than 100 kHz, several capacitor banks and inductor switching technique are used as discussed in chapter 3. Additionally, to guarantee covering the required range without any gap, sufficient overlapping between each two consecutive banks is required. However, this overlapping leads to non-monotonic DCO transfer function as shown in Figure 6.14.

Since non-linearity in DCO transfer function increases settling time considerably and increases spurs level, we propose a simple and effective technique to overcome this non-linear

behavioral. The proposed solution uses the third path of frequency error as shown in Figure 6.10 The proposed solution here is to enable only one capacitance bank during the operation of ADPLL. During acquisition mode, when the frequency error is high, cap bank #1 which provides highest frequency step is enable and the rest of banks are fixed to their middle value. Frequency error is monitored and the direction of DCO frequency (Increasing/Decreasing) is calculated and once the error decreases than certain programmable threshold, control word of first bank is hold and second capacitor bank is enable in convergence direction only. The same process is repeated across the four capacitor banks until frequency error diminishes.

6.6 Top level verification of 60 GHz ADPLL

Two design methodologies are used to verify the closed loop operation of ADPLL and the effect of non-idealities of its building blocks. First method depends on using MATLAB/SIMULINK behavioral verification. Complete and accurate MATLAB model of ADPLL (Figure 6.1) was implemented, by one of my group's colleague, to check the effect of TDC and DCO non-idealities. This model is used also to estimate the initial specifications of building blocks of ADPLL loop. Afterwards, another accurate modeling methodology based on Verilog-A and Verilog is used to complete top level verification of ADPLL.

6.6.1 Verilog-A/Verilog verification

This method depends on modeling each RF/analog block inside top-level of ADPLL (Figure 6.1) using Verilog-A to include all possible non-idealities. The DCO sub-system shown in Figure 6.1 is modeled based on measurement results of previous DCO chip (Chapter 3). Actual tuning range and frequency step of each capacitor bank are used to emulate the effect of DCO

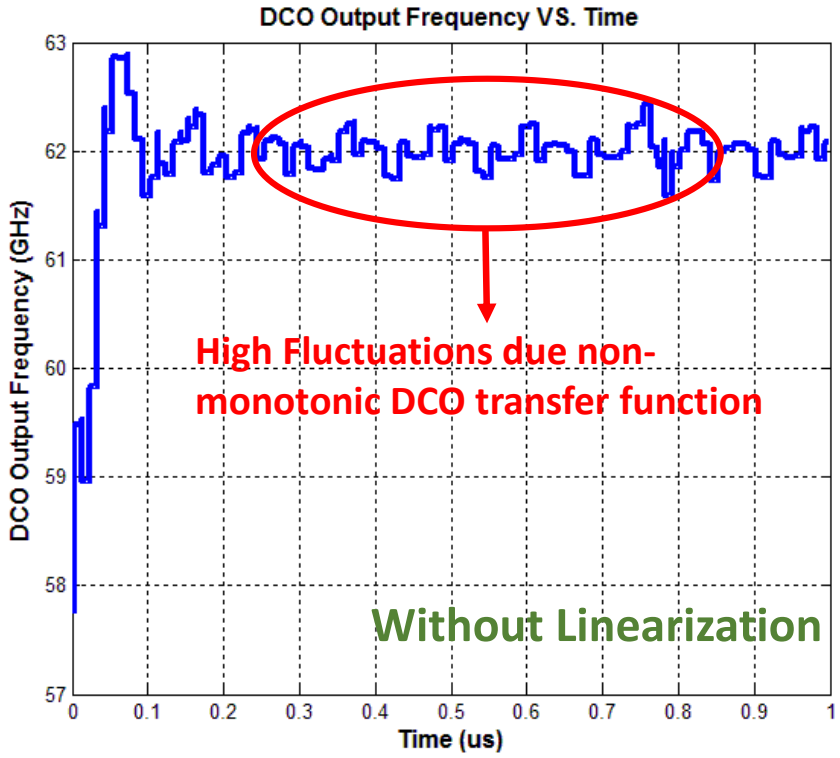
quantization noise and bands overlapping on output spectrum and settling behavioral, respectively.

The divider sub-system (Figure 6.1) is modeled to divide input frequency by four and to generate eight CMOS phases with uniform 45^{o} spacing. The divider's Verilog-A model adds random delay with sigma variation of 3 degree to each output phase to emulate phase mismatch effect. The integer counter in phase extraction path (Figure 6.1) is modeled to provide the integer ratio between *PH<0>* and reference frequency, random integer number is added at the counter output to model the effect of supply variation.

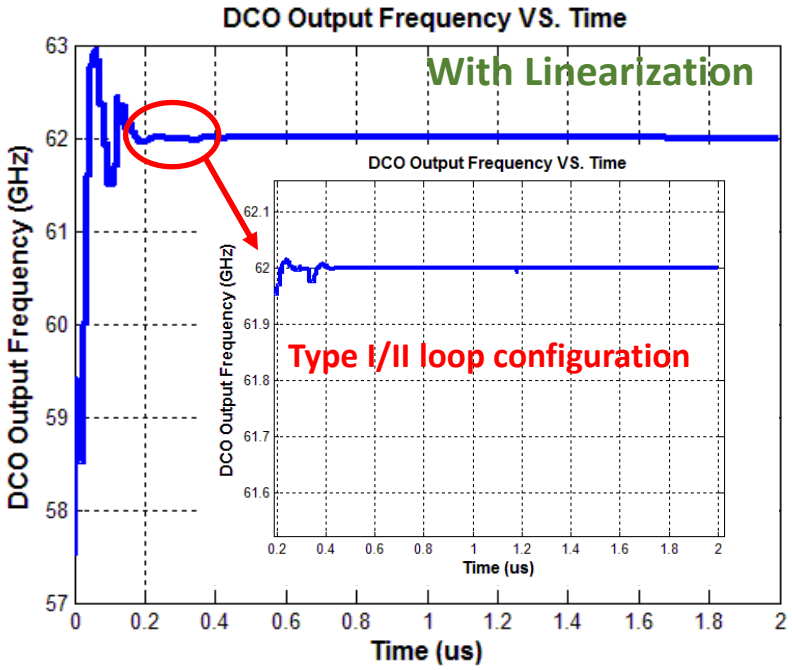
In order to model TDC accurately, FTDC stage (Figure 5.8 (b)) is modeled to include delay difference variation between fast and slow line. 700 fs sigma variation is used to emulate the actual delay difference variation of FTDC stage (Figure 5.10 (a)). TOP level schematic of FTDC is implemented by connecting the 32 stage. CTDC and CFI are also modeled based on Verilog-A of their basic units, time arbiter and sub-sampler. Voltage offset is added at the inputs of CTDC to emulate the effect of time offset in arbiter.

On the other hand, an automatically synthesized Verilog models with real time margins are used for the phase mismatch calibration algorithm, FTDC calibration engine, CFI calibration engine, and proposed digital loop (Figure 6.1). All digital and calibration blocks are clocked with the 100 MHz reference (REF) after re-timing with phase PH<0>.

Extensive AMS simulations are performed to verify the top-level performance of ADPLL and to guarantee that the actual specification of sub-systems' blocks meet the desired requirements of overall system. The following figures present some of these verification scenarios.

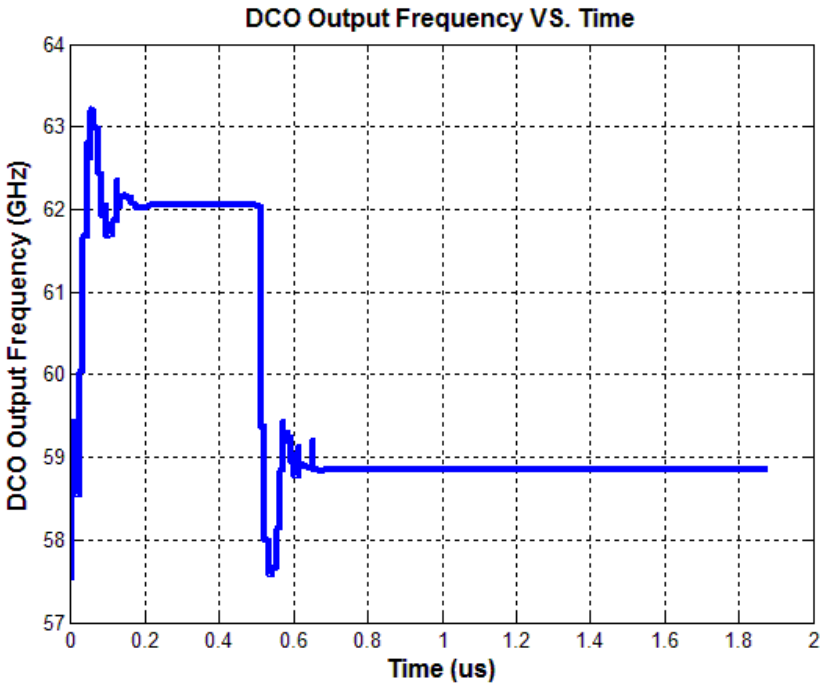


(a)

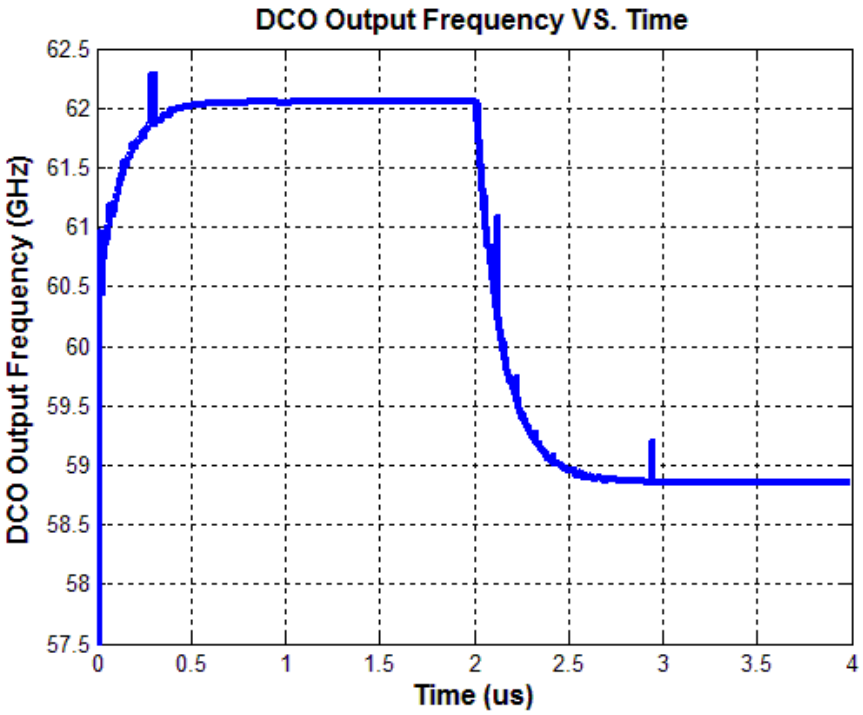


(b)

Figure 6.15 Simulated closed loop response (a) without and (b) with DCO linearization for a target frequency of 62 GHz.

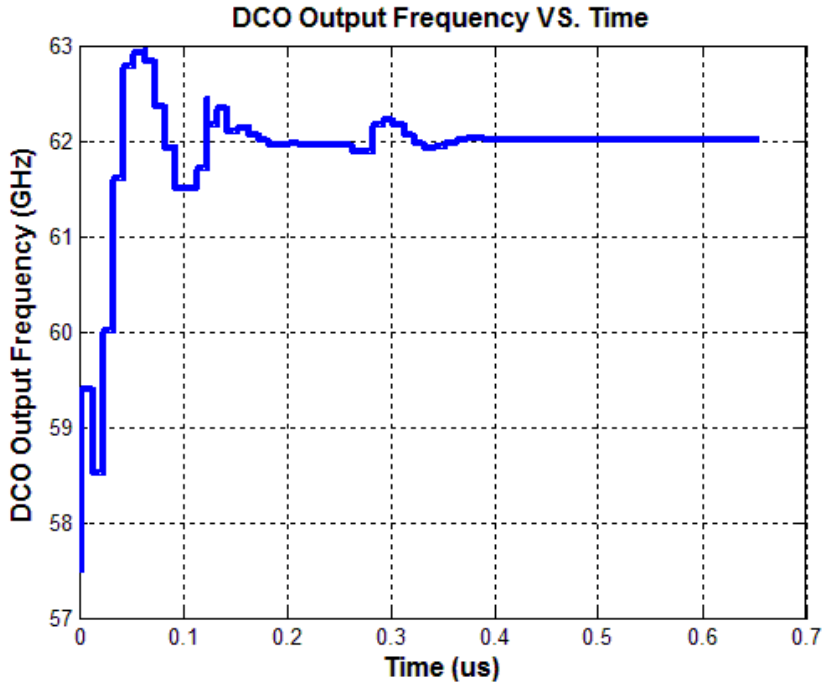


(a)

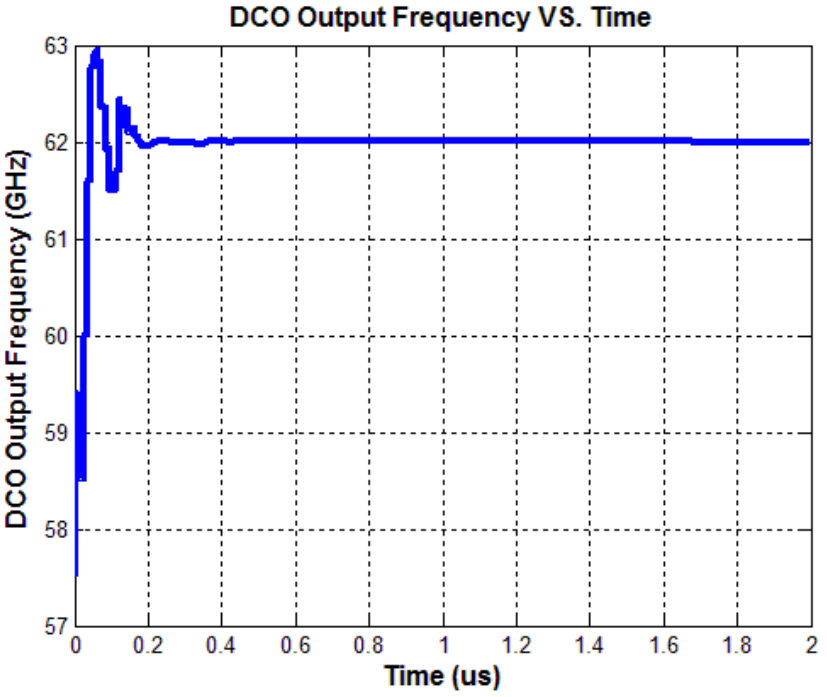


(b)

Figure 6.16 Simulated closed loop response when FCW switches from 155.0625 to 147.125 in case of phase margin equals (a) 55^{o} and (b) 75^{o}



(a)



(b)

Figure 6.17 Simulated closed loop response (FCW = 155.0625) with switching between Type 1 and Type II PLL: (a) without storing the error. (b) with storing the error

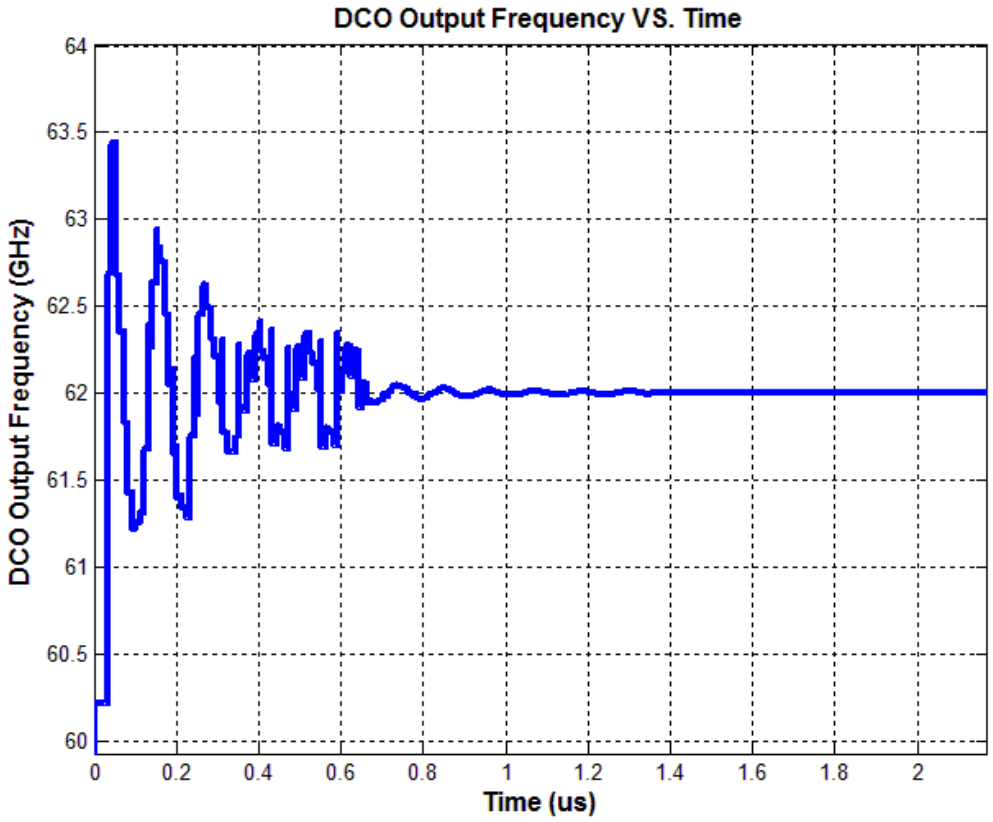


Figure 6.18 Simulated closed loop response with worst case phase margin of 22^{o}

Figure 6.15 shows the closed loop response with 62 GHz output frequency with and without DCO linearization. It can be observed that there are high fluctuations of +/- 0.5 GHz around the target frequency due to non-monotonic behavioral of DCO. Figure 6.16 shows the simulated closed loop response when FCW switches from 155.0625 to 147.125, which is corresponding to output frequency switching from 62.025 GHz to 58.85 GHz, for two different settings of loop filter coefficients (i.e., two different phase margin values). It can be observed that the simulated settling time (+/- 2% from the final value) is less than 220 ns with phase margin of 75^{o}.

Figure 6.17 shows that the simulated closed loop response for output frequency of 62.05 GHz with switching between Type 1 and Type II PLL. In Figure 6.17 (a), gear-shifter and integral part are used at different phase error threshold. It can be noticed that, although enabling the integral

part eliminate the steady state error, there are a frequency jump at the moment of integral part activation (i.e., at 0.3 µs). The main reason of this undesired jump is that the integral part deals with current phase error as a DC offset which should be eliminate, thus it takes some time to remove it. The solution to this problem is to store the phase error value before integral part activation by one cycle and subtract it at the activation [159]. Figure 6.17 (b) shows the response with error storing which eliminates the undesired frequency jump and reduce settling time. Finally, Figure 6.18 shows the simulated closed loop response with worst case phase margin of 20°

6.7 Characterization and discussion

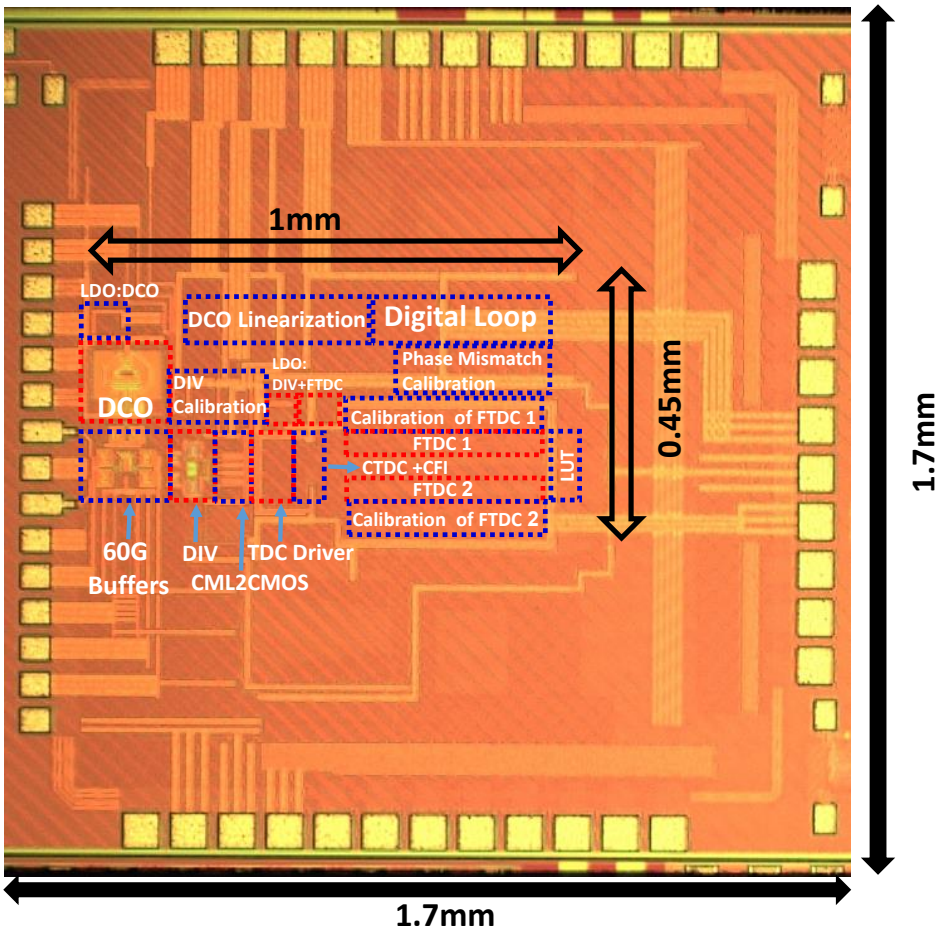


Figure 6.19 Die photo of ADPLL chip

Figure 6.19 shows the die photo of ADPLL chip which is fabricated in 65 nm CMOS. The core area of ADPLL is 0.45mm^2. Table 6-7 shows the area distributions of main blocks inside APDLL chip. It can be noticed that area of SRAM memories used for internal signal observation is large than active area of overall ADPLL chip.

Table 6-7 ADPLL area distribution

Block	Area (mm^2)
DCO	0.02
Divider + CML-to-CMOS	0.028
TDC + Counter	0.04
Phase mismatch calibration	0.02
Digital loop	0.056
FTDC calibrations	0.06
SRAM memories	0.6

Figure 6.20 shows a simplified diagram of the measurement setup of ADPLL chip. All the measurements were performed using on-wafer probing. Arbitrary waveform generator (AWG7002A) is used to generate external test signals for FTDC calibration. Mixed signal scope (MSO) is used to measure and store digital outputs. Network analyzer (N5247A-X) is used to generate the reference signal (100 MHz) and required signals to calibrate CFI stage.

The DCO output from the probe is split using a Quinstar power divider to generate two RF signals, which are then down-converted by Quinstar V-band mixers. An Agilent E5052B signal source analyzer provides 3.1-6 GHz LO signals to drive the mixers. The IF outputs from the mixers are down-converted again to below 7 GHz using an Agilent E5053A microwave down

converter and then input to the E5052B signal source analyzer, which is set up to perform a phase noise and output power measurements.

In order to reduce coupling between analog and digital blocks, they are separate by more than 200 µm, separate On-chip LDOs are used to provide supply voltage, separate grounds are used for analog and digital blocks, and separate supply voltages are used for ESD structure of analog and digital pads.

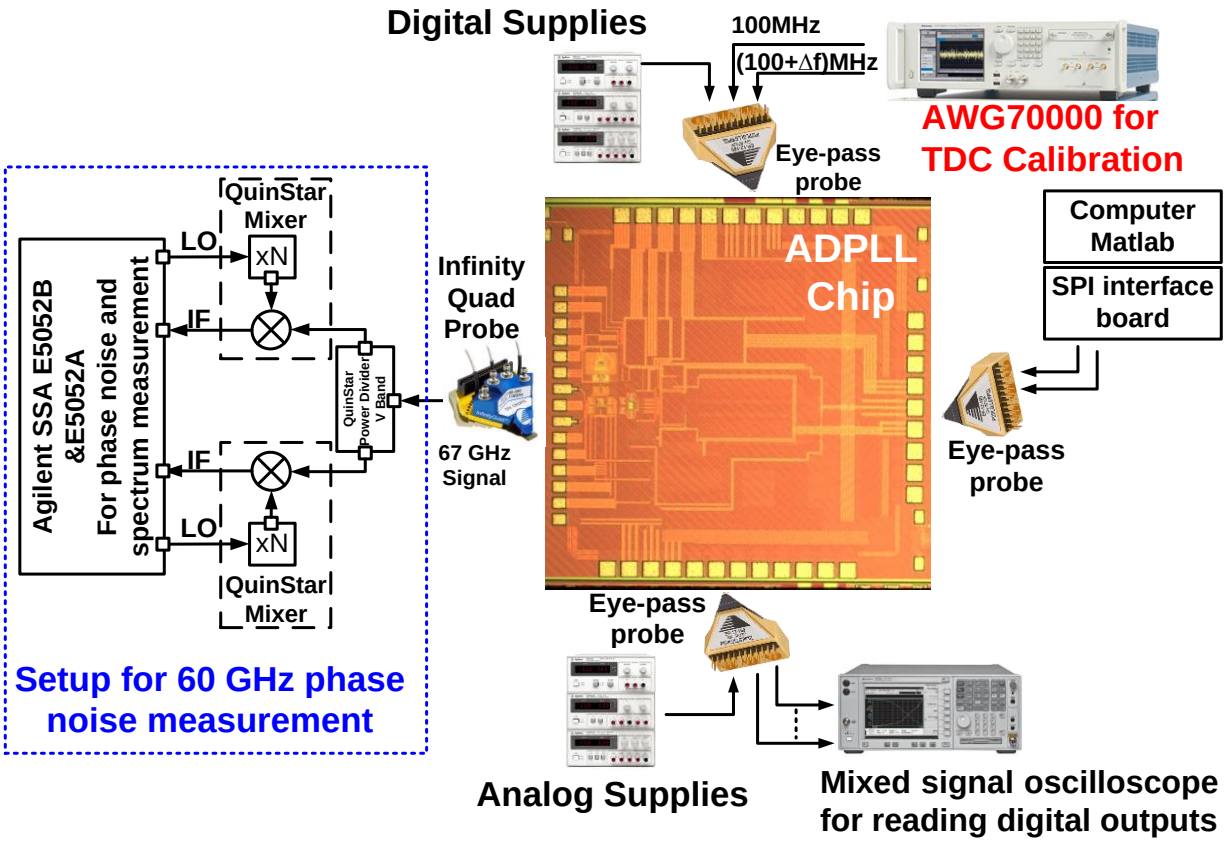


Figure 6.20 Measurement setup of 60 GHz ADPLL Chip

The ADPLL chip consumes 46 mA from a 1 V supply, Figure 6.21 shows the power consumption breakdown of ADPLL chip.

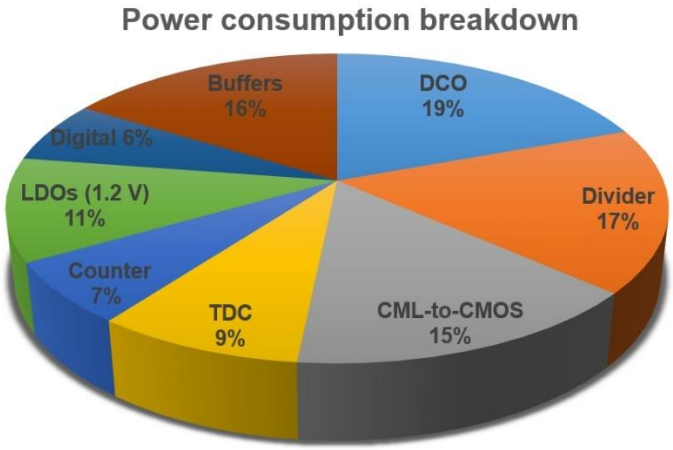


Figure 6.21 Power consumption breakdown of ADPLL chip

Table 6-8 Summary of tuning range for all possible configurations of DCO transformer

Tuning word	Word = "00"	Word = "01"	Word = "10"	Word = "11"
Covered Range (GHz)	50.2-55.1	53.2-58.3	56.9-62.7	59.1-66.4

Table 6-9 Summary of frequency step of capacitor banks for 60 GHz ADPLL

Capacitor bank	C1 (5 bits)	C2 (5 bits)	C3 (6 bits)	C4 (5 bits)
Frequency step	190 MHz	11.2 MHz	445 KHz	41 KHz

The measured tuning range is 28% (50.2-66.4GHz). Table 6-8 summarize the tuning range for all possible configurations of transformer, while Table 6-9 summarize the tuning step of each capacitor bank.

Figure 6.22 shows the worst case measured phase noise at carrier frequency of 65.3 GHz, where the in-band phase noise at 10 KHz offset frequency is -78.75 dBc/HZ and out-band phase noise at 10 MHz offset frequency is -121.39 dBc/Hz. Worst (best) case phase noise – measured at carrier frequency of 65.4 (50.8) GHz – are -79 (-83) dBC/Hz and -116(-126) dBC/Hz, at 0.1 and 10 MHz offset, respectively. Measured worst and best case RMS jitter is 258 fs and 223 fs of which meets the 802.11ad specification for 16-QAM.

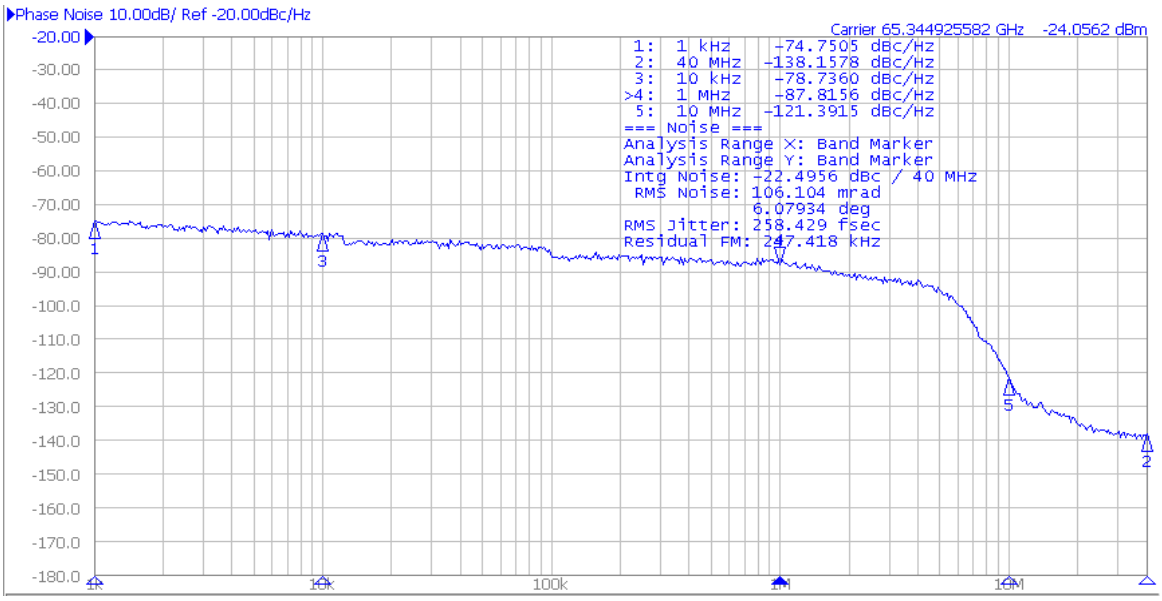


Figure 6.22 Worst case measured phase noise at 65.3GHz carrier frequency

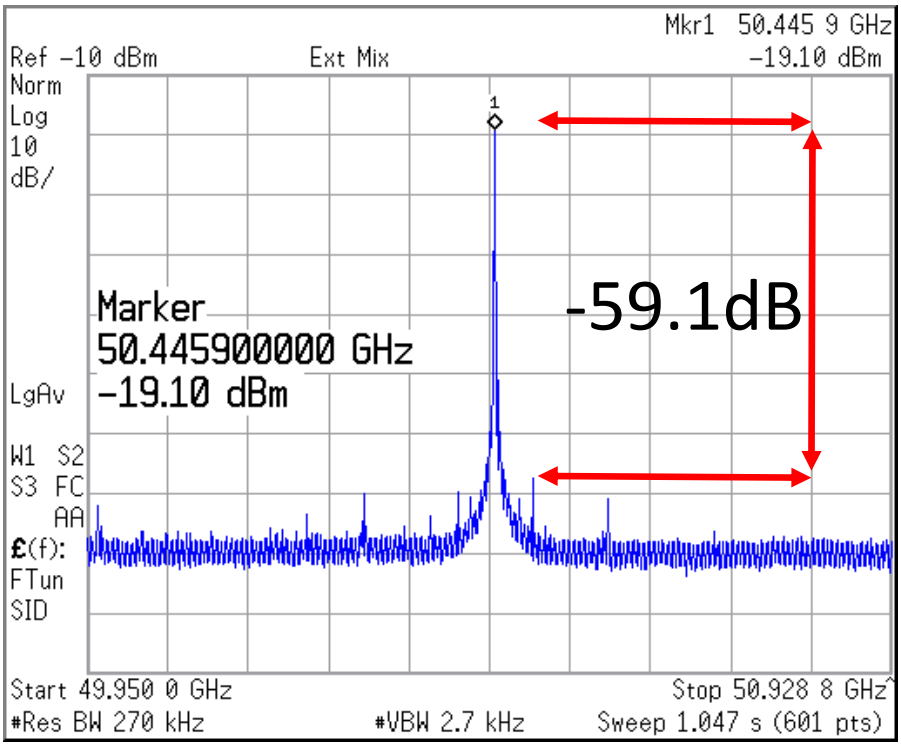


Figure 6.23 Measured spurs level at carrier frequency of 50.4GH

Table 6-10 Performance comparison of this ADPLL with recent 60 GHz PLL's including analog PLL's and the sole 60 GHz ADPLL reported to date.

Spec\ Ref #		ISSCC'09 [160]	JSSC'11 [19]	JSSC'14 [81]	JSSC'14 [79]	ISSC'14 [161]	JSSC'16 [34]	This Work
Architecture		CP analog PLL	20GHz analog PLL	CP analog PLL	TDC-ADPLL	Sub-sampling PLL	20G Sub-sampling PLL *	ADPLL
Type		INT-N	INT -N	INT -N	**FRAC-N**	INT-N	INT-N	**FRAC-N**
Output frequency (GHz)		57-66** (14.6%)	58-63 (8.3%)	58-68.3 (8.3%)	56.5-63.5 (11.6%)	53.8-63.3 (16.2%)	58.3-64.8 (10.5%)	**50.2-66.5 (28%)**
Ref. frequency (MHz)		100	36	135	100	40	40	100
Phase noise (dBc/Hz)	10KHz	-70	-60	-80	-75	-80	-75	**-79 ~ -83**
	1MHz	-75	**-95**	-91	-90	-88.3	-92	-88 ~ -92.7
	10MHz	-	-113	-108.5	-110	-108	-122	**-116 ~ -126**
Spurs level (dBc)		-42	-	-45	**-74**	-40	-73	-59.1 ~ -68
RMS jitter (fs)		-	-	238.4	590.2	**220**	290	223-261
Output Power (dBm)		-28	-	-20.34	0^{+}	-21	-18.2	$-3/-10^{++}$
FOM (dBc/Hz)	$\Delta f = 100KHz$	-166.9	-156.8	-182	-174	-179.6	-175.79	-181.2
	$\Delta f = 1MHz$	-151.9	-171.8	-173	-169	-167.9	-172.22	-172.2
	$\Delta f = 10MHz$	-	-169.8	-170.5	-169	-167.6	-182.7	**-184.2**
FOMT (dBc/Hz)	$\Delta f = 100KHz$	-170.2	-155.2	-180.4	-175.3	-183.8	-176.2	**-190.1**
	$\Delta f = 1MHz$	-155.2	-170.2	-171.4	-170.3	-172.1	-173.2	**-181.1**
	$\Delta f = 10MHz$	-	-168.19	-168.9	170.3	-171.8	-183.2	**-193.2**
Supply (V)		1.1	1.2	1.2	1.2	1	1	1
Power (mW)		78	80	**24**	48	42	32	46
Area (mm2)		0.82 With pads	1.68	0.192	0.48	0.16	1.09 With pads	0.45
Technology (nm)		45	65	65	65	40	65	65
$FOM = PN(\Delta f) - 20\log\left(\frac{F_{out}}{\Delta f}\right) + 10\log\left(\frac{Power(mW)}{1mW}\right)$				$FOM_T = PN(\Delta f) - 20\log\left(\frac{F_{out} * TR}{\Delta f * 10\%}\right) + 10\log\left(\frac{Power(mW)}{1mW}\right)$				

* Use Injection lock oscillator at third harmonic to generate output frequency from 20GHz PLL.
** Use two VCOs to cover the whole output range.
+ Using off-chip buffers
++ Simulated
Note: Bold face entries represent best-in-class benchmark.

Figure 6.23 shows the worst-case spur level at 50.4GHz, where the spurs level is -59.1dBc and it decreases by 17.8 dB when the different calibration techniques are enabled, thereby demonstrating their effectiveness.

Table 6-10 compares the proposed ADPLL with recent 60 GHz PLL's, including analog PLL's, reported to date. The ADPLL presented features also the widest tuning range, lowest phase noise, and the highest reported FoM_T among mm-wave ADPLL's reported to date, along with excellent spur performance.

7 Conclusion

With the explosive growth of mobile traffic demand, the contradiction between capacity requirements and spectrum shortage becomes the main bottleneck towards high date rate wireless communication systems. The millimeter-wave (mm-wave) frequency bands have recently emerged as a viable option to meet the exploding demand for wireless multimedia content over short ranges. Frequency synthesizers that can tune over wide bandwidths in finely spaced steps are essential components in wireless mm-wave applications. With all the advantages of all-digital frequency synthesizers, they remained restricted to low gigahertz operating frequencies since the design of DCOs, TDCs, and frequency dividers operating at mm-wave frequency poses enormous challenges, and the mitigation of those challenges remains an open problem.

This research explored the feasibility, advantages, implementation, and testing of millimeter-wave fractional-N digital frequency synthesizers. In addition, it proposed several design techniques to overcome the design challenges of the constituent blocks in mm-wave ADPLL's, thereby enhancing performance by reducing spurs, increasing tuning range and frequency resolution. The proposed architectures and techniques is suitable for all mm-wave applications below 100GHz, 60GHz frequency synthesizer was implemented in this work as an example to validate the proposed techniques. During the investigation of millimeter-wave fractional-N digital frequency synthesizers, several solutions are proposed and validated.

In chapter 3, the proposed mm-wave DCO employs switched coupled inductor and switched capacitor banks to achieve very wide tuning range (48.1 GHz ~61.3 GHz). In addition, a fine frequency tuning resolution of 39 KHz has been achieved using capacitive degeneration technique. Simple but effective calibration scheme is proposed to maintain the frequency

resolution and output swing across operating frequency range. The proposed DCO was fabricated in 65 nm CMOS, and it consumes only 10mW. With a measured phase noise lower than -114 dBc/Hz, at 10 MHz offset, the proposed DCO has an excellent figure-of-merit (-186.4 dB ~ -182.2 dB) and small silicon area of 0.032 mm2.

In chapter 4, we have proposed several new design techniques to enhance the operating frequency range and locking range of inductor-less mm-wave frequency dividers. These techniques are informed by a more refined analysis of the divider than available in the literature. The proposed design techniques, namely source coupling, current bleeding, multi-Vt design, adaptive bulk biasing and bulk modulation are demonstrated via three prototype designs.

A background calibration scheme is proposed to adaptively tune and optimize bias settings for a given input frequency, thereby enhancing robustness, reducing power consumption and resulting in a practically usable divider.

All proposed techniques are demonstrated through extensive characterization. To our knowledge, the resulting dividers achieve the widest bandwidth, smallest area and highest FOM_P compared to state-of-the-art dividers on 65nm process and older nodes. Furthermore, it has the lowest power consumption among inductor-less dividers at the 65nm node and is expected to benefit from technology scaling.

In chapter 5, we demonstrated the first TDC operates at mm-wave range (20-68 GHz) with finest time resolution (450 fs) reported to date. A synthesized digital calibration scheme based on statistical element selection is introduced to alleviate TDC nonlinearity results from PVT and random mismatch variations. The measured DNL and INL of a 65 nm CMOS two-step TDC

prototype are 0.65 LSB and 1.2 LSB, respectively. The 60 GHz TDC consumes only 11mW which results in best FOM_I over the state of the art.

A powerful on-chip calibration engines have been implemented to calibrate each sub-system of proposed mm-wave TDC to minimize TDC non-linearity. The calibration engines include serval features to cover different operating conditions. Extensive MATLAB and Verilog simulations have been performed to guarantee the calibration functionality.

In chapter 6, we demonstrated a 60 GHz all-digital phase-domain PLL that covers the widest reported frequency range (50-66 GHz) among 60 GHz PLLs [61]. The PLL incorporates extensive digital calibration of each sub-system to achieve 220 fs jitter, best (worst) phase noise of -83/-93/-126 (-79/-88/-116) dBc/Hz at 0.1/1/10MHz offset, -59 dBc spur and the highest reported FoM_T to date among mm-wave PLL's. The presented ADPLL features also the widest tuning range, lowest phase noise among mm-wave ADPLL's reported to date, along with excellent spur performance. Moreover, we demonstrated two different techniques to mitigate phase mismatch effect on ADPLL's performance and we proposed simple but effective design methodology to overcome the non-monotonic behavioral of DCO transfer function.

In the all demonstrated chips, the theoretical challenges have been investigated then extensive MATLAB system simulations, Verilog-A/Verilog AMS simulations, and circuit simulations have been performed to compare the theoretical limits with simulations and to verify the effectiveness of proposed solutions.

All fabricated chips include on-chip supply regulators that were design for sensitive blocks, such as the DCO, the DCML divider, and the fine TDC, in order to isolate them from supply

modulation effects. All the measurements of all fabricated chips were performed using on-wafer probing.

7.1 Future work

Several different future directions can be drawn based on the work presented in this thesis.

1. Extend the operating frequency of 60 GHz ADPLL to 71 GHz to serve the new V-band (57 GH- 71 GHz). This frequency extension requires some modifications of DCO core, and phase extraction path to accommodate higher operating frequency.
2. Alternatively, Sub-harmonic digital PLL can be implemented to serve the new V-band. The DCO center frequency can be scaled down to 32 GHz and DCML divide-by-2 insert before path extraction path. A frequency doubler will be used after the DCO to generate the target output frequency. Please note that the dynamic range of FTDC stage should be increased since the DCML divider generate only 4 phases in this case.
3. It can be noticed that 60 GHz transceiver based on direct conversion architecture is preferable in the next wireless communication generation due to low power consumption and small area. Therefore, the DCO architecture can be modified to generate Quadrature outputs to serve direct conversion 60 GHz transceiver.
4. Time-amplifier (TA) stage can be inserted after interface stage of TDC to relax the requirement of FTDC stage. This, in turn, will relax the complexity of TDC calibration schemes. In this case, a trade-off comparison between calibration requirements of TA and current calibration requirements of FTDC should be drawn to optimize the gain of time-amplifier and resolution of FTDC.

5. FTDC calibration uses an external dual channel signal source generator which requires long averaging to alleviate input jitter effects on calibration accuracy. The implementation of On-chip dual channel signal generator should be investigated. One possible solution is to implement it using two simple PLLs running at output low frequency (100MHz ~ 400MHz) to eliminate the need for off-chip source. This solution will reduce the complexity, cost, and run time of FTDC calibration, on the expense of higher power consumption.
6. The FTDC was designed to cover the quantization period of CTDC (7.4ps - 10ps) for output frequency between 50 GHz and 66 GHz. Therefore, it consists of 32 stage to cover this range with a time resolution of 400 fs. In order to improve in-band phase noise during real-time operation, the FTDC resolution can be adapted automatically based on output frequency value. The output of feedback counter can be monitored to estimate output frequency range, and for higher output frequencies, the delay control units inside FTDC stage can be tuned to increase FTDC resolution. In this case, the FTDC should be calibrated at different target resolutions and the output of calibration can be stored in on-chip SRAM. During real time operation, and based on output frequency range, the target resolution and corresponding calibration words can be loaded from this SRAM and feed into TDC.
7. In order to serve the next 5G communication system, a system level design of dual-bands (28 GHz/38 GHz) transceiver can be implemented to determine the specifications of ADPLL. Based on this study, the constituent blocks of current ADPLL can be modified and reused to implement a signal ADPLL server the dual bands.

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