High Dynamic Range CMOS-MEMS Capacitive Accelerometer Array with Drift Compensation

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ABSTRACT

This thesis explains the design, fabrication and characterization steps of a high dynamic range CMOS-MEMS capacitive accelerometer array and on-chip environmental sensors for bias drift compensation. Inertial navigation under harsh environments requires a high dynamic range accelerometer that can survive and provide continuous readout accuracy through shock events, while having a large dynamic range to capture fine-scale motions. The dynamic range target is set as 156 dB in accordance with navigation standard macro-electromechanical accelerometers, which corresponds to around 1 mG acceleration resolution in 50 kG input range. The small accelerometer cell design ensures shock survivability (e.g. up to 50 kG) by keeping the stress at the anchors below the fracture strength of thin-film oxide. Arraying multiple accelerometer cells in parallel lowers the fundamental thermomechanical noise limit set by the small mass of the individual accelerometer cells. Resonance frequency staggering between accelerometer cells suppresses ring-down oscillations. Parasitic capacitance of the high-impedance transduction signal is important to mitigate; undercut of the underlying silicon substrate and an aluminum etch of the top metal layer, incorporated in the CMOS-MEMS process flow, reduces the parasitic capacitance and improves sensitivity.

PTAT temperature sensors, piezoresistive stress sensors and resonator-oscillators integrated across the accelerometer chip provide high-resolution environmental measurements for the compensation of long-term bias and scale factor drift. Simultaneous measurements from the accelerometer and environmental sensors demonstrate the correlation between environmental variations and long-term drift. Finite-element analysis shows that the scale factor stability of the accelerometer can be improved up to 1 ppm given the sensor array's measurement resolution.

The CMOS-MEMS accelerometer system-on-chip is fabricated in a TowerJazz 0.18 μm CMOS process. The post-CMOS MEMS processing steps are tuned to reduce the top metal milling and sidewall polymer deposition. A reactive ion etch recipe is developed for the removal of the top metal in order to reduce the parasitic capacitance and eliminate the risk of metal creep at spring beam anchors, thereby improve the bias stability.

The PTAT temperature sensors have 3.1 mV/K measured sensitivity and 7.1 mK resolution with high repeatability. The compensation of the accelerometer readout for temperature variations down to 7.1 mK translates to 2.6 ppm scale factor stability for the accelerometer. The characterization of the stress sensors through the application of normal stress on the device package leads to an uncertainty in the amount of stress transferred to the stress sensors on the chip surface. The maximum measured stress sensitivity is 36.5 pV/Pa, which leads to 24.7 kPa stress resolution and translates to 1.7 ppm scale factor stability for the accelerometer without taking the stress attenuation into account. The measured sensitivity sets a lower bound on the sensitivity of the stress sensors implying that the stress resolution and the corresponding accelerometer scale factor stability is higher in practice. The measured frequency stability of the resonator-oscillator is 0.4 ppm, thereby the resonance frequency based variations of the accelerometer readout can be compensated to reach up to 0.8 ppm scale factor stability. However, the initial drift in the resonance frequency of the oscillators due to dielectric charging requires a long wait-time before these sensors can be used for accelerometer drift compensation.

The accelerometer array is demonstrated to have 23.7 mG/√Hz noise floor and 70 mG bias stability. The maximum input acceleration applied on the device is limited to 4 kG by the split Hopkinson bar test setup. Improvement of the setup to transfer acceleration amplitudes up to 50 kG should validate the designed input range of the accelerometer array and lead to 117 dB dynamic

range for the current design. The measurement bandwidth is fundamentally set by the 126 kHz resonance frequency of the accelerometer cells and can be further limited by filtering the readout signal to attenuate the transient oscillations faster. The nonlinearity of the accelerometer response is better than 1.2% in ±10 kG input range; however, it gets up to 19.0% in ±50 kG maximum input range.

The long term bias drift of the accelerometer is shown to be correlated with the temperature and stress variations. Compensation of the accelerometer readout based on the stress and temperature sensor measurements leads to an observable improvement in the long term drift. However, the bias stability of the accelerometer is limited by excessive flicker noise in the system, which is believed to result from noise folding from higher frequencies. Suppression of the flicker noise in the system should allow for a more detailed study of the effect of environmental variations on the accelerometer readout and evaluation of more elaborate fitting algorithms for model based prediction and compensation of the bias drift to reach the target bias stability and dynamic range.

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CHAPTER 1: INTRODUCTION

1.1 Motivation

This study demonstrates the potential to reach an unprecedented dynamic range with an open loop accelerometer design based on capacitive sensing. The CMOS-MEMS process integrates the accelerometer, readout circuits and environmental sensors on the same chip, hence forming a high dynamic range accelerometer system on chip. The small accelerometer cell design ensures survivability and measurement through shock events. The arrayed design helps reducing the thermal-mechanical noise floor set by the small mass of the accelerometer cell and increasing the sense capacitance to improve the transducer scale factor. Monolithic integration of the readout circuits minimizes the parasitic capacitance, hence increasing the transducer scale factor and linearity. On-chip environmental sensors measure the stress and temperature variations for long term scale factor and bias drift compensation.

Accelerometers are used in various fields including but not limited to automotive, biomedical, consumer electronics, robotics and military applications [1]. The particular emphasis in this thesis is on improving the performance of MEMS accelerometers for inertial navigation applications through high-shock environments, where the small size, high robustness and low cost (when fabricated on wafer scale) of micro-electromechanical accelerometers make them more preferable than their macro-electromechanical counterparts [2]. Inertial sensors are mostly aided by a GPS signal [3], since the long term bias instability of these sensors prevents their standalone usage for navigation [4]. Improved navigation performance can be obtained by improving the sensitivity and bias stability of the inertial sensors; however, any improvements in sensitivity (hence in the resolution for a given noise floor) inherently lead to a lower limit for the maximum measurable signal for a fixed dynamic range. On the other hand, the survivability and continued

readout accuracy of the sensors through shock events need to be guaranteed for navigation under harsh environments, which implies a need for the improvement of dynamic range of the sensors along with their resolution and stability. High dynamic range inertial sensors can be used in daily life for monitoring the mechanical impacts and vibrations experienced by the shipped packages while tracking their location until delivery [1]. One extreme application example is the inertial sensors used in munitions that need to provide an accurate readout starting from the high shock launch event until landing [5] for accurate navigation in the absence of a GPS signal.

High-G accelerometers are usually made by utilizing piezoresistive or piezoelectric sensing, due to the simplicity of the fabrication process and readout circuitry of the former and due to the wide operating temperature and frequency range along with the high linearity of the latter approach [6]. However, high-G accelerometers are designed for impact sensing and do not necessarily focus on the minimum detectable acceleration, long-term stability or readout errors due to low-frequency vibrations. Indeed, the constraints on the accelerometer for sensing high-G and low-G accelerations are contradictive. The impulsive nature of high shock events imply high frequency acceleration components to be detected, which sets a lower limit for the resonance frequency of the accelerometer in order to keep the scale factor of the accelerometer constant over the frequency range of interest and prevent the accelerometer signal of interest from getting above the resonance frequency. Increased resonance frequency implies stiffer springs for a given accelerometer mass leading to a smaller amount of displacement for a given acceleration, which creates a trade-off between the bandwidth of the accelerometer and the minimum detectable acceleration. On the other hand, the mass of the accelerometer needs to be decreased in order to keep the stress at the anchors below the material fracture strength when the accelerometer experiences a shock event. Decreased mass for the sensor leads to increased thermal-mechanical

noise, which sets a fundamental noise floor for the minimum detectable acceleration. Furthermore, the efforts to reduce the accelerometer mass inherently lead to reduced accelerometer dimensions, hence smaller sense capacitances that are comparable to parasitic capacitances. These challenges are addressed in this thesis through an arrayed capacitive accelerometer design fabricated in a CMOS-MEMS process, where the thermal-mechanical noise is averaged and reduced over the array and the ratio of sense capacitance to parasitic capacitance is maximized by reducing the parasitic capacitances through the finite-element-analysis based optimization of the routing and taking advantage of on-chip readout circuits thereby eliminating off-chip routing capacitance present in present two-chip capacitive accelerometer implementations.

The mass constraint on a high-G capacitive accelerometer inherently leads to a small accelerometer design with a low mechanical damping. Increasing the ratio of accelerometer mass to damping coefficient helps decreasing the thermal-mechanical noise; however, it simultaneously leads to a relatively high quality factor. The high quality factor results in transient vibrations at the resonance frequency, which translate to an AC signal that gets superposed on the acceleration signal. However, these AC vibrations can be attenuated by low-pass filtering given that they are outside the acceleration signal bandwidth. Reducing the ring-down time for these vibrations can simplify the filter design. This thesis introduces the idea of frequency staggering between the accelerometer cells in the array and theoretically shows that the ring-down time of the accelerometer can be reduced by taking advantage of rapid phase decoherence of the individual cell ringdown signals.

Measurement of low-G accelerations with high resolution is not enough to guarantee accurate readings over long time frames. Long-term scale factor and bias stability of MEMS accelerometers get affected by environmental variations, where the most pronounced effects are

that of temperature [7][8][9] and stress [10] variations. Coefficient of thermal expansion (CTE) and temperature coefficient of Young's modulus (TCE) of the materials are the two sources of temperature based drifts at the accelerometer output. Thermal variations affect the stiffness of the accelerometer springs through the variations in the dimensions of the spring beams due to expansion or contraction and the variations in the Young's modulus of the spring beam material. The changes in the stiffness of the accelerometer springs translate to changes in the resonance frequency of the accelerometer cells, which directly affects the mechanical scale factor of the accelerometer (i.e., the proof mass displacement for a given acceleration is inversely proportional to the square of the resonance frequency). The capacitive gap sizes also get affected from the thermal variations as well as from the compression or tension of the materials due to extrinsic stress, e.g., from die attach and packaging. The changes in the capacitive gaps translate to changes in the sense capacitance, which directly affects the electrical scale factor of the accelerometer (i.e., the voltage output for a given proof mass displacement is set by the capacitive gaps and the sense capacitance). In this thesis, the effects of temperature and stress variations on the scale factor are quantified through finite-element analysis in order to determine the maximum stress and temperature variation that can be tolerated for a given scale factor stability. These simulations inform the design of on-chip Proportional to Absolute Temperature (PTAT) sensors, piezoresistive stress sensors and resonator-oscillators, which are integrated in an on-chip system by taking advantage of the CMOS-MEMS process. The correlation between the accelerometer bias and scale factor with environmental sensor readouts as well as the potential to compensate the accelerometer readout based on environmental sensor outputs is investigated in order to improve the bias stability.

The aging of the transducer also reduces long-term scale factor and bias stability and repeatability. The metal layers in the CMOS process can potentially creep over time when they get

exposed to high stress levels repeatedly (e.g., at the anchors of the accelerometer cells). In order to maximize the stability of the accelerometer cells, the signal routing in the spring beams are made through the polysilicon layer and the spring beams are made out of silicon oxide. However, the metal layers have to be used for defining the structures in the CMOS-MEMS process [11] since they act as etch mask during the oxide etch step. This thesis introduces an aluminum etch step for the removal of the exposed metal layers on the chip after the oxide etch step for potentially improved scale factor and bias stability and repeatability over long time frames.

1.2 Background

1.2.1 Accelerometer Operation and Sensing Principles

An accelerometer with small proof mass displacements can be modeled as a damped harmonic oscillator by using a spring-mass-damper system as shown in Figure 1.1, a good overview of which can be found in [12]. The equation of motion in time domain is:

$$m\frac{\partial^2 x}{\partial t^2}+b\frac{\partial x}{\partial t}+kx=F \tag{1.1}$$

where x is the difference between the displacements of the stator (x_s) and rotor (x_r), m is the mass, b is the linear damping coefficient, k is the linear spring constant and F is the force exerted on the stator due to acceleration assuming no additional actuation or noise sources. Under the assumption of small proof mass displacements, any nonlinearity in damping and spring constant is neglected to simplify the calculations. The frequency response $H(s)$ of the accelerometer can be found as in (1.2) by using Laplace transformation, where $\omega_0=\sqrt{k/m}$ is the resonance frequency, $Q=\omega_0 m/b$ is the quality factor and $A(s)$ is the input acceleration.

$$X(s)=\frac{A(s)}{s^2+s\omega_0/Q+\omega_0^2}=H(s)A(s) \tag{1.2}$$

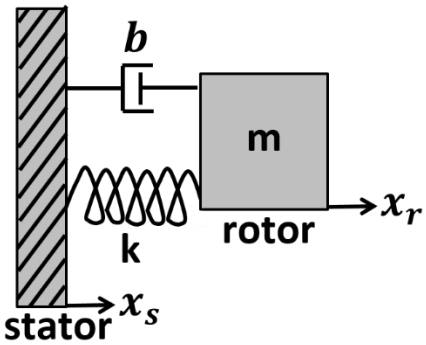


Figure 1.1. Spring-mass-damper model of an accelerometer.

The noise floor of accelerometers is fundamentally set by the thermally induced vibrations of the proof mass, which acts as an external force on the proof mass and is referred to the input of the sensor to find the noise equivalent acceleration density:

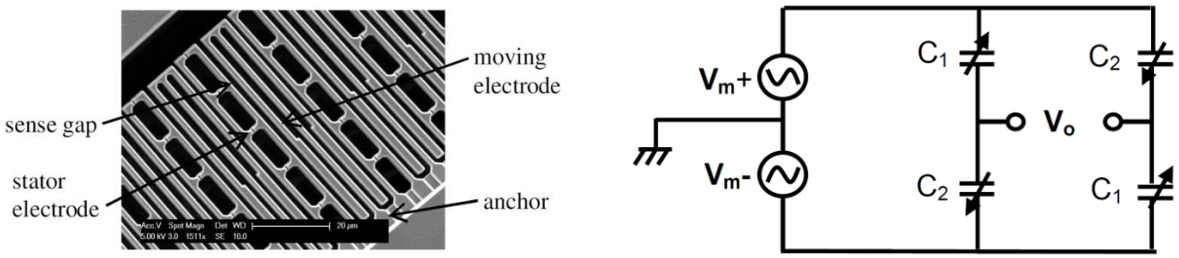
$$a_n = \frac{F_n}{m} = \frac{\sqrt{4k_B T b}}{m} = \sqrt{\frac{4k_B T \omega_0}{mQ}} \tag{1.3}$$

where k_B is the Boltzmann constant, T is the absolute temperature and $F_n = \sqrt{(4k_B T b)}$ is the thermally induced noise force density in units of N/√Hz. Increasing the resonance frequency to capture high frequency vibrations resultant from impacts and decreasing the mass to keep the stress at the anchors below the fracture limit of the material both increase the thermal-mechanical noise floor of the accelerometer in accordance with (1.3), hence limiting the resolution and dynamic range. Multiple accelerometer cells are connected in parallel and the thermal-mechanical noise is statistically averaged across an array of cells in order to improve the signal-to-noise ratio, hence the dynamic range of the accelerometer in this study. The equivalent acceleration density for N cells is given as:

$$a_n = \sqrt{\frac{4k_B T \omega_0}{mQN}} \tag{1.4}$$

Accelerometers do not directly measure the acceleration. Instead, the relative displacement of the proof-mass with respect to the accelerometer frame (x) is measured and the corresponding acceleration is calculated based on the transfer function of the sensor as given by (1.2). Almost all sensing mechanisms (i.e., capacitive, piezoresistive, piezoelectric, thermal, optical, electromagnetic, tunneling) have been employed in various accelerometer designs; however, the most widely used approaches are thermal, piezoelectric, piezoresistive and capacitive sensing schemes, which are also the sensing methods adopted by the industry. Examples of accelerometer designs utilizing different sensing methods along with the advantages and disadvantages of using these methods are explained in the rest of this section.

The most commonly used sensing principle for accelerometers is capacitive sensing. Figure 1.2 shows an example capacitive accelerometer design [13], which also forms the basis of the accelerometer design used in this thesis. All capacitive accelerometers rely on a sense capacitance formed between the rotor (i.e., the proof-mass) and stator electrodes, which varies as the proof-mass is displaced by the acceleration. The varying capacitor is connected in series with either a reference capacitor or another differentially varying capacitor in order to generate a voltage or current signal proportional to the change in capacitance, which is then sensed by using continuous-time voltage or transimpedance amplifiers or switched-capacitor circuits [14]. In the below example [13], the varying capacitors are connected to form a differential capacitive bridge (Figure 1.2(b)) and the output signal is sensed by using a voltage amplifier. Capacitive accelerometers have simple structures and low temperature sensitivity; however, the high impedance output node of the capacitive bridge increases the sensitivity of the readout to parasitic capacitances and electro-magnetic-interference (EMI) [14].



(a) (b)

Figure 1.2. (a) An example capacitive accelerometer and (b) the corresponding capacitive bridge model. The images are reprinted from [13] (Copyright © 2008, IEEE).

Early work shows that surface micromachined capacitive accelerometers can be monolithically integrated with CMOS readout circuits and the thermal-mechanical noise of the structure can be reduced below 1 μG/√Hz [15]. Initial designs demonstrate the possibility of micro-gravity measurements (< 1 μG) [16] and low-G measurements (< 1 mG) [17] by using capacitive sensing schemes. Today, it is also proven that high-G measurements [13] including shock tests (> 10 kG) [18] are possible by using capacitive accelerometer designs.

Piezoresistive sensing is another highly adopted sensing mechanism that competes with capacitive sensing [19]. In semiconductors, the strain dependent change in resistivity due to piezoresistive effect is about 50 times larger than the change in resistivity due to geometrical effects [20]. The piezoresistance coefficients of silicon and the dependence of these coefficients on crystallographic orientations, impurity concentrations and temperature are particularly well-characterized [20][21][22] given that it is the most common substrate in CMOS and MEMS processes. Aside from the fabrication simplicity, the most important advantage of piezoresistive sensing is the simplified readout circuitry. An example design in [23] connects two piezoresistors with two fixed resistors in order to form a full Wheatstone bridge. Using a Wheatstone bridge configuration allows the sense signal to be directly probed or easily amplified and filtered. On the

other hand, piezoresistors are highly sensitive to temperature. The temperature effects can be cancelled by using identical resistor designs fabricated in the same process and connected in a Wheatstone bridge configuration. Any remaining repeatable errors can be further corrected with electronics; however, non-repeatable errors over multiple temperature cycles still sets the fundamental limit for accuracy of these sensors [19].

Besides the thermal sensitivity of piezoresistors, the 1/f noise in the resistors [24][25] sets a fundamental limit on the stability of the static and low frequency measurements. Although there are some low-G piezoresistive accelerometer examples in literature [26][27], piezoresistive sensing is mostly utilized in high-G accelerometers [28][29] that are used in weaponry or shock testing. The resonance frequency of the mechanical structure, hence the measurement bandwidth is kept high in these accelerometers at the expense of reduced sensitivity [30].

Piezoelectric sensing is based on the direct piezoelectric effect where the electric polarization of the piezoelectric material changes as a result of mechanical deformation leading to charge accumulation on opposite sides of the material [31]. A good review of fabrication methods for piezoelectric sensors and applications can be found in [32]. Various piezoelectric materials have been utilized in accelerometer designs including polyvinylidene fluoride (PVDF) [33], zinc oxide (ZnO) [34], lead zirconate titanate (PZT) [35] and aluminum nitride (AlN) [36]. The typical structure of a piezoelectric sensor (or actuator) can be found in [37], where the piezoelectric material is sandwiched between two electrodes such that the mechanical deformation of the plates would lead to a sensible charge difference between the plates proportional to the amount of deformation.

Besides the self-generating nature of piezoelectric accelerometers that eliminate the need for an external power source for the transducer, they can operate over a wide frequency and

temperature range with high durability [38]. However, any piezoelectric sensor acts as a source capacitor with finite resistance that leads to an inherent high-pass filtering on the signal [38]. Therefore, piezoelectric accelerometers are not suitable for static and low frequency measurements or applications where the acceleration data needs to be integrated. The most common application of piezoelectric accelerometers is monitoring vibration on machines and structures [31]. They can also be utilized for shock testing [39], albeit with limited bandwidth compared to their piezoresistive counterparts.

Thermal accelerometers work based on convective heat transfer of a tiny heated fluid bubble in a sealed cavity, demonstrated for the first time in 1997 [40]. An example sensor structure can be found in [41], where the sensor is integrated with CMOS on the same chip. Typically, a resistive heater in the central beam heats the fluid (e.g., air) surrounding the beam. The heated fluid bubble in the cavity displaces in response to acceleration as illustrated in [42], which leads to a differential change in the resistances of the resistors in the side-beams. The two sensing resistors are usually connected with two reference resistors on the substrate in Wheatstone bridge configuration [43], which provides a differential output voltage proportional to acceleration. The signal from the Wheatstone bridge can be amplified with a simple instrumentation amplifier, where the flicker noise of the first circuit block becomes critical for the acceleration resolution. The flicker noise limit of the amplifier is overcome by using chopper stabilization or correlated double sampling [44]. Alternatively, a low noise transimpedance amplifier can be used for reading out current from thermopile detectors [45].

The most prominent advantage of thermal accelerometers is avoiding a proof-mass, hence avoiding mechanical ringing and temperature hysteresis [46]. These sensors provide shock tolerance (up to 50 kG) and high bias stability [47], albeit with a bias dependence on temperature

[46]. They also lend themselves to be monolithically integrated with CMOS circuits [48][49]. However, thermal accelerometers have inherently low measurement bandwidth (typically below 100 Hz) which can be increased up to 1 kHz by operating the sensor in a negative thermal feedback loop [50]. Sigma-delta (ΣΔ) modulation can also be employed to push the bandwidth above 100 Hz, such that it is limited by the bandwidth of air convection instead of the thermal inertia of temperature probes [51]. The limited bandwidth of these sensors prevents their usage in high frequency measurements including shock tests. The power requirement for heating the central beam and compensating for the heat leakage through the substrate also makes them unsuitable for battery-powered applications. However, the inherent low-pass filtering on the signal increases their vibration immunity and makes these sensors a good fit for applications like electronic stability control (ESC) [46], predictive drop sensing [52] or tilt detection [53][54].

Optical sensing mechanisms are mostly based on the detection of the variation in the peak wavelength [55] or intensity [56][57] of the light coming out of an optical cavity, which is designed as a Fabry-Perot (FP) cavity [55][56] or a photonic-crystal cavity [57]. A distinct feature of optical sensing is its immunity to electromagnetic interference (EMI), which makes it suitable for use near strong electromagnetic fields (e.g., power transformers) [58]. In optical accelerometer designs, the laser source and optical detector are usually off-chip components coupled to the system through optical fibers. The on-chip integration of all optical components and detection circuits is not currently feasible, preventing the commercial use of this sensing scheme.

Electromagnetic sensing is based on the detection of varying electromagnetic fields upon acceleration. The first electromagnetic accelerometer was demonstrated in 1994 [59], where the mutual coupling between a movable coil on a proof-mass and a stationary coil in parallel is utilized. Driving current through one of the coils induces a voltage across the secondary coil that depends

on the distance between the two coils, hence the acceleration. In a different design [60], the magnetic field is used for providing force feedback to the accelerometer by driving current to the coils on the proof-mass in the presence of fixed permanent magnets surrounding the proof mass. Inductive sensing can also be considered under this category, which can be readily integrated in a CMOS process by routing metal traces to form inductive loops. The variable inductors are formed in the spring beams and connected with capacitors to make on-chip LC-tank oscillators in [61], where the acceleration leads to a differential inductance variation that is observed as resonance frequency shifts detected by a counter after mixing the signals from the differential oscillators. Eddy-current sensing principle also involves the detection of inductance change, which occurs as the distance between planar coils (i.e., inductors) and conductive targets changes upon acceleration. Driving current through the coils generates magnetic fields and induce Eddy currents on the conductive targets, which generates secondary magnetic fields that change the coil inductances. The proposed accelerometer design in [62] places the conductive targets on the proof mass and fixes the planar coils above and below the proof mass. The inductance of top and bottom coils vary differentially as the proof-mass is displaced by acceleration. The proposed detection scheme in the same study forms LC oscillators by using the coil inductances and takes the ratio of oscillation amplitudes after demodulating the signals from the oscillators. The theoretically expected 13 $\mu G/\sqrt{Hz}$ noise floor, 370 Hz bandwidth and ± 4 G input range are comparable to some of the capacitive accelerometers. However, electromagnetic sensing principles are rarely used in practice. To date, no electromagnetic accelerometer is demonstrated to take stable micro-G measurements for navigation applications or survive and measure impacts in high-G tests.

Tunneling accelerometers work based on the variation of tunneling current between a sharp tip and a counter electrode. Direct tunneling is only possible when the gap between the tip and the

electrode is kept on the order of 1 nm, whereas field emission tunneling is observable at larger gaps [63]. Using direct tunneling, 0.1 μG/√Hz noise floor was demonstrated in 10 Hz to 200 Hz frequency band [64]. Later, 22.8 mG acceleration resolution in 50 Hz to 2 kHz frequency band was reported by Yeh and Najafi [65] and 0.5 mG/√Hz acceleration noise floor in 1.25 Hz to 100 Hz frequency range was reported by Dong and coworkers [66]. The sharp tip (e.g., tip area < 0.1 μm^2 in [66]) needed for enhancing the electric field complicates the fabrication process of these accelerometers. The distance between the tip and the counter electrode is maintained by operating the tunneling sensors in a negative electrostatic feedback loop. Although these sensors are shown to provide high acceleration resolution, the variations in the distance between the tip and the counter electrode over long time frames affect the stability of the measurements taken with these sensors, hence making them more suitable for dynamic measurements [67].

1.2.2 Low-G Capacitive MEMS Accelerometers

A good review of operation principles, sensing methods and noise sources in low-G MEMS accelerometers can be found in [68]. Most of the low-G accelerometer designs in literature and in the market utilize capacitive sensing, therefore this section explores different readout methods for capacitive sensing, compares performances of different designs and gives motivations for choosing one or the other.

Open-loop capacitive accelerometers have simple structures; however, the dependence of acceleration signal on the change in sense capacitances arises linearity concerns. The linearity of the acceleration response can be estimated based on the linearity of the capacitance change with proof-mass displacement [69]. The transducer sense capacitances are usually arranged in a capacitive bridge configuration and the capacitance change due to acceleration is translated to a voltage signal at the capacitive bridge output when a continuous-time or a switched-capacitor

voltage amplifier is used for readout. Since the capacitive bridge output nodes have high impedances, keeping a stable DC bias at these nodes becomes crucial for long term stability. Subthreshold transistors are used for biasing the capacitive bridge outputs at the drain potential of the input transistors in [70], where a continuous-time voltage amplifier is used for signal amplification. A more elaborate continuous-time voltage amplifier is presented in [71], where the capacitive bridge outputs are switched-biased at 1/16 of the modulation frequency and additional calibration schemes are used for cancelling the modulated transducer offset signal (i.e., the AC offset) and the DC electronics offset at the amplifier input. Switched-capacitor amplifiers can reduce the impedance at the capacitive bridge outputs by forming a virtual ground with negative feedback loop around the amplifier. They are used in closed-loop accelerometer configurations in most cases; however, they can also be used for signal amplification in an open-loop configuration [72]. As an alternative to voltage amplification, transimpedance amplifiers can be utilized for amplifying the output current of the capacitive bridge. The virtual ground at the input of transimpedance amplifiers also reduce the sense node impedance, hence the effect of parasitic capacitance. Flicker noise of the amplifier becomes crucial for low frequency measurements in all cases; however, it can be alleviated by modulating the acceleration signal and using circuit techniques like chopper stabilization and correlated double sampling [73].

Closed-loop accelerometers operate in an electrostatic force feedback loop, which counteracts the proof-mass movements through electrostatic forces and minimizes the nonlinearity due to sense capacitance change. The force-feedback can be implemented with an analog signal proportional to the acceleration [74][75]. However, the most widely used approach is sigma-delta ($\Sigma\Delta$) modulation which generates a digital feedback signal [76][77]. The $\Sigma\Delta$ modulation technique increases the measurement resolution beyond the limits of the analog-to-digital converter (ADC)

by oversampling the low frequency acceleration signals, hence relaxing the ADC specifications for a given noise floor. On the other hand, the 1-bit quantizer in ΣΔ control loops introduces a nonlinearity and including a high-Q MEMS transducer makes it harder to stabilize the control loop leading to a need for numerical simulation tools [78]. The stability of the voltage source used for force feedback affects the measurement stability in closed-loop accelerometers, which can be improved by using high stability voltage references [77]. The mass residual motion is another source of noise that arises with closed-loop operation and dominates the noise floor at low sampling frequencies [79]; however, it can be minimized by increasing the sampling frequency [15]. A detailed review of ΣΔ modulator architectures used for closed-loop accelerometer and gyroscope applications can be found in [80].

Recently, a charge-balanced accelerometer design was demonstrated as a different type of closed-loop accelerometer [81], where the feedback changes the potential on the stator electrodes symmetrically in order to keep the charge on the rotor constant. Implementing a high loop gain minimizes the charge variation on the rotor, hence reducing the effect of parasitic capacitance on the acceleration signal and leading to improved measurement linearity compared to open-loop readout. As opposed to force-feedback architectures, the purpose of the charge-balanced operation is to prevent any force-feedback on the rotor that can interfere with the operation. The feedback potential applied on the stator electrodes is also interpreted as the acceleration signal.

All capacitive sensing methods discussed so far detect the amplitude change in the signal at the output of the capacitive bridge formed by the transducer. An alternative approach is designing MEMS resonator-oscillators connected to accelerometer proof-mass and detecting the shifts in their resonance frequencies proportional to the acceleration. Typically, two identical resonator-oscillators are placed on opposite sides of the proof-mass such that the proof-mass

displacement compresses the spring beams of one resonator while tensioning the other one, thereby leading to a differential change in the natural resonance frequencies of the resonators [82][83]. The common-mode changes in the resonance frequencies (e.g., due to the temperature effects) are cancelled to first order through differential sensing [84][85]. Unlike the other accelerometer types, resonant accelerometers require more complex vacuum packaging for realizing high-Q oscillators and improving the noise performance [86]. The near-carrier phase noise of the oscillators sets the frequency stability, hence the acceleration resolution of resonant accelerometers. The flicker noise of the front-end circuitry becomes crucial in setting the phase noise of the oscillator [86], therefore a high-gain and low-noise readout circuit is needed for high resolution measurements [87].

The low-G accelerometers are considered in two categories in this section: micro-G accelerometers that have enough resolution to be used for inertial navigation and consumer grade accelerometers that have milli-G resolution for daily use in consumer electronics and automotive applications such as electronic stability control and airbag triggering. Different accelerometer designs are sampled from the market and literature to compare the performance that can be obtained with different readout methods. The selected designs are all based on capacitive sensing as it is the primarily used sensing method for low-G accelerometers that leads to state of the art resolution, low power dissipation and allows for closed-loop operation.

Table 1.1. Comparison of commercial micro-G accelerometers

	Honeywell Q-Flex® QA2000-030	**Colibrys, MS1010**	**Zwahlen, et.al., Colibrys [88]**	**Physical Logic LTD., MAXL-OL-2070**	**Physical Logic LTD., MAXL-CL-3030**
Type	Quartz, Macro-ElectroMech.	MEMS, Open-Loop	MEMS, Sigma-Delta	MEMS, Open-Loop	MEMS, Sigma-Delta
Scale factor	1.2 - 1.46 mA/G	270 mV/G	-	16.5 mV/G	13 mbit/G
Noise floor	< 70 μG-rms (10-500 Hz)	34 μG/√Hz	2 μG/√Hz	< 5 μG/√Hz	< 70 μG/√Hz
Resolution	< 1 μG	5 μG	1 μG	100 μG	50 μG *****5 μG [69]
Bandwidth	> 300 Hz	> 200 Hz	300 Hz	300 Hz	300 Hz
Input range	± 60 G	± 10 G	± 15 G	± 70 G	± 30 G
Dynamic range	155.6 dB	126 dB	143.5 dB	116.9 dB	116 dB *****136 dB [69]
Linearity/VRE	< 20 μG/G^2-rms (50-500 Hz); < 60 μG/G^2-rms (500-2000 Hz)	290 μG/G^2 (50-2000 Hz); 0.3% of full range	< 20 μG/G^2 (50-1000 Hz)	0.3% of full range	0.1% of full range
Power	< 480 mW	7.6 mW	100 mW	< 42.9 mW	< 450 mW
Maximum shock	250 G	1500 G	4000 G	500 G	500 G
Output	Analog	Analog	Digital	Analog	Digital

***** Improvements on resolution and dynamic range of this product are reported in literature [69], although not yet commercially available.

Inertial navigation requires low-noise sensors with high bias stability to provide accurate measurements through the navigation task. Honeywell Q-Flex® QA2000-030 provides better than 1 μG resolution threshold in 300 Hz bandwidth with ± 60 G input range and is used as the navigation standard. InnaLabs AI-Q-2030 is another navigation grade accelerometer made in Europe with the same specifications. These sensors are quartz macro-electromechanical and quartz pendulous accelerometers, respectively, which do not tolerate high shock levels (> 250 G). On the

other hand, MEMS sensors have smaller sizes and can tolerate much higher impacts. Besides, MEMS sensors have low cost due to batch fabrication and lower power dissipation compared to their macro-electromechanical counterparts. The two major companies that develop navigation grade MEMS accelerometers are Colibrys and Physical Logic LTD. The best performing products of these companies along with the recent improvements they reported in literature are compared to the navigation standard Honeywell QA2000-030 accelerometer in Table 1.1.

The open-loop accelerometers have simpler readout circuits and much lower power dissipation compared to the closed-loop designs. However, the open-loop designs are prone to nonlinearities as the capacitive gaps change with acceleration. This leads the companies to develop closed-loop accelerometers to improve the linearity of their sensors at the expense of increased readout complexity and power dissipation. The comparison between Colibrys MS1010 and Honeywell QA2000-030 shows that an open-loop MEMS accelerometer can provide a comparable resolution to a macro-electromechanical sensor in a similar bandwidth with $\sim$ 60 times lower power dissipation and 6 times higher shock tolerance at the expense of reduced linearity, which underlines the potential of open-loop MEMS accelerometers.

Table 1.2. Comparison of micro-G accelerometers in literature

	Pastre, et. al. [89]	**Sonmez, et. al. [90]**	**Amini, et. al. [91]**	**Wang, et. al. [92]**	**Zou, et. al. [93]**
Type	MEMS, Sigma-Delta	MEMS, Sigma-Delta	MEMS, Sigma-Delta	MEMS, Resonant	MEMS, Resonant
Scale factor	21 μG/LSB	-	-	280 Hz/G	9418 Hz/G
Noise floor	1.15 μG/√Hz	6.2 μG/√Hz	> 4 μG/√Hz	1.2 μG/√Hz	144 nG/√Hz
Resolution	19.9 μG-rms	3.2 μG	2 - 8 μG	0.4 μG	1 μG-rms
Bandwidth	300 Hz	250 Hz	500 Hz	< 190 Hz	50 Hz
Input range	± 11 G	± 20 G	-	± 20 G	± 0.05 G
Dynamic range	114.8 dB	136 dB	95 dB	154 dB	94 dB
Linearity/VRE	-	0.3% of full range	-	-	-
Power	12 mW	16.7 mW	4.5 mW	4.37 mW	-
Maximum shock	-	-	-	-	-
Output	Digital	Digital	Digital	Analog/Dig.	Analog

Note: RMS noise is reported for resolution when the bias stability measurements are not available.

The academic research efforts are concentrated on sigma-delta accelerometers and resonant accelerometers to reduce the noise floor and improve the resolution over what has been obtained with open-loop designs in order to meet the stringent navigation requirements. The most successful designs demonstrated so far are compared in Table 1.2. The 0.4 μG bias stability reported in [92] is the state of the art resolution achieved with a MEMS accelerometer. Recently, another resonant accelerometer was reported to achieve 0.16 μG resolution with 427 Hz/G scale factor [94]; however, there is no further characterization results available regarding the other performance parameters of this accelerometer. The maximum shock tolerance and linearity of the micro-G accelerometer designs are secondary concerns that comes after resolution, hence usually not tested and reported in literature.

The repeatability of bias and scale factor of the accelerometers as well as their drift with temperature are also critical for navigation applications, although they are not included in the comparisons. The characterization results for these parameters are provided in the datasheets of the commercial products; however, they are rarely investigated for designs in literature as they can potentially be improved with proper calibration and compensation for any given design.

Table 1.3. Comparison of commercial consumer grade accelerometers

	Analog Devices, ADXL 345	**Bosch Sensortec, BMA 456**	**NXP, MMA1200KEG**	**ST Micro-electronics, H3LIS331 DL**	**TDK, IAM-20381**
Type	MEMS, Open-Loop	MEMS, Open-Loop	MEMS, Open-Loop	MEMS, Open-Loop	MEMS, Open-Loop
Scale factor	4 mG/LSB	0.49 mG/LSB	8 mV/G	49 mG/LSB	0.12 mG/LSB
Noise floor	< 1.1 LSB-rms	120 μG/√Hz	13.7 mG/√Hz	15 mG/√Hz	135 μG/√Hz
Resolution	4 mG	0.49 mG	350 mG-rms (0.1 Hz - 1 kHz)	49 mG	0.12 mG
Bandwidth	< 1600 Hz	< 684 Hz	400 Hz	780 Hz	< 218 Hz
Input range	± 16 G	± 16 G	± 281 G	± 100 G	± 4 G
Dynamic range	72 dB	90.3 dB	> 58 dB	66.2 dB	90.4 dB
Linearity/VRE	0.5% of full range	0.5% of full range	2% of full range	2% of full range	0.25% of full range
Power	< 0.35 mW	< 0.54 mW	< 30 mW	0.75 mW	0.7 mW
Maximum shock	10000 G	10000 G	2000 G	10000 G	10000 G
Output	Digital	Digital	Analog	Digital	Digital

Consumer grade accelerometers are available from various manufacturers with a range of specifications that can fit different applications. Low-cost and low-power operation are important for these sensors to be used in mobile applications, hence taking advantage of the low power dissipation and reduced complexity of open-loop designs. The noise floor of consumer grade

accelerometers vary in 0.1 mG/√Hz to 10 mG/√Hz range, leading to sub-mG to tens of mG resolution. These sensors can survive shocks up to 10 kG; however, they are usually designed to sense accelerations only below 100 G with less than 1 kHz measurement bandwidth. The linearity of these sensors are not as critical as in the navigation applications; however, the nonlinearity is usually kept below 2% of the full range. Table 1.3 provides a comparison of commercially available accelerometers sampled from different manufacturers for different acceleration ranges.

Consumer grade thermal accelerometers are also available from MEMSIC; however, these accelerometers have higher power consumption and significantly lower measurement bandwidth compared to the commercially available capacitive accelerometers (e.g., MXA2500E has 17.3 mW power consumption and 17 Hz bandwidth in 1 G input range). The only advantage of thermal accelerometers is their shock immunity due to operation without a proof-mass as evidenced by the 50 kG shock survivability of MXA2500E.

Table 1.4. Comparison of consumer grade accelerometers in literature

	Luo, et. al. [95]	**Xie, et. al. [96]**	**Li, et. al. [97]**	**Sung, et. al. [98]**	**Langfelder, et. al. [99]**
Type	MEMS, Closed-Loop	MEMS, Open-Loop	MEMS, Open-Loop	MEMS, Resonant	MEMS, Resonant
Scale factor	41 mV/G	0.5 mV/G/V	1 V/G	24.7 Hz/G	240 Hz/G
Noise floor	1 mG/√Hz	6 mG/√Hz	-	-	-
Resolution	17.3 mG-rms	-	0.2 mG	0.7 mG	0.2 mG
Bandwidth	300 Hz	< 9.4 kHz	< 1.3 kHz	60 Hz	100 Hz
Input range	> ± 13 G	> ± 27 G	± 1 G	± 10 G	± 8 G
Dynamic range	> 57.5 dB	-	74 dB	83 dB	92 dB
Linearity/VRE	-	-	0.05% of full range	< 2% of full range	< 2% of full range
Power	-	-	-	-	115 μW
Maximum shock	> 30000 G	-	-	1200 G	-
Output	Analog	Analog	Analog	Analog	Analog

The consumer grade accelerometers in literature are either open-loop designs or resonant accelerometers. The force-feedback accelerometers operating in sigma-delta loops mostly aim for micro-G resolution; however, [95] is a good example of a consumer grade force-feedback accelerometer that reduces the circuit complexity to the level used in open-loop designs by making use of an analog feedback loop. Table 1.4 compares select designs from the literature with consumer grade performance specifications. The bandwidths of the open-loop accelerometers are bounded by their resonance frequencies for comparison; however, the readout circuits and data acquisition method should set the bandwidth in practice. Open-loop accelerometers provide more

freedom in setting the bandwidth compared to force-feedback loops, where the proper operation of the feedback loop in the presence of a high-Q MEMS element can bring additional constraints.

1.2.3 High-G MEMS Accelerometers

Acceleration levels above 100 G can be considered as high-G and such acceleration levels are regularly measured during the crash tests in automotive industry [100]. However, there are applications such as structural destruction, collision or munition tests where acceleration signals well above 10 kG needs to measured, which is above the maximum tolerable shock input for most low-G accelerometers. The specifications of high-G accelerometers are set to measure the impacts generated by pyroshock events, which are described in standards like NASA HDBK-7003 and MIL-STD-810F. Mechanical shock events are explicitly distinguished from pyroshock events in MIL-STD-810F standards in terms of the expected acceleration amplitudes and frequencies. Mechanical shock events are described as smaller impacts (e.g., < 100 G) with frequency components up to 10 kHz and durations below 1 second. On the contrary, pyroshock is generated by an explosive or propellant activated device and can have frequency components in 100 Hz to 1 MHz band, reaching up to 300 kG amplitude in less than 20 ms (the time duration can be as short as 50 μs).

One of the challenges in designing high-G accelerometers is to ensure that the measurement bandwidth is enough to capture the high frequency acceleration components generated by shock events, which implies a high resonance frequency for the transducer. The inverse relationship between the resonance frequency and the scale factor of the transducer makes it harder to sense low acceleration levels and limits the dynamic range; however, this does not become a concern when the only purpose of the accelerometer is to measure impacts. A general rule-of-thumb for setting the resonance frequency of the transducer is to keep it at least five times higher than the

maximum signal frequency to be measured by the device [101]. However, any small excitation at the resonance frequency can lead to substantial oscillations and failure in under-damped systems. Mechanical filters are designed to limit the transferred frequency components to the transducer and electrical filters are added to the signal path to increase the damping in the system transfer function in [101] in order to minimize the ringing upon shock event. The high frequency acceleration components above the bandwidth of the filters are not measured in this case; however, [102] discusses that the measurements above a certain frequency (e.g., > 20 kHz) does not necessarily provide valuable information. Over-range stops can limit the proof-mass movement, thereby preventing the excessive stress at the anchors and increasing the maximum shock input that can be tolerated by the accelerometer [103]. The over-range stops can also be used for damping the oscillations at resonance frequency [104], hence reducing the ringing at the output signal. However, the contact with the over-range stops is also likely to alter the signal fidelity.

A good review on the development of high-G accelerometers, particularly the most commonly used piezoresistive and piezoelectric accelerometer designs, can be found in [6]. The piezoresistive accelerometers are preferred for the simplicity of their structure, fabrication process and readout circuitry. On the other hand, piezoelectric accelerometers are great fits for high-G measurements due to their linear operation over a wide temperature and frequency range. Since most of the commercially available high-G accelerometers and most of the high-G accelerometer designs reported in literature are based on piezoresistive and piezoelectric sensing, this section focuses on comparing the performances of different piezoresistive and piezoelectric high-G accelerometer designs.

Table 1.5. Comparison of commercial piezoresistive high-G accelerometers

	Bruel & Kjaer 4570	**PCB, 3501B1260KG**	**Meggit, 7270A-6K**	**Meggit, 7270A-60K**	**Meggit, 7270A-200K**
Scale factor	4 mV/G	3 μV/G	30 μV/G	3 μV/G	1 μV/G
Noise floor	3.5 mG/√Hz	-	-	-	-
Resolution	150 mG-rms	-	-	-	-
Bandwidth	1.85 kHz	20 kHz	20 kHz	100 kHz	150 kHz
Input range	± 500 G	± 60 kG	± 6 kG	± 60 kG	± 200 kG
Dynamic range	70.4 dB	-	-	-	-
Linearity/VRE	< 1% of full range	< 1% of full range	-	-	-
Power	< 120 mW	-	-	-	-
Maximum shock	10000 G	-	18000 G	180000 G	200000 G
Output	Analog	Analog	Analog	Analog	Analog

Table 1.6. Comparison of commercial piezoelectric high-G accelerometers

	Bruel & Kjaer 4371	**Kistler, 8702B500M5**	**Kistler, 8742A5**	**PCB, 350D02**	**Meggit, 7255A-01**
Scale factor	9.8 pC/G	10 mV/G	1 mV/G	0.1 mV/G	0.1 mV/G
Noise floor	-	-	-	-	-
Resolution	0.24 mG	10 mG-rms	130 mG-rms	0.5 G-rms (1 Hz - 10 kHz)	0.5 G-rms (2 Hz - 10 kHz)
Bandwidth	0.1 Hz - 12.6 kHz	2 Hz - 7 kHz	1 Hz - 10 kHz	4 Hz - 10 kHz	3 Hz - 10 kHz
Input range	$\pm$ 6 kG	$\pm$ 500 G	$\pm$ 5 kG	$\pm$ 50 kG	$\pm$ 50 kG
Dynamic range	148 dB	> 94 dB	> 91.7 dB	> 100 dB	> 100 dB
Linearity/VRE	-	< 1% of full range	1% of full range	< 2.5% of full range	< 3% of full range
Power	-	< 120 mW	< 600 mW	< 600 mW	< 480 mW
Maximum shock	20000 G	5000 G	50000 G	150000 G	300000 G
Output	Analog	Analog	Analog	Analog	Analog

Piezoresistive and piezoelectric accelerometers sampled from major high-G accelerometer manufacturers are compared in Table 1.5 and Table 1.6, respectively. The noise floor and the resolution is not a particular concern for high-G accelerometer designs, hence not reported in some cases. The input ranges of these accelerometers vary from 500 G to 200 kG and bandwidths are usually kept at or above 10 kHz. The high frequency acceleration components become more significant at higher impacts, which is reflected by the increased measurement bandwidth for the devices with higher input range in Meggit 7270A series. MEMS piezoresistive accelerometers provide up to 200 mV full scale output [102], therefore their scale factor is adjusted inversely proportional to their input range as observed by comparing the Meggit 7270A- 6K, 60K and 200K models. A similar reasoning applies to piezoelectric accelerometers, which is seen from the comparison between Kistler 8702B500M5, Kistler 8742A5 and PCB 350D02 models. The

sensitivity of the bias and scale factor to temperature is important for high-G accelerometers as for the low-G accelerometers; however, an additional concern is the shift in these parameters after impact. Piezoresistive accelerometers do not exhibit a shift unless they are damaged, whereas piezoelectric accelerometers are prone to bias shift [101] and deserves more attention during the design. Another important metric for the high-G accelerometers is their linearity, which is usually kept below 3% of the full range.

Table 1.7. Comparison of high-G accelerometers in literature

	Fan, et. al., [105]	**Okojie, et. al. [106]**	**Wang, et. al. [107]**	**Wung, et. al. [108]**	**Andre, et. al. [109]**
Type	MEMS, Piezoresistive	MEMS, Piezoresistive	MEMS, Piezoresistive	MEMS, Piezoresistive	MEMS, Piezoelectric
Scale factor	0.516 μV/G	213 nV/G	1.43 μV/G/5 V	3 μV/Vexc/G	30 pC/G
Noise floor	-	-	-	-	-
Resolution	-	-	-	-	-
Bandwidth	< 573 kHz (designed)	253 kHz (designed)	220 kHz	232.4 kHz (designed)	-
Input range	± 44614 G	± 40 kG	> ± 10 kG	± 3 kG	± 50 kG
Dynamic range	-	-	-	-	-
Linearity/VRE	4.5% of full range	-	9.54% of full range	0.11% of full range	-
Power	-	-	-	-	-
Maximum shock	200000 G (designed)	100000 G (designed)	-	-	-
Output	Analog	Analog	Analog	Analog	Analog

Most of the high-G accelerometer designs in literature use piezoresistive sensing. A comparison of select designs from literature is given in Table 1.7. The table reports the resonance frequencies of the devices as the upper bounds on their bandwidth, which can be limited to lower

values by the readout circuit when needed. Due to difficulties in generating shock events, the designs in the literature are tested up to 50 kG even if they can potentially handle higher accelerations.

1.2.4 Sources of Scale Factor and Bias Drift

The effects of environmental variations and aging on the sensors show up as frequency dependent noise at the output of the sensors. Unlike white noise, frequency dependent noise is correlated and cannot be reduced by averaging the readout signal over longer times [110]. This noise is observed as a drift at the output of the sensor over time. Hermetic packaging of the sensor can eliminate the effects of humidity and pressure variations by fixing the gas content and pressure in the package [111][112]; however, it does not help with the temperature and stress variations. The stress effects can be reduced by tweaking the mechanical design such as using suspensions [10] or stress relaxation mechanisms [113]. The temperature effects can also be reduced by ovenizing the sensor [8][114][115], thereby minimizing the thermal fluctuations. However, the most widely used approach for reducing the effects of stress and temperature variations is sensing these variations, modeling their correlation with the sensor output and compensating the sensor signal in accordance.

Ovenization of the sensor is a simple form of thermal compensation that does not require establishing a correlation between the temperature measurements and the sensor output. Instead, the temperature variations are sensed and the whole chip is heated in a control loop to minimize these variations, which increases power consumption. On the other hand, determining the correlation between the temperature and stress measurements and the sensor signal allows the numerical compensation of the sensor data or the design of closed-loop control systems with higher efficiency. Accelerometer measurements are compensated based on temperature measurements in

[116] by post-processing the measurement data, leading to improved bias stability over an extended time frame. The stress effects are compensated by post-processing the measurements from an ovenized gyroscope and on-chip stress sensors in [117], where a significant improvement is observed in long term stability demonstrating the importance of the stress effects on the sensor output even after minimizing the thermal fluctuations with ovenization.

The scale factor and bias drift of a sensor are related but distinct concepts. The temperature and stress can affect the scale factor of the accelerometer cells designed in this study through the variations in the capacitive gaps and the resonance frequency. The sensitivity of the accelerometer is also dependent on the stress and temperature based variation of the modulation voltage amplitude and the transfer function of the readout circuit, which can be minimized by using a stable modulation voltage source and employing closed-loop circuits. The scale factor variations are observed as variations at the sensor output at a fixed input excitation. On the contrary, the bias of the accelerometer refers to the output signal at zero input excitation. The bias stability of the designed accelerometer can be set by the bias stability of the readout circuit or any asymmetric changes in the modulation voltage amplitudes and capacitive gaps. However, the lateral curl of the spring beams after releasing the accelerometer cells imitates a DC input acceleration and leads to a non-zero acceleration signal at the output, hence preventing the stability measurement of the accelerometer output at truly zero input excitation. Therefore, the stability measurements at zero input acceleration shows the combined effect of bias and scale factor instabilities of the accelerometer design.

The temperature and stress effects on the scale factor of the accelerometer are estimated in this study. On-chip auxiliary sensors are designed for measuring the temperature and stress variations with high enough resolution to reach ~ 1 ppm scale factor stability upon compensation.

Once the correlation between the accelerometer drift and the environmental variations is determined, the subsequent compensation of the output signal should improve the bias and scale factor stability simultaneously.

1.3 Post-CMOS MEMS Fabrication Process

The most common sensing method for MEMS accelerometers is capacitive sensing, where acceleration generates a voltage or current signal at the output of the capacitive bridge formed by the transducer. The amplitude of the acceleration signal decreases as the parasitic capacitance at the capacitive bridge output (e.g., the capacitance from the signal routing to substrate) increases. The effect of any parasitic capacitance at the bridge output is minimized when a transimpedance amplifier or a switched capacitor circuit is used for sensing the acceleration signal, since the impedance of the sense node is reduced by a virtual ground at the input of these circuits. Continuous-time voltage amplifiers do not look attractive since they have a high input impedance and their input transistor capacitance adds to the parasitic capacitance at the capacitive bridge output; however, they provide the best measurement resolution when the parasitic capacitance is kept small [14]. Monolithic integration of the MEMS transducer and readout circuits eliminates the need for chip-to-chip bonding, thereby reducing the length of the signal routing between the transducer and circuits and minimizing the parasitic capacitance. The driving motivation behind the CMOS-MEMS designs is the ability to fabricate the CMOS circuits and MEMS transducers on the same chip, hence placing the front-end circuits very close to the transducer to minimize the parasitic capacitance of the signal line and maximize the scale factor of the transducer.

The standard post-CMOS MEMS processing steps and the process details for the capacitive accelerometer array fabricated in this study are discussed in chapter 3. A wide range of MEMS devices are fabricated by using post-CMOS MEMS processing, including accelerometers [95],

gyroscopes [118], RF resonant demodulators [119], electro-thermally actuated micro-mirrors [120], frequency reconfigurable RF circuits [121][122] with variable MEMS capacitors [123] and micromachined inductors [124], gas chemical sensors [125][126], humidity sensors [127] and implantable stress sensors [128].

Curling in the mechanical structures upon release is a well-known problem in post-CMOS MEMS processes. The stress built in the metal-dielectric beams leads to vertical stress gradients and curling, which reduces the fidelity of the fabricated structures and degrades the device performance. In addition, the finite lithography precision causes misalignments between different metal layers used in the beams and leads to lateral stress gradients and curling. Vertical curling can reduce the sense capacitances in a capacitive MEMS accelerometer, whereas lateral curling creates a differential change in sense capacitances, hence an offset signal at the capacitive bridge output. The effects of vertical curl on device performance can be minimized by using curl matching techniques (e.g., designing a curl match frame [129][130]). The amount of lateral curl can be reduced significantly by using a tapered beam design, where the higher level metal layers are made narrower to minimize the lateral stress gradients present in the beams after post-CMOS MEMS processing [130].

The other well-known problem in CMOS-MEMS devices is the charging in oxide during operation [131]. The trapped charges in the oxide change the effective potential on the MEMS structures. This problem is not specific to CMOS-MEMS devices and has already been investigated for capacitive RF MEMS switches, where different models were developed to explain the charge trapping [132][133]. The charging effects are also clearly observed as resonance frequency drift in MEMS resonators [134][135]. A Frenkel-Poole emission based model is proposed for the dielectric charging in CMOS-MEMS resonators [136]. The metal-dielectric

composition of the CMOS-MEMS structures along with the thin polymer layer deposited on the sidewalls during the etch steps inevitably arise the charging problem in CMOS-MEMS devices. Model based compensation of the charging effects on device performance and the potential improvements in fabrication steps to minimize charging effects are active research topics with a great potential to improve the performance of various CMOS-MEMS devices.

1.4 Thesis Contributions

Today, there is no accelerometer that can be used for navigation through high-shock environments. Micro-G accelerometers (e.g., the navigation standard Honeywell Q-Flex® QA2000-030) are designed to minimize the noise floor and maximize the long term readout stability. The maximum input range of navigation grade accelerometers is usually below 100 G. On the contrary, high-G accelerometer designs (e.g., Endevco 7255A-01 Isotron ®) concentrate on obtaining linear and repeatable shock measurements. The acceleration resolution of high-G accelerometers is usually not reported as it is not a primary concern for the target applications. Figure 1.3 compares the acceleration range covered by different accelerometer models and the acceleration range aimed by the design in this study.

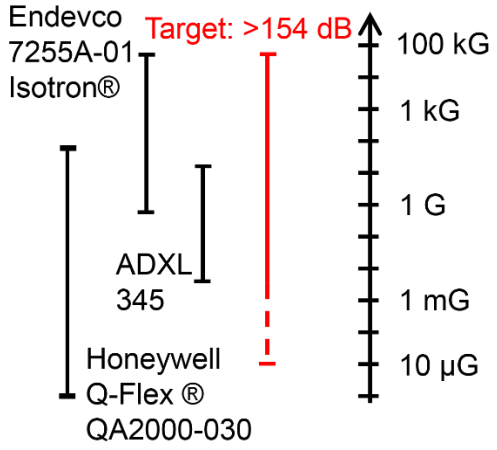


Figure 1.3. Acceleration range covered by different accelerometer models.

This thesis investigates the design trade-offs of high dynamic range accelerometers and the resultant challenges in fabrication and testing. The accelerometer design is considered in conjunction with on-chip readout circuits (for improved sensitivity) and auxiliary environmental sensors (for improved stability) in order to optimize the system level performance. The monolithic integration of the capacitive accelerometer array, the readout circuits and the auxiliary sensors (i.e., PTAT temperature sensors, piezoresistive stress sensors and resonator-oscillators) in the CMOS-MEMS process leads to a high dynamic range accelerometer system-on-chip. The performance of the individual system components as well as the performance of the full system are evaluated in order to verify the model predictions and understand the sources of any deviations.

Simulation based design of the high dynamic range CMOS-MEMS capacitive accelerometer array is explained, post-CMOS MEMS processing steps are discussed and experimental results are presented in milli-G to kilo-G acceleration range. The temperature and stress effects on the scale factor stability of the transducer are estimated through finite-element analysis. PTAT temperature sensors, piezoresistive stress sensors and resonator-oscillators are designed to sense the temperature and stress variations with enough resolution to compensate the accelerometer scale factor stability up to ~1 ppm. The designed auxiliary sensors are used for demonstrating the correlation between the environmental variations and the accelerometer drift. The bias stability of the accelerometer system is improved by compensating the accelerometer readout based on the auxiliary sensor measurements. Ultimately, a design and testing methodology is established for the high-dynamic range accelerometer system with a capacitive accelerometer array and on-chip environmental sensors.

The particular contributions of this thesis are as follows:

- A low noise, high resonance frequency CMOS-MEMS capacitive accelerometer array is designed for sensing accelerations over a wide dynamic range including shock pulses.
    - Finite-element analysis is utilized for accurately extracting the capacitances of a released accelerometer cell and signal routings. The extracted sense and parasitic capacitances are used for estimating the scale factor of the transducer. The parasitic capacitance is minimized to improve the transducer scale factor, hence maximizing the acceleration resolution for a given noise floor. The coupling capacitance from the modulation signal to the readout is minimized to prevent the readout circuit from saturating due to modulation signal feedthrough and reduce the contribution of the modulation voltage source to the accelerometer noise floor.
    - Finite-element analysis is also used for estimating the displacement profile and the stress at the anchors at target maximum acceleration (i.e., 50 kG) in order to ensure shock survivability.
    - The noise contributions of readout circuit components and modulation voltage sources to the accelerometer noise floor are analyzed in order to determine the expected accelerometer bias stability.
- Frequency staggering between the accelerometer cells in the array is proposed as a method of reducing the ringing upon shock events, albeit not experimentally verified.
    - The built-in random variations in the spring beam widths is investigated through scanning electron microscope (SEM) images.
    - A figure of merit is defined to capture the tradeoff between the ring-down time and the transducer scale factor, and used to compare different array designs.

    - The theoretical improvement in ring-down time is demonstrated by designing an example array with 312 accelerometer cells and simulating the transient response to shock events in Simulink® (The MathWorks, Inc., Natick, MA).
- The accelerometer system is taped-out in a 0.18 μm CMOS process and post-CMOS MEMS processing steps are optimized for the realization of the devices.
    - The oxide etch time is minimized for reduced milling on the top metal and reduced polymer deposition on the sidewalls.
    - An aluminum etch process is developed for removing the top metal on the accelerometer cells in order to eliminate possible bias instabilities arising from metal creep on the spring beams and in order improve the transducer scale factor by reducing the parasitic capacitance of the signal routing.
- The noise contributions of testbed components, modulation voltage source, environmental variations and dielectric charging are experimentally investigated to understand the sources of accelerometer bias drift and identify the possible improvements to reach the ultimate bias stability.
- A split Hopkinson bar test setup and a custom designed fixture are utilized for inducing shock pulses on the testbed in order to test high-G performance and understand the consequences of shock events on the die attach, wire bonds and soldered testbed components as well as the accelerometer cells.
- On-chip environmental sensors are designed for ~1 ppm target scale factor stability. The correlation between the sensor measurements and the accelerometer drift is investigated.
    - Finite-element analysis is used for extracting the effect of capacitive gap variations on the sense capacitances and the effect of temperature variations on the resonance

frequency of the accelerometer cells. The temperature and stress dependent changes in the capacitive gaps are also extracted through finite-element analysis. The variations in the sense capacitances and the resonance frequency of the accelerometer cells are translated to scale factor variations. The auxiliary sensors are designed to provide enough resolution to reach ~1 ppm scale factor stability once the accelerometer readout is compensated for the temperature and stress variations.

  - PTAT temperature sensors and piezoresistive stress sensors are designed in the CMOS process. The sensitivities and noise floors of these sensors are experimentally verified to match the model predictions closely.
  - Resonator-oscillators are designed with a similar structure to accelerometer cells for tracking the resonance frequency variations of the accelerometer directly, assuming the resonance frequencies of the two structures are affected from the environmental variations similarly. The resonator-oscillators exhibit frequency drift due to dielectric charging and require a long wait-time before stable operation. However, they are useful for investigating the effects of post-processing steps on the dielectric charging.
  - The correlation between the environmental variations and the accelerometer drift is demonstrated through least-squares fitting of the PTAT and piezoresistive stress sensor measurements on the accelerometer readout.

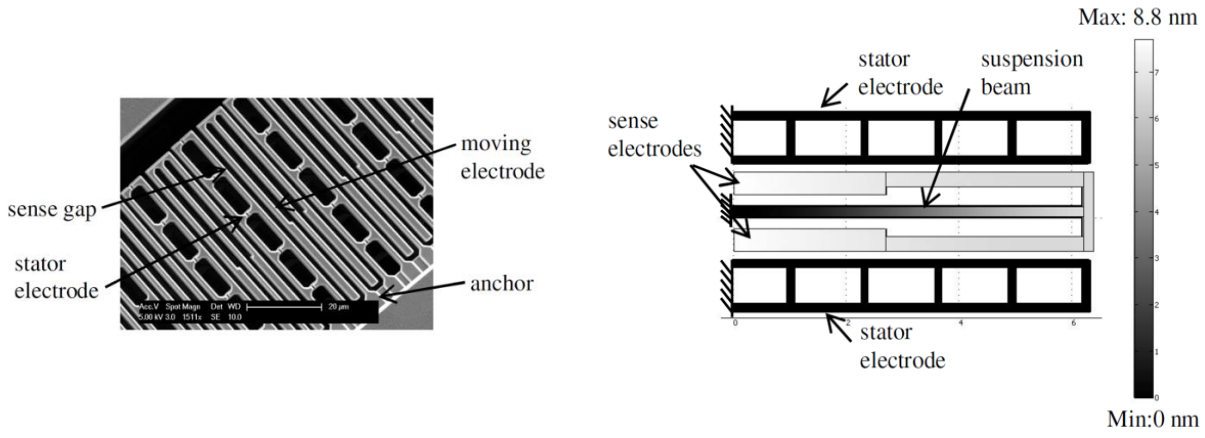
- The bias stability of the accelerometer array is improved over long time frames by compensating the accelerometer readout for temperature and stress variations based on the PTAT and piezoresistive stress sensor measurements.

- Comparison of experimentally measured performance of system components with the model predictions validates the understanding of the physics and design of the packaged accelerometer system.

CHAPTER 2: DESIGN AND ANALYSIS OF THE CAPACITIVE ACCELEROMETER ARRAY

2.1 Mechanical Design of the Accelerometer Cell

The designed high dynamic range CMOS-MEMS capacitive accelerometer array improves on a previous open-loop high-G accelerometer design [13]. The previous design (Figure 2.1) has a smaller area per accelerometer cell, which creates constraints on the cell design. Finite-element analysis is used to maximize the uniformity of displacement in the sense direction to improve linearity; however, the small area restricts the degrees of freedom for adjusting the mass to obtain guided-end displacement for the spring beam. In addition, the narrow folded beams cannot be treated as a rigid mass. The stators are designed as electrodes connected to each other with rigid beams for higher stiffness in the sense direction. Although the design minimizes the stator area, different designs of the rotor and stators imply different amounts of vertical curl after release. The vertical curl mismatch can reduce the sensitivity and increase the bias drift as discussed in section 0, which are both critical for maximizing the dynamic range. The simulated displacement of the accelerometer cell at 1 kG is around 8.8 nm (Figure 2.1 (b)) which implies 880 nm displacement at 100 kG target maximum input acceleration of the design. Higher displacement per input acceleration (i.e., higher compliance for the spring beams) is desirable for pushing the lower end of the dynamic range and making the sensor useful for low-G (or micro-G) applications.



(a) (b)

Figure 2.1. Prior work on high-G CMOS-MEMS capacitive accelerometer array. (a) SEM of the released accelerometer cell. (b) Simulated displacement at 1 kG input acceleration. The images are reprinted from [13] (Copyright © 2008, IEEE).

The accelerometer design in this study aims for a high-G sensor with high measurement resolution and stability for navigation under harsh environmental conditions. The first four metal-dielectric bi-layers of a 0.18 µm CMOS process (TowerJazz, Newport Beach, CA) are used in the design. The proof mass of the accelerometer cell comprises a folded metal-oxide cantilever (Figure 2.2) with higher stiffness compared to the prior high-G accelerometer design. The mass distribution is adjusted to create guided-end displacement for the spring beams and parallel-plate motion for the electrodes. Similar rotor and stator designs improve curl matching as detailed in section 0. In design, increasing mass of the accelerometer cell lowers the thermomechanical noise while under constraints on the deflection of the cell and the stress at the anchors to ensure high-G survivability. High resonance frequency of the accelerometer cells (i.e., 118 kHz) provides enough bandwidth to capture high frequency acceleration components induced by shock events. The two spring beams in parallel increase the torsional stability of the rotor and stators. Rigid interconnects between the stator springs minimize stator deflection upon impact. The exact design of the accelerometer cell is covered in this section. Finite-element analysis informs the resonance

frequency, maximum displacement at the target maximum input acceleration (i.e., 50 kG) and the corresponding stress at the anchors. Analytical calculations estimate the damping and thermomechanical noise floor of the accelerometer cells.

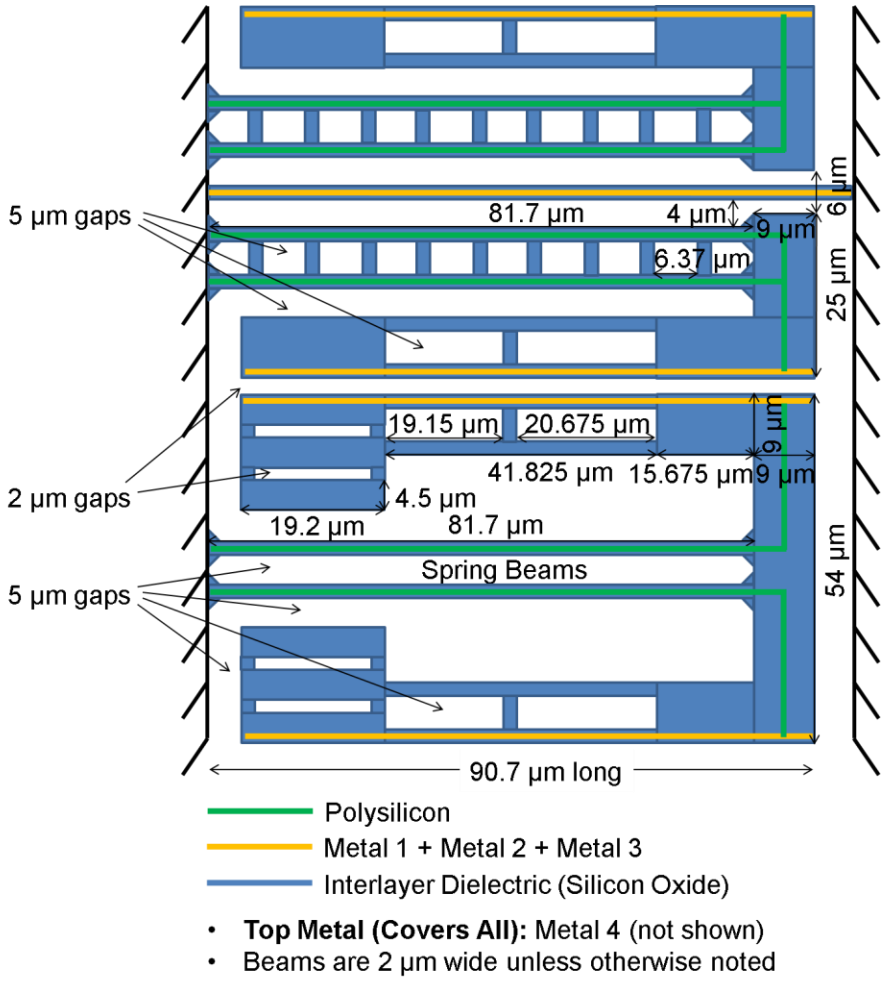


Figure 2.2. Cartoon drawing of the accelerometer cell design.

2.1.1 Bandwidth and Input Range

The bandwidth of the accelerometer is fundamentally set by the resonance frequency of the accelerometer cells. Measurement of acceleration components in a 20 kHz band is enough to obtain meaningful information regarding the shock response of the structure on which the accelerometer is attached [102]. Setting the measurement bandwidth of the accelerometer as 20 kHz requires the

resonance frequency of the accelerometer cells to be above 100 kHz (i.e., at least five times higher than the maximum signal frequency to be measured by the device) [101].

The spring constant for the guided-end motion of the two parallel spring beams is calculated as:

$$k=2E_{ox}h_s\frac{w_s^3}{l_s^3} \tag{2.1}$$

where h_s, w_s and l_s are the height, width and length of a single beam, respectively. The Young's modulus of oxide (E_{ox}) is taken as 70 GPa [137] and the spring constant is calculated as 10.15 N/m. The resonance frequency depends on the mass that moves during resonant motion. The displacement of the spring mass close to the anchors of the spring beams is negligible, thereby the mass closer to the anchors is expected to have less effect on the resonance frequency compared to the mass at the guided-end of the beams. The displacement of different points across the spring beams is determined by the mode shape, thereby the effective mass of the spring beams depends on the mode shape. Rayleigh-Ritz method [138] can be used when calculating the effective mass of the spring beams in accordance with the mode shape. This method equates the maximum kinetic energy and the maximum potential energy of a spring beam at resonance, which is valid when the accelerometer is modeled as a linear second-order spring-mass-damper system. Assuming sinusoidal time-domain motion for the spring beams, the kinetic energy (K) for a spring beam can be written as:

$$K=\int_0^{l_s}\frac{1}{2}m_l v_y(x)^2\mathrm{d}x=\int_0^{l_s}\frac{1}{2}m_l\left(\frac{\partial(y(x)\cos(\omega_0 t))}{\partial t}\right)^2\mathrm{d}x=\int_0^{l_s}\frac{1}{2}m_l\omega_0^2\,y(x)^2\cos(\omega_0 t)^2\,\mathrm{d}x \tag{2.2}$$

where m_l is the mass of the spring beam per unit length, $v_y(x)$ is the velocity of the spring beam as a function of position through the length of the spring beam (assuming the spring beam lies along

the x direction as in Figure 2.2), *y(x)* is the mode shape in spatial domain (assuming displacement in y direction) and ω_0 is the resonance frequency. The potential energy (*P*) can be written as:

$$P = \frac{1}{2} k_y \, y(x)^2 \tag{2.3}$$

where k_y is the spring constant in the direction of displacement (i.e., y direction). The maximum kinetic energy is calculated when the sinusoidal term is maximized (i.e., when it is unity) and the maximum potential energy is calculated where the displacement is maximum (i.e., at the guided end of the spring beams). The maximum kinetic energy and the maximum potential energy for a spring beam are equated as:

$$\int_0^{l_s} \frac{1}{2} m_l \omega_0^2 \, y(x)^2 \mathrm{d}x = \frac{1}{2} k_y \, y(l_s)^2 \tag{2.4}$$

Resonance frequency is calculated as:

$$\omega_0 = \sqrt{\frac{k}{m}} \tag{2.5}$$

as discussed in section 1.2.1. Substituting *k* with k_y from (2.4) and *m* with m_{eff}, and equating the resonance frequency in the two equations, the effective mass of the spring beam can be calculated as:

$$m_{eff} = \frac{\int_0^{l_s} m_l \, y(x)^2 \mathrm{d}x}{y(l_s)^2} \tag{2.6}$$

For guided-end motion, the mode shape of a cantilever beam is given as [139]:

$$y(x) = \cosh\left(\frac{\lambda_i x}{l_s}\right) - \cos\left(\frac{\lambda_i x}{l_s}\right) - \sigma_i \left(\sinh\left(\frac{\lambda_i x}{l_s}\right) - \sin\left(\frac{\lambda_i x}{l_s}\right) \right) \tag{2.7}$$

where λ_i and σ_i are coefficients that depend on the mode number (i), which are 2.365 and 0.9825 respectively for the first mode of a guided-end beam. Taking the integral in (2.6) by substituting the mode shape gives:

$$m_{eff} = 0.3965 m_l l_s = 0.3965 \rho_{ox} w_s h_s l_s \tag{2.8}$$

The density of oxide (ρ_{ox}) is taken as 2200 kg/m^3 [140] in the mass calculation. The effective mass of the two spring beams is added to the mass of the remaining cell and the total mass (m) of the accelerometer cell is calculated as 19×10^{-12} kg. The resonance frequency is estimated by using the calculated spring constant and effective mass:

$$f_0 = \frac{\sqrt{\frac{k}{m_{eff}}}}{2\pi} \tag{2.9}$$

The calculated resonance frequency (116.2 kHz) matches well with the simulated resonance frequency (118 kHz) of the accelerometer cells (Figure 2.3). The high resonance frequency of the designed accelerometer cells allows sensing the high frequency (e.g., > 20 kHz) components of the shock pulses.

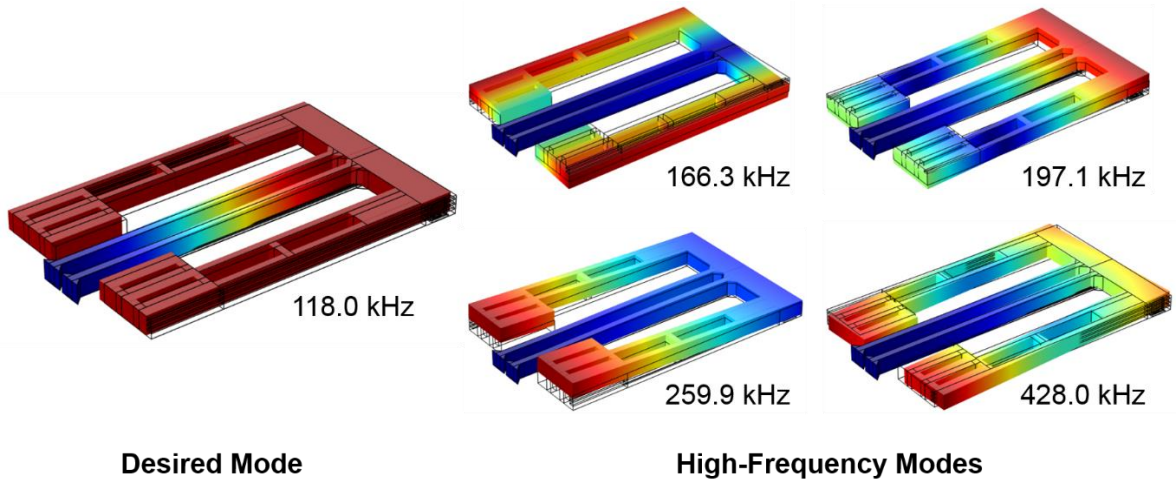


Figure 2.3. High-frequency modes of the designed accelerometer cell.

The small accelerometer cell design helps ensure that the desired mode shape is obtained for the fundamental mode of oscillation. Figure 2.3 shows the mode shape at 118 kHz resonance frequency and the next four modes of oscillation at higher frequencies. The rocking motion of the proof mass leads to the second mode of oscillation at 166.3 kHz resonance frequency. The third mode of oscillation is observed at 197.1 kHz resonance frequency, which is set by the stiffness of the spring beams in the vertical direction. The following higher frequency oscillations are seen at 259.9 kHz and 428 kHz resonance frequencies due to the out-of-plane and in-plane motion of the folded cantilevers, respectively. The oscillations at 428 kHz result in a differential change in sense capacitances, thereby it is important to keep this mode well separated from the fundamental mode of oscillation and minimize its effect on the acceleration measurements.

The input range of the accelerometer is fundamentally set by the survivability of the accelerometer cells, which can be ensured by designing to mitigate the stress at the anchors at a given level of impact. The stress at the anchors is dependent on the anchor area and the force applied on the spring beams upon acceleration. Assuming a fixed anchor area, the shock survivability of the accelerometer cells can be improved by reducing the force (F) generated on the spring beams for a given input acceleration (a), which is directly proportional to the mass (m) of the accelerometer cells (i.e., $F = m \times a$). Reducing the mass increases the thermal-mechanical noise of the accelerometer cells; however, the signal to noise ratio of the accelerometer array can be preserved by increasing the number of cells and statistically averaging the signal from multiple cells running in parallel in the array. Once the thermal-mechanical noise is suppressed, the remaining noise sources in the system (e.g., readout circuit noise, modulation voltage noise or correlated dielectric charging noise) sets the noise floor and resolution. When the proof-mass displacement at maximum input acceleration is fixed, the corresponding proof-mass displacement

at the target minimum input acceleration decreases as the lower end of the input range is pushed for higher performance. This implies that increasing the target maximum input acceleration will increase the minimum detectable input acceleration by the same amount, hence leading to the same dynamic range unless the noise floor is decreased. The potential noise sources are further discussed in the following sections.

The linearity of the accelerometer response over the input range is critical for the accuracy of the collected data (unless nonlinearity is calibrated for each device and compensated in the readout). In capacitive sensing methods, the linearity of the change in sense capacitance with proof-mass displacement can significantly affect the linearity of the accelerometer response. In the designed accelerometer, weighting at the ends of the folded beams of the rotor create a balanced moment acting on the central pair of spring beams to induce guided-end deflection resulting in parallel-plate motional capacitance. An ideal parallel-plate capacitance results in improved linearity since differential sense capacitances are connected in a capacitive divider relation, thereby canceling the parallel-plate nonlinearity when parasitic capacitance in neglected. The linearity of the response is extracted from finite element analysis in the following sections when the scale factor of the accelerometer is calculated. As mentioned earlier, the effect of the residual nonlinearity can be further reduced by calibration and compensation.

The guided-end displacement of the rotor and the maximum von-Mises stress exerted at the anchors are simulated in COMSOL® (COMSOL, Inc., Burlington, MA) by applying a boundary load on the structure. The target maximum measurable input acceleration is set as 50 kG, corresponding to a 0.94 μm displacement within the 2 μm capacitive gap (Figure 2.4) that handles the transient oscillations safely. The survivability of the accelerometer cells is ensured by constraining the von-Mises stress at the anchors at 50 kG acceleration. The fracture strength of

oxide is reported as 810 MPa in [141], which is measured on a 1 μm thick PECVD oxide film. The small mass of the accelerometer cells keeps the von-Mises stress at the anchors (Figure 2.5) an order of magnitude below the reported fracture strength.

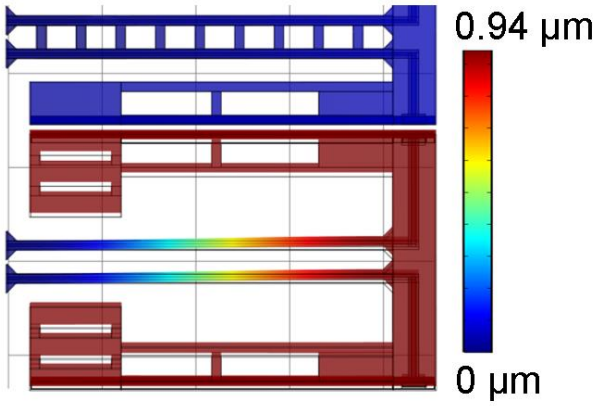


Figure 2.4. Finite-element analysis of displacement of the accelerometer cell under 50 kG acceleration.

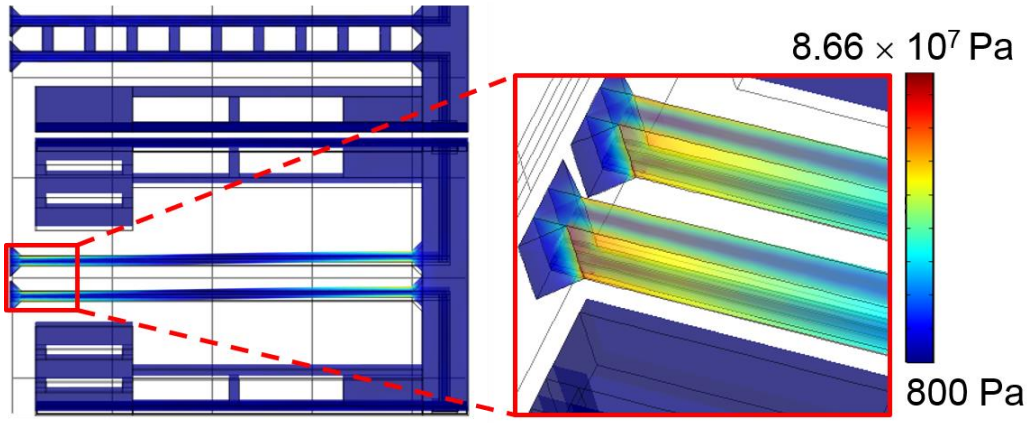


Figure 2.5. Finite-element analysis of von-Mises stress at the flexure anchors under 50 kG acceleration.

2.1.2 Damping and Thermal-Mechanical Noise Floor

The acceleration noise floor is fundamentally set by the thermal-mechanical noise of the proof mass and can be minimized by either maximizing the mass or minimizing the damping of the accelerometer array based on (1.3). The accelerometer array is operated in ambient conditions,

therefore the dominant damping mechanism is viscous air damping. The total damping (b) is estimated as 4.81×10^{-8} kg/s with 79.4% contribution from squeezed film damping and 20.6% contribution from Stokes damping. A detailed discussion of viscous air damping can be found in [142].

Squeezed-film damping (b_{sq}) is caused by the movement of two parallel plates normal to each other such that the air pressure between them changes. When the plates get close to each other, the pressure between the plates greatly increases and the gas is squeezed out from the gap. When the plates move away from each other, the pressure between the plates drop and the surrounding gas flows towards the gap. The viscous drag of the air moving in and out of the gap (g_0) creates damping on the proof mass, which is estimated as:

$$b_{sq} = \frac{\eta_{air} L \left(\frac{h}{g_0}\right)^3}{1+6K_p} \tag{2.10}$$

where η_{air} is the viscosity of air, L is the length of the parallel plates and h is the height of the plates. This equation assumes that the length of the parallel plates is much larger than their height such that the air flow during proof mass oscillation is mainly in the vertical direction. The correction factor at the denominator (i.e., $1 + 6 \times K_n$) is based on the Knudsen number (K_n) [143] and accounts for any slip-flow on the plate surfaces. The Knudsen number is defined as the ratio of the mean free path of the gas molecules (λ_{air}) to the gap between the plates (g_0),

$$K_p = \frac{\lambda_{air}}{g_0} \tag{2.11}$$

and calculated as 0.035 in our design in air. The squeezed-film damping for an accelerometer cell is calculated as 3.82×10^{-8} kg/s including the damping from the capacitive gaps on both sides.

Stokes damping (b_{st}) and Couette damping (b_c) are slide-film damping mechanisms. The moving proof-mass displaces the air above and below its surface, which leads to drag force on the proof mass and damping. The velocity of the moving air decays as the distance from the proof-mass increases. The distance at which the velocity of air decays by a factor of 1/*e* (i.e., 0.368) is defined as penetration depth (δ). The penetration depth is dependent on the oscillation frequency (ω) and is calculated as:

$$\delta = \sqrt{\frac{2\eta_{air}}{\rho_{air}\omega}} \tag{2.12}$$

where ρ_{air} is the density of air. When the distance of the nearest plate to the proof mass is much smaller than the penetration depth, Couette damping becomes the dominant slide-film damping mechanism and the gap between the proof mass and the nearest plate (i.e., usually the substrate) is used for damping calculations. When there is no nearby plate that can affect the air flow such that the penetration depth is smaller than the distance to the nearest plate, Stokes damping becomes the dominant slide-film damping mechanism and the penetration depth is used for damping calculations.

Couette damping (b_c) arises from the air flow between the accelerometer proof mass and a nearby plate, which can be the substrate. It is approximately estimated as:

$$b_c = \eta_{air}\frac{A}{d} \tag{2.13}$$

where *A* is the bottom surface area of the accelerometer cell and *d* is the distance between the proof mass and the substrate. The estimation is based on the Navier-Stokes equation under the assumptions that the air flow is steady and incompressible, the pressure gradient is zero and the distance between the proof mass and the substrate is much smaller than the proof mass width. The

last assumption implies a linear velocity profile between the proof mass and the substrate. However, this assumption is not right for the accelerometer cell as the expected distance between the proof mass and the substrate (i.e., 75 μm) is larger than the width of the accelerometer cell (i.e., 54 μm).

Stokes damping (b_{st}) results from the air movement above and below the accelerometer proof mass. Since there is no nearby plate that can limit the air flow above and below the proof mass, the penetration depth is used for estimating the damping:

$$b_{st}=2\eta_{air}\frac{A}{\delta} \tag{2.14}$$

where A is the top or bottom surface area of the accelerometer cell. The maximum oscillation frequency is taken as the resonance frequency of the accelerometer cell (i.e., 118 kHz) and the minimum penetration depth is calculated as 6.3 μm, which sets an upper bound for the Stokes damping contribution to the overall damping. The maximum expected Stokes damping on an accelerometer cell is estimated as 9.90×10^{-9} kg/s when the proof mass oscillates at resonance frequency.

The quality factor of the accelerometer cell is calculated as 293 by using the estimated mass of an accelerometer cell (i.e., 19×10^{-12} kg) and the simulated resonance frequency (i.e., $\omega_0=741.4$ rad/s):

$$Q=\frac{\omega_0(b_{sq}+b_{st})}{m} \tag{2.15}$$

The calculated quality factor and mass translate to 0.15 mG/√Hz thermomechanical acceleration noise floor per accelerometer cell ($\sqrt{\overline{a_{nc,th}^2}/\Delta f}$), which is calculated as:

$$\sqrt{\frac{\overline{a_{nc,th}^2}}{\Delta f}} = \frac{\sqrt{4k_B T b}}{m} \tag{2.16}$$

Increasing the number of cells increases the total damping and mass at the same time. However, the thermal-mechanical noise force scales up proportional to the square-root of damping and when divided by mass the corresponding acceleration noise scales down proportional to the square-root of number of cells. From another perspective, the uncorrelated white noise is statistically averaged over multiple accelerometer cells. The thermomechanical acceleration noise floor of an N cell array ($\sqrt{\overline{a_{na,th}^2}/\Delta f}$) is calculated as:

$$\sqrt{\frac{\overline{a_{na,th}^2}}{\Delta f}} = \sqrt{\frac{\overline{a_{nc,th}^2}/\Delta f}{N}} \tag{2.17}$$

The accelerometer cells are made small in order to reduce their mass and ensure their shock survivability. However, the small dimensions inevitably lead to a small damping and an underdamped system with a high quality factor. For a fixed resonant frequency, the ring-down time constant (τ) of an underdamped system increases with the quality factor [12],

$$\tau = \frac{2Q}{\omega_0} \tag{2.18}$$

which is undesirable for a fast and accurate response. The ring-down time constant of an accelerometer cell is calculated as 0.87 ms, which also applies to the full array assuming identically same accelerometer cells. However, the small random variations between the resonance frequencies of the accelerometer cells due to CMOS and post-CMOS MEMS process variations lead to an incoherence between different cells in the array, hence decreasing the ring-down time. The resonance frequency of groups of accelerometer cells can also be staggered by design, leading

to further improvements in the ring-down time and a faster responding accelerometer array as detailed in section 2.6. The mechanical design parameters of the accelerometer cell discussed up to this point are summarized in Table 2.1.

Table 2.1. Mechanical design parameters of the accelerometer cell

	Design Value
Calculated mass (m)	19×10^{-12} kG
Calculated spring constant (k)	10.15 N/m
Calculated resonance frequency ($f_{0,c}$)	116.2 kHz
Simulated resonance frequency (f_0)	118 kHz
Maximum Stokes damping (b_{st})	9.90×10^{-9} kg/s
Squeezed-film damping (b_{sq})	3.82×10^{-8} kg/s
Total damping (b)	4.81×10^{-8} kg/s
Quality factor (Q)	293
Ring-down time (τ)	0.79 ms
Thermomechanical noise ($\sqrt{\overline{a_{nc,th}^2}/\Delta f}$)	0.15 mG/√Hz

2.2 Curl Matching

The vertical and lateral stress gradients built in the structures during CMOS and post-CMOS MEMS processing steps curl the spring beams in the CMOS-MEMS devices upon release as discussed in Chapter 1. The spring beams are designed to be metal-free once the top metal is etched upon the completion of the oxide etch. The signal routing in the spring beams is made through the polysilicon layer and no metal layers are used other than the top metal that defines the beams. The purpose of this effort is to prevent any bias drift due to creeping metal at the accelerometer anchors upon repeated exposure to stress during shock events. However, the absence of intermediate metal layers in the spring beams also helps minimize the lateral stress

gradients without tapering the beams. On the other hand, the vertical stress gradients still exist and lead to vertical curl upon release. If the rotor and stator springs and trusses are designed differently, the resultant vertical curls are expected to be different. The obvious effect of curl mismatch between the rotor and stators is the reduction of overlapping sidewall area between the rotor and stator electrodes, hence the reduction of sense capacitance. However, a less obvious but more critical effect is the variation of sense capacitance as the curl mismatch changes with temperature. The variation in sense capacitance translates to temperature dependent drift in bias and scale factor unless it is compensated for thermal variations.

The stators in the first-generation design of the accelerometer cell are simply the modulation signal electrodes connected to each other with rigid beams to increase the stiffness in the sense direction. Although the stator beams are sized similar to the spring beams of the rotor (Figure 2.6), the metal layers routed through the stator beams changes the vertical stress gradients in the beams significantly. The rotor spring beams curl upwards by 0.95 μm whereas the stator beams curl downwards by 0.78 μm upon release, which adds to 1.73 μm maximum vertical curl mismatch (Figure 2.7). The curl of the beams are expected to change in the opposite directions with temperature variations, hence increasing the variation in sense capacitance and bias drift.

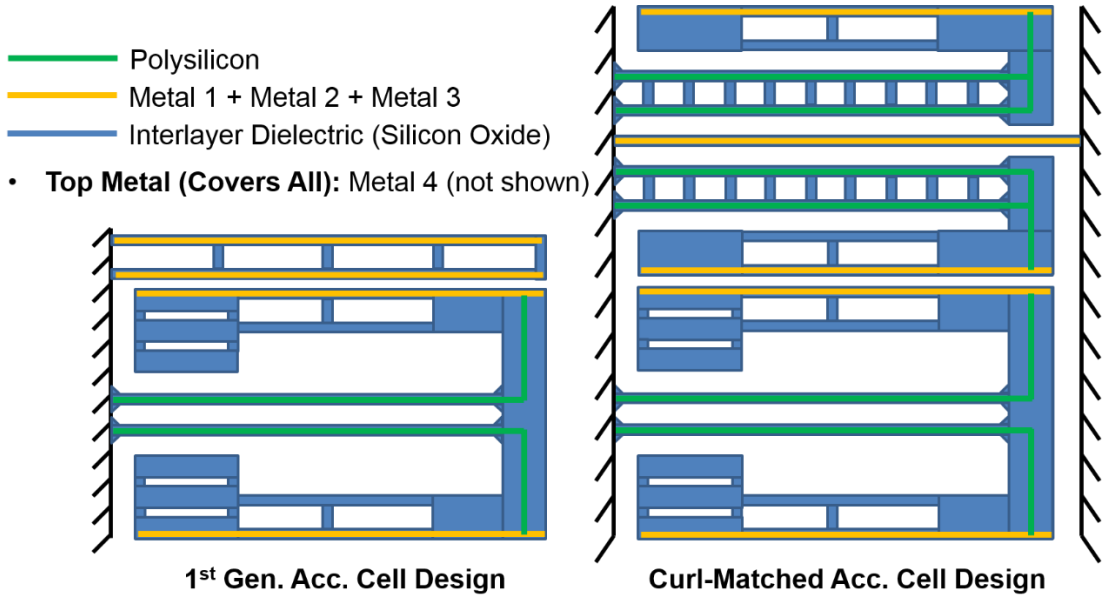


Figure 2.6. First-generation accelerometer cell design compared to the curl-matched design used in the accelerometer system.

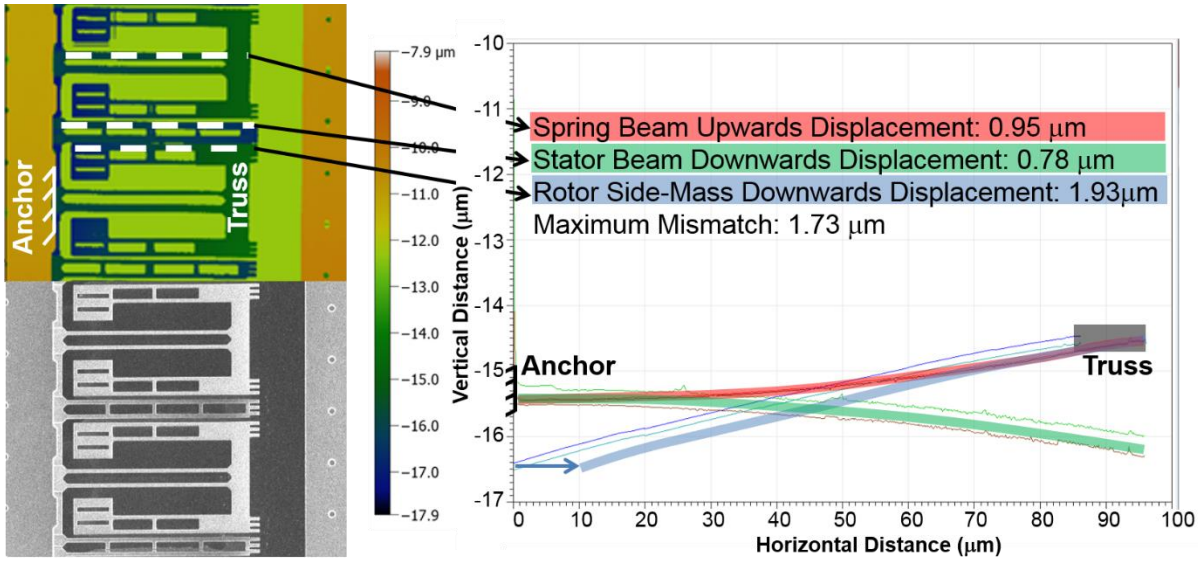


Figure 2.7. Optical profilometer measurement of vertical curl on the first-generation accelerometer cells.

Similarly designed spring beams and the electrodes of the rotor and stators minimize the vertical curl mismatch as well as the variation in mismatch as a function of temperature. The optical profilometer measurements on released accelerometer cells (Figure 2.8) show that the stator

and rotor springs curl upwards by 140 nm and 195 nm, respectively. On the other hand, both the stator and rotor electrodes make use of all three metal layers below the top metal for increased sense capacitance, hence curling downwards by 0.9 μm and 1.075 μm, respectively. Both the upwards and downwards curling are lower compared to that observed on the first-generation chip, which is believed to be due to run-to-run variations in built-in stress. The matched spring and electrode designs lead to 120 nm maximum measured vertical curl mismatch and improve bias stability by minimizing the temperature dependent variations in mismatch. The residual mismatch between the spring beams is due to the rigid connections between the stator springs that minimize the lateral displacement of the stators upon acceleration. The residual mismatch between the electrodes is due to the differences in the electrode structures, which could be eliminated by matching the electrode designs at the expense of increased accelerometer cell footprint.

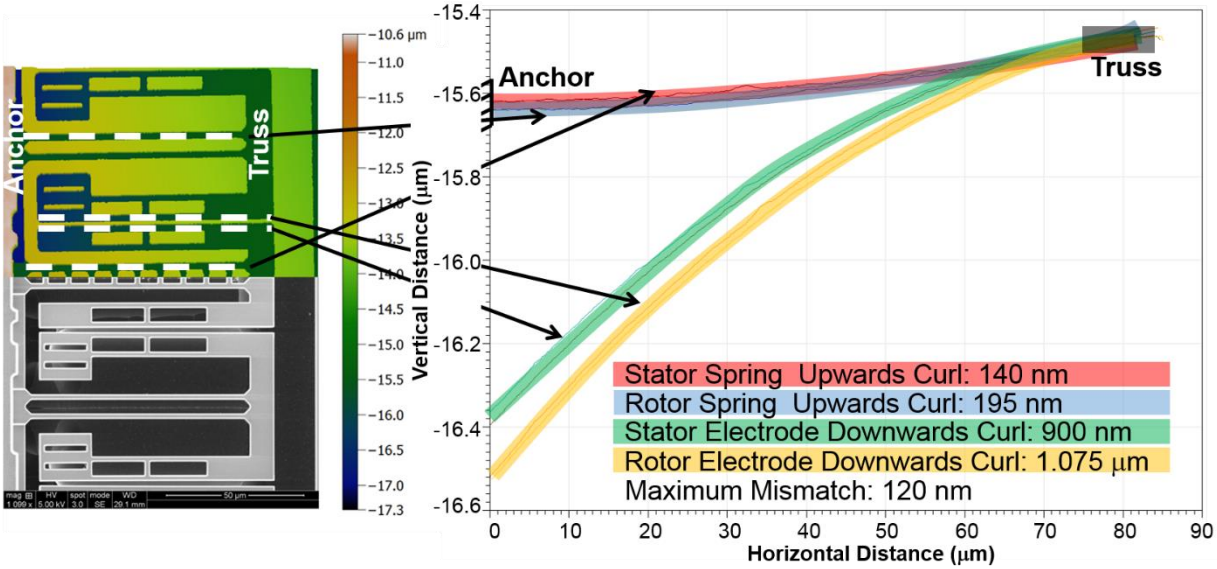


Figure 2.8. Optical profilometer measurement of vertical curl on the curl-matched accelerometer cells.

2.3 Electrical Design of the Accelerometer Cell

The electrical model of the accelerometer cell and the required signal routings are determined based on the selected sensing method. The discussion in Chapter 1 indicated that the most common sensing method used for low-G accelerometers is capacitive sensing, whereas the two most common sensing methods for high-G accelerometers are piezoresistive and piezoelectric sensing. Optical sensing methods also attract interest particularly for high-resolution acceleration measurements. However, high-stability optical readouts require benchtop laser sources and photodetectors, which implies a need to carry the signal with fiber optic cables that increases system complexity and adds challenges to miniaturization.

The low temperature sensitivity, low power dissipation and DC measurement capability of capacitive sensing brings it forward for navigation applications. The maximum possible input-referred sensitivity (i.e., the scale factor of the transducer) is set by the output swing of the on-chip circuits and the input acceleration range. Assuming a unity-gain rail-to-rail buffer with 1.8 V supply voltage and 50 kG input acceleration range, the maximum allowed transducer scale factor would be 18 μV/G (i.e., 0.9 V/50 kG). The on-chip parasitic capacitance limits the transducer scale factor in practice as discussed in this section; however, the designed accelerometer array scale factor is still kept above 1 μV/G while satisfying the bandwidth, input range and thermal-mechanical noise requirements for a high dynamic range accelerometer. The implementation of the accelerometer design and capacitive sensing scheme in CMOS-MEMS process enables monolithic integration of the transducer, readout circuits and auxiliary sensors to form an accelerometer system-on-chip with drift compensation.

Capacitive accelerometers are commonly operated in a force-feedback loop to achieve micro-G resolution and navigation-grade performance. However, the required voltage level for the

force-feedback at high-G becomes unfeasible to use in a CMOS process. For example, 50 kG acceleration exerted on a 20×10^{-12} kg accelerometer cell translates to 9.8 μN force ($F = m \times a$; G ≅ 9.8 m/s^2) on the cell. The electrostatic force feedback is calculated as:

$$F_e = \frac{1}{2} V^2 \frac{dC_0}{dx} \tag{2.19}$$

where V is the voltage across the capacitive gap and C_0 is the sense capacitance. One can assume 100 μm length and 5 μm height for the accelerometer's parallel-plate electrodes and reduce the capacitive gap (g_0) down to the post-CMOS MEMS process limits (e.g., 0.5 μm) given that the proof mass displacement is expected to be minimized by the force feedback. Applying parallel plate approximation and using the assumed electrode and gap sizes lead to 8.85 fF sense capacitance (C_0), and 1.77×10^{-8} F/m rate of change of capacitance with proof-mass displacement (i.e., $dC_0/dx \cong C_0/g_0$). In this case, the feedback voltage (V) should be approximately 33 V in order to generate the required force to counteract the proof-mass motion, which is well above the maximum allowed voltage in sub-micron CMOS technologies.

Resonant accelerometers also make use of capacitive sensing and actuation, thereby can be implemented in a CMOS-MEMS process. Although the common-mode frequency drift of the resonators (e.g., the temperature effects) can be mostly cancelled by differential sensing, the cancellation of the frequency drift due to charging cannot be guaranteed. CMOS-MEMS resonant accelerometers are likely to suffer from significant bias drift given the well-known dielectric charging problem in CMOS-MEMS resonators.

Open-loop operation is more preferable than closed-loop operation due to reduced system complexity, simpler readout circuits and lower power consumption. In addition, the fundamental limit on the measurement bandwidth is set by the resonance frequency of the transducer since the

readout circuits are not likely to limit the bandwidth. The most significant drawback of open-loop operation is the effect of the nonlinear change in the sense capacitance on the accelerometer response over the input range. However, the guided-end displacement of the proof mass and the differential change in the sense capacitances provide linear operation over a wide input range as shown in this section. The nonlinearity errors over the full input range can be further improved by calibration.

In open-loop operation, the acceleration signal at the capacitive bridge output can be amplified by using a voltage amplifier, a transimpedance amplifier or a switched-capacitor amplifier. The virtual ground at the input of the transimpedance amplifier and switched-capacitor amplifier minimizes the effect of parasitic capacitance. However, continuous-time voltage amplifiers potentially provide better resolution when the parasitic capacitance is small as discussed in [14], which is usually the case for a CMOS-MEMS accelerometer. The input impedance of a continuous-time voltage amplifier is high by definition, therefore the capacitive-bridge output remains as a high-impedance node and the parasitic capacitance becomes important in setting the scale factor of the transducer. The best scale factor is obtained when the ratio of parasitic capacitance to sense capacitance is minimized. Therefore, the best designs have sense capacitance that is much higher relative to the parasitic capacitance.

The sense capacitance of the accelerometer cell is set by the distance between the electrodes along with the length and height of the electrodes. The 2 μm spacing between the electrodes and 5.5 μm accelerometer height (4.9 μm when the top metal is removed) ensure a simple and repeatable post-CMOS MEMS process for the release of the structures. The length of the electrodes is limited by the beam length constraints. These variables can be tuned to increase the sense capacitance at the expense of increased process complexity and device footprint. However,

increasing the sense capacitance is not the only way of increasing the acceleration sensitivity. Reducing the parasitic capacitance is equally important for maximizing the sensitivity, which is further discussed in the following sub-sections. Minimizing the signal and noise feedthrough from the modulation lines to the readout is also critical for reducing the signal offset and improving the signal to noise ratio.

Two accelerometer cells are shown with the signal routings in Figure 2.9. The same routing scheme is implemented across the whole array, with the cell bridges connected in parallel, thereby the differential capacitive bridge model in Figure 2.9 is applicable to the whole array. The proof-mass displacement upon acceleration changes the capacitances across the bridge and results in a differential acceleration signal at the bridge output.

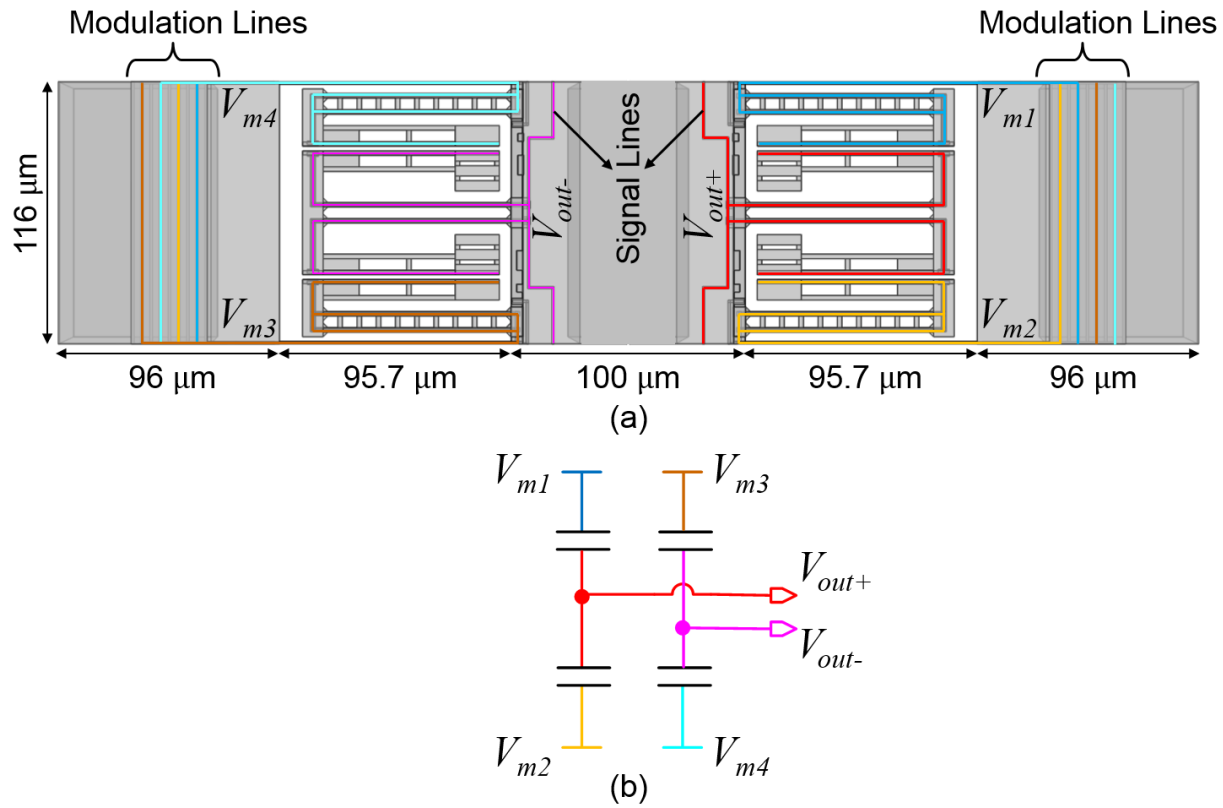


Figure 2.9. (a) Accelerometer cells with routings and (b) the corresponding schematic representation.

The routing of the acceleration signal has utmost importance in setting the parasitic capacitance to ground and coupling capacitances to modulation voltage lines. The modulation voltage lines are routed on a completely separate area at the expense of increased device footprint (Figure 2.9) in order to minimize modulation voltage coupling to the acceleration signal lines. Fixed-fixed beams are used to carry the modulation signal to the stator electrodes. The acceleration signal line is shielded from the modulation voltage lines wherever they have to be routed in parallel. The acceleration signal routing is kept far from the shields to minimize the parasitic capacitance. However, most of the parasitic capacitance is due to the grounded top metal cover above the signal routing and to the substrate below the signal routing. The parasitic capacitance to substrate is minimized by routing the acceleration signal close to the edge of the release area and taking advantage of the lateral silicon undercut. The isotropic silicon etch step in the post-CMOS MEMS process must be tuned to adjust the lateral undercut length and remove the substrate underneath the acceleration signal routing. The parasitic capacitance to top metal can be avoided by completely etching the top metal after the MEMS oxide etch.

2.3.1 Sense Capacitance

The nominal value of the sense capacitance depends on whether the top metal layer is removed after the oxide etch step or kept on the accelerometer cells. The simulated sense capacitance per one side of a single accelerometer cell (C_0) drops from 3.43 fF to 3.07 fF if the top metal layer is removed. However, removal of the top metal significantly reduces the parasitic capacitance as shown in the following sub-section, hence increasing the scale factor of the transducer.

The scale factor of the accelerometer depends on the change in sense capacitance with proof-mass displacement as discussed later in this section, therefore accurate estimation of the

scale factor requires an accurate model of the dependence between the sense capacitance and the capacitive gap. The 3D finite-element model of the accelerometer cell is used to simulate the change in sense capacitance by running a parametric sweep on the capacitive gap. Figure 2.10 compares the estimated change in sense capacitance based on the 3D finite-element analysis to that obtained by analytic analysis based on a first-order parallel-plate approximation when the top metal is removed. The fringing electric fields lead to higher capacitance values and a smaller rate of change with displacement, which are not captured in the parallel-plate approximation. A fourth-order polynomial fits on the simulated capacitance values for modeling the change of sense capacitance as a function of capacitive gap. The fitted polynomial is used to calculate the change in sense capacitance with proof-mass displacement when estimating the scale factor of the accelerometer later in this section. Figure 2.11 shows the comparison between the simulated sense capacitance and that obtained by using first-order parallel-plate approximation when the top metal is present, which can be used for estimating the scale factor of the accelerometer when the top metal is not removed after oxide etch.

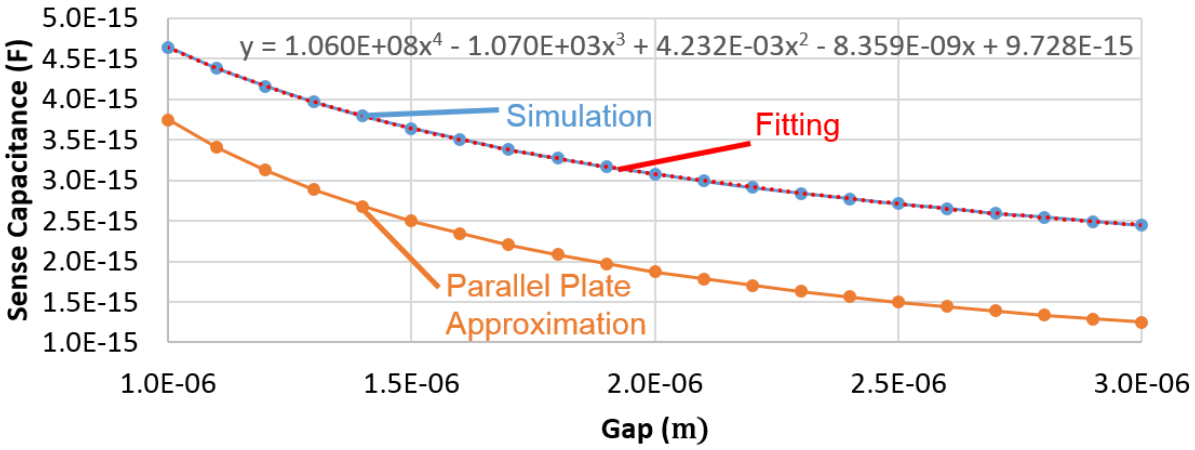


Figure 2.10. Simulated change in sense capacitance as a function of capacitive gap when the top metal is removed.

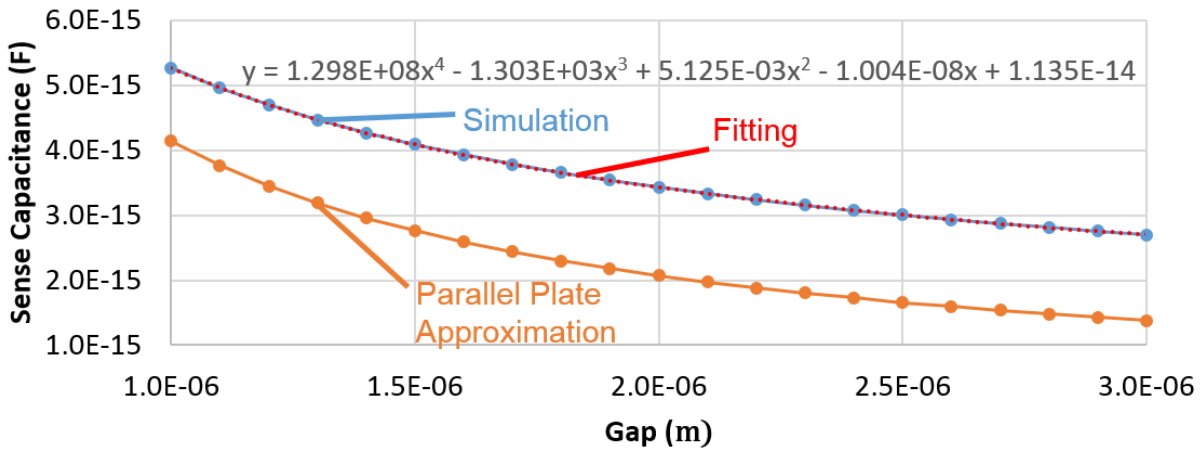


Figure 2.11. Simulated change in sense capacitance as a function of capacitive gap when the top metal is present.

2.3.2 Parasitic and Coupling Capacitances

The input-referred scale factor of the accelerometer depends on the ratio of the parasitic capacitance (C_p) to sense capacitance as detailed in the next sub-section. For a given sense capacitance, minimizing the parasitic capacitance translates to maximizing the scale factor of the accelerometer. The front-end amplifiers should be placed as close as possible to the accelerometer array in order to minimize the routing length and the parasitic capacitance. An accurate estimation of the parasitic capacitance of the acceleration signal routing is obtained by using the 3D finite-element model of the accelerometer cell (Figure 2.12). The simulation informs the capacitances to top metal (when present), substrate and shields while accounting for 30 µm substrate undercut.

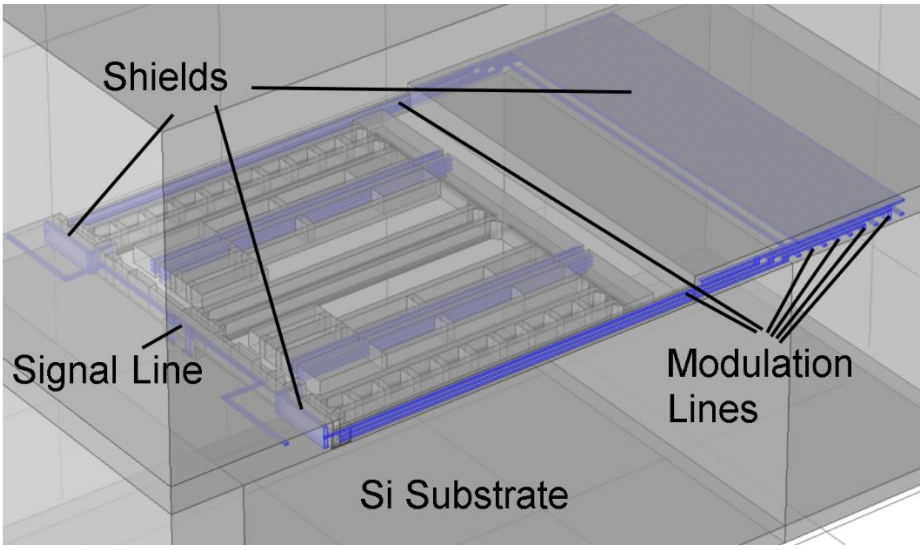


Figure 2.12. Finite-element model of the accelerometer cell for capacitance extraction.

The coupling capacitance between the bridge output signal and modulation voltage lines determines the direct modulation feedthrough. The differential bridge rejects common-mode feedthrough. However, differential feedthrough – when the coupling to the differential acceleration signal lines is not identical – is indistinguishable from the acceleration signal and translates to a DC offset acceleration once the signal is demodulated to baseband. The DC offset acceleration is also expected to arise if the spring beams of the rotors undergo lateral curl from residual stress gradients. Precautions are taken in the readout circuit design to cancel this offset to a great extent in order to prevent saturation of the circuit. However, any external noise coupled into the system through modulation signal wiring may not be cancelled completely and can still limit the accelerometer resolution. Therefore, it is important to accurately estimate the coupling capacitances to the modulation voltage lines and minimize them by re-routing the signals where possible.

Table 2.2. Simulated sense, parasitic and coupling capacitances per accelerometer cell

	With Top Metal	**Without Top Metal**
Sense capacitance per side (C_0)	3.43 fF	3.07 fF
Parasitic capacitance to top metal ($C_{p,tm}$)	11.26 fF	-
Parasitic capacitance to substrate ($C_{p,sb}$)	1.38 fF	2.99 fF
Parasitic capacitance to shields ($C_{p,sh}$)	0.58 fF	1.95 fF
Total parasitic capacitance to ground (C_p)	13.22 fF	4.94 fF
Coupling capacitance from V_{m+} to signal ($C_{c,mp}$)	43.1 aF	103.9 aF
Coupling capacitance from V_{m-} to signal ($C_{c,mn}$)	43.1 aF	102.0 aF
Coupling capacitance between V_{m+} and V_{m-} ($C_{c,pn}$)	20.63 fF	20.70 fF
Capacitance from V_{m+} to ground ($C_{g,mp}$)	40.18 fF	37.57 fF
Capacitance from V_{m-} to ground ($C_{g,mn}$)	39.13 fF	36.54 fF

The simulated sense capacitance per side (C_0), parasitic capacitance to ground (C_p) and coupling capacitances from the modulation voltage lines to the acceleration signal line are listed in Table 2.2 for the accelerometer cell design shown in Figure 2.12. The coupling capacitances from the modulation voltage lines to the acceleration signal line refer to the unwanted fixed-capacitance coupling, hence excluding the sense capacitance. The coupling capacitances between the modulation voltage lines and from the modulation voltage lines to ground do not have a direct impact on the accelerometer operation; however, these capacitances are also extracted to have a complete model of the system. The complete model of an accelerometer cell including the parasitic and coupling capacitances listed in Table 2.2 is shown in Figure 2.13.

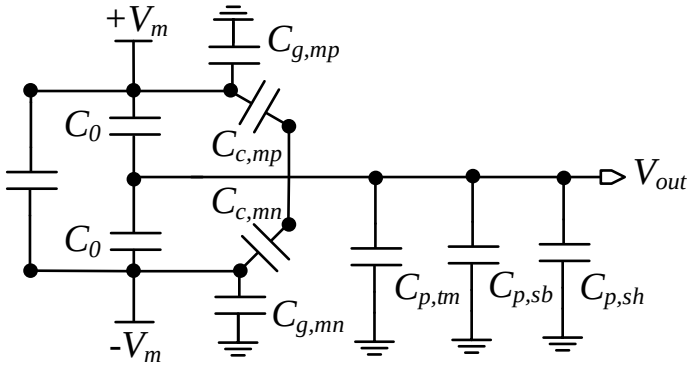


Figure 2.13. Complete model of an accelerometer cell including all the parasitic and coupling capacitances.

2.3.3 Lateral Curl of the Transducer

The lateral curl of the accelerometer cells leads to a mismatch between the sense capacitances and results in an offset signal at the transducer output (i.e., transducer offset), which is indistinguishable from a DC acceleration input. The transducer offset can be investigated based on the differential capacitive bridge model of the accelerometer array. Figure 2.14 shows the generic model, where the sense capacitances, parasitic capacitances and the modulation voltage sources are numbered for identification.

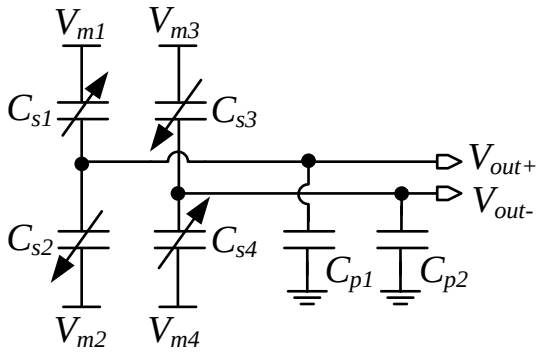


Figure 2.14. Generic differential capacitive bridge model of the accelerometer array.

The modulation voltages can be either square or sinusoidal waveforms. The output voltage (V_{out}) can be expressed in terms of the modulation voltages and sense capacitances:

$$V_{out}=V_{m1}\frac{C_{s1}}{C_{s1}+C_{s2}+C_{p1}}+V_{m2}\frac{C_{s2}}{C_{s1}+C_{s2}+C_{p1}} \\ -V_{m3}\frac{C_{s3}}{C_{s3}+C_{s4}+C_{p2}}-V_{m4}\frac{C_{s4}}{C_{s3}+C_{s4}+C_{p2}} \tag{2.20}$$

The sense capacitances are written based on parallel-plate approximation in (2.21), where ε0 is the permittivity of free space, A is the area of the sense capacitance (i.e., the sidewall area of the sense electrode), $x_{off,1}$ and $x_{off,2}$ are the offset displacements due to lateral curl and x_a is the displacement due to acceleration. The offset displacements are assumed to be slightly different on the two sides of the capacitive bridge and the displacement due to acceleration is assumed to be in the same direction as the offset displacement.

$$V_{out}=V_{m1}\frac{\frac{\varepsilon_0 A}{g_0-x_{off,1}-x_a}}{\frac{\varepsilon_0 A}{g_0-x_{off,1}-x_a}+\frac{\varepsilon_0 A}{g_0+x_{off,1}+x_a}+C_{p1}}+V_{m2}\frac{\frac{\varepsilon_0 A}{g_0+x_{off,1}+x_a}}{\frac{\varepsilon_0 A}{g_0-x_{off,1}-x_a}+\frac{\varepsilon_0 A}{g_0+x_{off,1}+x_a}+C_{p1}} \\ -V_{m3}\frac{\frac{\varepsilon_0 A}{g_0+x_{off,2}+x_a}}{\frac{\varepsilon_0 A}{g_0+x_{off,2}+x_a}+\frac{\varepsilon_0 A}{g_0-x_{off,2}-x_a}+C_{p2}}-V_{m4}\frac{\frac{\varepsilon_0 A}{g_0-x_{off}-x_a}}{\frac{\varepsilon_0 A}{g_0+x_{off,2}+x_a}+\frac{\varepsilon_0 A}{g_0-x_{off,2}-x_a}+C_{p2}} \tag{2.21}$$

The displacement due to acceleration can be ignored when calculating the offset signal due to lateral curl and the expression in (2.21) can be simplified as:

$$V_{out}=V_{m1}\frac{1}{1+\frac{g_0-x_{off,1}}{g_0+x_{off,1}}+\frac{C_{p1}}{\frac{\varepsilon_0 A}{g_0-x_{off,1}}}}+V_{m2}\frac{1}{1+\frac{g_0+x_{off,1}}{g_0-x_{off,1}}+\frac{C_{p1}}{\frac{\varepsilon_0 A}{g_0+x_{off,1}}}}$$
$$-V_{m3}\frac{1}{1+\frac{g_0+x_{off,2}}{g_0-x_{off,2}}+\frac{C_{p2}}{\frac{\varepsilon_0 A}{g_0+x_{off,2}}}}-V_{m4}\frac{1}{1+\frac{g_0-x_{off}}{g_0+x_{off,2}}+\frac{C_{p2}}{\frac{\varepsilon_0 A}{g_0-x_{off}}}} \quad (2.22)$$

Two of the modulation voltages (e.g., V_{m2} and V_{m4}) are assumed to be ground for simplicity and the required V_{m3} voltage to cancel the offset signal is calculated as:

$$V_{m3}=V_{m1}\frac{1+\frac{g_0+x_{off,2}}{g_0-x_{off,2}}+\frac{C_{p2}}{\frac{\varepsilon_0 A}{g_0+x_{off,2}}}}{1+\frac{g_0-x_{off,1}}{g_0+x_{off,1}}+\frac{C_{p1}}{\frac{\varepsilon_0 A}{g_0-x_{off,1}}}} \quad (2.23)$$

Assuming that the parasitic capacitances are four times higher than the nominal sense capacitance (i.e., $C_{p1} \cong C_{p2} \cong 4\varepsilon_0 A/g_0$) and assuming the offset displacements are ten times smaller than the capacitive gap (i.e., $x_{off,1} \cong x_{off,2} \cong g_0/10$), setting V_{m3} approximately 1.2 times higher than V_{m1} (e.g., V_{m3} = 1.8 V; V_{m1} = 1.5 V) should cancel the offset signal due to lateral curl. The offset voltage at the output can be zeroed regardless of the simplifying assumptions made for the calculations. The idea of tuning the modulation voltage amplitude at each node independently is used for cancelling the transducer offset generated by feedthrough from the modulation voltage lines or the lateral curl of the rotor springs.

2.3.4 Scale Factor of the Transducer

The output voltage can be expressed with a more compact formula by making simplifying assumptions regarding the sense capacitances and modulation voltage sources. The amplitudes of the V_{m1} and V_{m3} sources as well as the V_{m2} and V_{m4} sources are set close to each other when the

transducer offset is not significant (e.g., less than 1/100th of the capacitive gap). The V_{m1} and V_{m3} sources should also be differential with the V_{m2} and V_{m4} sources for maximizing the scale factor. In addition, C_{s1} and C_{s4} capacitors as well as the C_{s2} and C_{s3} capacitors are designed to have the same nominal value and change similarly with the acceleration or due to lateral curl. Without loss of generality, the capacitive bridge model can be simplified as shown in Figure 2.15.

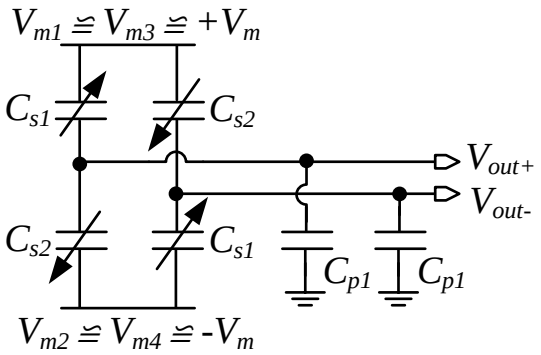


Figure 2.15. Simplified differential capacitive bridge model of the accelerometer array.

The simplified expression for the output voltage can be written based on the simplified capacitive bridge model:

$$V_{out}=2V_m\frac{C_{s1}-C_{s2}}{C_{s1}+C_{s2}+C_{p1}} \tag{2.24}$$

The sense capacitances are written based on parallel-plate approximation in (2.25), where the offset displacement due to lateral curl is assumed to be negligible.

$$V_{out}=2V_m\frac{\frac{\varepsilon_0 A}{g_0-x_a}-\frac{\varepsilon_0 A}{g_0+x_a}}{\frac{\varepsilon_0 A}{g_0-x_a}+\frac{\varepsilon_0 A}{g_0+x_a}+C_{p1}} \tag{2.25}$$

This expression can be simplified to see the effect of parasitic capacitance on the scale factor of the transducer:

$$V_{out}=2V_m\frac{x_a/g_0}{1+\frac{C_{p1}}{2\frac{\varepsilon_0 A g_0}{g_0^2-x_a^2}}} \tag{2.26}$$

The output voltage is proportional to the ratio of the displacement to the nominal capacitive gap when the parasitic capacitance is negligible. The response is perfectly linear when the parallel plate approximation is used as the differential capacitive bridge cancels the nonlinearity in the capacitance change with displacement. However, the sensitivity increases with increasing displacement when the parasitic capacitance is comparable to the sense capacitance, hence leading to a higher nonlinearity as the input acceleration increases. Assuming a small acceleration input that leads to a small displacement relative to the capacitive gap (i.e., $x_a << g_0/10$), the expression in (2.26) can be written as:

$$V_{out}=2V_m\frac{x_a/g_0}{1+\frac{C_{p1}}{2C_0}} \tag{2.27}$$

This expression shows that increasing the ratio of sense capacitance to parasitic capacitance increases the scale factor of the transducer. Therefore, reducing the parasitic capacitance has utmost importance in accelerometer design as it improves the sensitivity and linearity simultaneously, which are both critical for increasing the dynamic range.

The change in sense capacitance is estimated more accurately by finite-element analysis compared to parallel-plate approximation. Therefore, C_{s1} and C_{s2} capacitances in (2.24) are substituted by the fourth-order polynomial fit and evaluated for different amounts of proof-mass displacement corresponding to different acceleration inputs. The parasitic capacitance per unit cell (C_{p1}) should include both the total estimated parasitic capacitance based on simulations and the additional parasitic capacitance per cell due to the input capacitance of the readout circuit. The

characterized accelerometer array in this study consists of 56 accelerometer cells in total, thereby one side of the differential capacitive bridge is formed by 28 cells connected in parallel. The capacitance of the input transistor (i.e., 917 fF) is divided by the number of cells in the half array (i.e., 28) to find the additional parasitic capacitance per cell as 32.75 fF, which is slightly higher than the total sense and parasitic capacitance per cell (i.e., 20.08 fF) even when the top metal is present.

The output voltage is normalized with $2V_m$ and plotted as a function of displacement in Figure 2.16 and Figure 2.17. Figure 2.16 assumes that the parasitic capacitance is partially reduced by etching the top metal during post-CMOS MEMS process. Figure 2.17 accounts for the parasitic capacitance to the top metal and demonstrates its effect on the sensitivity.

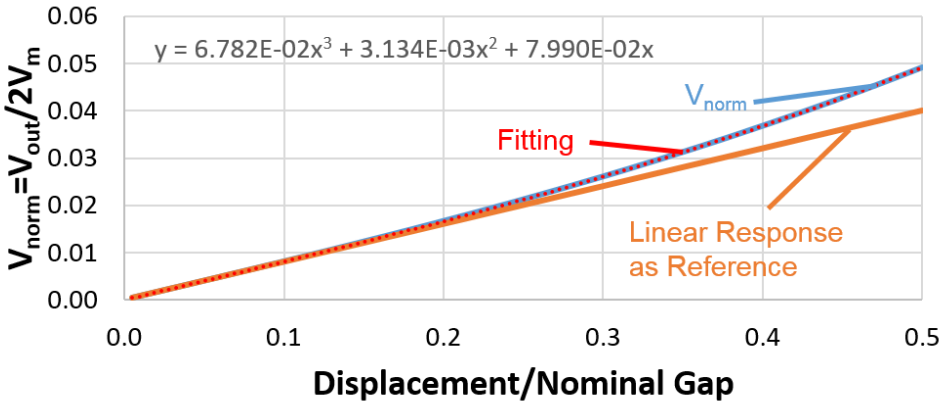


Figure 2.16. Normalized output voltage as a function of proof-mass displacement when the top metal is removed.

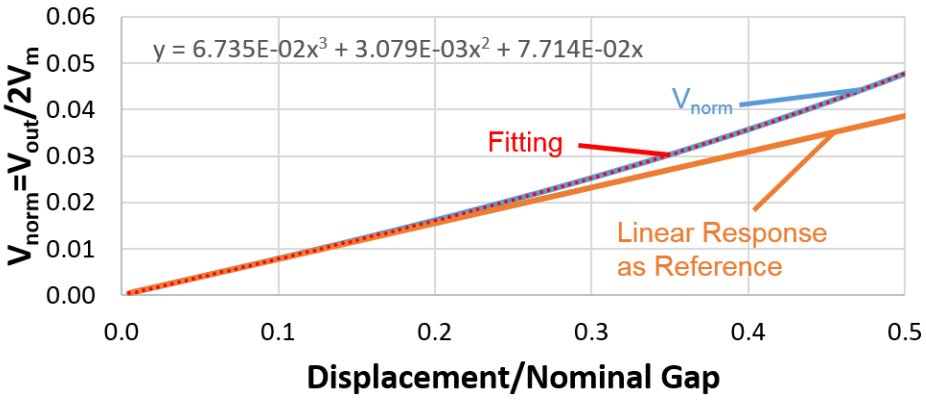


Figure 2.17. Normalized output voltage as a function of proof-mass displacement when the top metal is present.

The nonlinearity of the accelerometer response is estimated as 19.0% of the full range (50 kG) (Figure 2.18) when the top metal is removed. However, the linearity particularly gets worse above 0.5 μm displacement, such that the estimated nonlinearity is only 3.4% of the range up to 20 kG and 1.2% of the range up to 10 kG. Removing the top metal does not significantly affect the nonlinearity as the parasitic capacitance is dominated by the circuit input capacitance.

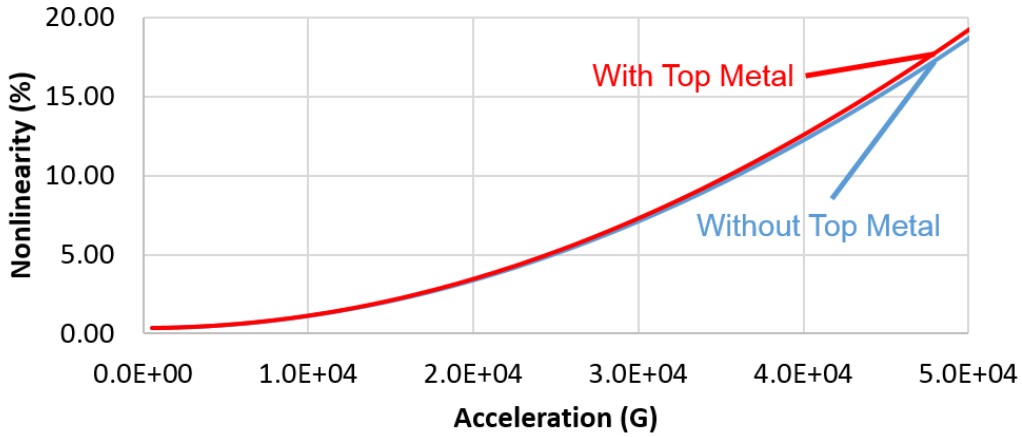


Figure 2.18. Nonlinearity of the accelerometer response in 50 kG acceleration input range.

The profiles observed in Figure 2.16 and Figure 2.17 are equally applicable to a half-bridge configuration. The most important advantage of the differential bridge configuration is cancelling

the common-mode bias drift of the transducer and the common-mode noise on the acceleration signal lines. Besides, the acceleration signal at the differential bridge output is two times higher with only √2 times increase in the noise floor compared to the half-bridge configuration, leading to √2 times higher signal to noise ratio. A third-order polynomial is fit on the normalized voltage values for modeling the change of output voltage as a function of proof-mass displacement. The fitted polynomial is used to calculate the rate of change of output voltage with proof mass displacement (i.e., $dV_{out} / dx = 2V_m \times dV_{norm} / dx$). The scale factor of the accelerometer cell (i.e., dV_{out} / da) can be obtained by using the relationship between the acceleration and proof-mass displacement (i.e., dx / da) based on the transfer function of the accelerometer. For excitation frequencies up to 20 kHz, the s^2 and sw_0/Q terms in the denominator of (1.2) have negligible contribution compared to the ω_0^2 term given the high resonance frequency (i.e., 118 kHz) of the accelerometer cells. Using the simplified transfer function (i.e., $dx / da \cong 1 / \omega_0^2$), the scale factor of the transducer (S_T) is:

$$S_T = \frac{dV_{out}}{da} = \frac{dV_{out}}{dx}\frac{dx}{da} = 2V_m \frac{dV_{norm}}{dx}\frac{1}{\omega_0^2} \tag{2.28}$$

One last simplification can be made on the differential capacitive bridge model of the accelerometer array given in Figure 2.15 by assuming equal capacitance values (i.e., C_0) for C_{s1} and C_{s2} at zero acceleration (and assuming zero offset, e.g., due to lateral curl). The infinitesimal change in the value of the C_{s1} and C_{s2} capacitances per infinitesimal proof-mass displacement can be represented as dC_0 / dx. This assumption eliminates the need for a separate model for the normalized output voltage dependence on displacement, such that the scale factor can be simply estimated based on the capacitance simulations:

$$S_T = \frac{dV_{out}}{da} = \frac{dV_{out}}{dx}\frac{dx}{da} = 2V_m \frac{1}{2C_0 + C_{p1}}\ 2\frac{dC_0}{dx}\frac{1}{\omega_0^2} \tag{2.29}$$

The rate of change of the sense capacitance with displacement (i.e., dC_0/dx) is obtained by taking the derivative of the fitted polynomial in Figure 2.10. It should be underlined that this expression is accurate only when the initial values and the infinitesimal changes of the C_{s1} and C_{s2} capacitances are approximately equal, which is the case when the lateral curl of the springs is small and proof-mass displacement is small e.g., below 0.1 μm (corresponding to 5 kG acceleration).

The scale factor of the accelerometer array is estimated as 1.28 μV/G based on Figure 2.16 and 1.29 μV/G based on (2.29). The estimation assumes that the top metal is etched during post-CMOS MEMS processing, therefore the sense capacitance (C_0) is taken as 3.07 fF. The total capacitance (i.e., $2C_0 + C_{p1}$) in the denominator of the expression in (2.29) increases only by ~1.2x (i.e., from 43.82 fF to 52.82 fF) when the top metal is present. The rate of change of sense capacitance with displacement (i.e., dC_0 / dx) scales approximately proportional to the value of the sense capacitance, thereby the higher sense capacitance (i.e., 3.43 fF) in the presence of top metal increases the scale factor by ~1.1x and compensates for some of the reduction in scale factor due to the additional parasitic capacitance. Taking these effects into account, the scale factor of the accelerometer array is estimated as 1.24 μV/G when the top metal is not etched. The estimated scale factor based on Figure 2.17 matches the estimation of (2.29) exactly.

2.4 Schematic Design of the Readout Circuit

The schematic of the accelerometer readout circuit is shown in Figure 2.19, where the ZI-HF2LI lock-in amplifier (Zurich Instruments, Zürich, Switzerland) both generates the modulation voltages and performs the numerical demodulation and filtering functions once the data is acquired through its internal 16-bit analog to digital converter (ADC). Alternatively, the modulation and

demodulation functions can be performed by analog switches, the signal can be filtered by an analog filter and the analog-to-digital conversion can be made by a data acquisition card (e.g., NI-USB-6212, National Instruments, Austin, TX) as shown in Figure 2.20. The readout circuit in Figure 2.20 is implemented on a printed-circuit board with off-the-shelf circuit components, the schematics of which are provided in Appendix B.

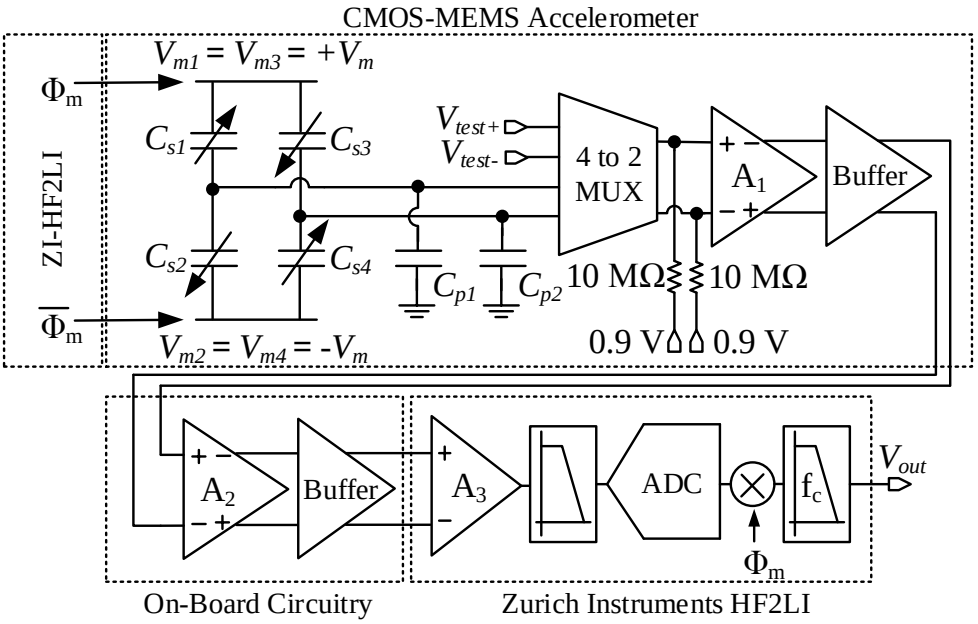


Figure 2.19. Schematic of the accelerometer readout circuit utilizing a lock-in amplifier.

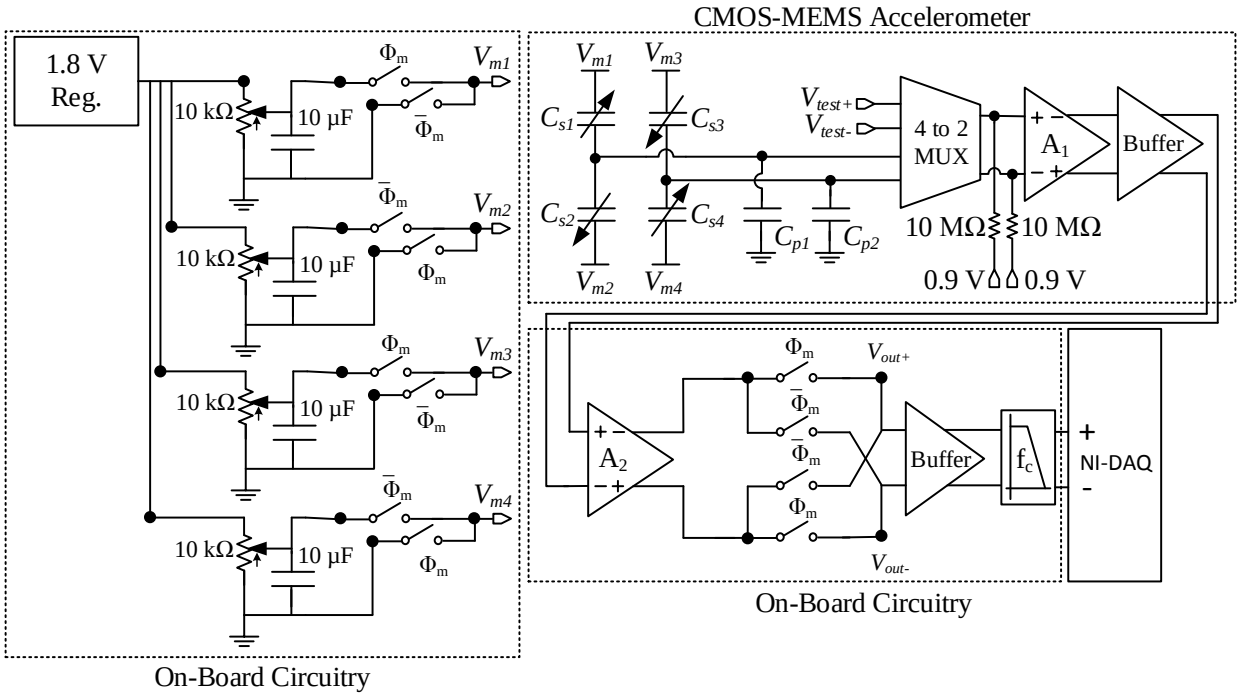


Figure 2.20. Schematic of the accelerometer readout circuit implemented with off-the-shelf circuit components.

The stator electrodes carry differential sinusoidal modulation voltages ($+V_m$ and $-V_m$) with 1.8 V peak-to-peak (pp) amplitude. The deflection of the proof mass due to acceleration varies the sensing capacitors in the capacitive bridge (C_{s1} to C_{s4}) leading to a differential modulated signal at the capacitive bridge output proportional to the acceleration. The on-chip amplifier and buffer circuits are designed by Xiaoliang Li under the guidance of Prof. Jeyanandh Paramesh at Carnegie Mellon University. The transistor level designs of these circuits are provided in Appendix A1 of this thesis. The input capacitance of the front-end amplifier is set as 917 fF to approximately match the total sense and parasitic capacitance of 28 accelerometer cells (per input) when the top metal is present. The on-chip multiplexer enables the application of test inputs to verify the functionality and extract the noise floor of readout circuits. The high impedance input nodes of the first gain stage (A_1) are biased at 0.9 V by off-chip voltage regulators through 10 MΩ resistors. The

acceleration signal passes through on-chip (A_1) and on-board (A_2) gain stages with a combined DC gain of 336 V/V, and then on to an input range amplifier (A_3) if the ZI-HF2LI is used for data acquisition. In the ZI-HF2LI, the signal passes through an anti-aliasing filter with 50 MHz cut-off frequency, and is digitized, demodulated and filtered (fourth order; f_c = 1 kHz). Alternatively, the signal first is demodulated, then filtered by a second-order analog filter (f_c = 1 kHz) and digitized by the NI-DAQ. In this case, the filter both limits the signal bandwidth and acts as an anti-aliasing filter before data acquisition.

Table 2.3. Supply voltage and power consumption of the major components in the readout circuit

	Supply Voltage	**Power Consumption**
On-chip amplifier and buffer (simulated)	+ 1.8 V	20.4 mW
On-board amplifier and buffer	± 3.3 V	79.2 mW
Analog second-order filter	± 5 V	20 mW
AOCJY3-A oven controlled crystal oscillator	+5 V	1000 mW
NI-USB 6212 data acquisition card	+4.5 V	< 1800 mW

The supply voltage levels and the power consumption of the on-chip and on-board circuit components as well as the clock source and data acquisition card are listed in Table 2.3. The measured on-chip power consumption is 41.2 mW and includes the power consumption of piezoresistive field-effect transistors (piezoFET) sensors (not discussed in this thesis), which cannot be powered down during the measurements. The simulated power consumption is dominated by the buffer (i.e., 18.6 mW); however, the amplifier power consumption is also significant (i.e., 1.8 mW) for reducing the input referred white noise floor, hence maximizing the measurement resolution. The on-board circuits are also low-noise components and dissipate a significant amount of power; however, the power consumption of the on-board circuitry can be

reduced by selecting low-power components. One of the major sources of power consumption is the oven-controlled crystal oscillator (OCXO) used for generating the clock signal for on-board modulation and demodulation. The phase noise of the clock source can translate to acceleration noise as discussed in the following section. The oven-controlled crystal oscillator is selected for its outstanding frequency stability specification (5 ppb in 0 °C to + 50 °C temperature range); however, a lower-end oscillator can be used for reducing the power consumption as long as the phase noise of the clock source does not limit the acceleration noise floor. The other major source of power consumption is the data acquisition card. The power consumption for data acquisition can also be reduced by implementing the data acquisition components on the chip with particular attention to power; however, it is out of scope of this study.

2.4.1 Offset Cancellation

The rotor spring beams undergo lateral curl upon release due to the lateral stress gradients built in the beams during the CMOS and post-CMOS MEMS fabrication steps. The lateral curl in the beams and the differential feedthrough from the modulation voltage lines to the acceleration signal line are the two sources of DC acceleration signal offset at the accelerometer output, which is called the "transducer offset". The on-board amplifiers are prone to saturate when the transducer offset at the capacitive bridge output is above 5 mV, which corresponds to 4.1 kG acceleration and approximately 100 nm lateral displacement when the top metal is not etched. The lateral curl of the released accelerometer cells never exceed 100 nm; however, the generated offset voltage is still undesirable as it limits the ability to reduce the input range of the ADC and leads to a need for higher number of bits to resolve the small acceleration levels. Independent tuning of the amplitudes of each individual modulation signal helps cancel the transducer offset to a great extent.

The input offset voltage of the on-chip amplifier is another source of concern for saturation, since it goes through both on-chip and on-board gain stages along with the acceleration signal. To be more precise, the input offset voltage of all the circuit stages can be referred to the capacitive bridge output and the total DC offset at the bridge output is called the "circuit offset". The circuit-offset signal is at baseband before demodulation, therefore it gets shifted to the modulation frequency after the demodulation step and gets filtered subsequently. Increasing the modulation frequency helps with attenuating the modulated circuit offset signal, hence minimizing its effect in the acceleration signal band of interest. However, the circuit offset should still be minimized to prevent the readout circuitry from saturating. The resistive biasing at the input of the first-stage amplifier provides the flexibility to tune the bias voltage at the two inputs independently and compensate the effect of circuit offset when needed.

2.4.2 Chopper Stabilization

The signal-processing steps implemented by the readout circuit stages are lumped into amplifier, demodulator and low-pass filter blocks (with f_c cut-off frequency) and the expected power spectrum at the output of each block is shown in Figure 2.21. The modulation signal is assumed to be a sinusoid and the modulation frequency (f_m) is set as the flicker noise corner frequency of the readout circuit. The chopper stabilization technique minimizes the effect of circuit flicker noise on the accelerometer readout through the modulation and demodulation of the acceleration signal. The differential modulation voltages applied on the stators (i.e., across the capacitive bridge) modulates the acceleration signal generated by the proof-mass displacement. This prevents the acceleration signal spectrum from overlapping with the flicker noise spectrum of the amplifier circuits at the output of the transducer. Increasing the input transistor sizes of the on-chip amplifier decreases the flicker noise and the noise corner [71], hence simplifying chopper

stabilization by reducing the required modulation frequency and circuit bandwidth. The demodulator in the readout circuit comes after the gain stages and brings the acceleration signal spectrum to baseband while shifting the flicker noise of the amplifier circuits to modulation frequency. Filtering the acceleration signal after demodulation suppresses the flicker noise of the amplifier circuits. The filtered acceleration signal has minimum flicker noise contribution from the circuits as illustrated by the final power spectrum in Figure 2.21, which improves the bias stability of the accelerometer.

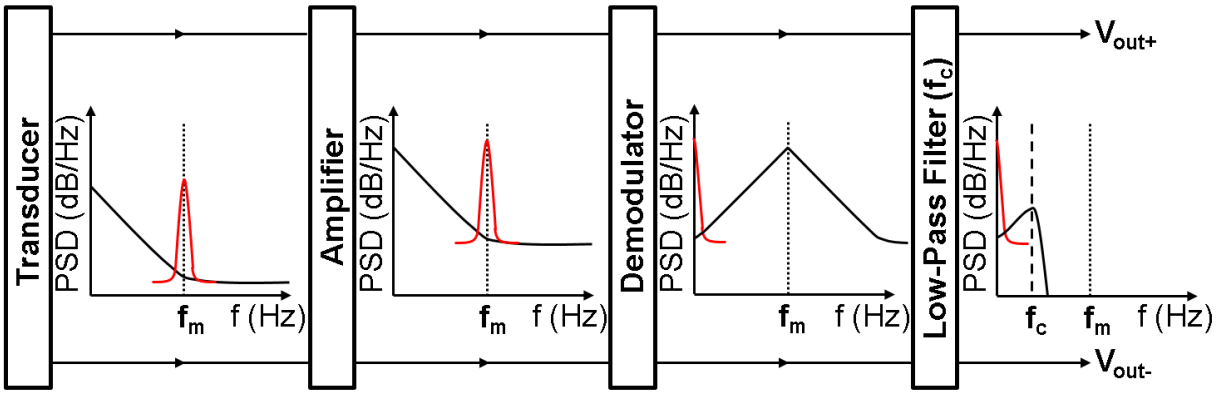


Figure 2.21. The accelerometer output spectrum after each signal-processing step.

2.5 Noise Analysis

The accelerometer readout circuit shown in Figure 2.20 is repeated in Figure 2.22, where the noise sources in the signal path are included for further discussion. The noise contributions of the on-chip amplifier and buffer stages are modeled as a single noise voltage ($\sqrt{\overline{v_{n,A1}^2}/\Delta f}$) added at the input of the on-chip amplifier (A_1). Since the noise of the on-chip buffer is divided by the gain of the amplifier (i.e., ~ 16.1 V/V) when it is referred to the amplifier input, $\sqrt{\overline{v_{n,A1}^2}/\Delta f}$ is expected to be dominated by the amplifier noise. Similarly, the noise contribution of the on-board amplifier

and buffer stages is modeled as a noise voltage ($\sqrt{\overline{v_{n,A2}^2}/\Delta f}$) added at the input of the on-board amplifier (A_2). The thermal-electrical noise of the biasing resistors at the input of the on-chip amplifier is modeled by adding noise voltage sources ($\sqrt{\overline{v_{n,R1}^2}/\Delta f}$ and $\sqrt{\overline{v_{n,R2}^2}/\Delta f}$) in series with the biasing resistors. The noise of the DC voltage signal generated by the regulator and the additional switching noise can also contribute to the acceleration noise floor. All the noise contribution from modulation and demodulation steps are modeled as noise voltages ($\sqrt{\overline{v_{n,m1}^2}/\Delta f}$ to $\sqrt{\overline{v_{n,m4}^2}/\Delta f}$) added to the modulation voltage lines (V_{m1} to V_{m4}). The low-pass filter noise and the input noise of the data acquisition system get divided by the gain of the amplifier stages when referred to the output of the capacitive bridge, therefore are not likely to limit the noise floor. In addition, the gain of the amplifier stages can always be increased to bring the signal above the noise floor set by the filter and the data acquisition system. Therefore, the noise contribution of the filter and the NI-DAQ will not be discussed further.

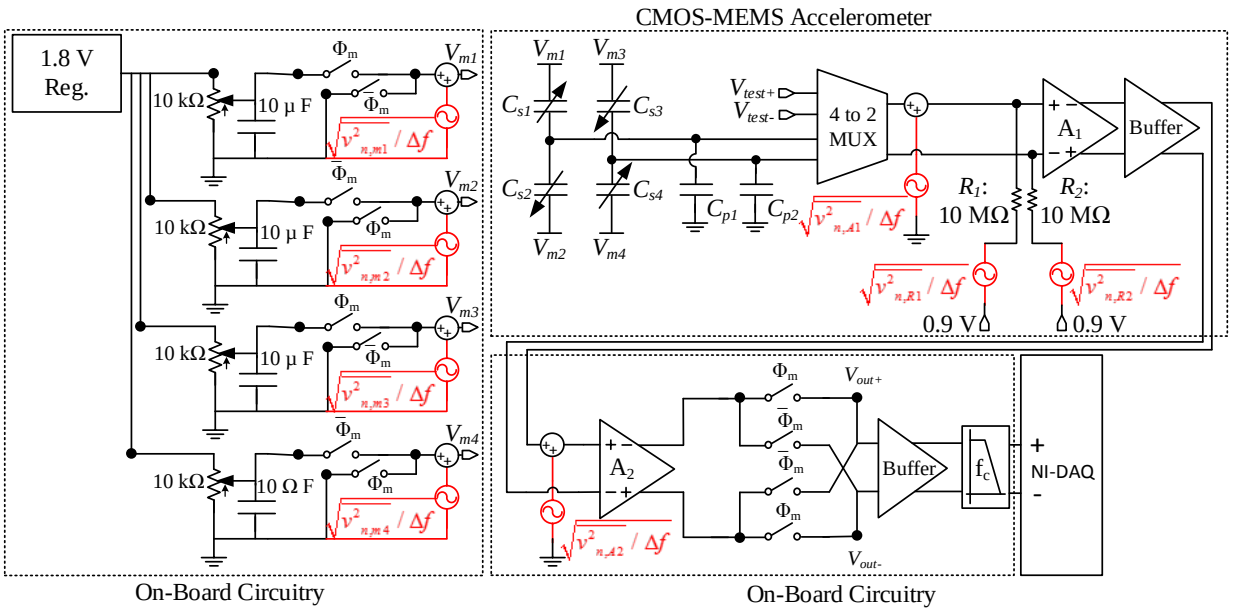


Figure 2.22. Schematic of the accelerometer readout circuit including the noise sources.

2.5.1 Amplifier Stages

The input-referred noise power density of the on-chip amplifier and buffer ($\sqrt{v_{n,A1}^2/\Delta f}$) is simulated in Cadence ® (Cadence Design Systems, Inc., San Jose, CA) by using the noise models of the CMOS process and provided in Figure 2.23. The AC response analysis of the circuit in Cadence also gives the total estimated gain and phase shift for the on-chip circuits (Figure 2.24). The output-referred noise power density can be calculated by multiplying the input-referred noise power density with the gain of the on-chip circuits. Setting the modulation frequency above the flicker noise corner helps with chopping the flicker noise of the on-chip circuits completely; however, requires a large bandwidth for the on-board circuits. After chopper stabilization, only the circuit noise in a small band around the modulation frequency contributes to the acceleration noise floor. The noise profile can be approximated as white noise and the noise density of the circuit at the modulation frequency can be taken as the noise floor.

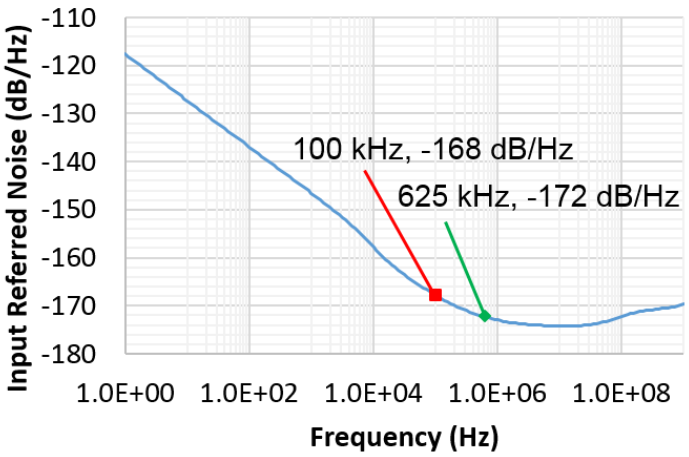
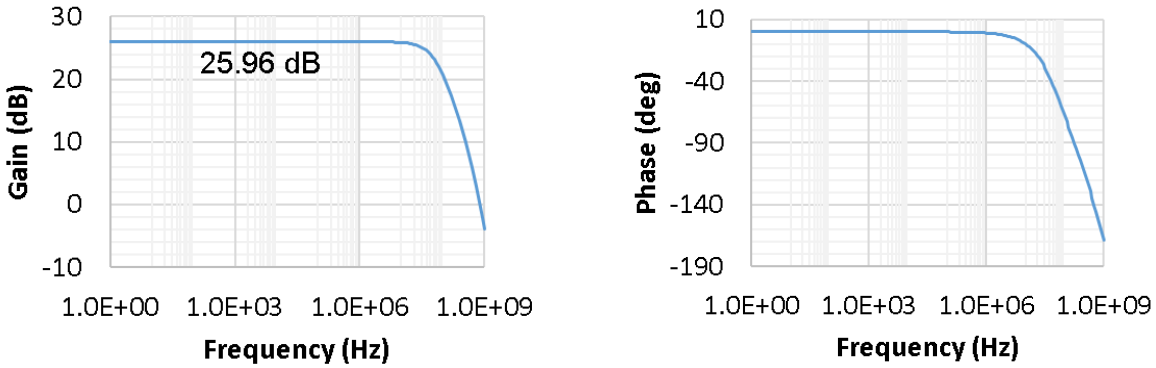


Figure 2.23. Simulated noise spectrum of the on-chip circuits referred to the amplifier input.



(a) (b)

Figure 2.24. (a) Simulated gain and (b) phase shift of the on-chip circuits.

The input-referred amplitude noise power density of the on-board circuits ($\sqrt{\overline{v_{n,A2}^2}/\Delta f}$) gets divided by the on-chip circuit gain when referred to the capacitive bridge output for the acceleration noise calculation. Since the on-chip circuit gain is designed to be around 16.1 V/V, the amplitude noise requirement for the on-board circuits is significantly relaxed. The input-referred noise power density of the on-board circuits is dominated by white noise with value 4 nV/√Hz at frequencies above 10 kHz, hence not significantly affecting the acceleration noise floor.

2.5.2 Input Biasing

The DC biasing at the input nodes of the on-chip amplifier is needed to prevent the bias levels of these high-impedance nodes from drifting. Resistive biasing is used for its simplicity and the bias voltages are generated off-chip for having flexibility in tuning the voltage levels to cancel the circuit offset. The thermal noise generated by the resistors add to the noise generated by the amplifier stages, therefore the biasing resistors should have a low resistance. On the other hand, the resistance of the biasing resistors should be significantly higher than the impedance of the parasitic capacitance at the modulation frequency in order to prevent signal attenuation.

The input transistors of the on-chip amplifier have 917 fF capacitance, which is slightly higher than the total sense and parasitic capacitance of the 28 cells connected to each input. The total capacitive loading due to the sense and parasitic capacitances of 28 cells and the input capacitance of the amplifier becomes approximately 1.5 pF when the top metal is present and 1.2 pF when the top metal is removed. The impedance of 1.2 pF capacitance at modulation frequencies above 100 kHz is less than 1.3 MΩ, therefore setting the biasing resistors as 10 MΩ ensures negligible signal attenuation at modulation frequencies above 100 kHz. The thermal noise power density of a resistor (R) at room temperature is:

$$\sqrt{\overline{v_{n,R1}^2}/\Delta f}=\sqrt{\overline{v_{n,R2}^2}/\Delta f}=\sqrt{4k_BTR} \tag{2.30}$$

where $\sqrt{\overline{v_{n,R1}^2}/\Delta f}$ = 400 nV/√Hz for R = 10 MΩ. The noise of the biasing resistors is significantly higher than the simulated input-referred amplitude noise of the on-chip circuits above 100 kHz. However, unlike the circuit noise, the noise of the biasing resistors is filtered by the low-pass filter formed at the on-chip amplifier inputs by the biasing resistors and the capacitive loading. The cut-off frequency of the first-order RC low-pass filter formed at each amplifier input by the 10 MΩ

biasing resistor and the 1.2 pF capacitive load is calculated as 13.3 kHz (i.e., $f_c = 1 / 2\pi RC$), which reduces to 10.6 kHz when the capacitive load is 1.5 pF due to top metal.

The total noise contribution of the input bias resistors ($\sqrt{\overline{v_{n,Rb}^2}/\Delta f}$) is calculated by adding the noise power density of the two resistors (*i.e.*, $v_{n,Rb}^2 = v_{n,R1}^2 + v_{n,R2}^2$). The combined noise power density of the on-chip circuits ($\sqrt{\overline{v_{n,A1}^2}/\Delta f}$) and the biasing resistors ($\sqrt{\overline{v_{n,Rb}^2}/\Delta f}$) is simulated in Cadence and referred to the capacitive bridge output (Figure 2.25). The effect of the described RC low-pass filter is clearly observed in the simulations. The noise contribution of the biasing resistors to the acceleration noise floor can be minimized by increasing the modulation frequency used for chopper stabilization.

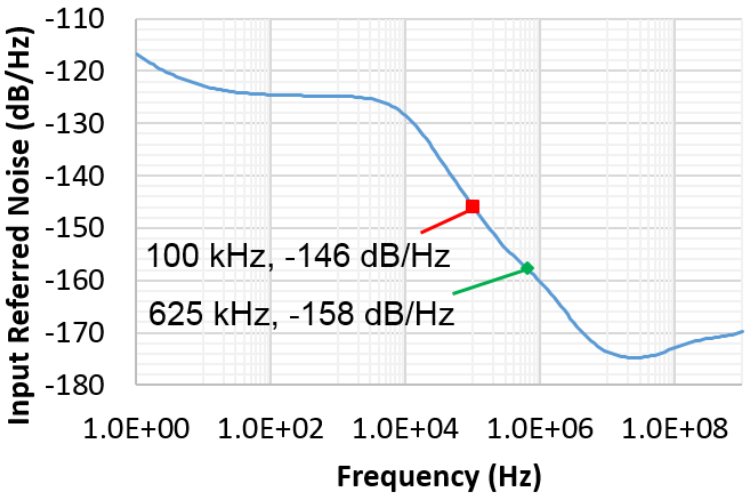


Figure 2.25. Combined noise power density of the on-chip circuits and the biasing resistors at the capacitive bridge output when the top metal is present.

2.5.3 Modulation Voltage Source

The modulation voltage waveform can have both amplitude noise coming from the voltage source used for generating the DC potential and phase noise (i.e., jitter) coming from the clock

source used for switching the DC potential on and off when generating the square modulation waveform. The analysis of the amplitude and phase noise components at different harmonic frequencies of the square waveform is more tedious than the analysis of the amplitude and phase noise of a single-tone sinusoidal waveform. Therefore, the analytical noise analysis in this section is made for a sinusoidal modulation and demodulation waveform, which is valid when ZI-HF2LI lock-in amplifier is used for modulation and demodulation. However, the logic behind the analysis and the conclusions can also be extended to square waveforms.

A sinusoidal modulation signal ($V_m(t)$) with amplitude V_{m0} and frequency f_{m0} is represented as:

$$V_m(t)=\left(V_{m0}+v_{n,m}\right)\cos\left(2\pi f_{m0}\,t+\varphi_{n,m}\right) \tag{2.31}$$

where $v_{n,m}$ is the amplitude noise and $\varphi_{n,m}$ is the phase noise. The sinusoidal demodulation signal ($V_d(t)$) is represented similarly with amplitude V_{d0} and frequency f_{m0} as follows:

$$V_d(t)=(V_{d0}+v_{n,d})\cos\left(2\pi f_{m0}\,t+\varphi_{n,d}\right) \tag{2.32}$$

where $v_{n,d}$ is the amplitude noise and $\varphi_{n,d}$ is the phase noise. Since the acceleration signal is ideally at much lower frequencies (e.g., >10 times lower) than the modulation signal, any phase shift (φ_s) introduced at the modulation frequency can be assumed to be the same for all acceleration components and simply added to the modulation signal. The modulated and amplified acceleration signal ($A_m(t)$) before demodulation and filtering is:

$$A_m(t)=\left(V_{m0}+v_{n,m}\right)\cos\left(2\pi f_{m0}\,t+\varphi_s+\varphi_{n,m}\right)G_C\frac{2}{2C_0+C_p}\,\frac{dC_0}{dx}\frac{1}{w_0^2}\left(A_0+A_s\cos\left(2\pi f_a t\right)\right) \tag{2.33}$$

where G_C is the combined gain of the amplifier stages, A_0 is the noise-free offset acceleration, A_s is the noise-free acceleration signal amplitude and f_a is the noise-free acceleration frequency

($f_a << f_{m0}$). After the multiplication of (2.33) by the demodulation signal, the demodulated and filtered acceleration signal ($A_d(t)$) amplitude is:

$$A_d(t) = \frac{(V_{m0}+v_{n,m})(V_{d0}+v_{n,d})}{2}\cos\left(\varphi_s+\varphi_{n,m}-\varphi_{n,d}\right) \times G_C \frac{2}{2C_0+C_p}\frac{dC_0}{dx}\frac{1}{w_0^2}\left(A_0+A_s\cos(2\pi f_a t)\right) \quad (2.34)$$

A small-angle approximation for the phase-noise components simplifies this expression:

$$A_d(t) \cong \frac{(V_{m0}+v_{n,m})(V_{d0}+v_{n,d})}{2}\left(\cos(\varphi_s) - \sin(\varphi_s)\left(\varphi_{n,m}-\varphi_{n.d}\right)\right) \times G_C \frac{2}{2C_0+C_p}\frac{dC_0}{dx}\frac{1}{w_0^2}\left(A_0+A_s\cos(2\pi f_a t)\right) \quad (2.35)$$

The first observation to make on this expression is that the ratio of $v_{n,d}$ to V_{d0} and $v_{n,m}$ to V_{m0} determines the effect of amplitude noise on the acceleration signal-to-noise ratio. Therefore, a stable voltage supply with low amplitude noise should be used for generating the modulation voltages. The second observation is that the increased phase shift reduces the acceleration signal amplitude while increasing the effect of phase noise of the modulation signals on the acceleration signal output. This implies that reducing the phase shift introduced by the amplifier stages by increasing the circuit bandwidth should improve the signal-to-noise ratio when phase noise is the dominant noise source. However, the phase noise of the modulation and demodulation waveforms should be correlated and cancel each other to a great extent when the two waveforms are generated by the same source, thereby should not dominate the noise floor.

The performed noise analysis assumes that all the modulation waveforms (i.e., V_{m1} to V_{m4}) are generated by the same source and all the noise voltages (i.e., $v_{n,m1}$ to $v_{n,m4}$) are correlated such that they propagate similar to the modulation voltage signals. The AC offset cancellation method

used in this study requires the modulation voltage amplitudes to be independently tuned as previously discussed. In order to keep the correlation between the modulation voltage waveforms, the DC voltage levels are generated by a common regulator and tuned by the help of potentiometers on the testbed. The modulation and demodulation switches are all controlled by the same high stability clock source, hence keeping the correlation between the phase noises. Therefore, the conclusions made in this section are still applicable to the testbed used for the accelerometer characterization.

2.5.4 Total Acceleration Noise Floor

The total acceleration noise floor is calculated by adding the noise power contributions from the amplifier stages, input biasing resistors, modulation voltage sources and the transducer itself. The noise contribution of the on-chip amplifier stages dominates. Assuming the modulation frequency is set above 100 kHz, the simulated input-referred amplitude noise power density of the on-chip circuits ($\sqrt{\overline{v_{n,A1}^2}/\Delta f}$) at 100 kHz (i.e., 4 nV/√Hz) can be used to bound the noise contribution from the amplifier stages. The on-chip circuit noise profile around the modulation frequency can be approximated as white noise as long as the signal bandwidth is limited to less than one-tenth of the modulation frequency. The corresponding calculated acceleration noise floor ($\sqrt{\overline{a_{n,A1}^2}/\Delta f}$) is 3.2 mG/√Hz, using the scale factor of the accelerometer array with top metal (i.e., 1.24 μV/G).

The total noise power density of the input biasing resistors ($\sqrt{\overline{v_{n,Rb}^2}/\Delta f}$) is 565.7 nV/√Hz, whose effect is reduced at higher frequencies due to the first-order RC low-pass filter formed at the circuit input. Simulations show that the noise contribution of the biasing resistors at 100 kHz (i.e., 49.9 nV/√Hz) is larger than the contribution of the on-chip circuits and increases the input

referred noise floor to 50.1 nV/√Hz. The corresponding acceleration noise floor ($\sqrt{\overline{a_{n,Rb}^2}/\Delta f}$) of the accelerometer array with top metal is 40.3 mG/√Hz at 100 kHz, which can be decreased by increasing the modulation frequency.

The modulation voltage sources do not lead to a fixed amount of noise at the output of an ideal accelerometer array. Assuming the modulation voltages are generated by the same voltage source and the noise amplitudes scale similar to the modulation signal, (2.35) shows that the modulation voltage noise does not show up at the accelerometer output when the input acceleration is zero. However, the lateral curl of the spring beams of the accelerometer leads to an offset acceleration signal in practice (i.e., transducer offset). Tuning the amplitudes of the modulation voltage signals (e.g., by using potentiometers with negligible noise compared to modulation voltage noise) to reduce the offset acceleration signal should simultaneously reduce the noise contribution from the modulation signals based on the assumption that the noise amplitudes scale along with the modulation signal amplitudes. Assuming a residual offset signal around 50 mV at the readout circuit output, the voltage offset referred to the capacitive bridge output is calculated as 148.8 μV by using the combined gain of the amplifier stages (i.e., 336 V/V). The corresponding acceleration offset is 120 G, using the scale factor of the accelerometer array with top metal. Dividing the residual offset acceleration (i.e., 120 G) with the signal-to-noise ratio of the modulation voltage source (i.e., V_{m0} /$\sqrt{\overline{v_{n,m}^2}/\Delta f}$) yields the resultant acceleration noise due to modulation voltage source ($\sqrt{\overline{a_{n,m}^2}/\Delta f}$), assuming complete phase noise cancellation and zero amplitude noise contribution during demodulation. A higher the signal-to-noise ratio of the modulation voltage source results in a lower the acceleration noise contribution. Assuming a

modulation voltage source with 0.9 V amplitude (i.e., 1.8 V peak-to-peak) and maximum 10 μV/√Hz noise floor at low frequencies (e.g., < 10 Hz), the acceleration noise floor is 1.3 mG/√Hz. The analysis shows that the modulation voltage noise contribution to the acceleration noise floor is negligible when the transducer offset cancellation scheme simultaneously cancels the modulation voltage noise at the output under the assumption that the modulation voltage noise at different nodes (i.e., $\sqrt{\overline{v_{n,m1}^2}/\Delta f}$ to $\sqrt{\overline{v_{n,m4}^2}/\Delta f}$) is correlated. When the transducer offset cancellation scheme is not used, the expected acceleration noise floor should be calculated based on the real offset acceleration instead of the residual offset signal. A high-G accelerometer design implies a significant offset acceleration even for a small lateral curl in the proof mass springs. However, as the example time domain measurement in Chapter 5 shows, the measured offset signal at the output is always below 100 mV even without any attempt for offset cancellation implying negligible lateral curl (i.e., < 5nm).

The thermomechanical noise of the designed accelerometer cell (i.e., 0.15 mG/√Hz) leads to 28.3 μG/√Hz acceleration noise floor per circuit input after noise averaging across 28 cells of the half array. The differential acceleration noise floor of the transducer ($\sqrt{\overline{a_{n,tr}^2}/\Delta f}$) is 40.0 μG/√Hz by adding the noise power contributions from the two sides of the capacitive bridge. Given all the other noise sources mentioned above (that adds up to 40.4 mG/√Hz), the thermomechanical noise floor of a single accelerometer cell (i.e., 0.15 mG/√Hz) is negligible and averaging across multiple cells is not needed. However, multiple accelerometer cells are needed to reach micro-G resolution if the circuit noise floor is reduced or the accelerometer cells are made more compliant.

Increasing the number of accelerometer cells in the array increases the total sense capacitance, thereby allows increasing the input transistor sizes for improved circuit noise

performance. Using larger input transistors reduces the input-referred noise floor of the readout circuit while simultaneously reducing the scale factor of the transducer due to increased parasitic capacitance. The signal to noise ratio can be maximized by sizing the input transistors in accordance with the total sense and parasitic capacitance of the transducer and the limiting noise source in the circuit [71]; however, such an optimization is not performed for the characterized accelerometer array in this study.

Table 2.4. Summary of accelerometer gain and noise sources assuming 100 kHz modulation

	Design Value
Transducer scale factor with top metal (S_T)	1.24 μV/G
Combined gain of amplifiers (G_C)	336 V/V
Noise from on-chip amplifier ($\sqrt{\overline{a_{n,A1}^2}/\Delta f}$)	3.2 mG/√Hz
Noise from input biasing resistors ($\sqrt{\overline{a_{n,Rb}^2}/\Delta f}$)	40.3 mG/√Hz
Noise from modulation voltage sources ($\sqrt{\overline{a_{n,m}^2}/\Delta f}$)	1.3 mG/√Hz
(56 Cells) Transducer noise ($\sqrt{\overline{a_{n,tr}^2}/\Delta f}$)	40.0 μG/√Hz
Total equivalent acceleration noise ($\sqrt{\overline{a_{n,tot}^2}/\Delta f}$)	40.4 mG/√Hz

The estimated transducer scale factor with top metal, the combined gain of the amplifier stages and the estimated noise contributions from the defined noise sources are summarized in Table 2.4. The total estimated equivalent acceleration noise for the array ($\sqrt{\overline{a_{n,tot}^2}/\Delta f}$) is calculated as 40.4 mG/√Hz by adding the noise powers of the individual noise sources. The acceleration noise can be approximated as white as long as the phase noise of the modulation voltage waveform is cancelled to a great extent and the amplitude noise of the modulation voltage source exhibits white noise behavior. The estimation assumes 100 kHz modulation frequency and sets an upper bound

on the accelerometer noise floor. The bandwidth of the on-board amplifier used in the testbed is around 800 kHz, therefore the noise characterization is made at 625 kHz modulation frequency generated by using a high stability clock source at 10 MHz as discussed in Chapter 5. The estimated on-chip amplifier noise at 625 kHz is 2 mG/√Hz and the biasing resistor noise is 10 mG/√Hz leading to an estimated accelerometer noise of 10.2 mG/√Hz.

2.5.5 Allan Deviation and Bias Stability

The noise sources considered so far are expected to lead to a white noise profile at the accelerometer output, implying a fixed noise density across the signal bandwidth. In this case, the root-mean-square (rms) noise observed in time domain is expected to change proportional to the square-root of the signal bandwidth such that the resolution of the accelerometer can be increased simply by reducing the bandwidth when the application allows. However, frequency dependent noise is expected to dominate the acceleration signal spectrum at low frequencies even when the readout circuitry is designed to contribute only white noise. Environmental variations (e.g., temperature, humidity, pressure and stress variations), charge accumulation, exposure to magnetic field or radiation can lead to variations in the accelerometer output over long time frames. Besides, the aging of the accelerometer over time (e.g., creeping top metal at the anchors of the accelerometer cells upon repeated exposure to stress due to shock pulses) can change the transducer response to acceleration or environmental variations, hence adding on the long-term variations of the sensor output. These effects may not be observable in a short time frame if the variations at the accelerometer output are insignificant compared to the white noise. However, the output signal is expected to drift when the accelerometer is allowed to run for a long time (e.g., minutes, hours or days). The drift of the output signal at zero input acceleration is called bias drift.

The long-term components of drift (e.g., $1/f$, $1/f^2$, etc.) cannot be suppressed simply by reducing the bandwidth, hence setting the resolution of the accelerometer over long averaging times.

The noise power density at the accelerometer output can be measured by using a spectrum analyzer at frequencies down to about 1 Hz. However, the bias drift of the accelerometer may become dominant to white noise only after minutes of operation. The observation of the noise at very low frequencies (very long times) requires equally small resolution bandwidth for the spectrum analyzer, hence making such measurements with that equipment impractical. Instead, the noise is analyzed using time-domain data collected over long times. One way of quantifying the noise in the collected data is calculating the power spectral density, which can be made by using software tools like MATLAB® (The MathWorks, Inc., Natick, MA). An alternative way of analyzing the effect of the frequency dependent noise on the sensor output is using Allan variance, which is a type of two-sample variance. Allan variance was first adopted as a statistical tool to quantify the long-term frequency stability of precision oscillators as explained in great depth in [110]. However, it is an equally useful tool for estimating the long-term drift behavior of any sensor, including inertial sensors. The calculation of Allan variance is based on the difference between two consecutive time domain samples of the sensor signal. The sampling period used for collecting the data is called the integration time (τ_0) and the calculated Allan variance becomes valid only for this integration time. The Allan variance at different integration times can be evaluated by collecting the data at different sampling rates. In order to eliminate the need for repeated data collection with various sampling rates, the originally collected data (x_1, x_2, x_3, …, x_N) is divided into bins with m samples (e.g., one bin includes: x_{i+1}, x_{i+2}, x_{i+3}, …, x_{i+m}) and the average of each bin is taken (e.g., $\overline{x_i}$) to see the effect of increasing the integration time (by a factor of m)

on the signal profile. Given N data points collected with τ_0 sampling period, Allan variance at $m\tau_0$ integration time is found by using N/m non-overlapping bins as follows:

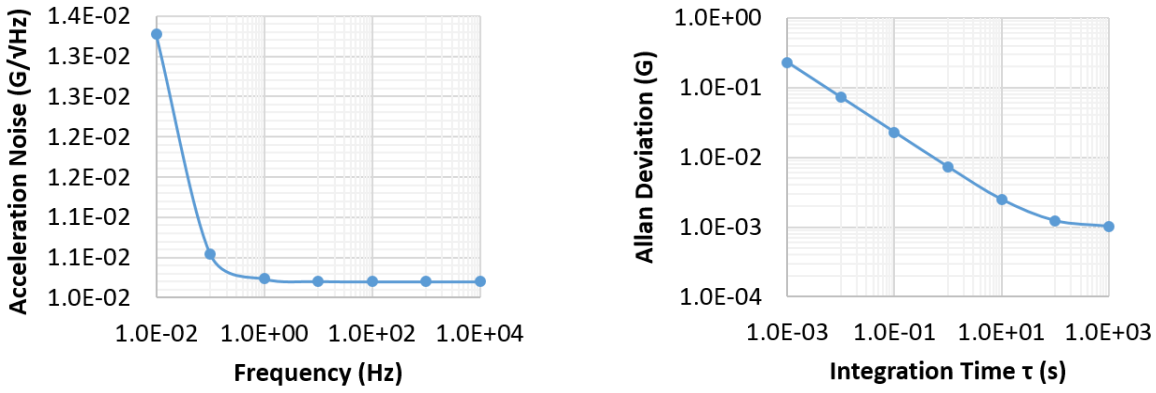
$$\sigma(m\tau_0)^2=\frac{1}{\frac{N}{m}-1}\sum_{i=1}^{\frac{N}{m}-1}\frac{(\overline{x_{i+1}}-\overline{x_i})^2}{2} \tag{2.36}$$

It is also possible to create bins with overlapping data points to generate a higher number of bins and improve the confidence intervals on the Allan variance calculation; however, this study uses non-overlapping bins and follows the formulation given in (2.36).

Allan deviation is obtained by taking the square-root of the Allan variance of the data. The profile of the change in Allan deviation as a function of integration time helps with predicting the type of noise in the system. The conversion between Allan deviation and noise power spectrum of the data is made by using simple closed-form expressions under certain assumptions as explained in [110]. This study is particularly interested in the observation of the limiting effects of f^{-2} (i.e., random-walk), f^{-1} (i.e., flicker) and f^{0} (i.e., white) noise on the stability of accelerometer bias and scale factor. Output fluctuations due to white noise can be reduced by limiting the measurement bandwidth, which shows up as a reduction in Allan deviation inversely proportional to the square-root of integration time (i.e., $\tau^{-1/2}$). On the other hand, flicker noise leads to a fixed Allan deviation that cannot be reduced with averaging. Random-walk noise leads to a rise in Allan deviation proportional to the square-root of integration time (i.e., $\tau^{+1/2}$), implying that the drift of the output signal is expected to increase over long time frames.

The minimum Allan deviation that can be obtained by tuning the integration time gives the maximum possible stability for the sensor measurements, hence called “bias stability”. Figure 2.26 shows the targeted acceleration noise spectrum and the corresponding Allan deviation plot for the

accelerometer when the modulation frequency is set to 625 kHz. The estimated white noise floor at 625 kHz sets the Allan deviation at short integration times. Improving the bandwidth of the testbed circuits to allow higher modulation frequencies can reduce the white noise floor, hence the Allan deviation at short integration times. The drift in the bias and scale factor of the accelerometer sets the Allan deviation and bias stability at longer integration times. The navigation standard macro-electromechanical accelerometers are demonstrated to provide up to 156 dB dynamic range (e.g., Honeywell Q-Flex® QA2000-030 has < 1 μG bias stability and 60 G input range). Given the 50 kG designed input range of the accelerometer cells, 1 mG bias stability is a realistic target for the first demonstration of a high dynamic range CMOS-MEMS accelerometer. The bias and scale factor drift is expected to be dominated by environmental variations. The compensation of the environmental variations by using the on-chip auxiliary sensor measurements should improve the bias stability to milli-G levels (e.g., 1 mG is targeted in Figure 2.26). The dynamic range of the designed accelerometer system is expected to go up to 154 dB after compensation.



(a) (b)

Figure 2.26. (a) Targeted acceleration noise spectrum and (b) corresponding Allan deviation for the accelerometer when the modulation frequency is set to 625 kHz.

2.6 Array Design for Reduced Ring-Down Time

The small accelerometer cell design implies a small mass per cell that keeps the stress at the anchors below the fracture strength of oxide and ensures the survival of the cells upon high-G events. On the other hand, the small damping in the accelerometer lead to an inherently underdamped system with around 0.8 ms ring-down time for the transient oscillations at the resonance frequency (118 kHz). While these oscillations superpose on the acceleration signal, they can be attenuated by low-pass filtering as long as they are outside the acceleration signal bandwidth of interest (e.g., 20 kHz). To increase the signal bandwidth further, the arrayed design used in the accelerometer system provides a degree of freedom for varying the resonance frequencies of individual accelerometer cells in the array and introducing incoherence between their ring-down oscillations. Such tuning of the resonance of individual cells modifies the ring-down profile of the acceleration signal and can reduce the ring-down time significantly, alleviating the specifications on low-pass filtering.

The resonance frequencies of the accelerometer cells are more sensitive to variations in spring beam dimensions (that lead to variations in spring constant) compared to variations in truss and/or folded-beam dimensions (that lead to variations in mass). Introducing significant variations in resonance frequency (e.g., doubling) by varying the mass implies significant changes in the accelerometer design. Such variations in resonance frequency are obtained more easily by designing each cell's spring beams with a different width increment. Increasing the range of resonance frequencies implemented on the accelerometer array reduces the ring-down time and decreases the energy under the ring-down curve of the array; however, higher resonance frequencies also imply reduced acceleration sensitivity and lead to a trade-off between sensor speed and resolution. This trade-off can be made based on a figure of merit that compares the

squared-sensitivity to the energy under the ring-down curve of the array. Since the sensitivity of the array is proportional to the averaged m/k ratio (i.e., $1/\omega_0^2$) of individual cells, the ratio of the mean-square (m/k) to energy under the ring-down curve is defined as the figure of merit of the system. Different frequency staggering schemes are evaluated based on the desire for the highest figure of merit (i.e., simultaneous high sensitivity with low energy under the ring-down curve).

The process variations introduce measurable random variations in the spring beam width. The spring beams of four consecutive accelerometer cells (i.e., 8 beams in total) are imaged on one of the preliminary chip designs fabricated in the same CMOS process (Figure 2.27 (a)) in order to estimate the standard deviation of the spring beam width. High contrast scanning electron microscope images are taken at the truss-end, anchor-end and center area of the beams (Figure 2.27 (b)). The images are converted to black and white (i.e., binary) format in MATLAB as shown in Figure 2.27 (c) and the width of the spring beam segments are determined by counting the number of white pixels in the images instead of measuring manually. The length correspondence of a single pixel is determined by dividing the length of the scale bar in the images with the total number of pixels in the scale bar. The measurements taken from the three beam segments are averaged to obtain the width of each beam. The standard deviation of the spring beam width measurements is 15.8 nm, which is very close to the measurement resolution (i.e., 15.5 nm/pixel). As an estimate of a maximum limit, the standard deviation of the spring constant is estimated to be 0.25 N/m and the standard deviation of the mass of an accelerometer cell is estimated to be 2.82×10^{-14} kg by assuming the same standard deviation for the entire accelerometer cell geometry, and ignoring deviations in height and individual CMOS layer thicknesses. The estimated standard deviation of the resonant frequency is calculated as 1.44 kHz, which is dominated by the standard deviation of the spring constant.

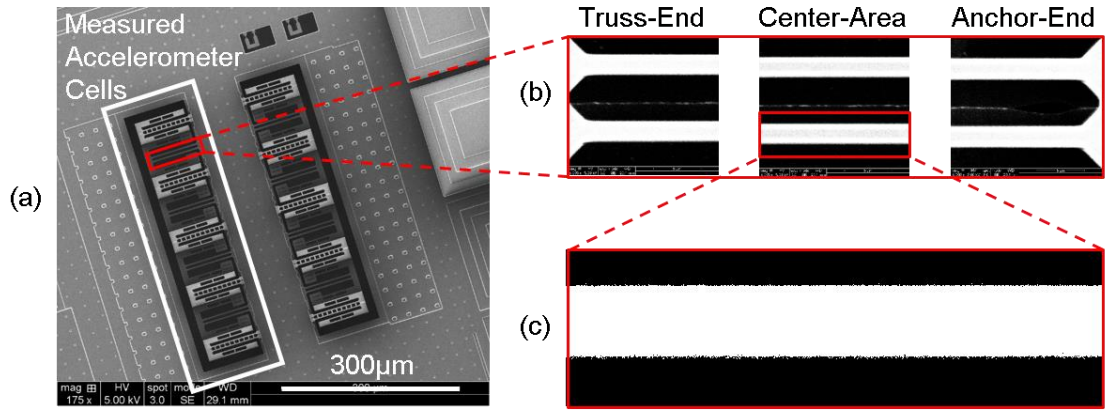


Figure 2.27. (a) Preliminary accelerometer array used for the estimation of the standard deviation of the spring beam width. (b) Example high contrast scanning electron micrographs of spring beam segments. (c) Example black and white image used for determining the segment width by counting the white pixels.

As inherent variation is relatively small, the ring-down time can be altered by intentionally designing each cell to have a different resonant frequency. An example array with 312 accelerometer cells is designed to demonstrate the theoretical improvement in sensor speed, albeit not fabricated and verified experimentally. The implemented resonance frequencies are constrained to stay between 120 kHz and 240 kHz, so that the sensitivity of any given accelerometer cell in the array is no more than four times lower than that of a "standard" 118 kHz accelerometer cell. The frequency range is divided into twelve bins with 10 kHz increments (Figure 2.28) and each bin is assigned an even number of cells that adds up to 156 cells and forms one side of the capacitive bridge. The number of accelerometer cells in each bin is set inversely proportional to the sensitivity of the cells, such that the reduced signal amplitude of the stiffer accelerometer cells is compensated by using a higher number of such cells so that the superimposed response is ensured to have similar amplitude contributions from different frequency components. An even number of identical accelerometer cells in the half bridge ensures that the cells can be interdigitated to average the linear process variations across the array, although no

such variations are observed in the measurements taken on the eight cell array. The two sides of the capacitive bridge are made identical (i.e., the designed half bridge is replicated), so that a differential accelerometer bridge can properly cancel the common-mode environmental effects. The inherent random variations in the mass and spring beam width lead to random resonance frequency variations between the accelerometer cells, which reduce the ring-down time and increase the figure of merit by about five times compared to having perfectly identical cells as seen on the step response of the accelerometer array to 50 kG acceleration (Figure 2.29). However, deliberately staggering the resonance frequencies of groups of accelerometer cells further improves the ring-down behavior as indicated by an order of magnitude higher figure of merit (Figure 2.29).

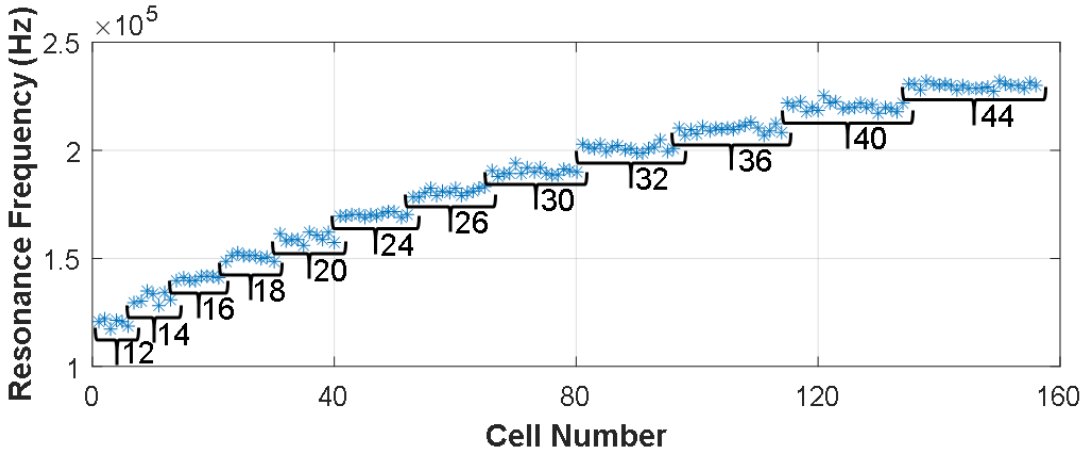


Figure 2.28. Resonance frequency staggering across the half bridge in 120 kHz – 240 kHz range.

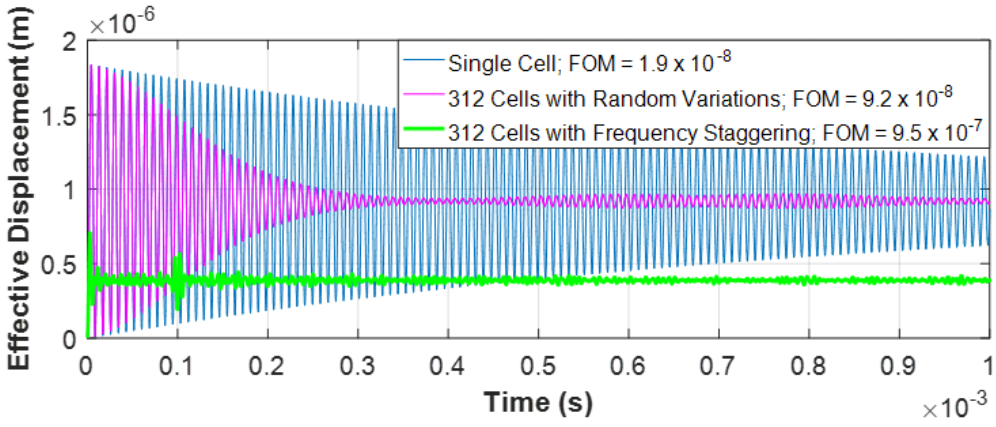


Figure 2.29. Improved step response with frequency staggering.

The response of the accelerometer array to a 400 μs long half-sine acceleration pulse with 50 kG amplitude is simulated with a subsequent second-order Butterworth filter with 50 kHz cut-off frequency (Figure 2.30). The frequency-staggered array significantly suppresses the ring-down oscillations compared to oscillations from a similarly sized array with (or without) random variations. The frequency-staggered array has 2.4 times lower sensitivity compared to a standard accelerometer cell design (with 118 kHz resonance frequency); however, the reduction in sensitivity may be a tolerable trade-off given the significant improvement in sensor speed. The figure of merit used for comparing the transient responses can be modified for any desired system specification to design the optimum solution.

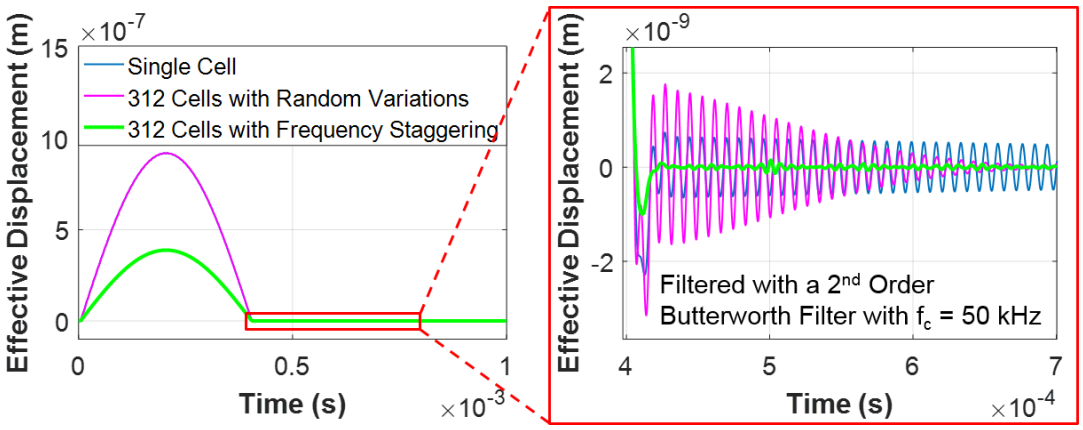


Figure 2.30. Transient response of a frequency staggered accelerometer array to a 400 µs long half-sine acceleration pulse.

2.7 Alternative Single-Mass Design

Taking the 56 cell accelerometer array as reference, a single-mass accelerometer is designed (Figure 2.31) to match the mass and the spring constant of half array (i.e., 28 cells) that connects to one input of the readout circuit. The rotor is designed by arraying 25% empty square pieces such that the proof mass has 5 µm × 5 µm holes in every 5 µm, so that the silicon etch and release steps can be performed easily during post CMOS-MEMS processing. The mass of the rotor matches the total mass of 28 accelerometer cells in half array. The spring beams have the same dimensions as the ones used in the arrayed design. There are two spring beams per cell in the arrayed design that adds up to 56 beams for half array. The same number of beams are distributed on the two sides of the single-mass design (i.e., 28 spring beams on each side). Having the large proof mass anchored through the spring beams on both sides should lead to guided-end displacement and parallel-plate motion of electrodes as in the arrayed design. Since the ratio of spring constant to mass is preserved, the calculated resonance frequency (i.e., $\omega_0 = \sqrt{k/m}$) of the single-mass design and hence the rotor displacement for a given acceleration is equal to that of an accelerometer cell in the array. Since the anchor area of the spring beams, the force per spring for

a given acceleration and the resultant displacement are preserved, the stress on the spring beams is expected to be the same as in the arrayed design and the single-mass design is expected to survive at 50 kG target maximum input acceleration. The single-mass design also allows routing the acceleration signal and modulation voltages through different anchor areas as in the case of the arrayed design, therefore the feedthrough from the modulation voltages to the signal line can be minimized in both cases.

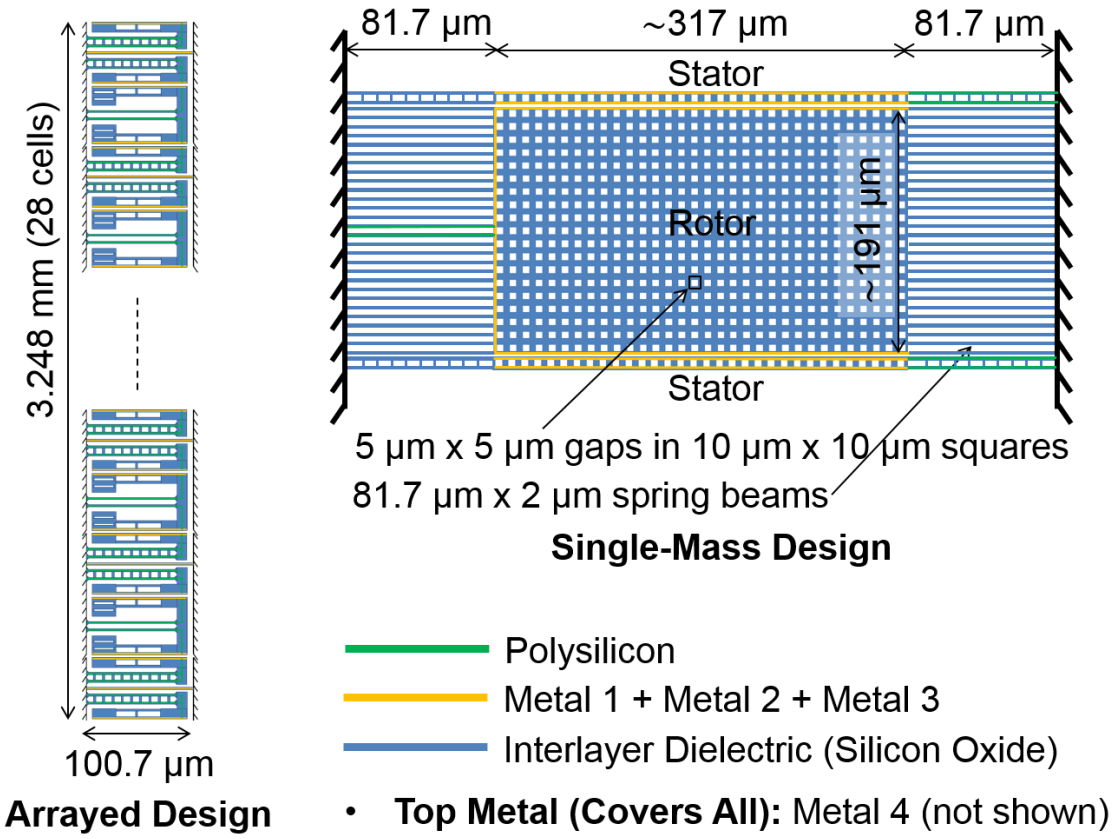


Figure 2.31. Single-mass accelerometer design compared to arrayed design.

Curl mismatch between the rotor and stators is a potential problem for the single-mass design. The spring beams of the rotor and stators are expected to curl similarly as in the arrayed design; however, the narrow stators in the single-mass design can go through additional buckling upon release. The stators can be made wider to minimize the buckling at the expense of increased

area. Matching the stator design exactly to the rotor design would triple the area and lead to a similar device footprint as the arrayed design, hence eliminating the area advantage of the single-mass design.

Another important problem with the single-mass design is the increased ring-down time. The ring-down time is proportional to the ratio of mass to damping coefficient (i.e., $\tau = 2m/b$) for a second-order underdamped system. The mass of the single-mass accelerometer is equal to the total mass of the accelerometer cells in half array. However, the damping is expected to be lower than the total damping exerted on the cells in half array hence increasing the ring-down time. Stokes damping scales proportional to the top and bottom surface area of the device as discussed in section 2.1.2, therefore the total Stokes damping exerted on the accelerometer cells in half array should be approximately the same as that exerted on the single-mass design. However, squeezed-film damping scales proportional to the total electrode length, thereby it is 7.6 times lower for the single-mass design compared to the total squeezed-film damping exerted on the cells in half array. Therefore, the mass to damping ratio and hence the ring-down time becomes 3.2 times higher for the single-mass design. The individual accelerometer cells in the arrayed design allows frequency staggering by varying the width of the spring beams, which is an additional degree of freedom to reduce the coherence between the ring-down oscillations of individual accelerometer cells, thereby further reduce the ring-down time. On the contrary, spring beams of the single-mass design effectively form a single spring and inherently average all the variations, hence not allowing any improvements in ring-down behavior.

The thermomechanical noise floor scales proportional to the ratio of square root of damping to mass (i.e., $\sqrt{b/m}$) and inversely proportional to the number accelerometer cells connected in parallel as discussed in section 2.1.2. Given the same total mass for the single-mass and arrayed

designs, the 3.2 times reduction in total damping leads to 1.8 times lower thermomechanical noise floor for the single-mass design. The arrayed design would require 3.2 times more cells (i.e., 90 cells) and hence 3.2 times larger area than the current design (i.e., 10.7 times larger area than the single-mass design) to average the thermomechanical noise to the same level.

The sense capacitances of individual accelerometer cells are added up in the arrayed design. Given the same capacitive gap and device height for all cells, the sense capacitance scales with the total electrode length (i.e., the electrode length per accelerometer cell times the number of cells). The electrodes are 85.7 μm long on the accelerometer cells and add up to 2.4 mm for 28 cells, whereas the electrode length is only 317 μm on the single-mass design, which leads to 7.6 times reduction in sense capacitance. However, the arrayed design requires signal routing through the whole array (i.e., 3.248 mm long) for connecting the accelerometer cells together before the signal is input to the readout circuit. The readout circuit can be placed close to the single-mass design and the routing length can be reduced (e.g., up to 10 times) to reduce the routing capacitance, thereby preserve the ratio of routing capacitance to sense capacitance and get similar acceleration sensitivity when the routing capacitance is the dominant source of parasitic capacitance. On the other hand, when the circuit input transistors are sized to improve the noise performance, the parasitic capacitance is likely to be dominated by the circuit input capacitance instead of the routing capacitance. Assuming both the sense capacitance and the routing capacitance are reduced by 7.6 times in the single-mass design, the calculated scale factor of the transducer reduces from 1.29 μV/G (i.e., the scale factor of the arrayed design) to 0.22 μV/G when interfaced with the preamplifier used in this study. The circuit input capacitance can be reduced (e.g., by 7.6 times) to restore the scale factor; however, smaller input transistors lead to a higher circuit noise floor and a lower signal to noise ratio as discussed next.

The white noise and flicker noise of a CMOS transistor are modeled at the transistor gate as [144]:

$$\sqrt{\overline{v_{n,CMOS}^2}} = \sqrt{\frac{4k_B T\delta}{g_m}} + \sqrt{\frac{K}{C_{ox}WL}\frac{1}{f}} \tag{2.37}$$

where k_B is the Boltzmann constant, T is the absolute temperature, C_{ox} is the gate-oxide capacitance per unit area, W is the transistor width, L is the transistor length, δ and K are process dependent parameters and g_m is the transconductance of the transistor given as [145]:

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th}) \tag{2.38}$$

where μ_n is the mobility of electrons, V_{GS} is the gate to source voltage of the transistor and V_{th} is the threshold voltage needed to turn on the transistor. The transconductance of the transistor can also be written as a function of drain current (I_D) to observe the relationship between the transconductance and power consumption (power consumption is determined by the current drawn from the power supply for a given supply voltage):

$$g_m = \frac{2I_D}{V_{GS} - V_{th}} \tag{2.39}$$

The input transistor length (L) of the preamplifier used in this study is set to the minimum possible length in the CMOS process (i.e., 180 nm), thereby the transistor size and input capacitance are reduced by decreasing the transistor width (W). Reducing the capacitance of the input transistors by 7.6 times restores the scale factor of the single-mass design to 1.29 μV/G at the expense of increasing both the flicker noise and thermal noise by 2.8 times (i.e., proportional to $1/\sqrt{W}$), hence decreasing the signal to noise ratio. The resolution of the accelerometer and hence the dynamic range is improved by minimizing the readout circuit noise and maximizing the transducer scale factor simultaneously. Taking (2.37) as reference, the circuit noise is minimized

by maximizing the input transistor width in accordance with the power budget. Once the circuit noise is minimized and the circuit input capacitance is set, maximizing the sense capacitance becomes crucial for improved acceleration resolution.

The scalability of the arrayed design allows increasing the sense capacitance proportional to the number of cells used in the array at the expense of increased area. On the other hand, a single-mass design needs to be resized carefully when a higher sense capacitance is desired. The single-mass design in Figure 2.31 is modified to increase the sidewall area and hence the sense capacitance (Figure 2.32) to demonstrate some of the problems. The modified design is comparable to a full array in terms of the sense capacitance. The rotor and stator comb fingers overlap for 85.7 μm of their length with 2 μm spacing, thereby the sense capacitance and squeezed-film damping per side are similar to that obtained in the arrayed design. The comb-fingers are made 20 μm wide in order to increase their resonance frequency and reduce their displacement upon acceleration. The width of the rotor is set as 200 μm to provide high stiffness in the vertical direction, which leads to 3.3 times larger mass than that of the arrayed design and requires 3.3 times more spring beams in parallel to preserve the resonance frequency. Using the same spring beam design requires placement of 366 spring beams, which increases both the rotor area and the mass. The spring beam width is increased to 4 μm and 44 spring beams are used in the single-mass design to keep the area around 1.5 times smaller compared to the arrayed design (excluding the anchor area needed on the sides in both cases), since reduced area is the most prominent motivation for a single-mass design. Although the overall area is smaller, all the proof mass area contributes to Couette and Stokes damping in the single-mass design, hence increasing the total damping and thermomechanical noise of the single-mass design above that of the arrayed design.

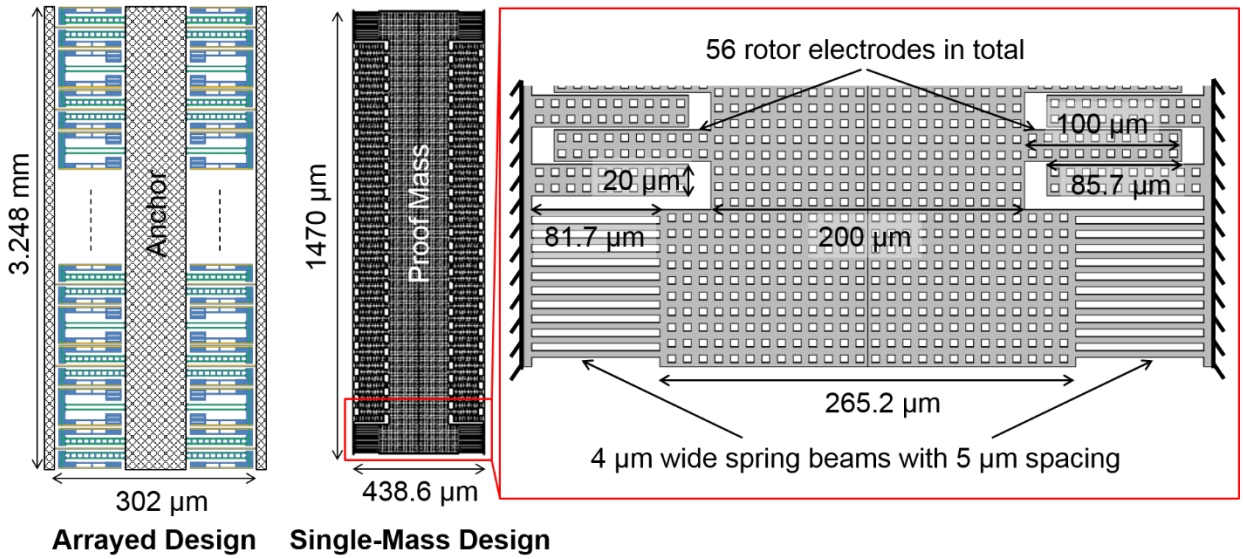


Figure 2.32. Larger single-mass accelerometer design with higher sense capacitance.

The mode shapes of the four modes closest in frequency to the desired mode are shown in Figure 2.33. The low frequency modes of the large proof mass need to be suppressed to improve linearity and minimize cross-axis sensitivity. To that end, the spring beam thickness can be increased by using higher metal layers where possible and the proof mass can be anchored at multiple points through its length. The small number of spring beams also leads to 8.3 times larger force per spring beam in this design for only 2 times larger cross-sectional area, hence implying higher amount of stress at the anchors upon shock events. Curl mismatch between the rotor and stators is another obvious problem in this design, since the vertical curl of the spring beams only displaces the rotor.

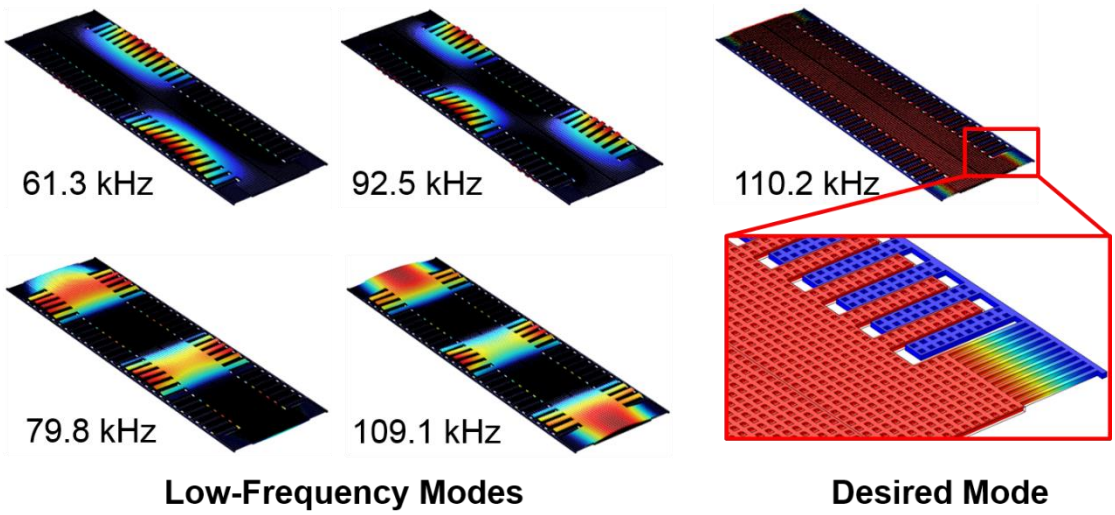


Figure 2.33. Low-frequency modes of the larger single-mass accelerometer design.

In conclusion, a single-mass design can occupy a smaller area compared to an arrayed design. However, curl mismatch between the rotor and stators is a potential problem for a single-mass design that can reduce the bias stability. Frequency staggering is not an option for a single-mass design, therefore the burden of filtering the ring-down oscillations increases for the low-pass filter. The input-referred sensitivity of a single-mass design is likely to be limited by the parasitic capacitance when the input transistors are sized to minimize the circuit noise floor within the power budget. Increasing the sense capacitance of a single-mass design leads to device dimensions comparable to an arrayed design and introduces additional low frequency modes on the large suspended proof mass. On the contrary, an arrayed design is easily scaled by connecting more accelerometer cells in parallel to obtain the desired sense capacitance. The higher degrees of freedom in design, easier curl matching between the small rotor and stators, and improved ring-down behavior of the arrayed design makes it preferable in this study to improve the bias stability and measurement bandwidth for high dynamic range operation.

CHAPTER 3: POST-CMOS MEMS PROCESS FOR THE CAPACITIVE ACCELEROMETER ARRAY

3.1 Standard Process Flow

The standard post-CMOS MEMS processing steps are described in [11], and illustrated in Figure 3.1 for a sample accelerometer array fabricated in this study. The mechanical structures are composed of metal-dielectric layers of the CMOS process. Different number of layers can be used at different parts of the design, which provides flexibility to satisfy the design requirements. The first processing step is the anisotropic dry etch of the dielectric (i.e., silicon oxide) in fluorine chemistry (i.e., CHF_3 and O_2 with optional CF_4 gases in the etch chamber). The top metal layers, which can be different layers at different parts of the chip, get exposed to the plasma in the chamber once the oxide above them is etched and get partially milled through the process (e.g., approximately 350 nm of milling in [11]). The selectivity of the etch chemistry ensures that the oxide is etched down to the silicon substrate before the metal layers are completely milled, which makes it possible to use the top metal layer as an etch mask. The mechanical structures are conveniently defined by the layout of the top metal and no additional mask is needed during the post-processing steps. The minimum width of the defined shapes and the minimum spacing are fundamentally set by the design rules of the CMOS process, both of which reduce as the process node becomes smaller. The thickness of the mechanical structures can be varied from < 1 μm to > 5 μm dependent on the layer thicknesses in the CMOS process and the number of layers used in the design. The silicon substrate underneath the MEMS devices acts as the sacrificial material and is etched in a different fluorine chemistry (i.e., SF_6 and O_2 gases present in the etch chamber) to release the devices. The exposed silicon areas are first etched anisotropically in order to prevent premature release of the structures. Then, the isotropic etch step removes the silicon underneath

the mechanical structures and completes the release process. The isotropic and anisotropic silicon etch times can be adjusted dependent on the dimensions of the structure to be released to set the desired lateral undercut length and the required gap between the released structures and the silicon substrate. The anisotropic silicon etch step can also be completely removed without adversely affecting the process for select devices [11].

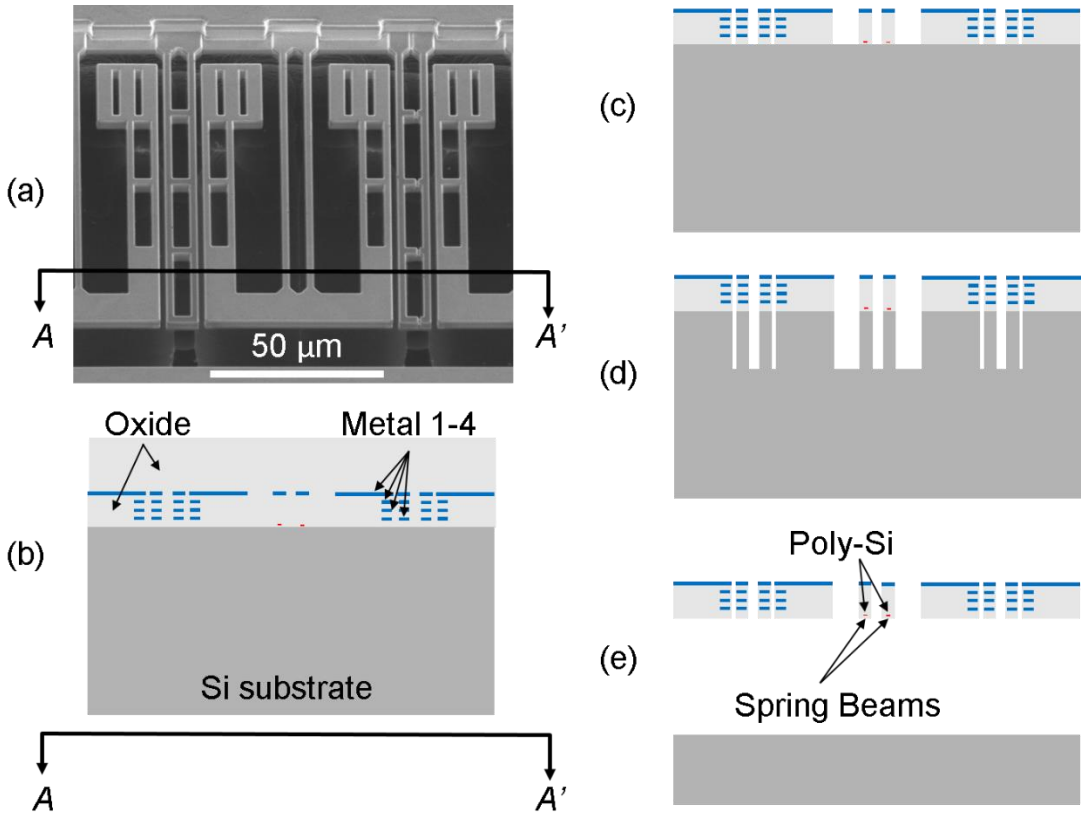


Figure 3.1. Standard post-CMOS MEMS process flow used in the fabrication of accelerometer arrays. (a) a sample accelerometer array. (b) after foundry processing. (c) anisotropic oxide etch. (d) anisotropic silicon etch. (e) isotropic silicon etch for releasing accelerometer cells.

3.2 Process Details for the Accelerometer Array

3.2.1 Oxide Etch of 2.5 mm × 2.5 mm Chips

The oxide etch is run in the Plasma Therm 790 reactive ion etch (RIE) system by using the CHF_3, CF_4 and O_2 gases. The chamber is pumped down for 2 h before starting the process in order

to minimize the moisture (i.e., the amount of hydrogen) in the chamber, since hydrogen can react with fluorine radicals in the plasma to form HF and attack the metals, oxide and adhesion layers through the long oxide etch step if not pumped down properly.

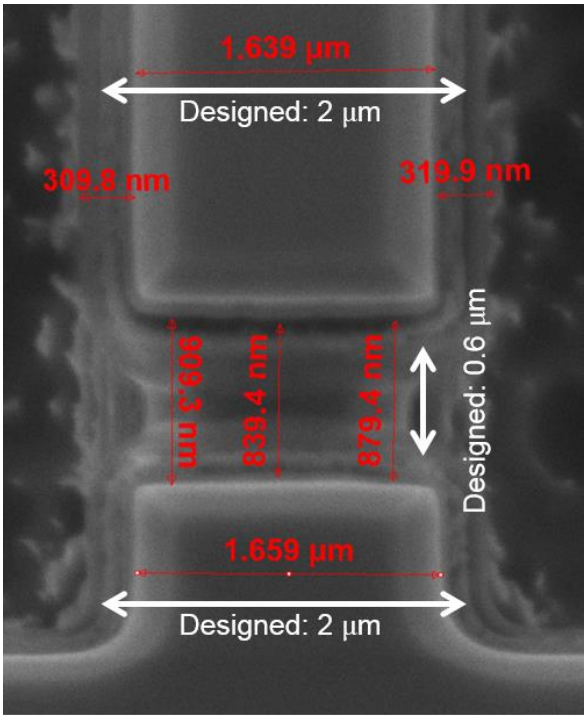
Table 3.1. Oxide etch process details

	O_2 (sccm)	**CF_4 (sccm)**	**CHF_3 (sccm)**	**Pressure (mTorr)**	**RF Power (W)**	**DC Bias (V)**	**Time (min)**
Pressure stab.	50	10	10	100	-	-	2
Gas stab. (×3)	95	20	20	100	-	-	5
Gas stab. (×1)	95	20	20	100	-	-	10
Oxide etch	95	20	20	100	68	280	360
O_2 purge	20	0	0	250	-	-	1
O_2 clean	20	0	0	250	100	300	15

The details of the oxide etch process are provided in Table 3.1. First, the chamber pressure is stabilized to 100 mTorr by pumping the etch gases (i.e., CHF_3, CF_4 and O_2) into the chamber. The pressure stabilization step is followed by three cycles of gas stabilization steps. The chamber is evacuated for 10 min after each cycle and finally filled with the etch gases through another 10 min gas stabilization step before the plasma is ignited. Once the plasma is ignited, the main oxide etch step is run with 68 W RF power and 280 V DC bias voltage for 360 min. The chamber is evacuated for 5 min upon the completion of the oxide etch step and O_2 is pumped back into the chamber for the following oxygen plasma step. The purpose of the oxygen plasma treatment is to etch some of the polymer deposited on the sidewalls of the accelerometer cells during the long oxide etch step. Although it does not completely remove the sidewall polymer, running it for 15 min helps obtain cleaner sidewalls.

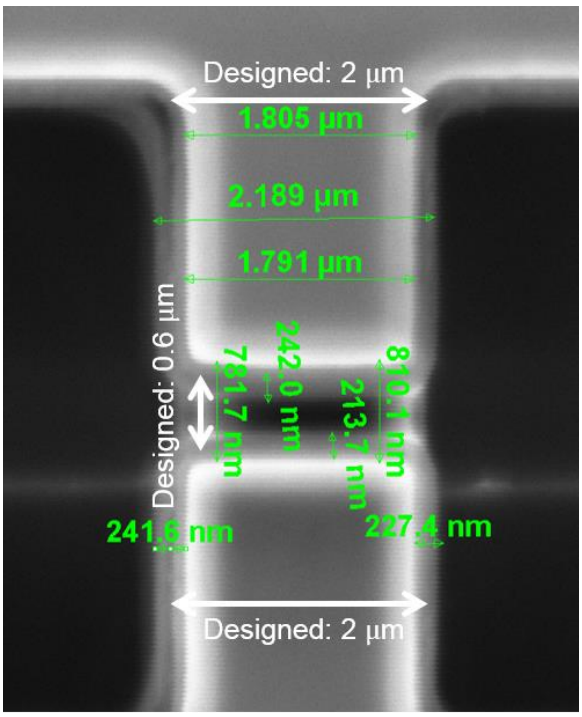
The 360 min oxide etch step can be optionally divided into two steps in order to tweak the gas flow and chamber pressure towards the end of the etch. Reducing the gas flow and the chamber pressure leads to faster removal of the unreacted species from the chamber, hence reducing the polymer formation on the sidewalls. Reducing the pressure also increases the etch anisotropy, thereby can be used for increasing the sidewall steepness at the expense of increased top metal milling.

Figure 3.2 (a) shows the etch results of a 400 min single-step oxide etch process without subsequent oxygen plasma treatment. Figure 3.2 (b) shows the etch results when the etch time is reduced to 360 min, the CHF_3 and CF_4 flow rates are reduced to 10 sccm in the last 10 min of the process and an additional 15 min oxygen plasma treatment is applied. The significant milling of the top metal (~ 175 nm) is reduced by 75 nm and the sidewall polymer thickness (~ 315 nm) is reduced by 80 nm upon the reduction of the etch time and inclusion of the oxygen plasma step. The oxide-etch time and the polymer deposition on the sidewalls should be significantly reduced by using STS Aspect Advanced Oxide Etcher (AOE), which uses inductively coupled plasma for etching the oxide. However, this system has been down for repairs through the course of this study.



Top Metal Milling: ~ 175 nm
Polymer Deposition: ~ 315 nm

(a)



Top Metal Milling: ~ 100 nm
Polymer Deposition: ~ 235 nm

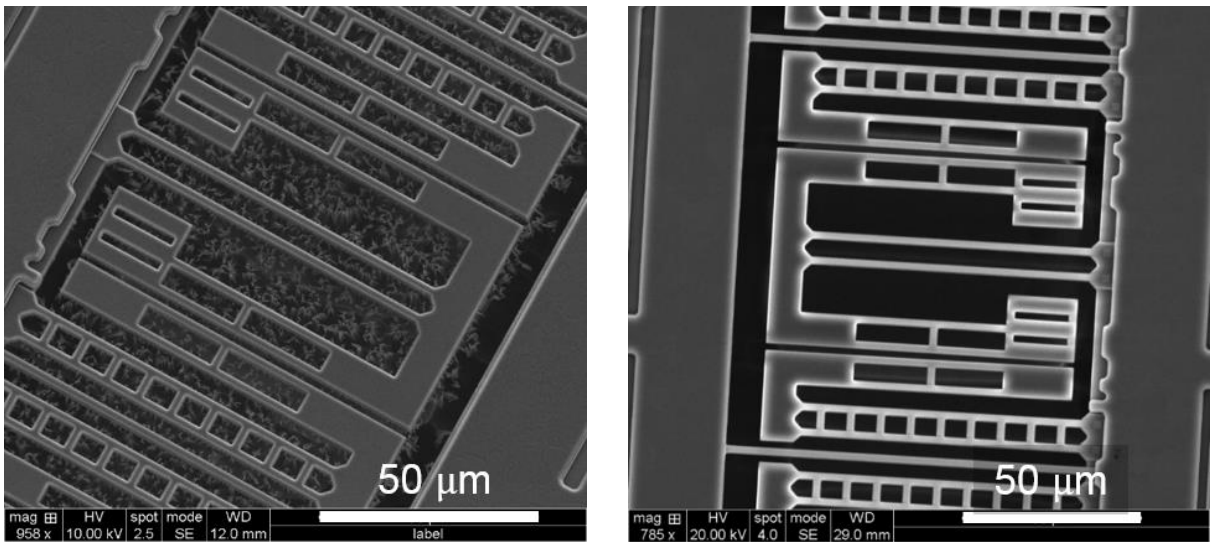
(b)

Figure 3.2. (a) After 400 min single-step oxide etch process. (b) After 360 min oxide etch step with reduced gas flow in last 10 min and additional oxygen plasma treatment for 15 min.

3.2.2 Oxide Etch of 5 mm × 5 mm Chips

The CMOS-MEMS dielectric etch in the Plasma-Therm 790 RIE system leads to aluminum-based polymer re-deposition on the etch area of 5 mm × 5 mm chips (Figure 3.3 (a)) due to the larger exposed aluminum area and increased amount of milling. The polymer re-deposition is a composite material formed by milled aluminum reacting with the CF_4 and CHF_3 gas fed to the RIE chamber. The polymer deposits in the etched field stay after the release process and prevent the accelerometer cells from moving appropriately. These issues are worst in the center of the chip, and are less significant along the sides of the chip where the characterized 56 cell accelerometer array is located. Therefore, the accelerometer cells towards the center of the array

are more affected from this problem compared to the cells at the edges of the array, where the polymer deposits are negligible. Covering the edges of the chip that are not related to the released MEMS devices (e.g., the bond-pad area) with photoresist reduces the total exposed aluminum area on the chip before the oxide etch step and eliminates the re-deposition problem leading to a cleaner etch (Figure 3.3 (b)). The photoresist (e.g., AZ4620 or AZ4400) is painted on the bond pads instead of doing lithography in order to expedite the process. The thickness of the photoresist on the bond pads varies from 3 μm to 5 μm after painting, and gets removed during the oxide etch step in about 90 min. The oxide etch process is periodically interrupted to re-paint a fresh layer of photoresist on the bond pads, with three layers in total painted. Residual resist is cleaned by using acetone at the end of the process.



(a) (b)

Figure 3.3. (a) Aluminum-based polymer re-deposition on the etch area of 5 mm × 5 mm chips during oxide etch. (b) Improved etch results when the bond-pad area is covered with photoresist mask during etch.

3.2.3 Silicon Etch and Release

The anisotropic and isotropic silicon etch steps are run in the STS Multiplex inductively coupled plasma (ICP) RIE system by using the SF_6, C_4F_8 and O_2 gases. The etch recipes used in

the anisotropic etch and release (i.e., isotropic etch) steps are based on [131]. However, instead of fixing the pressure of the chamber, the throttle position is fixed to 58% during the anisotropic etch step and 82% during the isotropic etch step. Fixing the throttle position prevents the system from trying to stabilize the chamber at a fixed pressure level and provides more repeatable results. The anisotropic etch step consists of alternating etch and passivation cycles using the Bosch Deep RIE (DRIE) process [146]. The passivation cycle uses C_4F_8 for the formation of polymer on the sidewalls, which protects the sidewalls from SF_6 gas during the etch cycle hence minimizing the lateral etch and maximizing the etch anisotropy. The etch cycle uses O_2 gas in addition to SF_6 for the removal of the sidewall passivation, hence preventing the passivation from accumulating over etch cycles. The 12 s etch cycles are followed by 8 s passivation cycles in the process. The typical anisotropic etch recipe used in post-CMOS MEMS processes runs for 45 cycles (i.e., 15 min) and results in up to 50 µm etch depth. The silicon etch process is completed by releasing the structures through a silicon isotropic etch step, which uses only the SF_6 gas. The typical 7 min run time leads to 10 µm undercut in the etch area.

Wiring capacitance was simulated with COMSOL by using the finite-element model of the accelerometer cell shown in Figure 2.12. Figure 3.4 (a) illustrates 10 µm and 30 µm isotropic etch depths on the model assuming an initial 45 µm anisotropic etch depth. The capacitance to substrate, shields and top metal (when present) are extracted from the simulations to find the total parasitic capacitance due to acceleration signal wiring per cell. Figure 3.4 (b) shows that increasing the lateral undercut length from 5 µm to 30 µm leads to 58% reduction in the wiring parasitic capacitance if the top metal is removed. The wiring capacitance reduces by only 25% when the top metal is present, since the capacitance to top metal dominates the wiring parasitic capacitance.

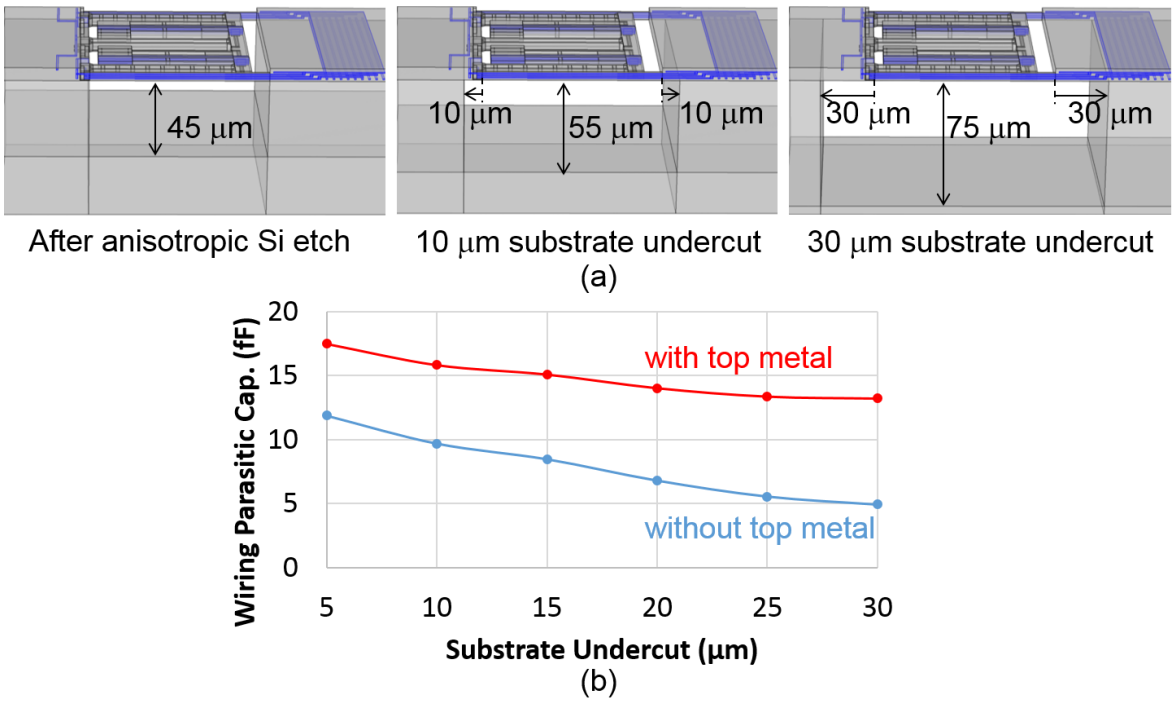


Figure 3.4. Wiring parasitic capacitance simulation. (a) Various isotropic etch depths. (b) Change in parasitic capacitance with substrate undercut.

The accelerometer cells are anchored to a 100 µm-wide silicon area in the designed accelerometer array, therefore the undercut length can be increased up to 30 µm and possibly beyond in order to minimize the parasitic capacitance and maximize the sensitivity. The parasitic capacitance is simulated for 30 µm lateral undercut length and the scale factor is calculated in accordance during the design step. The lateral undercut length can be measured under optical microscope when the top metal is removed; however, the substrate underneath the routing area is not visible when the routing area is covered with the top metal. Release-test structures (Figure 3.5) are used on the chip to help characterize the lateral etch rate of the isotropic etch step and ensure 30 µm lateral undercut length when the top metal is present. These are simple square plates that are spaced from the anchor areas by the same distance as the folded beams of the accelerometer cells are spaced from the anchor area (i.e., 5 µm). The side length of the square plates are made

twice as long as the desired lateral etch depth, since the substrate underneath the plate is attacked by the RIE from all sides. The plates are anchored through narrow and thin spring beams made by using the first metal layer in CMOS, so that the built-in vertical stress gradients in the beams lead to vertical curl upon releasing the square plates. These structures are inspected under optical microscope after completing the release.

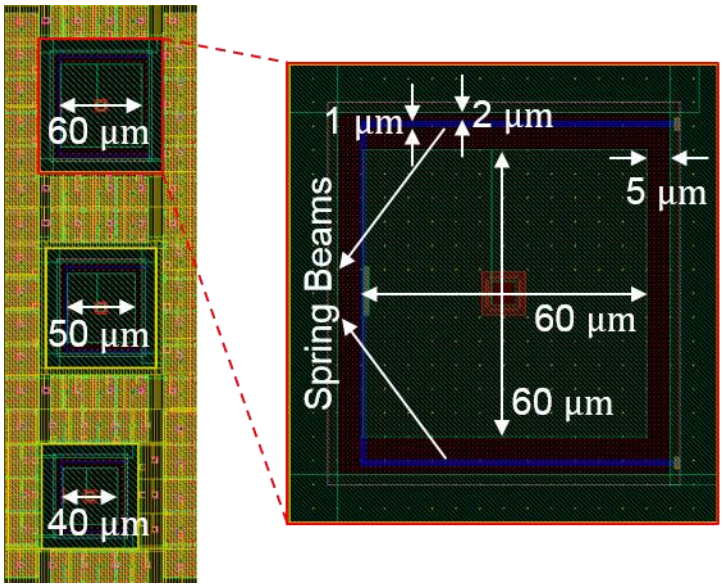


Figure 3.5. Release-test structures used for informing 20 µm, 25 µm and 30 µm undercut length.

The typical isotropic silicon etch time (i.e., 7 min) provides approximately 10 µm lateral undercut as measured under optical microscope (Figure 3.6) after removing the top metal on the chip. Increasing the lateral undercut from 10 µm to 30 µm reduces the estimated routing capacitance per cell from 15.84 fF to 13.22 fF on the chips with top metal and from 9.70 fF to 4.94 fF on the aluminum-etched chips. However, the sensitivity increases only by 5.1% (i.e., from 1.18 µV/G to 1.24 µV/G) on the chips with top metal and by 11.2% (i.e., from 1.16 µV/G to 1.29 µV/G) on the aluminum-etched chips since the parasitic capacitance is dominated by the input capacitance of the readout circuit (e.g., 917 fF capacitance of an input transistor is 3.4 times higher than 271.6 fF total wiring capacitance of 28 cells on the aluminum-etched chips with 10 µm

substrate undercut). Therefore, no particular effort is made in this study to tweak the isotropic etch process and increase the lateral undercut length.

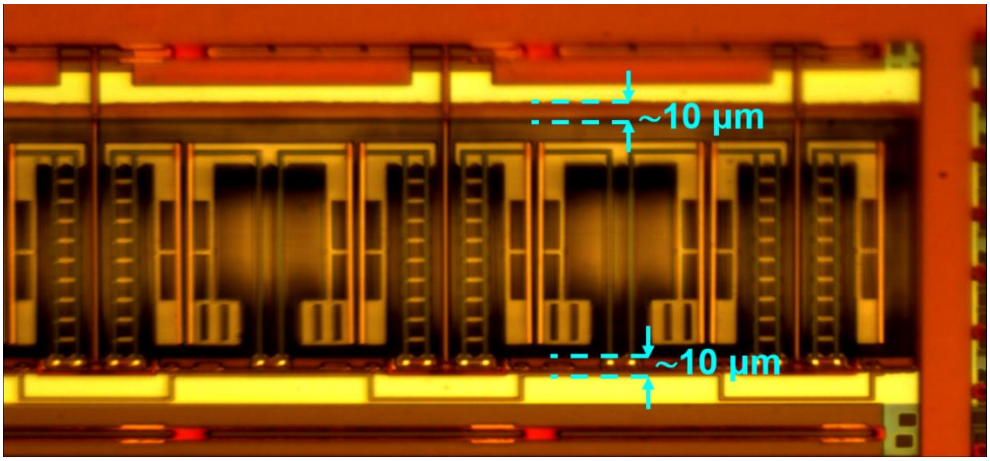


Figure 3.6. Undercut length observed under optical microscope after top metal removal.

3.3 Top Metal Etch for Stability Improvement

The presence of CMOS aluminum on the high-stress regions of the MEMS structures (e.g., anchor- and truss-end points of the accelerometer springs) is a potential source of bias drift at very long integration times (or after high shock) due to the anticipated effect of metal creep on the spring behavior. However, the top metal has to be present over the MEMS devices as a etch mask to define the mechanical structure and it has to be present across the rest of the chip in order to protect the remaining sensors and circuits from exposure to the oxide etch. Once the anisotropic oxide etch is completed, the top metal is no longer needed and can be removed from the chip in order to reduce the risk of metal creep on the accelerometer springs and also reduce the parasitic capacitance introduced by the signal routing (given that the top metal is grounded across the whole chip except for the MEMS areas, where the top metal is connected to the same potential as the MEMS structure).

The removal of the CMOS aluminum in a wet etchant (Transene aluminum etchant A) leads to a different problem: the deposited polymer on the sidewalls of the accelerometer structure during the long oxide etch step in the Plasma-Therm 790 RIE system delaminates and forms randomly distributed polymer stringers. The polymer stringers stay on the structures even after the silicon release step as seen on one of the first-generation accelerometer devices in Figure 3.7. Reducing the aluminum etch time to 4 min does not lead to a significant reduction in the polymer delamination. The delamination problem can be eliminated by etching the sidewall polymer completely by using a post-etch residue remover (e.g., EKC 265) before the wet aluminum etch process.

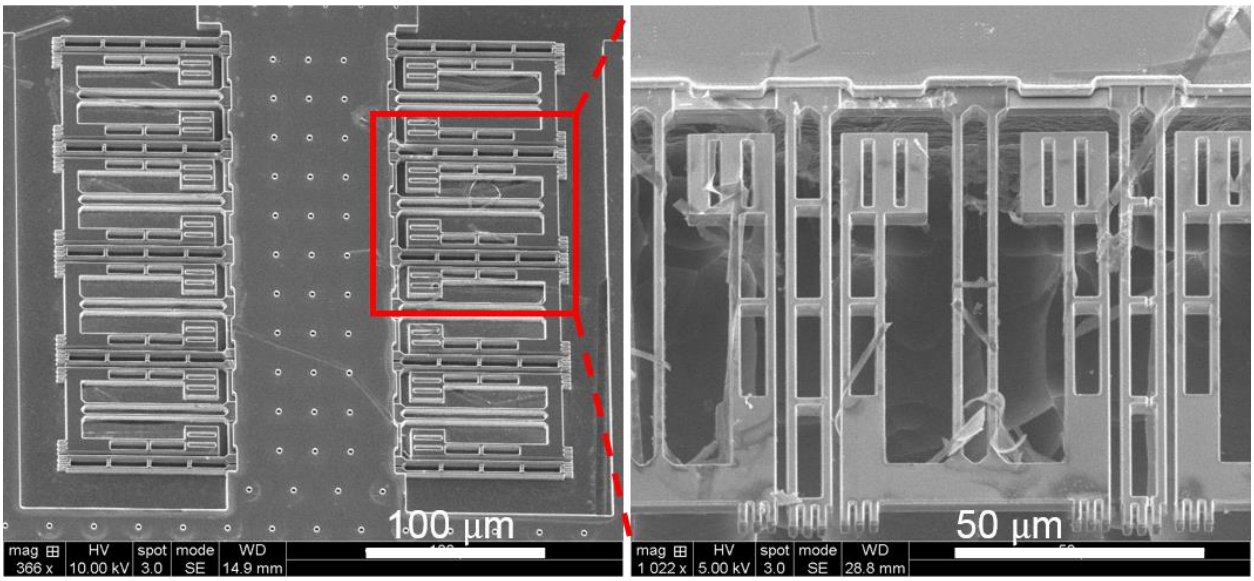


Figure 3.7. Sidewall polymer delamination upon CMOS aluminum etch in type A Transene aluminum wet etchant.

The polymer delamination from the sidewalls can also be avoided by using an anisotropic dry aluminum etch step instead of using a wet etchant. To that end, the Plasma-Therm Versaline ICP RIE system is utilized for chlorine-based dry etch of the CMOS aluminum with 25 sccm Cl_2, 5 sccm BCl_3 and 70 sccm Ar. An initial gas stabilization step runs for 30 s. The aluminum etch

process is run at 5 mTorr chamber pressure with 400 W ICP power and 125 W bias power. The etch rate of the process was around 0.6 μm/min, thereby the metal-4 layer on the accelerometer cells (approximately 0.5 μm thick) was successfully removed with a 60 s etch time. Figure 3.8 shows the accelerometer cells of one of the first-generation accelerometer devices after etching the top metal (i.e., metal-4) on the accelerometer cells while leaving the (more than 5 times thicker) metal-6 cover across the rest of the chip. The polymer delamination problem is successfully avoided and the chip is clean of particulate artifacts after the anisotropic dry aluminum etch step.

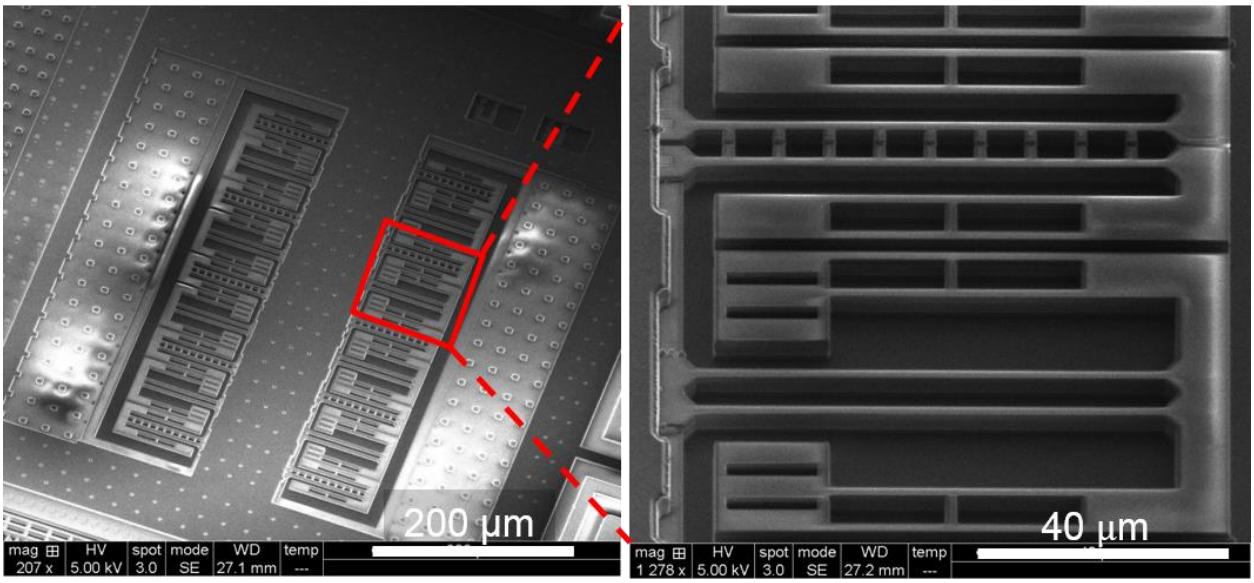


Figure 3.8. Accelerometer cell after etching the metal-4 CMOS layer with chlorine-based dry aluminum etch.

The complete removal of the top metal from the chip is achieved by running 7 cycles of 45 s aluminum etch steps. A longer gas stabilization step (i.e., 180 s) is repeated before each etch cycle in order to leave ample time for the chip to cool down. The sample heating is not a problem for wafer-level processes since the electrode that holds the wafer is actively cooled to room temperature. However, the accelerometer chips are processed individually and mounted on a wafer by using a thin layer of photoresist, which slows down the heat dissipation.

The complete removal of the top metal implies that the bond pads need to be protected with a photoresist mask. This patterning requires an additional photolithography step to cover the bond pads and an additional oxygen RIE step to remove the residual photoresist on the bond pads after the completion of the metal etch. Selective removal of the metal-4 on the accelerometer by timing the etch process eliminates the risk of metal creep at high stress regions while leaving the metal-6 on the bond pads, hence eliminating the need for bond-pad protection. However, the accelerometer signal routing area (i.e., the anchor area) is also covered with metal-6 to minimize the parasitic capacitance when the top metal is not removed. In this case, the parasitic capacitance between the accelerometer signal routing line and the top metal can only be eliminated by etching the metal-6 layer while protecting the bond-pads. The preliminary experiments on etching the metal-6 layer in the presence of photoresist on the bond pads led to re-deposition on the accelerometer cells as shown in Figure 3.9. The re-deposited material is particularly rich in aluminum content and is believed to occur due to residual chlorine on the devices that forms hydrochloric acid upon exposure to atmosphere and leads to corrosion on the sidewalls.

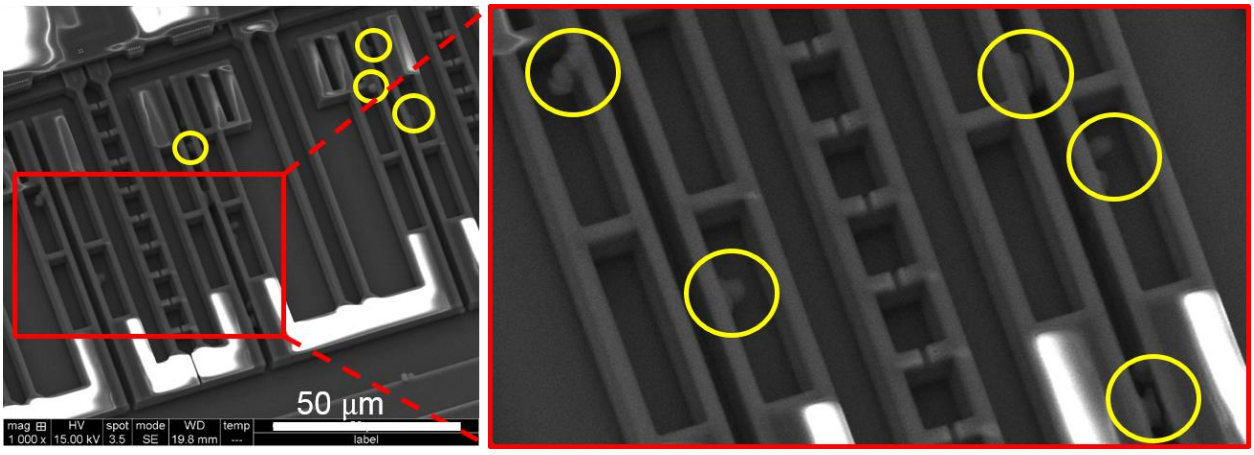
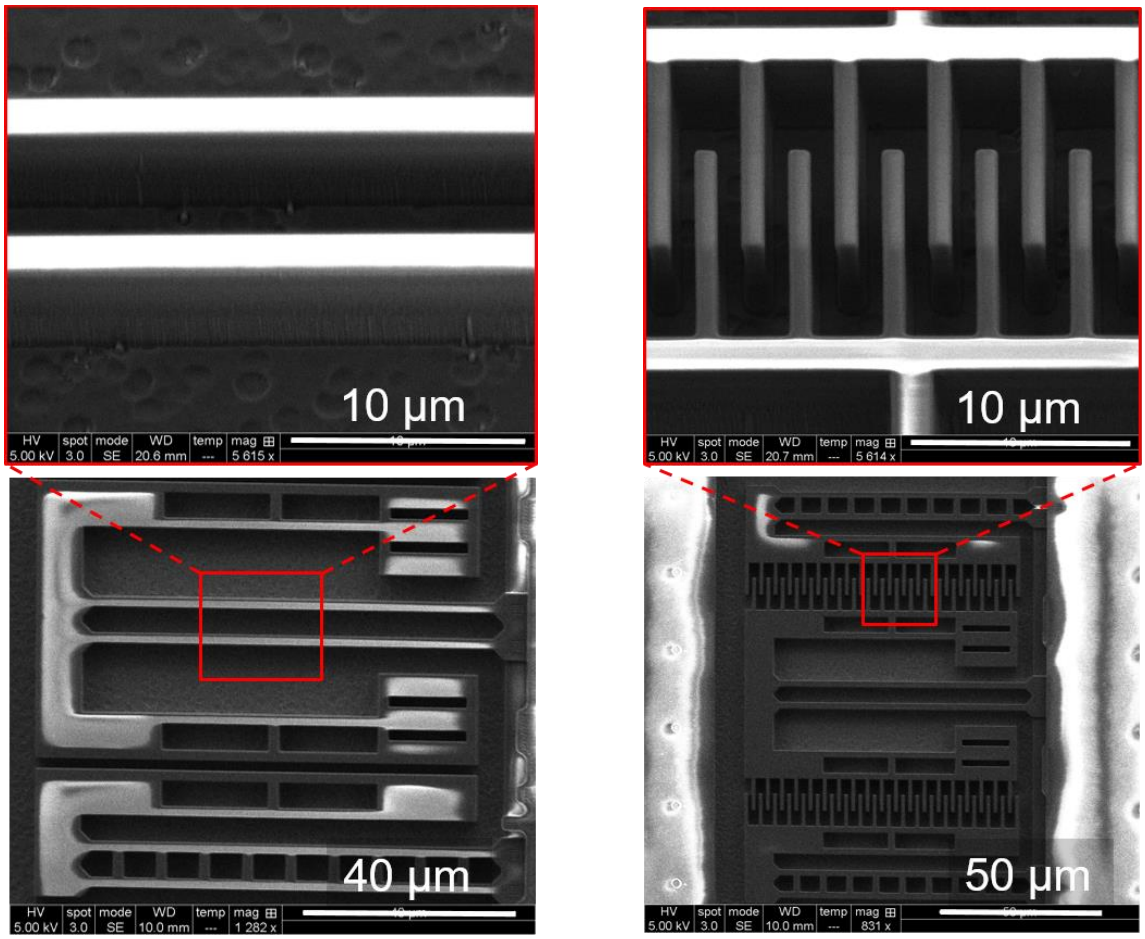


Figure 3.9. Re-deposition due to corrosion on the accelerometer sidewalls (circled in yellow) after 7 cycles of chlorine-based dry aluminum etch.

Two additional steps are added to the dry aluminum etch process in order to avoid the chlorine residues and eliminate the corrosion problem. The sample is plasma-etched by running 2 cycles of 60 s Ar plasma right after the aluminum etch step, before venting the Versaline ICP RIE chamber and exposing the sample to atmosphere. The process is run with 70 sccm Ar flow rate at 45 mTorr chamber pressure, 400 W ICP power and no bias power. The high chamber pressure and removal of the bias power aim to increase the isotropy of the physical etch and removal of the chlorine from the sidewalls. The chamber is vented after the Ar plasma treatment and the sample is immediately transferred to a hot (e.g., 85 °C) DI water bath in order to remove any remaining chlorine on the sidewalls by forming hydrochloric acid upon reaction with water, which is diluted and removed in the bath before any corrosion takes place. The sample is kept in the bath for half an hour and agitated a few times in this time frame. Figure 3.10 shows an example accelerometer cell and a resonator-oscillator after the amended aluminum etch process. Due to increased etch rate of the Plasma-Therm Versaline ICP RIE system after equipment movement and maintenance, the metal-6 layer is completely removed at the end of 4 cycles. The sidewall polymer is also removed on the sample in Figure 3.10 through EKC 265 etch performed by Mary Elizabeth Galanko before the aluminum etch, which helps with sidewall flatness as evident from the zoomed images.



(a) (b)

Figure 3.10. (a) Accelerometer cell and (b) resonator-oscillator after EKC 265 etch, dry aluminum etch, argon plasma treatment and warm DI bath.

3.4 Summary of Process Improvements

The oxide etch recipe reported in section 3.2.1 provides repeatable results for 2.5 mm × 2.5 mm chips. Reducing the gas flow to the chamber towards the end of the process (e.g., in the last 10 min) and running an oxygen plasma treatment (e.g., for 15 min) at the end of the process help reduce the sidewall polymer thickness and increase the sidewall steepness. Aluminum re-deposition is observed in the etch area when the same recipe is used for 5 mm × 5 mm chips. The re-deposition problem arises due to milling on the large exposed

aluminum area. Covering the bond-pad area with photoresist reduces the amount of exposed aluminum and solves the re-deposition problem.

The CMOS aluminum on the anchor- and truss-end points of the accelerometer springs is prone to creep and change the spring constant, thereby lead to bias drift over long time frames or after shock events. Removal of the top metal in a wet etchant (e.g., Transene aluminum etchant A) leads to polymer delamination from the sidewalls. Instead, Plasma-Therm Versaline ICP RIE system is used to dry etch the top metal. The bond pads are protected with a photoresist mask during the process. The etch is performed in multiple cycles and the gas stabilization time is kept long (i.e., 180 s) between the cycles to leave enough time for heat dissipation through the thin photoresist layer used for mounting the chip on the wafer. The chlorine residues lead to material clusters on the accelerometer sidewalls after the dry aluminum etch step. Following the dry etch step with an Ar plasma treatment (e.g., 2 cycles of 60 s) and hot DI water bath (e.g., 30 min at 85 °C) helps remove the chlorine residues on the sidewalls and solves the re-deposition problem. Removing the top metal eliminates the risk of metal creep and simultaneously reduces the wiring parasitic capacitance.

Increasing the substrate undercut from 10 μm (i.e., the typical lateral undercut length obtained after 7 min isotropic silicon etch) to 30 μm reduces the calculated wiring parasitic capacitance per accelerometer cell from 9.70 fF to 4.94 fF and makes it comparable to the sense capacitance per side (i.e., 3.07 fF) when the top metal is removed. The isotropic silicon etch time can be increased to undercut the substrate underneath the acceleration signal wiring by 30 μm and beyond in order to improve the scale factor of the transducer.

CHAPTER 4: ENVIRONMENTAL SENSORS FOR LONG-TERM BIAS STABILITY

4.1 Environmental Effects on Long-Term Stability

Environmental variations are potential sources of scale factor and bias drift over long time frames as discussed in section 1.2.4. The effects of humidity and pressure variations can be eliminated by hermetically packaging the sensor; however, the effects of temperature and stress variations cannot be avoided. This chapter discusses the estimation of temperature and stress effects on the scale factor of the accelerometer and design of auxiliary sensors to measure the temperature and stress variations for long-term drift compensation.

First, the estimation of temperature and stress effects on the sense capacitance and resonance frequency is discussed. The corresponding variation in the scale factor of the accelerometer is calculated based on the scale factor formula derived in section 2.3.4. Next, the design and characterization of a PTAT temperature sensor, piezoresistive stress sensors and a resonator-oscillator are discussed respectively. These sensors are designed to provide high resolution temperature, stress and resonance frequency measurements to investigate the correlation between environmental variations and long-term drift of the accelerometer. The performance summary of the designed sensors shows a close agreement between the measurements and design predictions.

4.2 Estimation of Scale Factor Drift

The expression given in (2.29) for the transducer scale factor can be rewritten by substituting the dC_0/dx term with C_0/g_0 in order to see the stress and temperature effects on the scale factor more clearly:

$$S_T = \frac{dV_{out}}{da} = \frac{dV_{out}}{dx}\frac{dx}{da} = 4V_m \frac{1}{2C_0 + C_{p1}} \frac{C_0}{g_0} \frac{1}{\omega_0^2} \tag{4.1}$$

where V_m is the modulation voltage amplitude, C_0 is the sense capacitance, C_{p1} is the total parasitic capacitance (including the input capacitance of the readout circuit) at each output node of the capacitive bridge, g_0 is the nominal capacitive gap and ω_0 is the resonance frequency of the accelerometer cells. The proof mass displacement (x) is assumed to be much smaller than the nominal capacitive gap (g_0) and parallel-plate approximation is used when substituting the C_0/g_0 term for simplifying the calculations. The changes in the sense capacitance (C_0) are dominated by the changes in the capacitive gap, therefore the dependence of the scale factor on these variables (i.e., C_0 and g_0) can be lumped together. The capacitive gaps can change both as a result of stress and temperature variations, hence the dependence of transducer scale factor on both stress and temperature. The scale factor also depends on the resonance frequency (ω_0), which can drift with temperature variations. The temperature dependence of resonance frequency is simulated by using the 3D finite-element model of the accelerometer, where the temperature dependence of Young's modulus of oxide springs is taken into account. The temperature and stress effects on the capacitive gaps are also simulated by using the 3D finite-element model, albeit after simplifying the model by removing the routing lines. The estimated variations in the capacitive gaps and the resonance frequency are translated to scale factor variations by using (4.1). Once the scale factor dependence on the temperature and stress is quantified, the required temperature and stress resolution for a target scale factor stability of 1 ppm is calculated. The temperature and stress sensors are designed to reach the desired resolutions, so that the compensation of the acceleration signal based on the temperature and stress measurements can improve the scale factor stability to the target level.

4.2.1 Drift with Temperature Variations

The temperature variations affect the scale factor by changing both the capacitive gaps and the resonance frequency. First, the effect of capacitive gap variations on the scale factor is

estimated. To that end, the sense capacitance (C_0) within (4.1) is substituted by its parallel-plate approximation to yield:

$$S_T = 2V_m \frac{1}{1+\frac{C_{p1}}{\frac{2\epsilon_0 A}{g_0}}} \frac{1}{g_0} \frac{1}{\omega_0^2} \tag{4.2}$$

A small variation in the capacitive gap (Δg) leads to a small variation in the scale factor (ΔS_T), which can be approximated by taking the first term in the Taylor series expansions of the ($g_0 + \Delta g$) terms evaluated in (4.2):

$$\frac{\Delta S_T}{S_T} = -\frac{\Delta g}{g_0}\left(1+\frac{1}{1+\frac{2C_0}{C_{p1}}}\right) \tag{4.3}$$

The sense capacitance (C_0) and the parasitic capacitance (C_{p1}) for the accelerometer cell with top metal are estimated as 3.43 fF and 45.97 fF based on the finite-element model shown in Figure 2.12 in section 2.3. Substituting these values in (4.3) leads to 1.87 ppm estimated scale factor variation for 1 ppm change in capacitive gaps. Removal of the top metal reduces the variation to 1.86 ppm, which is not a significant improvement since the parasitic capacitance is still dominated by the circuit input capacitance as discussed in section 2.3.4.

The temperature dependent change in the capacitive gaps is simulated in COMSOL® for the accelerometer cells without top metal assuming 30 μm substrate undercut (Figure 4.1). The coefficient of thermal expansion (CTE) of silicon and oxide are taken as 2.6×10^{-6}/K and 0.6×10^{-6}/K [147], respectively. The substrate is fixed at the bottom and a guided-end condition is imposed on the sidewall of the anchor area as shown in Figure 4.1 to account for the constraint set by the millimeter long anchor area of the array. The displacements of the capacitance sidewalls

on the rotor and stators are averaged (e.g., the sidewall area of one of the stators is highlighted in cyan in Figure 4.1 across which the displacement is averaged) and subtracted from each other to obtain the average capacitive gap change at a given temperature. The temperature of the whole structure is changed uniformly and the resultant change in capacitive gap is plotted in Figure 4.2. The temperature dependent change in the capacitive gap is extracted as 1.8×10^{-4} μm/K.

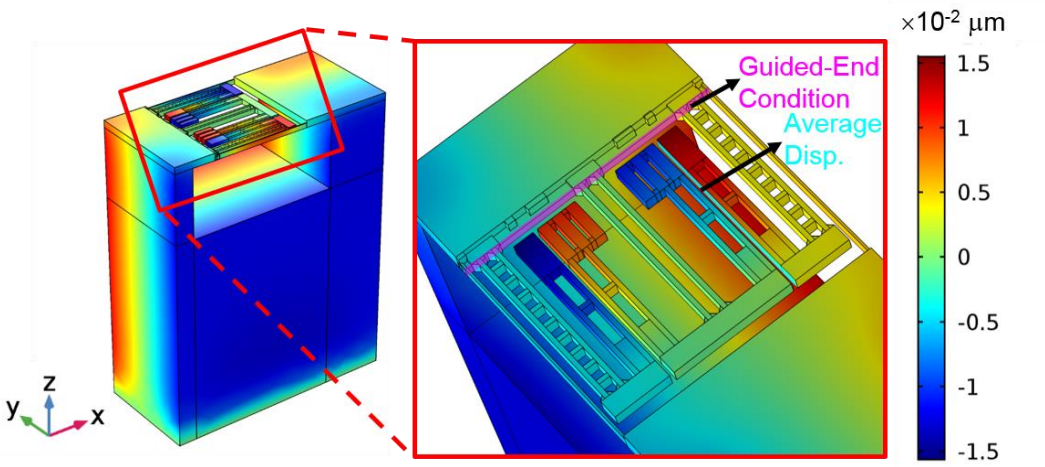


Figure 4.1. Displacement field in y-direction at 100 °C.

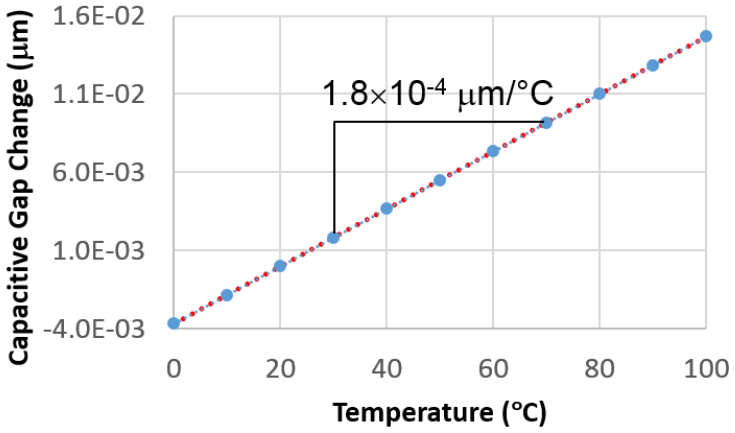


Figure 4.2. Capacitive gap dependence on temperature.

Taking the room temperature as reference (i.e., T_0 = 20 °C), the change in capacitive gap ($\Delta g/g_0$) is 1.80×10^{-3} ppm per 1 ppm change in temperature ($\Delta T/T_0$). Using (4.4), the temperature

dependent change in the transducer scale factor due to capacitive gap variations (i.e., $\Delta S_{T,g}/S_T$) is estimated as $-3.35 \times 10^{-3}\ \Delta T/T_0$ for the accelerometer cells without top metal.

$$\frac{\Delta S_{T,g}}{S_T} = -1.80\times10^{-3}\frac{\Delta T}{T_0}\left(1+\frac{1}{1+\frac{2C_0}{C_{p1}}}\right) \tag{4.4}$$

The effect of resonance frequency variations on the scale factor is obtained by taking the first term in the Taylor series expansion of the $(\omega_0 + \Delta\omega)$ term evaluated in (4.2):

$$\frac{\Delta S_{T,\omega}}{S_T} = -2\frac{\Delta\omega}{\omega_0} = -2\frac{\Delta f}{f_0} \tag{4.5}$$

The temperature dependent resonance frequency drift is estimated as 11.5 Hz/°C by using finite-element analysis (Figure 4.3). It is dominated by the temperature coefficient of Young's modulus of oxide (195.8 ppm/K) [148], which is the dominant material in the spring beams. Taking the room temperature as reference (i.e., T_0 = 20 °C), the change in resonance frequency ($\Delta\omega/\omega_0$) is 1.95×10^{-3} ppm per 1 ppm change in temperature ($\Delta T/T_0$). The resonance frequency change due to electrostatic spring softening with temperature dependent capacitive gap variations is negligible (i.e., about four orders of magnitude lower). Using (4.5), the temperature dependent change in the transducer scale factor due to resonance frequency variations ($\Delta S_{T,\omega}/S_T$) is estimated as $-3.90 \times 10^{-3}\ \Delta T/T_0$. The total temperature dependent change in the transducer scale factor ($\Delta S_{T,T}/S_T$) is $-7.25 \times 10^{-3}\ \Delta T/T_0$ by adding the contributions from the capacitive gap and resonance frequency dependent changes:

$$\frac{\Delta S_{T,T}}{S_T} = \frac{\Delta S_{T,g}}{S_T} + \frac{\Delta S_{T,\omega}}{S_T} \tag{4.6}$$

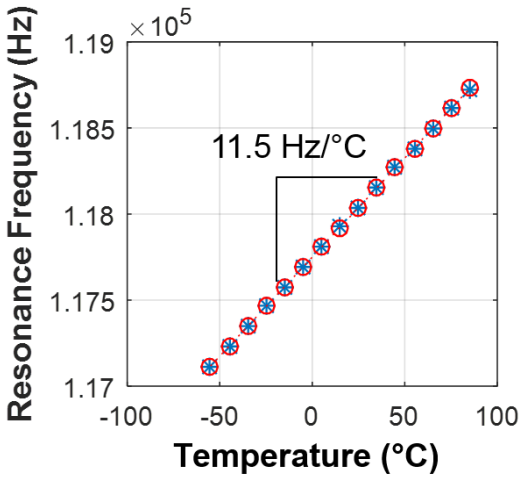


Figure 4.3. Resonance frequency dependence on temperature.

4.2.2 Drift with Stress Variations

The stress dependent capacitive gap variation is simulated in COMSOL® by using the same finite-element model in Figure 4.1. The Young's modulus of silicon (E_{si}) and oxide (E_{ox}) are taken as 165 GPa [149] and 70 GPa [137], respectively. A uniform tensile stress is applied in negative y-direction on one side of the silicon substrate as shown in Figure 4.4. The opposite side of the substrate is fixed. The guided-end condition on the sidewall of the anchor area is still applied as indicated in Figure 4.4. The displacement of the capacitance sidewalls on the rotor and stators are averaged as before to extract the average capacitive gap change at a given stress level on the substrate. The change in capacitive gap with stress is extracted as 7.5×10^{-5} µm/MPa from the plot shown in Figure 4.5.

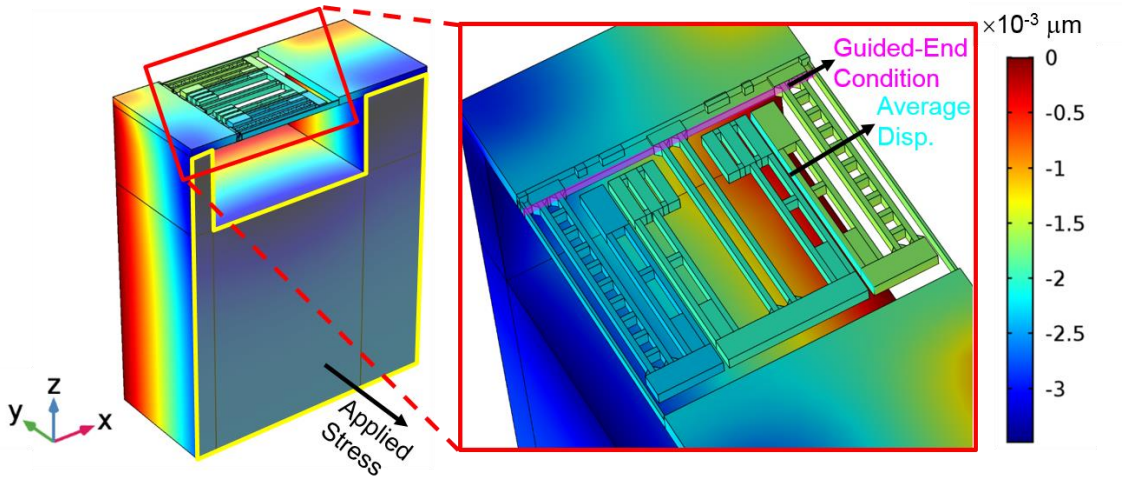


Figure 4.4. Displacement field in y-direction at 5 MPa stress on the substrate.

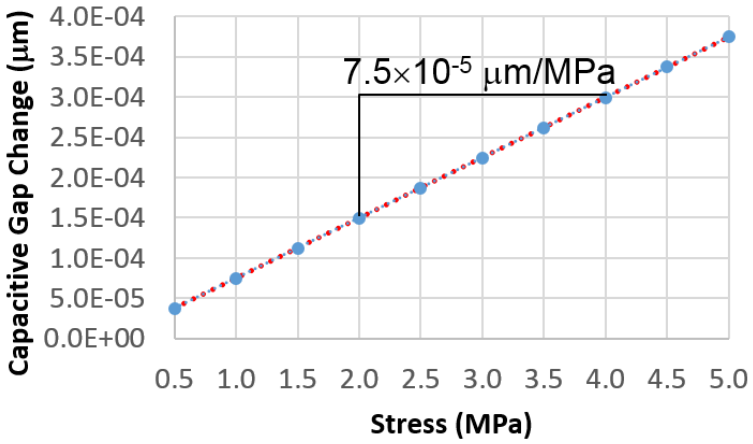


Figure 4.5. Capacitive gap dependence on stress.

The built-in stress on the chip after post-processing and packaging is estimated as 3.14 MPa by averaging the stress sensor measurements, assuming the stress sensor offsets are set by the built-in stress. Taking the built-in stress as reference (i.e., σ_0 = 3.14 MPa), the change in capacitive gap ($\Delta g/g_0$) is 1.18 × 10^{-4} ppm per 1 ppm change in stress ($\Delta\sigma/\sigma_0$). Using (4.7), the stress dependent change in the transducer scale factor ($\Delta S_{T,\sigma}/S_T$) is –2.19 × 10^{-4} $\Delta\sigma/\sigma_0$ for the accelerometer cells without top metal.

$$\frac{\Delta S_{T,\sigma}}{S_T} = -1.18\times10^{-4}\frac{\Delta\sigma}{\sigma_0}\left(1+\frac{1}{1+\frac{2C_0}{C_{p1}}}\right) \tag{4.7}$$

4.2.3 Environmental Sensors for a Target Scale Factor Stability

The scale factor drift of the accelerometer ($\Delta S_T/S_T$) is estimated by adding the individual contributions from the stress and temperature induced scale factor variations:

$$\frac{\Delta S_T}{S_T} = \frac{\Delta S_{T,T}}{S_T} + \frac{\Delta S_{T,\sigma}}{S_T} = -7.25\times10^{-3}\frac{\Delta T}{T_0} - 2.19\times10^{-4}\frac{\Delta\sigma}{\sigma_0} \tag{4.8}$$

If the temperature and stress variations (i.e., ΔT and $\Delta\sigma$) on the chip are sensed with high resolution, the resultant drift can be predicted with higher precision and compensated. The compensation can be made numerically once the data from the accelerometer and environmental sensors are captured. Alternatively, the transducer can be physically compensated on the chip by using a control loop. The required temperature and stress resolution (i.e., the measurement resolution for ΔT and $\Delta\sigma$) for a target scale factor stability (i.e., $\Delta S_T/S_T$) is calculated by using (4.8). When the scale factor drift is only due to temperature variations (i.e., $\Delta S_T/S_T = \Delta S_{T,T}/S_T$), the required temperature resolution (ΔT_{min}) for 1 ppm scale factor stability is 2.8 mK by using (4.9). Similarly, the required stress resolution ($\Delta\sigma_{min}$) for 1 ppm scale factor stability is 14.3 kPa by using (4.10) when the drift is only due to stress variations (i.e., $\Delta S_T/S_T = \Delta S_{T,\sigma}/S_T$).

$$\Delta T_{\min} = \frac{\left|\frac{\Delta S_T}{S_T}\right|_{min}}{7.25\times10^{-3}}T_0 \tag{4.9}$$

$$\Delta\sigma_{min} = \frac{\left|\frac{\Delta S_T}{S_T}\right|_{min}}{2.19\times10^{-4}}\sigma_0 \tag{4.10}$$

In practice, parts of the stress and temperature drift will be correlated and parts will be uncorrelated. In addition, the stress sensor measurements can be affected by temperature variations

and the temperature sensor measurements can be sensitive to stress variations. The stress and temperature can also vary across the chip, hence introducing additional uncertainty to the drift estimation when the measurements are taken only at one point on the chip. However, the temperature and stress sensors can be implemented with small footprints in the CMOS process, hence making it possible to use multiple sensors distributed across the chip. The stress and temperature gradients on the chip can be mapped by taking measurements at different positions on the chip in order to improve the accuracy of the drift estimation. The correlation between closely placed stress and temperature sensor signals can be studied to model the temperature effects on the stress sensors and the stress effects on the temperature sensors, hence calculating the absolute values of the stress and temperature changes more accurately. To that end, five different sensor areas are created in the first-generation accelerometer system (Figure 4.6) and nine different sensor areas are created in the second-generation accelerometer system (Figure 4.7). Piezoresistive stress sensors and proportional to absolute temperature (PTAT) circuits are designed for the target resolutions and placed closely in each sensor area.

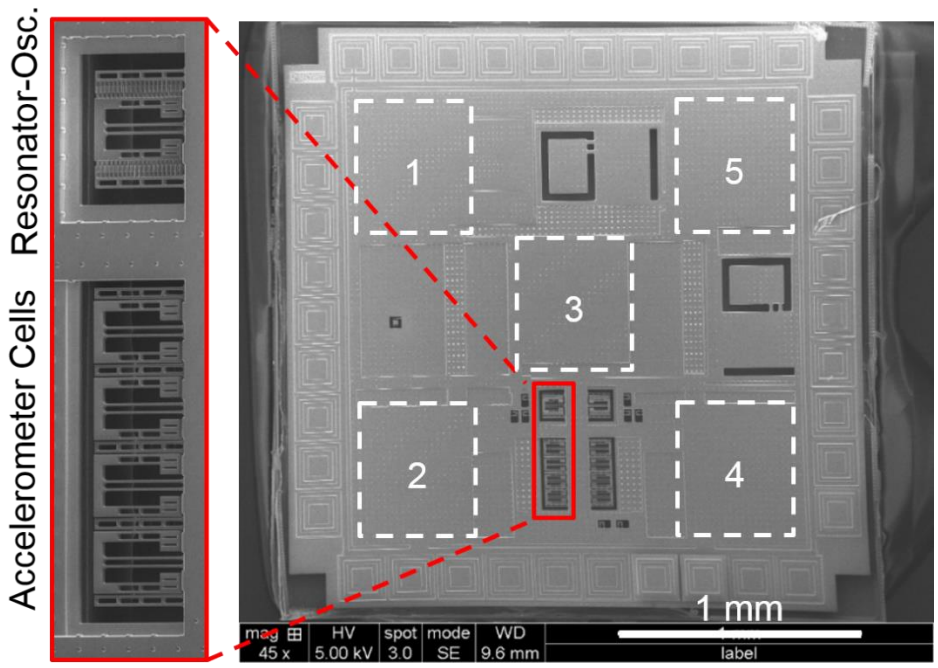


Figure 4.6. Environmental sensor areas in the first-generation accelerometer system.

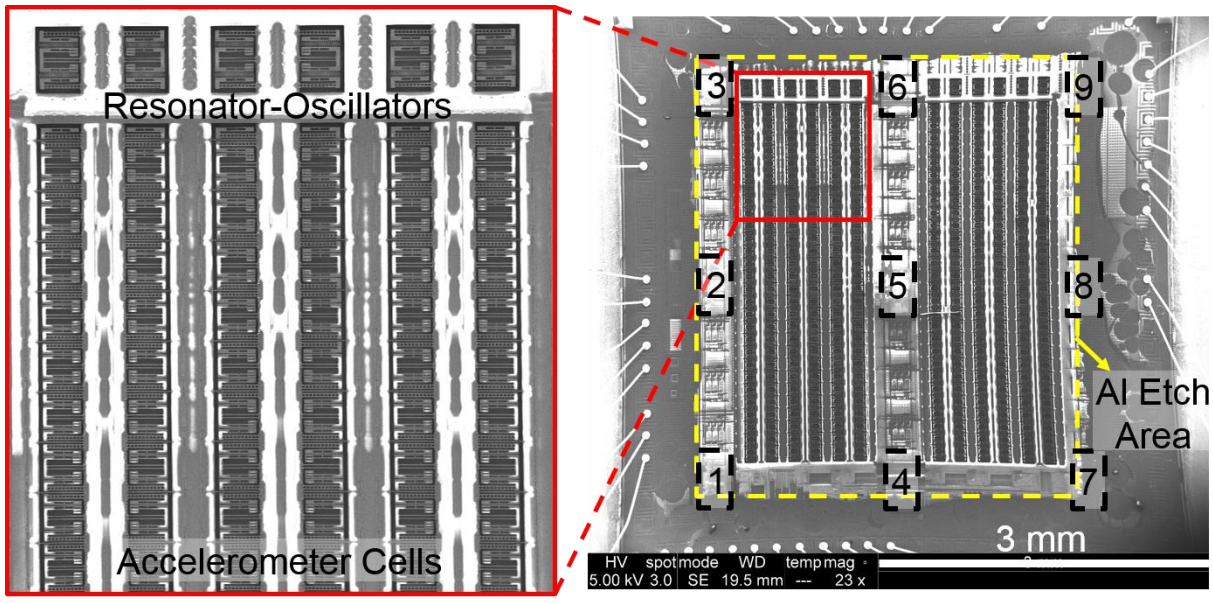


Figure 4.7. Environmental sensor areas in the second-generation accelerometer system.

The resonance frequency drift of the accelerometer cells can be tracked by using resonator-oscillators designed very similar to the accelerometer cells. The resonance frequency measurements taken from the resonator-oscillators can be directly used for compensating the scale

factor of the accelerometer based on the relationship given in (4.5). When the scale factor drift is only due to resonance frequency variations (i.e., $\Delta S_T/S_T = \Delta S_{T,\omega}/S_T$), the required frequency resolution (Δf_{min}) for 1 ppm scale factor stability is calculated as 59 mHz by using (4.11), which corresponds to 0.5 ppm frequency stability for the resonators.

$$\Delta f_{min} = \frac{\left|\frac{\Delta S_T}{S_T}\right|_{min}}{2} f_0 \tag{4.11}$$

The variations in the resonance frequencies of the individual accelerometer cells are averaged at the output of the accelerometer array. Multiple resonator-oscillators can be distributed between the accelerometer cells in order to reduce the uncertainty in the estimated resonance frequency variations and predict the scale factor drift more accurately. Both the first-generation (Figure 4.6) and the second-generation (Figure 4.7) accelerometer systems designed in this study have one resonator-oscillator placed at the end of each column of accelerometer cells.

4.3 Design and Characterization of the PTAT Temperature Sensor

4.3.1 PTAT Circuit Design

The PTAT temperature sensor design follows the topology in [150] and sized to achieve low flicker noise (Figure 4.8). The low power consumption (78 µW) and the moderate layout area (0.021 mm^2) of the designed sensor allow using multiple sensors in the accelerometer system placed at different positions on the chip for mapping the temperature gradients. The sensitivity (Figure 4.9 (a)) and noise floor (Figure 4.9 (b)) of the designed PTAT sensor are estimated by Cadence simulations based on the foundry device parameters in the 0.18 µm CMOS process (TowerJazz, Newport Beach, CA). The voltage resolution (Allan deviation) of the sensor is 13.8 µV based on the predicted flicker noise in the simulation. The temperature resolution of the sensor is 4.85 mK based on the sensitivity of the sensor (~ 2.84 mV/K) at room temperature.

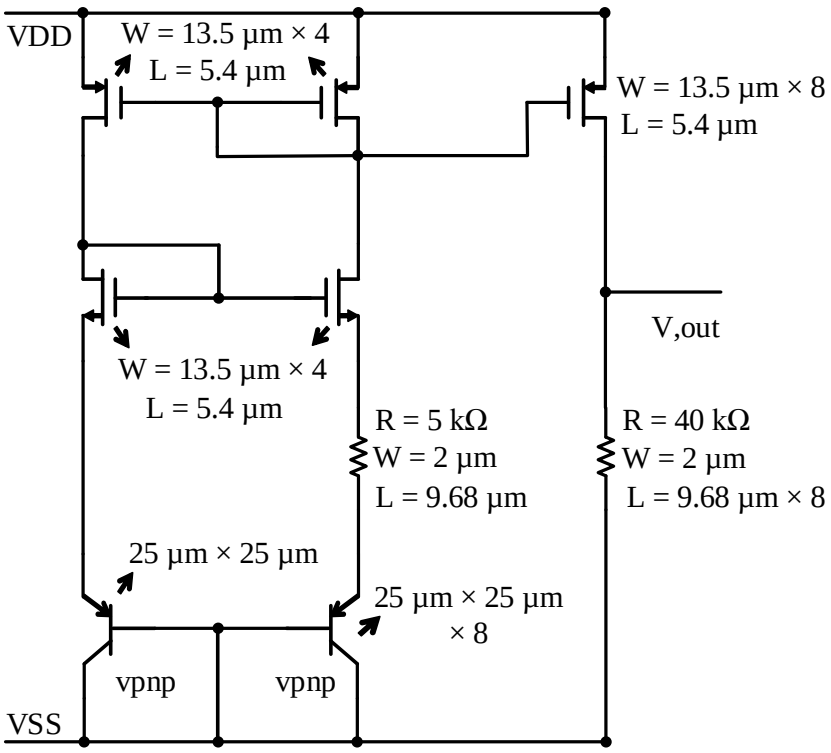
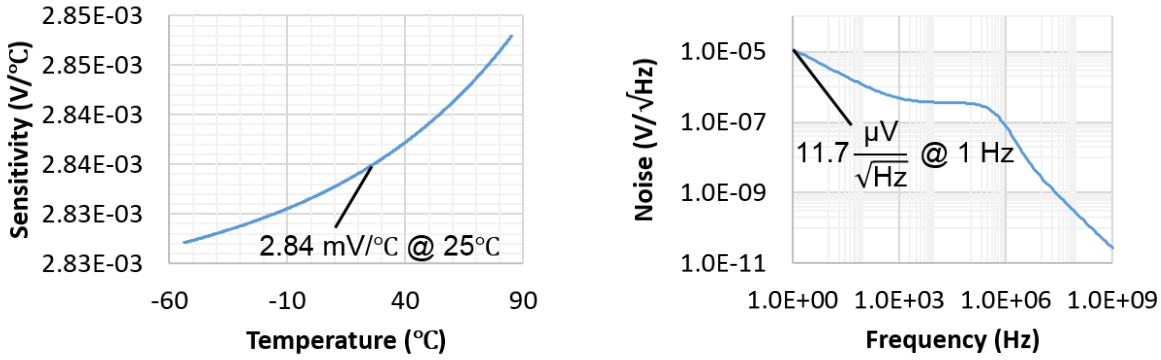


Figure 4.8. PTAT circuit design with transistor and resistor sizes.



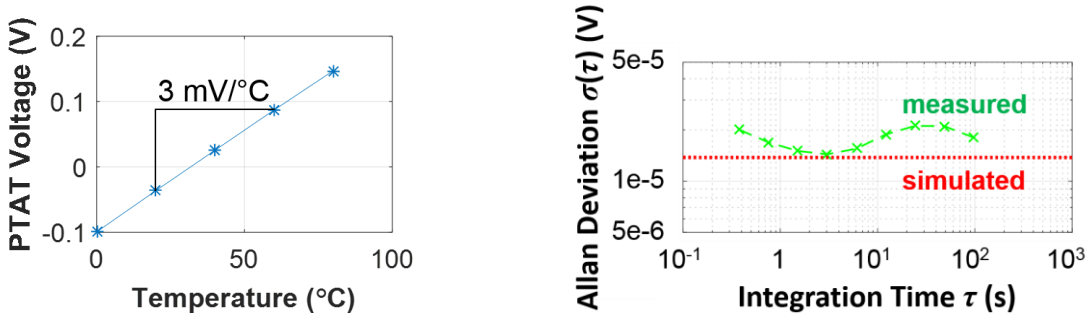
(a) (b)

Figure 4.9. (a) Simulated sensitivity and (b) noise floor of the PTAT temperature sensor.

4.3.2 Measured Temperature Resolution of the PTAT Temperature Sensors

The sensitivity and noise floor of the PTAT sensors are characterized in an environmental chamber from 0 °C to 80 °C. A scan-chain is implemented on the chip for selecting the output of one out of multiple temperature sensors. The output of the selected PTAT temperature sensor is

directly connected to a digital multimeter for DC voltage measurement. The measured sensitivity of four out of five sensors in the first-generation accelerometer system is 3 mV/K with one exceptional device that has 7.25 mV/K sensitivity. The measured Allan deviation of all the sensors is 20 µV, corresponding to 6.7 mK temperature resolution. Measurement data from one particular sensor is provided in Figure 4.10 as an example of typical performance, which agrees well with the design expectations. The fabricated PTAT sensor resolution corresponds to compensation of the accelerometer readout for 2.4 ppm scale factor stability.

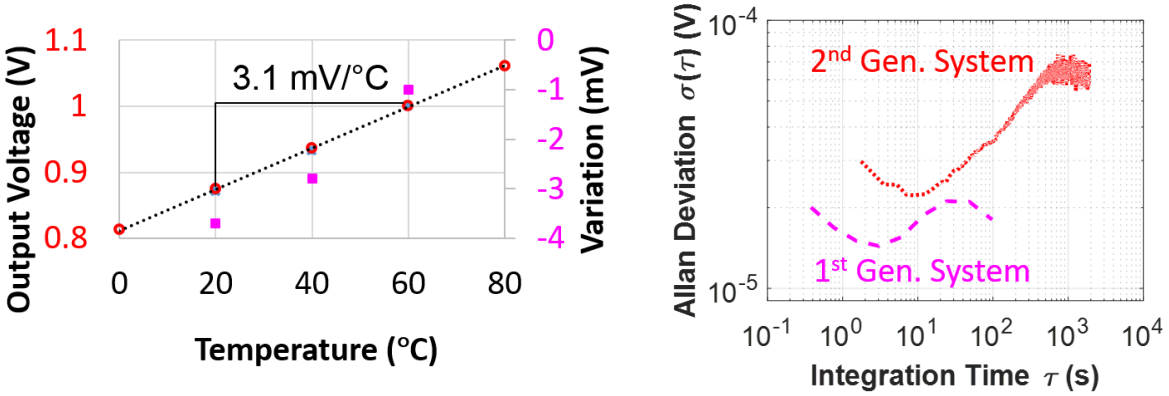


(a) (b)

Figure 4.10. (a) Measured sensitivity and (b) bias stability of a PTAT temperature sensor in the first-generation accelerometer system.

The sensitivity and noise floor are not characterized for all the PTAT temperature sensors in the second-generation accelerometer system, since the measured sensitivity and noise floor of the sensors in the first-generation system were highly repeatable. Figure 4.11 (a) shows the sensitivity measurement for a PTAT temperature sensor in the second-generation accelerometer system. Red data points are collected as the temperature is increased from 0 °C to 80 °C and blue data points are collected as the temperature is decreased from 80 °C to 20 °C. The difference between the red and blue data points (i.e., blue data points subtracted from the red data points) is plotted in magenta on the right y-axis, which shows less than 4 mV variation in output voltage that

corresponds to less than 1.3 °C hysteresis in temperature measurement. The hysteresis may be partially explained by the hysteresis in cooling the environmental chamber, although the chamber temperature is allowed stabilize for an hour before each measurement. Other sources of hysteresis and possible design improvements remains to be investigated. The measured sensitivity (3.1 mV/K) compares well with the typical 3 mV/K sensitivity obtained on the first-generation system chips. The measured 22 µV bias stability (Figure 4.11 (b)) is slightly worse than that obtained on the first-generation system chips (i.e., 20 µV), leading to a slightly worse temperature resolution (i.e., 7.1 mK). The measured temperature resolution corresponds to 2.6 ppm scale factor stability for the accelerometer when compensated for the temperature fluctuations.



(a) (b)

Figure 4.11. (a) Measured sensitivity and (b) bias stability of a PTAT temperature sensor in the second-generation accelerometer system.

4.4 Design and Characterization of the Piezoresistive Stress Sensor

4.4.1 Piezoresistive Stress Sensor Design in Silicon

The piezoresistive stress sensors are implemented by using resistors in the silicon substrate. The 0.18 µm CMOS process already has an n-well resistor model and layout (Figure 4.12) provided by the foundry. These resistors can be readily sized and used in the design of n-type piezoresistive stress sensors. However, this process uses (100) silicon wafers where the primary

flat lies along the x-axis and aligns with the [110] direction. P-type piezoresistors are expected to have higher sensitivity to normal stress in [110] direction. In order to evaluate their sensitivity experimentally, p-type piezoresistors are laid out directly in the p-type silicon substrate (Figure 4.13) following the structure of the built-in n-well resistors. The noise floor of the piezoresistive sensors is set by the flicker noise of the resistors, which scales inversely proportional to the resistor area [24]. Improved stress sensitivity implies that the target resolution can be achieved with smaller piezoresistors, hence reducing the sensor area.

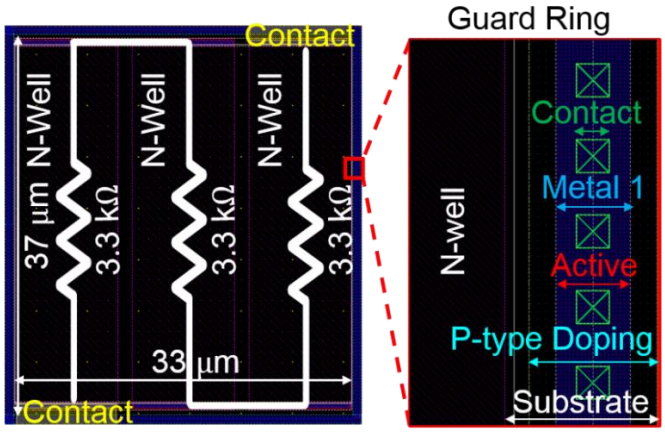


Figure 4.12. N-well resistor layout for n-type piezoresistive stress sensors.

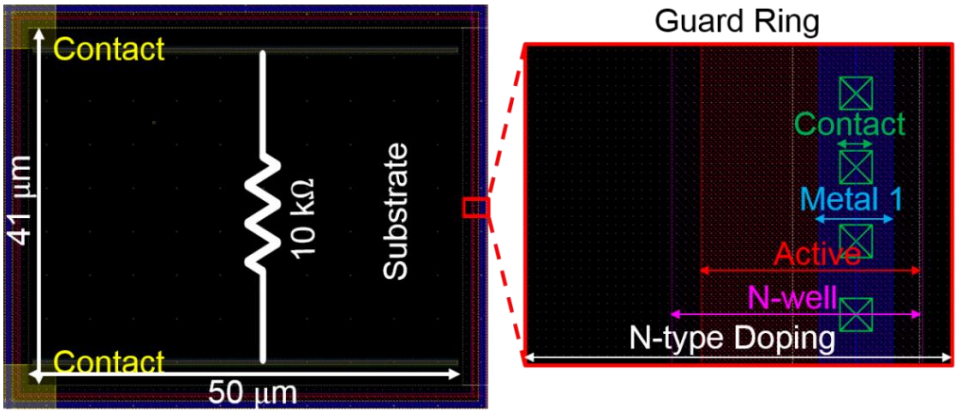
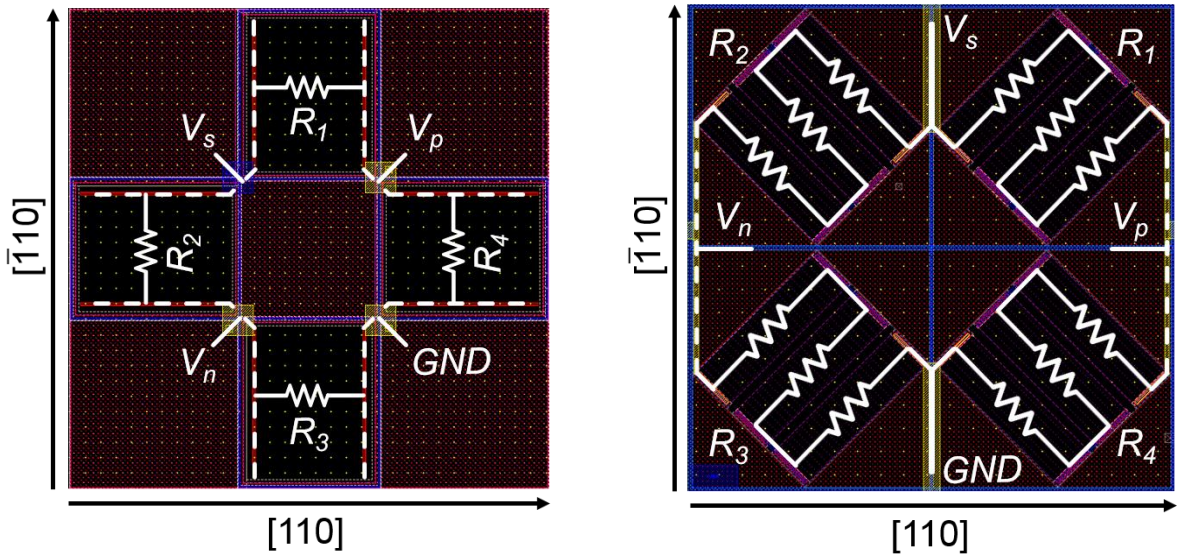


Figure 4.13. P-substrate resistor layout for p-type piezoresistive stress sensors.

Custom p-type silicon resistors (2050 μm^2/resistor) and foundry-cell n-type silicon resistors (1220 μm^2/resistor) are connected in a Wheatstone bridge configuration. The resistors lie parallel to the [110] and [$\bar{1}$10] directions in the normal stress sensors (e.g., Figure 4.14 (a)) and with 45° angle in the shear stress sensors (e.g., Figure 4.14 (b)). The piezoresistive coefficients of silicon (i.e., π_{11}, π_{12} and π_{14}) are specified for [100] oriented resistors in [22] and need to be transformed for resistors oriented at different angles with respect to the [100] direction. The stress and temperature dependent change in the resistance is formulated in [151] by taking the [110] direction as reference and assuming negligible change due to geometrical effects or nonlinear piezoresistivity.



(a) (b)

Figure 4.14. (a) Example p-type normal and (b) n-type shear stress sensors obtained by connecting the piezoresistors in a Wheatstone bridge configuration.

The changes in the resistances of [110] oriented (i.e., R_1 and R_3) and [$\bar{1}$10] oriented (i.e., R_2 and R_4) resistors in Figure 4.14 (a) are given by (4.12) and (4.13), respectively.

$$\frac{\Delta R_1}{R_1}=\frac{\Delta R_3}{R_3}=\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\sigma_{11}+\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\sigma_{22}+\pi_{12}\sigma_{33} \tag{4.12}$$

$$\frac{\Delta R_2}{R_2}=\frac{\Delta R_4}{R_4}=\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\sigma_{11}+\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\sigma_{22}+\pi_{12}\sigma_{33} \tag{4.13}$$

The temperature dependent changes in the resistances are neglected, since the temperature effects are ideally cancelled when the Wheatstone bridge is formed by using identical resistors (i.e., $R_1 = R_2 = R_3 = R_4 = R_0$) as in our case. The output signal of the piezoresistive bridge is then calculated as:

$$V_{out}=V_p - V_n=\frac{V_s(R_1+\Delta R_1)}{R_1+\Delta R_1+R_4+\Delta R_4}-\frac{V_s(R_2+\Delta R_2)}{R_2+\Delta R_2+R_3+\Delta R_3} \tag{4.14}$$

where V_s is the voltage across the bridge. This expression is written in terms of the piezoresistive coefficients as:

$$V_{out}=\frac{V_s R_0\pi_{44}(\sigma_{11}-\sigma_{22})}{2R_0+R_0[(\pi_{11}+\pi_{12})\sigma_{11}+(\pi_{11}+\pi_{12})\sigma_{22}+2\pi_{12}\sigma_{33}]} \tag{4.15}$$

The stress dependent resistance term in the denominator of (4.15) is small when the stress level is in the mega-Pascal range, therefore the output signal can be approximated as:

$$V_{out}=V_s\frac{\pi_{44}}{2}(\sigma_{11}-\sigma_{22}) \tag{4.16}$$

The output signal of the piezoresistive bridge is proportional to the difference of the normal stress in the [100] direction (i.e., x-axis) and [$\bar{1}$10] direction (i.e., y-axis). Given the small Poisson's ratio of silicon (i.e., 0.09 [152]), the difference can be approximated as a single stress component when the normal stress is applied particularly in x- or y-direction. In this case, the sensitivity to normal stress in x- or y-direction is $V_s \times \pi_{44} / 2$. The π_{44} coefficient is higher for p-type piezoresistors (i.e., 138.1×10^{-11} / Pa) compared to n-type piezoresistors (i.e., -13.6×10^{-11} / Pa), hence leading to higher normal stress sensitivity for p-type sensors. Assuming operation with a

1.8 V supply voltage, the sensitivity values of the p-type and n-type piezoresisitive normal stress sensors are 1.24 nV/Pa and 122.4 pV/Pa, respectively.

The changes in the resistances of [010] oriented (i.e., R_1 and R_3) and [100] oriented (i.e., R_2 and R_4) resistors in Figure 4.14 (b) are given by (4.17) and (4.18), respectively.

$$\frac{\Delta R_1}{R_1}=\frac{\Delta R_3}{R_3}=\frac{1}{2}\left[\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\sigma_{11}+\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\sigma_{22}\right] + \frac{1}{2}\left[\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\sigma_{11}+\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\sigma_{22}\right]+\pi_{12}\sigma_{33}+(\pi_{11}-\pi_{12})\sigma_{12} \tag{4.17}$$

$$\frac{\Delta R_2}{R_2}=\frac{\Delta R_4}{R_4}=\frac{1}{2}\left[\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\sigma_{11}+\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\sigma_{22}\right] + \frac{1}{2}\left[\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\sigma_{11}+\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\sigma_{22}\right]+\pi_{12}\sigma_{33}-(\pi_{11}-\pi_{12})\sigma_{12} \tag{4.18}$$

The temperature dependent changes in the resistances are neglected as before by assuming identical resistors (i.e., $R_1 = R_2 = R_3 = R_4 = R_0$). The output signal of the piezoresistive bridge follows (4.14), which is written in terms of the piezoresistive coefficients as:

$$V_{out}=\frac{2V_s R_0(\pi_{11}-\pi_{12})\sigma_{12}}{2R_0+R_0[(\pi_{11}+\pi_{12})\sigma_{11}+(\pi_{11}+\pi_{12})\sigma_{22}+2\pi_{12}\sigma_{33}]} \tag{4.19}$$

The stress dependent resistance term in the denominator of (4.19) is neglected assuming stress levels in mega-Pascal range, thereby the output signal is approximated as:

$$V_{out}=V_s(\pi_{11}-\pi_{12})\sigma_{12} \tag{4.20}$$

In this case, the output signal of the piezoresistive bridge is proportional to the shear stress (i.e., σ_{12}) and the sensitivity is $V_s \times (\pi_{11} - \pi_{12})$. The difference of the π_{11} and π_{12} coefficients is higher for n-type piezoresistors (i.e., -155.6×10^{-11} / Pa) compared to p-type piezoresistors (i.e., 7.7×10^{-11} / Pa), hence leading to higher shear stress sensitivity for n-type sensors. Assuming

operation with a 1.8 V supply voltage, the sensitivity values of the n-type and p-type piezoresistive shear stress sensors are −2.80 nV/Pa and +138.6 pV/Pa, respectively.

A foundry-supplied flicker noise model is only available for the high resistivity polysilicon resistors in the CMOS process. The noise floor of the stress sensors is estimated (Figure 4.15) by simulating the noise at the output of a resistive bridge formed by using high resistivity polysilicon resistors, assuming a similar noise model for the similarly sized piezoresistors implemented in the substrate. The resistor sizes are kept large in order to reduce the flicker noise and improve the stress resolution. The calculated voltage resolution (Allan deviation) at the bridge output is 0.62 µV based on the flicker noise extracted in simulation. The corresponding stress resolution for the n-type normal and n-type shear sensors are 5.1 kPa and 221.4 Pa, respectively. The normal stress resolution of the p-type piezoresistive sensor is expected to be an order of magnitude better (i.e., 500 Pa) due to higher normal stress sensitivity of p-type resistors, whereas the shear stress resolution of the n-type piezoresistive sensor is expected to be an order of magnitude worse (i.e., 4.5 kPa) due to lower shear stress sensitivity of n-type resistors. The piezoresistive coefficients used in estimating the sensitivities are reported for lightly doped silicon [151], which can drop substantially at higher doping levels (e.g., $> 10^{17}$ cm^{-3}) [153]. The unknown doping levels of the n-wells and the p-type substrate in the CMOS process as well as the assumption of similar noise floor for the high resistivity polysilicon resistors and the implemented piezoresistors introduce uncertainties to the sensitivity and resolution estimations. The sensitivity calculations are expected to hold to a great extent as long as the doping concentrations of the n-wells and the p-type substrate are not significantly higher than 10^{17} cm^{-3} however, the noise floor is prone to vary dependent on the effective height of the resistors or additional noise coupling from the substrate.

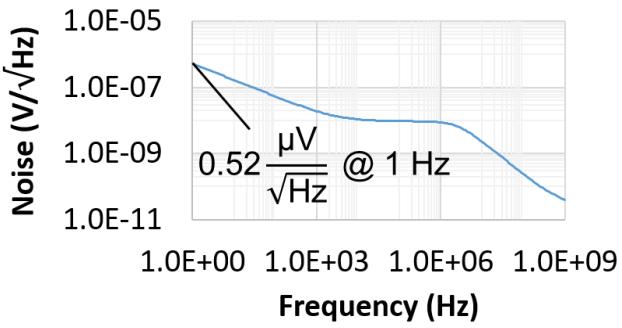
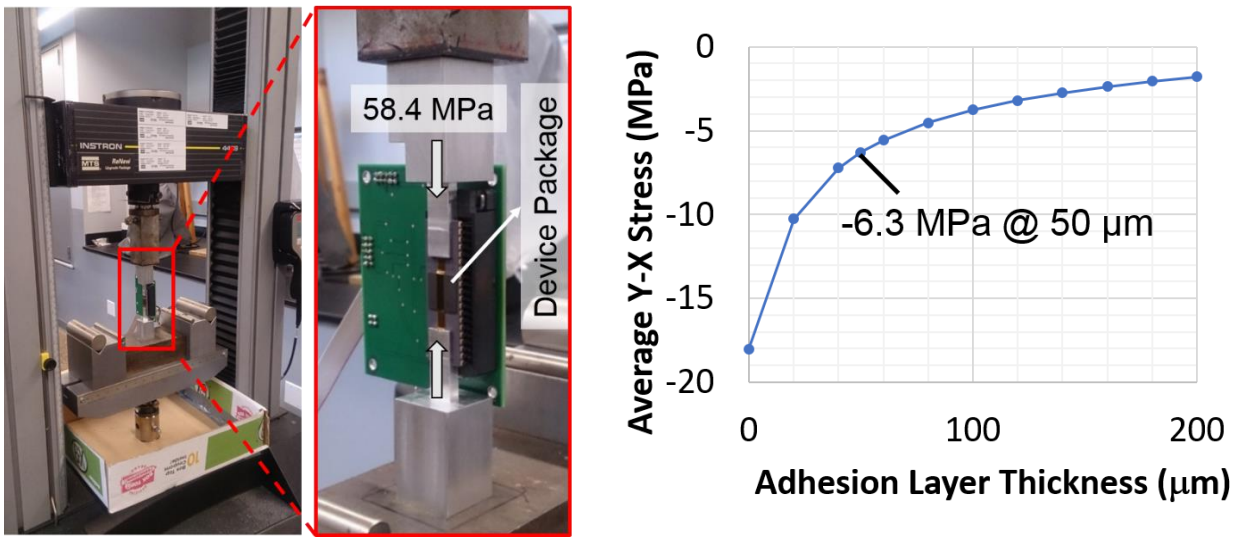


Figure 4.15. Simulated noise floor of the piezoresistive stress sensors, assuming similar noise for similarly sized high resistivity polysilicon resistors and piezoresistors built in the substrate.

The absolute resistance values of the piezoresistors do not have a direct impact on the sensitivity when set properly; however, the sensitivity can be reduced if the resistances are too high or too low. When the equivalent resistance of the Wheatstone bridge is made lower, the bridge draws a higher amount of current, which leads to both higher power consumption and higher voltage drop across the routing lines. Since the stress sensitivity is proportional to the potential across the bridge, most of the supply voltage should drop across the bridge to maximize the sensitivity. On the contrary, increasing the equivalent resistance of the Wheatstone bridge makes it more sensitive to resistive loads at the output. If the input resistance of the readout circuit or the measurement instrument (e.g., the digital multimeter) is comparable to the equivalent resistance of the bridge, the resultant voltage division will reduce the amplitude of the readout signal, hence reducing the stress sensitivity. Increasing the resistance of the piezoresistors also increases the white noise, which becomes critical when it starts to exceed the flicker noise in the signal band of interest. The resistances of the piezoresistors used in the designed sensors are set to 10 kΩ, which is a moderate value that allows a direct interface with a multimeter.

4.4.2 Test Setup and Calibration of On-Chip Stress Sensors

The Instron stress test setup used for the sensitivity characterization of the piezoresistive stress sensors is shown in Figure 4.16 (a). The test setup applies an axial compressive load up to 1 kN (~ 50 MPa) on the chip package, which gets transferred through the package to the on-chip piezoresistive stress sensors. The piezoresistive stress sensor output is directly connected to a multimeter for DC voltage readout. The chip is attached to a DIP-40 ceramic package by using silver-epoxy as the adhesive material. The effect of the die-attachment layer on the transfer of stress from the package to the substrate surface was simulated in COMSOL by Vincent Pey J. Chung at Carnegie Mellon University. The simulation is made for 2.5 mm × 2.5 mm chips of the first-generation accelerometer system and the stress is averaged across the area (indicated by white dashed lines in Figure 4.17) where the stress sensors are located. The transferred stress to the stress sensors on the substrate surface decreases as the adhesion layer thickness increases as seen in Figure 4.16 (b). A typical adhesion layer thickness of 50 μm leads to a nine-fold attenuation in the transferred stress at the substrate surface as shown in Figure 4.17.



(a) (b)

Figure 4.16. (a) Instron stress test setup for the sensitivity characterization of the piezoreresistive stress sensors. (b) The transferred stress from the package to the substrate surface as a function of adhesion layer thickness.

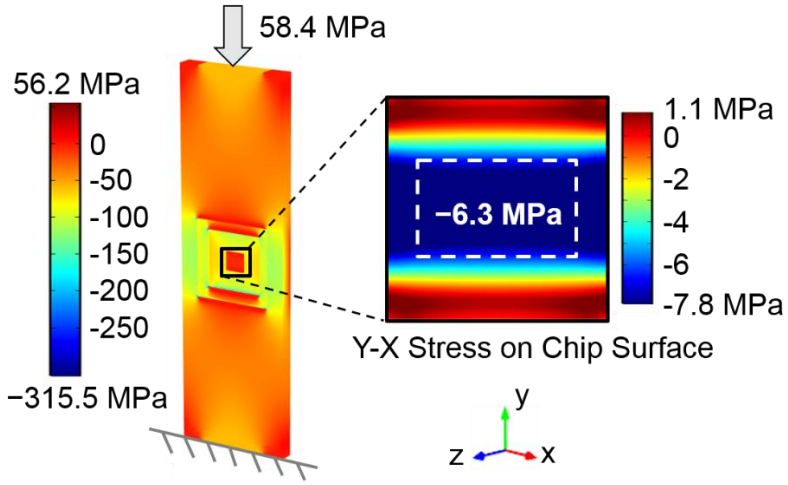


Figure 4.17. Nine-fold attenuation in the transferred stress for a typical adhesion layer thickness of 50 µm.

4.4.3 Measured Stress Resolution of the Piezoresistive Stress Sensors

The sensitivity values of the n-type and p-type piezoresistive normal stress sensors in the first-generation accelerometer system are evaluated. Example sensitivity and noise plots of the best-performing n-type and p-type stress sensors are provided in Figure 4.18. Assuming the nine-

fold stress attenuation at the substrate surface, the n-type normal stress sensor sensitivities for the tested samples as extracted from measurement vary from 55.1 pV/Pa to 240 pV/Pa, which bracket the expected sensitivity (i.e., 122.4 pV/Pa) from design. The p-type normal stress sensor sensitivities vary from 375 pV/Pa to 1.12 nV/Pa, which are lower than the designed sensitivity of 1.24 nV/Pa. Differences between designed and the extracted measured values are expected due to the stress at the exact die location, to the variation in the die adhesion layer thickness, and to the specific diffused resistor doping levels in the CMOS process.

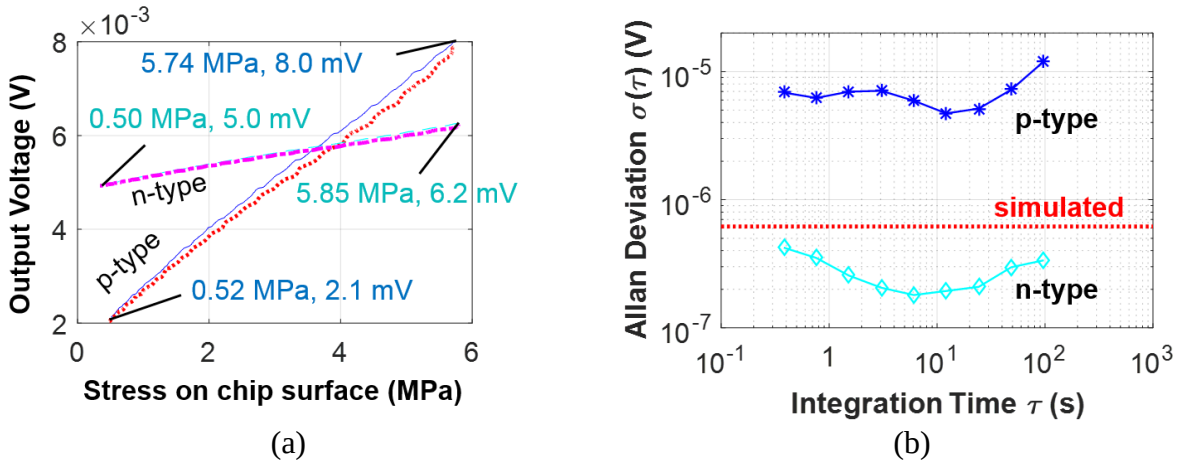


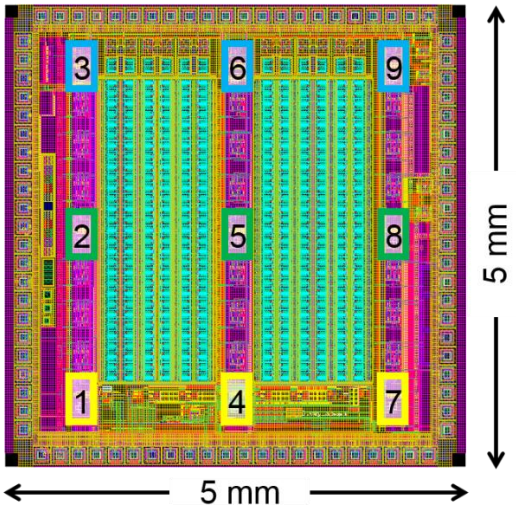
Figure 4.18. (a) The stress sensitivity of the best-case p-type (loading curve in blue, unloading curve in red) and n-type (loading curve in cyan and unloading curve in magenta) piezoresistive normal stress sensor, assuming 9x attenuation in the transferred stress at the substrate surface. (b) The Allan deviation of the stress sensors tested in (a).

The noise floor of some of the sensors on the sample chips are measured. Once again, assuming the nine-fold attenuation in stress at the substrate surface, the noise floor of the characterized n-type normal stress sensors (4 out of 9 sensors) varies from 0.9 kPa to 15.7 kPa, which bracket the expected noise floor (5.1 kPa) from design. The noise floor of the p-type normal stress sensors (3 out of 5 sensors) varies from 4.5 kPa to 36 kPa, which are much higher than the expected noise floor of 500 Pa. The higher noise floor of the p-type piezoresistive stress sensors compared to their n-type counterparts can be explained by the difference between the doping levels

of the n-wells and the p-type substrate. Since the n-type piezoresistive stress sensor performance is predicted better by the models and since the n-type sensors provide higher stress resolution (i.e., lower noise floor), only n-type normal and shear stress sensors are implemented in the second-generation accelerometer system. The best-case n-type normal stress sensor in the first-generation system can be used for compensating the accelerometer readout for 0.1 ppm scale factor stability.

The sensitivity of each n-type piezoresistive normal stress sensor in the second-generation accelerometer system is also characterized by using the Instron stress test setup. The sensor areas are numbered and the sensitivity of the normal stress sensor in each numbered area is listed in Figure 4.19. The stress sensors on the top row and the bottom row demonstrate similar sensitivities, whereas the sensors in the middle row demonstrate the highest sensitivity. The difference between the measured sensitivities is believed to come from the difference in the attenuation as the stress gets transferred from the ceramic package to the substrate surface. The average sensitivity of the normal stress sensors on the characterized sample is 26.04 pV/Pa, which compares well with the best-case sensitivity measured in the first-generation system (i.e., 26.7 pV/Pa, without taking the nine-fold stress attenuation into account). Figure 4.20 shows the best-case sensitivity (without taking any stress attenuation into account) and the typical bias stability of the n-type normal stress sensors in the second-generation accelerometer system. The measured bias stability for the stress sensors (i.e., ~ 0.9 μV) compares well with the sensors in the first-generation system (varying in the 0.2 μV to 2 μV range) as well as the estimated bias stability based on simulations (i.e., 0.62 μV). The average stress resolution is 34.6 kPa based on the average sensitivity and typical bias stability of the sensors. The calculated resolution improves proportional to the stress attenuation in practice. The nine-fold stress attenuation is simulated for the 2.5 mm × 2.5 mm chip size of the first-generation system, which may not hold exactly for the larger chip size (i.e.,

5 mm × 5mm) of the second-generation system. However, assuming nine-fold attenuation as before leads to 3.8 kPa stress resolution, which corresponds to 0.3 ppm scale factor stability for the accelerometer when compensated for the stress variations.



Sensor #	Sensitivity
1	19.86 pV/Pa
2	35.48 pV/Pa
3	16.64 pV/Pa
4	22.33 pV/Pa
5	36.46 pV/Pa
6	27.21 pV/Pa
7	20.30 pV/Pa
8	34.36 pV/Pa
9	21.70 pV/Pa

Figure 4.19. The measured sensitivity of n-type piezoresistive normal stress sensors at different sensor areas in the second-generation accelerometer system (without taking any stress attenuation into account).

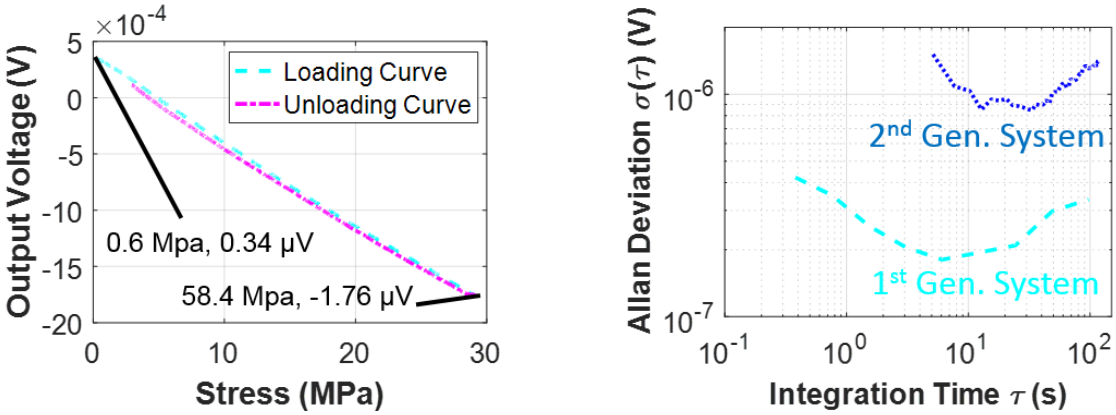


Figure 4.20. (a) The best-case sensitivity (without taking any stress attenuation into account) and (b) the typical bias stability measurement for an n-type normal piezoresistive stress sensor in the second-generation accelerometer system.

4.5 Design and Characterization of the Resonator Oscillator

4.5.1 Mechanical Design of the MEMS Resonator

The MEMS resonator is designed to match the geometry of the accelerometer cells closely (Figure 4.21) except the resonator uses comb-finger capacitive drives to improve the linearity of the capacitive change with displacement. The comb-fingers are made 10 μm long with 5 μm overlap area to allow up to 3 μm displacement while keeping the nonlinear force generated by the parallel-plate capacitance of the comb-finger tips an order of magnitude lower than the linear force generated by the change in the overlap area of the comb-fingers. The width of the comb fingers (i.e., 1 μm) and the capacitive gap between the comb-fingers (i.e., 1.25 μm) are kept small in order to fit 19 comb-fingers on the resonator proof mass and maximize the transduction force. The additional damping due to comb fingers is calculated as 2.91×10^{-8} kg/s, including 2.69×10^{-8} kg/s Couette damping (due to the air dragging in the gap between the comb fingers), 2.16×10^{-9} kg/s Stokes damping and 4.44×10^{-11} kg/s squeezed-film damping. The Stokes damping calculated for the accelerometer proof mass still apply to the resonator-oscillator proof mass; however, the squeezed-film damping due to the parallel-plate capacitance of the accelerometer cell is not relevant when calculating the damping of the resonator-oscillator. Adding the damping due to the proof mass motion, the overall damping of the resonator-oscillator is estimated as 3.90×10^{-8} kg/s, which leads to a higher quality factor estimation (i.e., $Q = 393$) than the accelerometer cell.

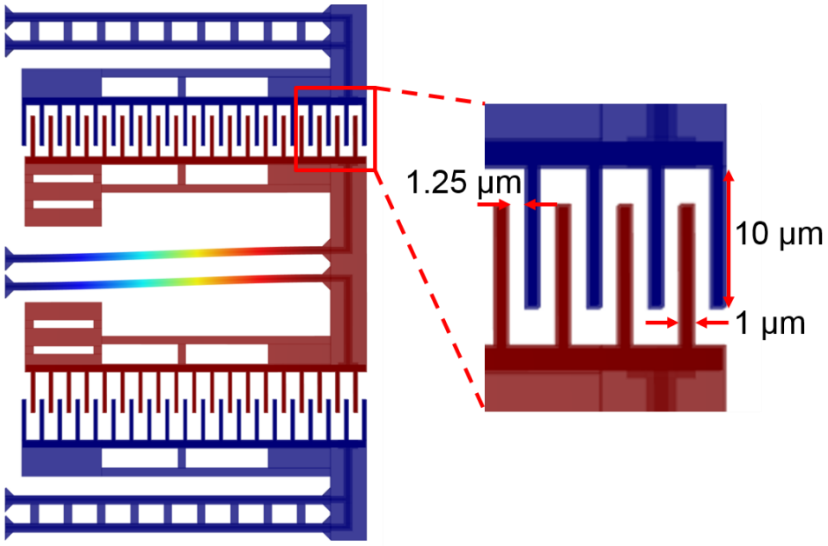


Figure 4.21. The MEMS resonator is designed similar to the accelerometer cell, so that the resonance frequency variations of the two sensors are matched to a great extent.

The resonator is oscillated by applying an AC voltage signal (V_{ac}) on the drive fingers, which generates an electrostatic force on the proof mass. The movement of the proof mass generates a motional current at the sense fingers, which is sensed to determine the amplitude and frequency of the oscillation. The resonator structure acts as a transducer that converts the voltage signal applied on the drive fingers to a proportional current signal at the sense fingers, and thereby can be modeled as an electrical equivalent circuit. To that end, the resonator is first modeled as a spring-mass-damper system similar to the accelerometer cells and the equation of motion is written for an arbitrary force (F) applied on the proof mass:

$$F = m\frac{\partial^2 x}{\partial t^2} + b\frac{\partial x}{\partial t} + kx \tag{4.21}$$

The relationship between the motional current (i_{mot}) and the velocity of the proof mass ($\partial x/\partial t$) is:

$$i_{mot} = V_p\frac{\partial C}{\partial t} = V_p\frac{\partial C}{\partial x}\frac{\partial x}{\partial t} \tag{4.22}$$

where V_p is the polarization voltage applied on the proof mass and ($\partial C/\partial x$) is the rate of change of sense and drive capacitances with displacement. Assuming the DC potential on the drive fingers (V_{dc}) is much lower than the polarization voltage, the total force applied on the proof mass (F) is:

$$F = F_{dc} + F_{ac} = \frac{1}{2}\left(V_p + V_{ac}\right)^2 \frac{\partial C}{\partial x} = \frac{1}{2}\left(V_p^2 + 2V_p V_{ac} + V_{ac}^2\right)\frac{\partial C}{\partial x} \tag{4.23}$$

which includes both a DC force term (F_{dc}) and an AC force term (F_{ac}). The AC force term sustains the oscillation and can be approximated by assuming the polarization voltage amplitude is much higher than the AC drive voltage amplitude (i.e., $V_p >> V_{ac}$):

$$F_{ac} \cong V_p V_{ac} \frac{\partial C}{\partial x} = \eta V_{ac} \tag{4.24}$$

The $V_p \partial C/\partial x$ term in (4.24) is substituted with η to indicate the proportionality between the AC force and AC drive voltage amplitudes for a given resonator design and polarization voltage. The same proportionality is present between the motional current and the velocity of the proof mass as shown in (4.22). In the next step, the displacement (x) and its derivatives in (4.21) are written in terms of the motional current, and the AC force term that generates the motional current is written in terms of the AC drive voltage:

$$V_{ac} = \frac{m}{\eta^2}\frac{\partial i_{mot}}{\partial t} + \frac{b}{\eta^2} i_{mot} + \frac{k}{\eta^2}\int_{-\infty}^{t} i_{mot}\, dt \tag{4.25}$$

In this equation, the m/η^2 term is defined as the motional inductance (L_m), the b/η^2 term is defined as the motional resistance (R_m) and the k/η^2 term is defined as the inverse of the motional capacitance ($1/C_m$). At resonance, the impedances of the motional inductance and capacitance cancel each other and the resonator behavior approaches to that of a resistor. Therefore, the relationship between the drive voltage (V_{ac}) and the motional current (i_{mot}) at resonance is simply set by the motional resistance of the resonator.

The equivalent circuit of the designed resonator is shown in Figure 4.22 along with the calculated values of the circuit components assuming 50 V polarization voltage. The capacitance (C_0) in parallel with the series R-L-C circuit, represents any parasitic coupling capacitance from drive fingers to sense fingers that leads to feedthrough current at the signal frequency (i.e., $i_{ac} = C_0 \partial V_{ac}/\partial t$). The resonance frequency can be calculated by using the motional inductance and motional capacitance values, which leads to the same expression used for calculating the resonance frequency of the accelerometer:

$$\omega_0 = \sqrt{\frac{1}{L_m C_m}} = \sqrt{\frac{k}{m}} \tag{4.26}$$

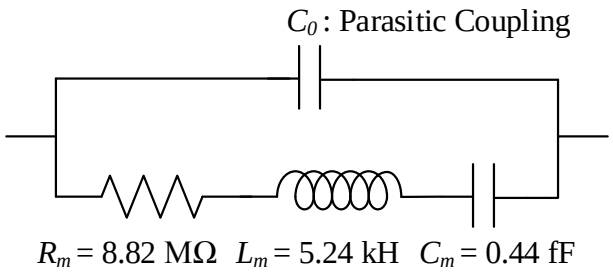


Figure 4.22. The equivalent circuit of the designed MEMS resonator.

For an ideal comb-drive, the capacitance change with displacement is perfectly linear (i.e., $\partial C/\partial x$ is constant). However, the misalignments between the comb-fingers due to lateral curl of the spring beams after release can introduce nonlinearities in capacitance change with displacement, which leads to electrostatic spring softening and a reduction in resonance frequency with increased polarization voltage amplitude [135]. The effective voltage across the capacitive gaps are prone to vary due to dielectric charging in CMOS-MEMS devices, therefore the charging

problem is expected to lead to resonance frequency drift as in [135] and potentially limit the frequency stability of the resonator-oscillator.

4.5.2 Oscillator Design with On-Chip Sustaining Amplifier

The oscillations of the resonator are sustained by a transimpedance amplifier (i.e., a sustaining amplifier), which senses the motional current at the sense fingers and provides an amplified voltage output to drive the oscillations (Figure 4.23). The loop gain is unity and the phase shift around the loop is around 360° when the oscillations reach steady state. However, the sustaining amplifier gain should be at least three times higher than the motional resistance in order to be able to start-up the oscillations [154]. The amplifier should also have a bandwidth greater than the oscillation frequency in order to prevent the signal attenuation, which implies a high gain-bandwidth product when both the oscillation frequency and motional resistance are high. The resonance frequency of the resonator-oscillator (simulated: 107.4 kHz, calculated: 105.3 kHz) is set by the mechanical design and is slightly lower than the resonance frequency of the accelerometer cells (simulated: 118 kHz, calculated: 116.2 kHz) due to the additional mass introduced by the comb fingers. On the other hand, the motional resistance can be reduced by decreasing the damping, increasing the polarization voltage and increasing the sense and drive capacitance by either decreasing the capacitive gap between the comb fingers or increasing the number of fingers. The easiest way to reduce the motional resistance is decreasing the damping by operating the resonator in vacuum; however, the simultaneous reduction in the damping of the accelerometer cells would lead to excessive ring-down time in this case. Instead, the minimum polarization voltage is set as 40 V in the design step, the capacitive gaps between the comb fingers are kept small (i.e., 1.25 μm) and maximum number of fingers are fit on the proof mass by making the comb fingers narrow (i.e., 1 μm). When the capacitive gaps are made smaller, the oxide etch

time may need to be increased to remove the oxide in the gaps completely. When the comb fingers are made narrower, the milling on the top metal during oxide etch step can lead to metal delamination during the silicon etch step unless the top metal is removed before the silicon etch.

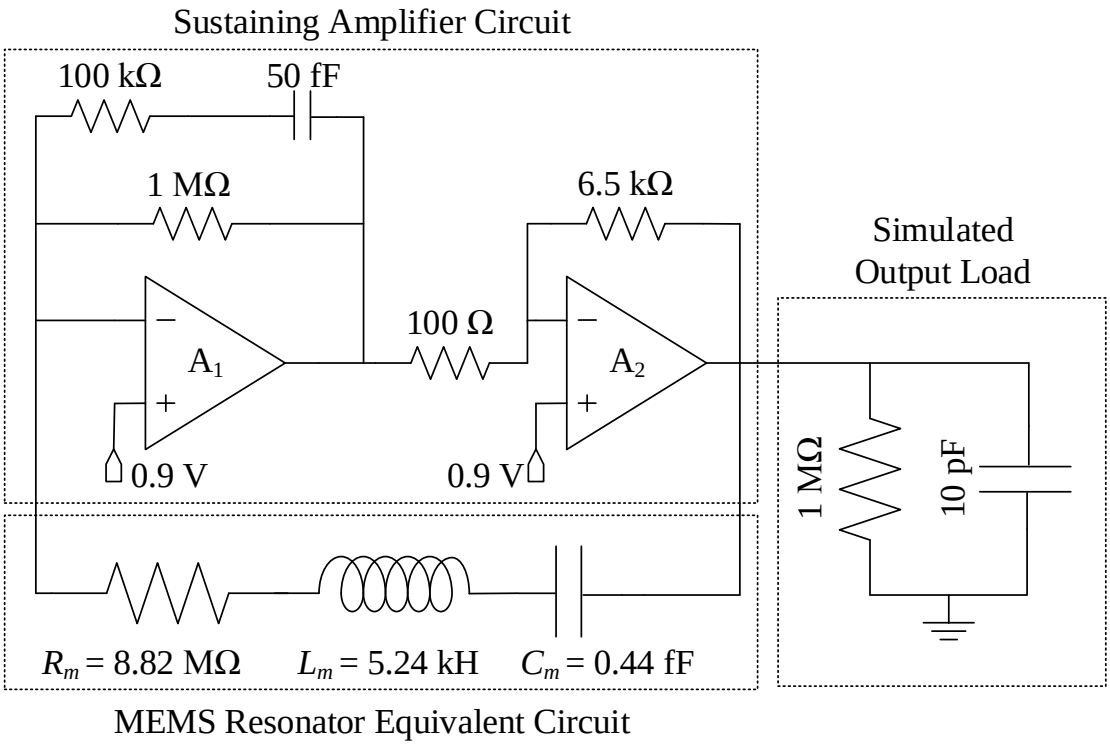
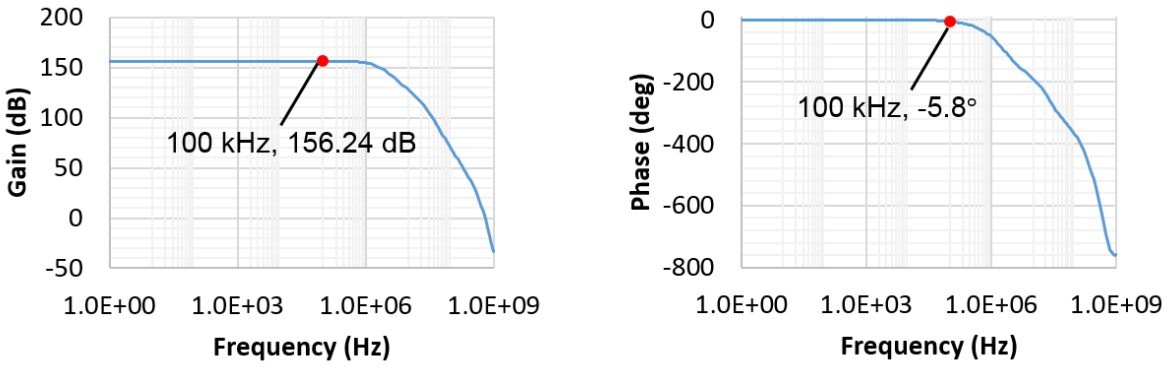


Figure 4.23. Resonator-oscillator circuit, where the transimpedance amplifier sustains the oscillations by forming a feedback loop around the resonator.

The sustaining amplifier is designed as a two-stage amplifier (Figure 4.23) with a transimpedance amplifier in the first stage and an inverting voltage amplifier in the second stage. The phase shift introduced by each amplifier stage is ideally 180°, leading to a total of 360° phase shift around the loop. The overall gain of the sustaining amplifier is 65 MV/A, which is set more than 5 times higher than the motional resistance of the resonator to ensure the start-up of oscillations. The simulated gain is 64.9 MV/A (Figure 4.24 (a)) and phase shift is around –6.6° (Figure 4.24 (b)). The simulated bandwidth is 1.4 MHz when the sustaining amplifier output is

loaded with 1 MΩ resistance and 10 pF capacitance to ground; however, the resistive load is much higher and the capacitive load is lower when the AC drive signal (V_{ac}) is routed and interfaced to a buffer on the printed-circuit board, hence implying higher bandwidth. The transistor level design of the operational amplifier used in the sustaining amplifier circuit is provided in Appendix A.2. The operational amplifier design is taken from legacy tape-out libraries and its gain-bandwidth product is improved by Mary Elizabeth Galanko at Carnegie Mellon University. The transimpedance amplifier stage is also designed by Mary Elizabeth Galanko.

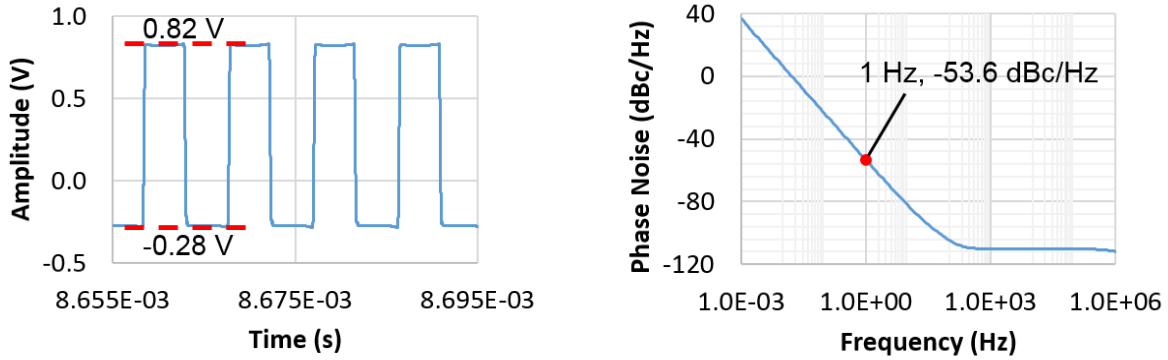


(a) (b)

Figure 4.24. (a) Simulated gain and (b) phase shift introduced by the sustaining amplifier.

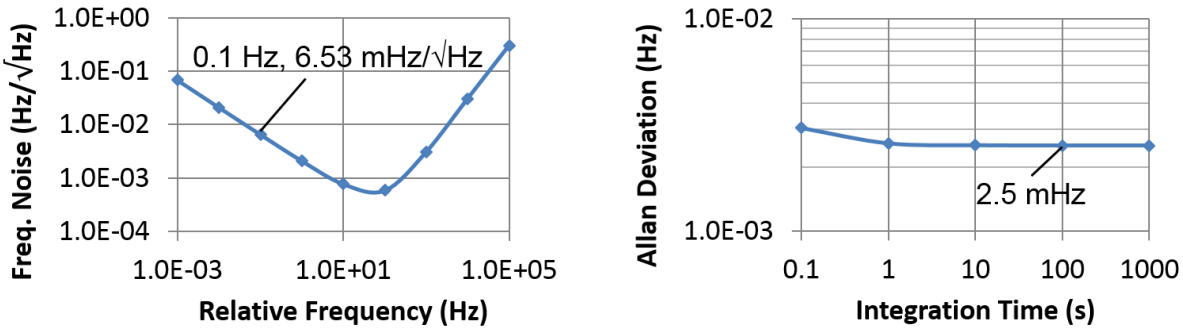
The resonator-oscillator is simulated by connecting the sustaining amplifier with the equivalent circuit model of the resonator as in Figure 4.23. The feedthrough capacitance of the resonator is excluded and the loading at the sustaining amplifier output (i.e., 1 MΩ resistance and 10 pF capacitance to ground) is included in the simulations. The voltage waveform at the output of the sustaining amplifier (i.e., V_{ac}) is monitored as the resonator-oscillator output. The peak-to-peak amplitude of the oscillation is set by the rail-to-rail voltage swing range of the sustaining amplifier and is around 1.1 V as shown in Figure 4.25 (a). The phase noise power of the oscillation waveform (Figure 4.25 (b)) is estimated by running a phase noise simulation. The frequency noise

power (i.e., $S_f(f_c)$) is calculated by multiplying the phase noise power (i.e., $S_\varphi(f_c)$) with the squared offset frequency from the carrier (i.e., $S_f(f_c) = f_c^2 \times S_\varphi(f_c)$ [155]). The frequency noise spectrum and the corresponding Allan deviation of the resonance frequency are plotted in Figure 4.26 (a) and Figure 4.26 (b), respectively. The estimated bias stability of the resonance frequency (i.e., ~ 2.5 mHz) corresponds to 0.02 ppm frequency stability for the resonator and satisfies the 0.5 ppm stability requirement for 1 ppm accelerometer scale factor stability.



(a) (b)

Figure 4.25. (a) The output voltage waveform and (b) the estimated phase noise of the resonator-oscillator.



(a) (b)

Figure 4.26. (a) The frequency noise spectrum and (b) the corresponding Allan deviation of the resonance frequency of the resonator-oscillator.

The phase noise estimation accounts for the resonator thermal-mechanical noise and the sustaining amplifier noise. The comb fingers used for sense and drive capacitors improve the

linearity of the capacitance change with displacement, hence reducing the potential noise contribution due to resonator nonlinearities [156] that is not accounted in the simulations. The polarization voltage source can also introduce additional noise [157]; however, the more critical problem that can arise in CMOS-MEMS devices is the continuous drift in the effective voltage across the capacitive gaps due to dielectric charging. The drift in the effective polarization voltage translates to resonance frequency drift when the capacitance change is not perfectly linear, thereby dielectric charging is the most likely problem to limit the frequency stability in practice.

4.5.3 Measured Frequency Stability of the Resonator-Oscillator

The first step before testing the resonator-oscillators is the release of the MEMS resonators in the post-CMOS MEMS process (Figure 4.27) along with the accelerometer cells. The charge traps in the CMOS dielectric and in the sidewall polymer deposited during the post-processing steps cause charge build-up, which reduces the effective voltage across the capacitive gaps and increases the resonance frequency continuously. The resonance frequency drift is observed on the resonator-oscillators in both the first-generation accelerometer system and the second-generation accelerometer system. In order to characterize the stability of the resonance frequency at steady state, one of the resonator-oscillators was allowed to run until random-walk behavior was observed. Reaching the steady-state operation took about 80 h, which is unacceptably long for practical use of these sensors in scale factor compensation of the accelerometer.

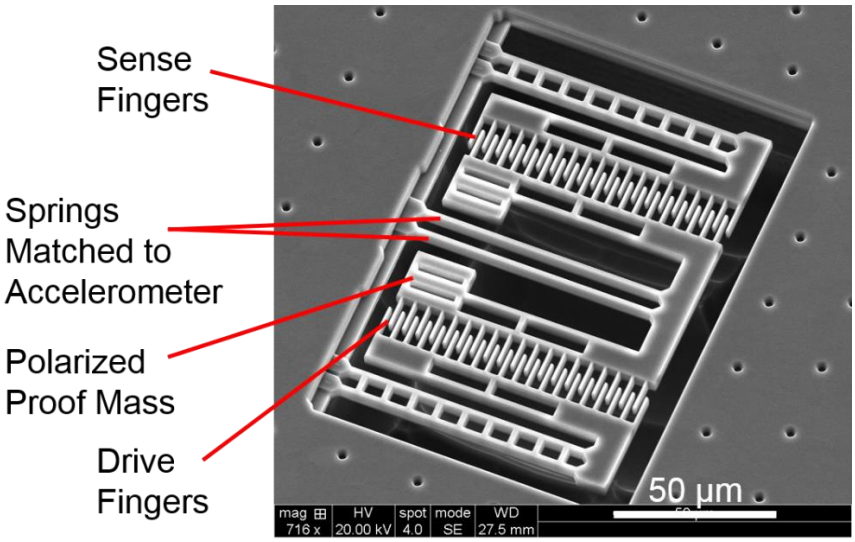
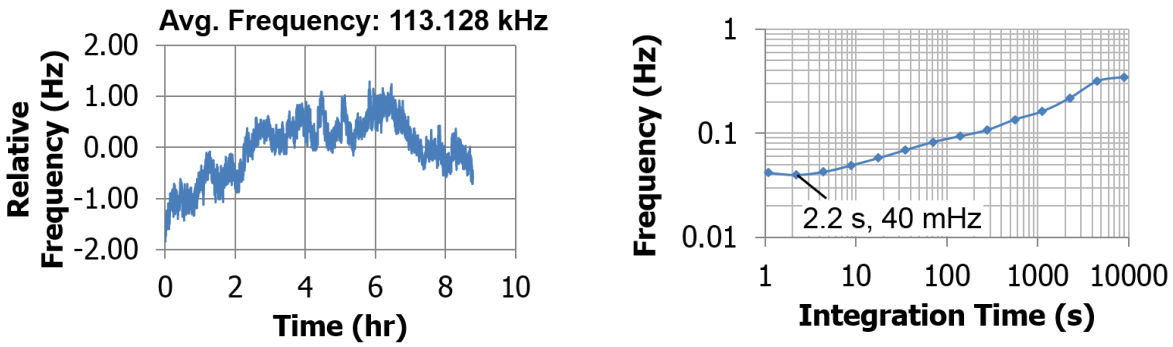


Figure 4.27. Scanning electron micrograph of a released MEMS resonator.

Once the steady-state operation was reached, frequency data was collected (Figure 4.28 (a)) to characterize the stability of the resonance frequency. The Allan deviation of the collected frequency data (Figure 4.28 (b)) indicates 40 mHz frequency resolution at around 2.2 s integration time, which corresponds to 0.4 ppm frequency stability for the resonator-oscillator and 0.8 ppm scale factor stability for the accelerometer. The peak to peak variation of the resonance frequency over about 9 h measurement time (Figure 4.28 (a)) is around 2.5 Hz, which corresponds to 22.1 ppm frequency stability for the resonator-oscillator and 44.2 ppm scale factor stability for the accelerometer. Assuming the resonance frequency variation is dominated by the variation of the spring constant due to temperature dependence of Young's modulus, the 2.5 Hz variation in resonance frequency corresponds to 0.22 °C variation in temperature. Therefore, the measured frequency stability of the resonator-oscillator is believed to be limited by the temperature and humidity variations in the environment, implying that it can possibly reduce the scale factor drift of the accelerometer even further with proper compensation.



(a) (b)

Figure 4.28. (a) The frequency drift of the resonator-oscillator at steady-state operation and (b) the corresponding Allan deviation.

The similarity in the mechanical designs of the resonator-oscillator and the accelerometer cells also leads to similar quality factors as indicated by the calculations. The quality factor of the resonator-oscillator is determined simply by observing the ring-up behavior (Figure 4.29) upon the application of polarization voltage and extracting the ring-up time constant ($\tau = 2Q / \omega_0$) from the experiment. The polarization voltage needs to be turned on with a sharp slope in order to approximate a step input, which is achieved by using a function generator (whose output corresponds to the red curve in Figure 4.29) and a 100x voltage amplifier (which amplifies the 500 mV function generator output to 50 V). The measured ring-up time (~ 1.025 ms) corresponds to a quality factor of about 365 in air, which is comparable to the estimated quality factor (i.e., $Q = 393$) based on hand analysis.

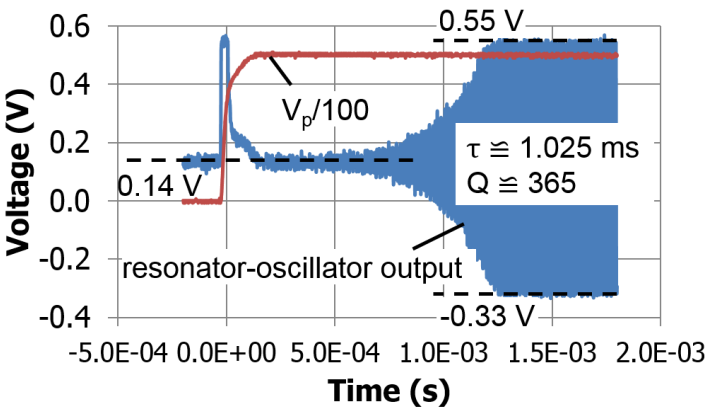


Figure 4.29. Measurement of resonator-oscillator ring-up time for determining the quality factor.

The charging behavior of the resonator-oscillators and the built-in potential on the structures due to charging are further investigated. Figure 4.30 (a) shows the drift in the resonance frequency of an oscillator when 50 V polarization voltage is applied with different duty cycles (with fixed 1 s ON-time), where the slope of the drift profile and the total drift increase as the duty cycle of the polarization voltage is increased. The drift in the resonance frequency is observed even when the proof mass is grounded for 80% of the time (i.e., 20% duty cycle), implying that the charging rate is higher than the discharging rate. The drift profile is slightly different when the experiment is repeated a week later (Figure 4.30 (b)) indicating that the built-in charge (i.e., the built-in potential) on the structure is prone to vary over time and affects the charging behavior. In order to have an idea about the magnitude of the built-in potential, the resonance frequency of the oscillator is measured at different polarization voltage levels as shown in Figure 4.31 and a second-order polynomial is fit on the measurements. The minimum polarization voltage magnitude needed for sustained oscillations is 37 V, therefore the measurements are made at polarization voltage magnitudes above 40 V. The fitted polynomial shows that the maximum resonance frequency is obtained when the polarization voltage is set to 1.6 V, which implies –1.6 V built-in potential. The

variation of the built-in potential over time and the dependence of charging behavior on the initial and final potentials of the proof mass need to be studied further to model the frequency drift of the resonator and stabilize its resonance frequency rapidly through controlled application of potentials. Since long wait times are needed for the resonance frequency to stabilize, the resonator-oscillators are not used in the system-level tests for bias drift compensation.

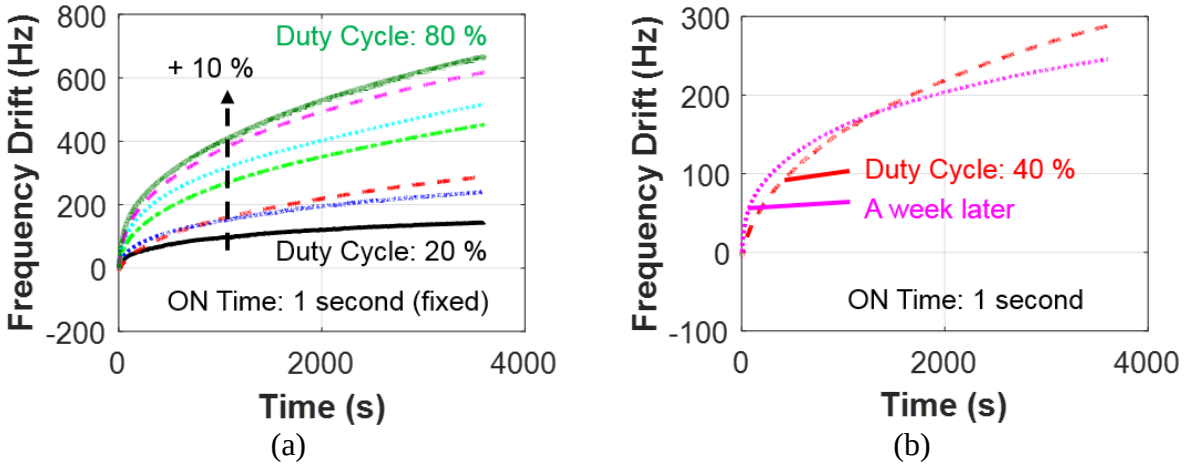


Figure 4.30. (a) Resonance frequency drift at 50 V polarization voltage with different duty cycles. The duty cycle is increased from 20% to 80% with 10% increments, which increases the slope of frequency drift. (b) The drift profile changes when the experiment is repeated a week later.

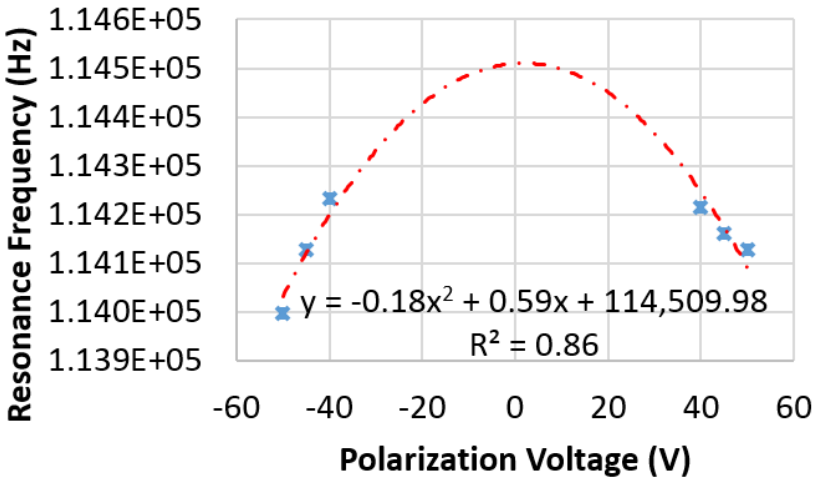


Figure 4.31. Built-in potential estimation based on resonance frequency measurements at different polarization voltages.

4.6 Performance Summary of Environmental Sensors

Table 4.1. Comparison of designed and measured PTAT and stress sensor specifications

	Sensitivity	**Resolution**	**$\Delta S_T/S_T$ Stability**
PTAT *(Designed)*	2.84 mV/K	4.85 mK	1.7 ppm
PTAT *(Measured- 1st Gen. Sys.)*	3 mV/K	6.7 mK	2.4 ppm
PTAT *(Measured- 2nd Gen. Sys.)*	3.1 mV/K	7.1 mK	2.6 ppm
P-type normal stress *(Designed)*	1.24 nV/Pa	500 Pa	0.03 ppm
P-type normal stress *(Measured- 1st Gen. Sys.)*	0.38 – 1.12 nV/Pa	4.5 – 36 kPa	0.3 – 2.5 ppm
N-type normal stress *(Designed)*	122.4 pV/Pa	5.1 kPa	0.4 ppm
N-type normal stress *(Measured- 1st Gen. Sys.)*	55.1 – 240 pV/Pa	0.9 – 15.7 kPa	0.1 – 1.1 ppm
N-type normal stress *(Measured- 2nd Gen. Sys.)*	149.8 – 328.1 pV/Pa	2.7 – 6 kPa	0.2 – 0.4 ppm

The PTAT temperature sensor is essentially a temperature sensitive circuit designed in the CMOS process. The foundry models provided for the fundamental circuit elements in the CMOS process help estimating the sensitivity and noise floor of the PTAT temperature sensor accurately through CADENCE simulations. The measured sensitivity and noise floor of the PTAT temperature sensor are in close agreement with the design predictions as seen in Table 4.1. The performance is repeatable from one sensor to the other on the same chip and from one run to the other in the same CMOS process. The measurement of temperature variations with 7.1 mK resolution and the compensation of accelerometer signal for these variations should lead to 2.6 ppm scale factor stability for the accelerometer.

The n-type piezoresistive stress sensors are designed by using the built-in n-well resistors in the process. The flicker noise is modeled only for high resistivity polysilicon resistors in the

process, therefore the noise simulations are made by using polysilicon resistors sized similar to the n-well resistors used in the sensor design. The measured noise floor of the n-type piezoresistive stress sensors is predicted closely, whereas the p-type piezoresistive stress sensors are found to exhibit higher amount of noise compared to their n-type counterparts. The sensitivities of both n-type and p-type stress sensors are estimated based on the piezoresistive coefficients reported in literature for lightly doped silicon. Assuming the transferred stress at the substrate surface is nine-fold attenuated compared to the applied stress on the ceramic package, the measured n-type piezoresistive sensor sensitivities closely match the predicted sensitivity as seen in Table 4.1. The sensitivities of the p-type piezoresistive sensors are higher than the n-type sensors but lower than predicted. The higher sensitivity of the p-type sensors is not enough to compensate for their high noise floor, hence leading to a lower stress resolution compared to their n-type counterparts. The n-type piezoresistive sensor behavior is predicted better by the models and the obtained stress resolution is higher, thereby the second-generation accelerometer system uses only n-type sensors. The best-case stress resolution obtained with the n-type piezoresistive stress sensors is 0.9 kPa in the first-generation system, which corresponds to a scale factor stability of 0.1 ppm for the accelerometer.

Table 4.2. Comparison of designed and measured resonator-oscillator specifications

	Designed	**Measured (1st Gen. Sys.)**
Quality factor	393	365
Resonance frequency	107.4 kHz	113.1 kHz
Frequency resolution	2.5 mHz	40 mHz
$\Delta S_T/S_T$ stability	0.02 ppm	0.8 ppm

The quality factor and the resonance frequency of the resonator-oscillator are closely predicted (Table 4.2). The measured frequency stability of an oscillator in the first-generation accelerometer system is 0.4 ppm once the dielectric charging reaches steady state. The measurement of resonance frequency variations with 40 mHz resolution and the compensation of accelerometer signal for these variations should lead to 0.8 ppm scale factor stability for the accelerometer. The measured frequency resolution of the resonator-oscillator is believed to be limited by the environmental variations, thereby the inherent frequency stability of the resonator-oscillator is believed to be higher (i.e., closer to the design prediction). However, the resonator-oscillators require a long wait time for the dielectric charging and frequency drift to settle before the frequency measurements can be used for compensating the scale factor of the accelerometer. The slope of the frequency drift is shown to increase with the duty cycle of the applied polarization voltage. The initial and final potential of the proof mass are believed to change the charging time constants, hence the frequency drift profile. The charging behavior needs to be investigated for different initial and final potentials on the proof mass under steady environmental conditions to model and predict the frequency drift before using the oscillators for scale factor compensation.

CHAPTER 5: CHARACTERIZATION OF THE CAPACITIVE ACCELEROMETER ARRAY

5.1 Accelerometer System Description

The accelerometer system was fabricated in TowerJazz CA18HA (0.18 μm CMOS) process, plus post-CMOS MEMS processing. Two accelerometer arrays are employed on the chip: a small array with 56 cells and a larger array with 280 cells with separate readout circuits (Figure 5.1). All the accelerometer readout circuits are designed by Xiaoliang Li at Carnegie Mellon University. The 280 cell accelerometer array (112 + 168 cell arrays combined) is interfaced with a more sophisticated readout circuitry. In the preliminary experiments, the measured noise floor of the 280 cell array with this readout circuit was higher, thereby this chapter focuses on the characterization of the 56 cell array with a simplified readout circuit.

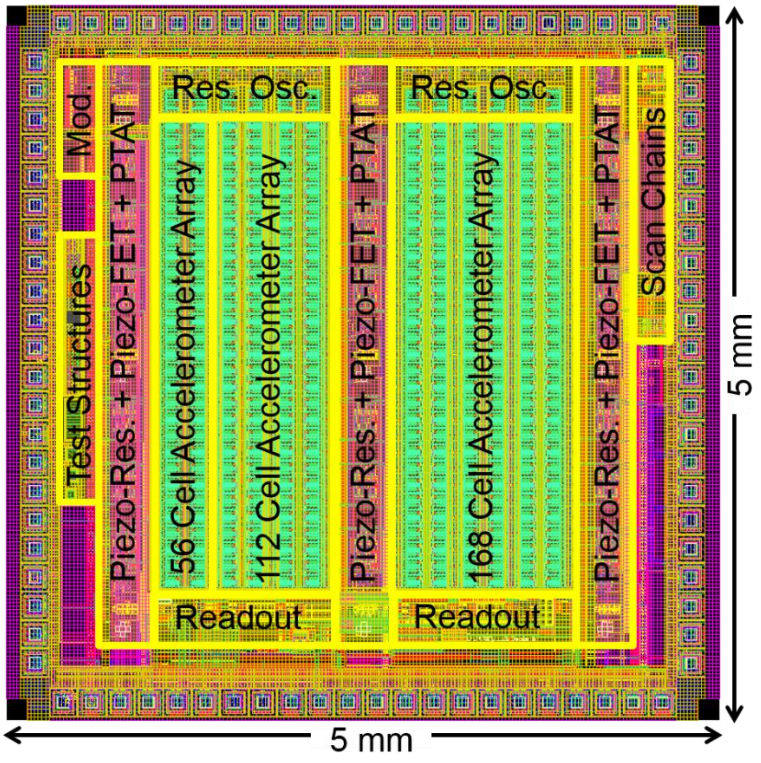


Figure 5.1. The complete accelerometer system-on-chip.

The 56 cell accelerometer array interfaces with a single-stage, low-noise, low-gain (24.1 dB), continuous-time voltage amplifier with hard-wired connections to the bond-pads for input biasing and off-chip modulation and demodulation. The low gain of the circuit reduces the risk of saturation due to AC or DC offset; however, the DC offset can be cancelled by tuning the input bias voltages and the AC offset can be cancelled by tuning the modulation voltage amplitudes as detailed in section 2.3.3. The simplified circuit topology, hard-wired connections to bond-pads and the off-chip generation of the modulation signal minimize the risk of failure for the readout circuitry.

The accelerometer system also consists of various auxiliary sensors for the measurement of environmental variations and subsequent compensation of the accelerometer readout. The system layout includes 12 resonator-oscillators, 9 PTAT temperature sensors, 9 n-type piezoresistive normal stress sensors and 9 n-type piezoresistive shear stress sensors distributed on the chip (Figure 5.1). The layout also includes piezo-FET stress sensor designs of Vincent Pey J. Chung, which are not characterized and discussed in this study.

The block diagram of the accelerometer system is shown in Figure 5.2. The PTAT temperature sensors, piezoresistive stress sensors and resonator-oscillators on the chip are selected by programming a scan chain through an Arduino® UNO (Arduino AG, Italy) interface on the board. A separate scan chain is programmed to independently power up (or power down) the resonator-oscillators. The outputs of temperature and stress sensors are directly routed to a multi-meter for recording the signal from one sensor at a time. The resonator-oscillator signal passes through a buffer on the board before it connects to a frequency counter, which records the resonance frequency of one oscillator at a time. A multiplexer selects between the circuit-test inputs and the capacitive bridge outputs on the chip. The signal from the on-chip readout circuit is

further amplified on the board before it gets demodulated, filtered and recorded. CMOS switches are employed on the board for generating the modulation waveform and performing demodulation. The switches are clocked by using a high stability (i.e., < 5 ppb frequency stability) oven-controlled crystal oscillator on the board. A continuous-time second-order low-pass filter ($f_c = 1$ kHz) is used for anti-aliasing before analog-to-digital conversion. National Instruments® (National Instruments Corporation, Austin, TX) NI-USB-6212 data acquisition system is used for recording the data. The modulation, demodulation, filtering and data-acquisition operations on the board can be bypassed to interface the testbed with Zurich Instruments® (Zurich Instruments AG, Switzerland) HF2LI lock-in amplifier. A detailed description of the testbed, including the printed-circuit board schematics with the part numbers for the employed off-the-shelf components are provided in Appendix B.

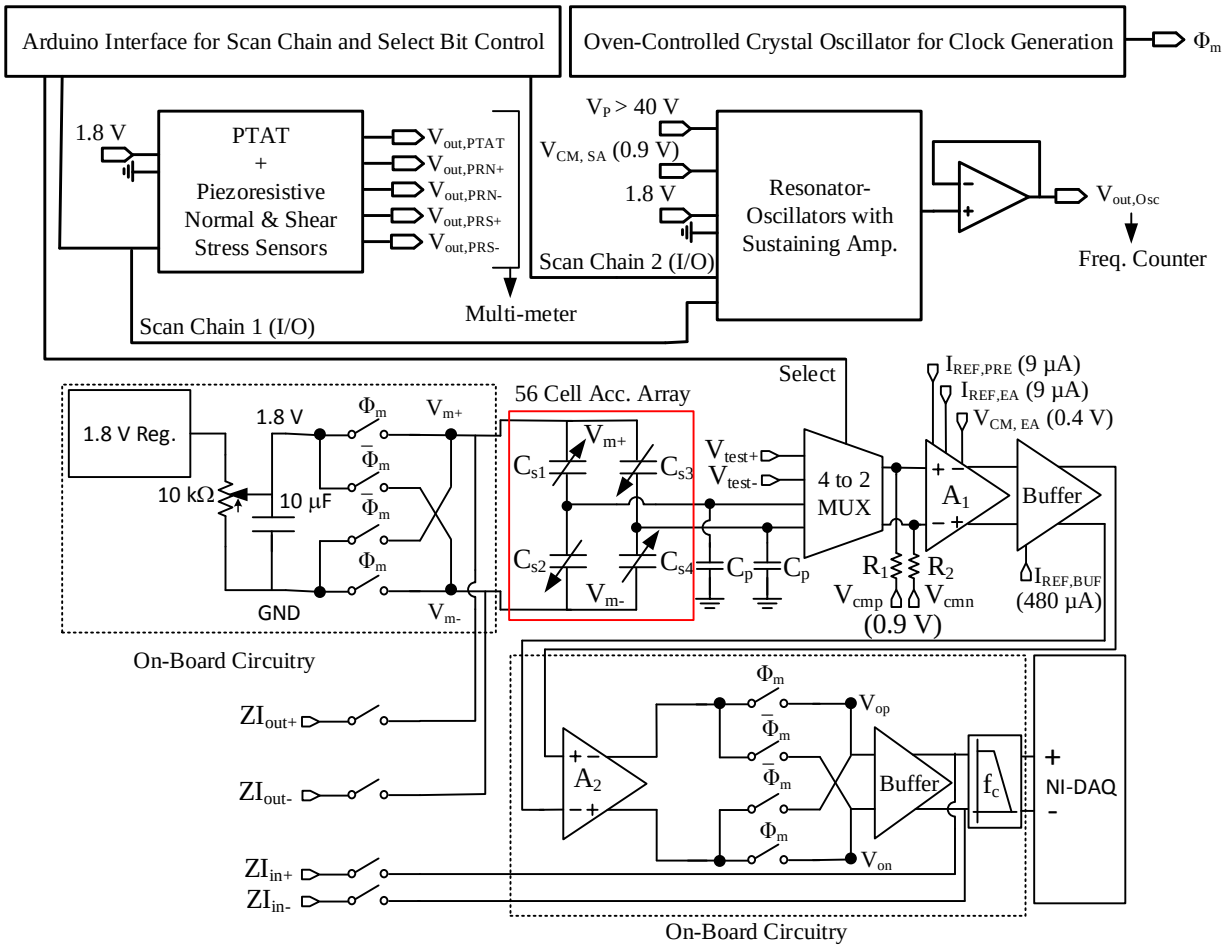


Figure 5.2. Block diagram of the accelerometer system.

5.2 Transducer Scale Factor

The effects of post-CMOS MEMS processing steps on the transducer scale factor are discussed in section 3.2.3. The substrate undercut obtained during the isotropic silicon etch process affects the parasitic capacitance of the signal routing, hence the scale factor. Removal of the top metal reduces the sense capacitance and parasitic capacitance simultaneously, thereby also affects the scale factor. The estimated transducer scale factor for the chips before the top metal removal is 1.18 μV/G when the lateral undercut length is around 10 μm. The scale factor is expected to reduce by 1.7% upon top metal removal (i.e., from 1.18 μV/G to 1.16 μV/G) when the lateral

undercut length is 10 μm, since the sense capacitance decreases (from 3.43 fF to 3.07 fF) whereas the total parasitic capacitance per cell does not change much (i.e., it reduces from 48.6 fF to 42.4 fF) as it is dominated by the capacitance to substrate underneath the accelerometer signal routing and circuit input capacitance. Sample chips were tested after the first attempts of post-CMOS MEMS processing (with the re-deposition problem on the etch area) and after the post-CMOS MEMS processing was modified (with the photo-resist mask on the edges of the chip to eliminate the re-deposition problem). The scale factor measurements on clean chips with and without top metal are compared.

The scale factor of the accelerometer is characterized by modulating the acceleration signal at 100 kHz and applying 100 Hz sinusoidal vibrations on a shaker table (Bruel & Kjaer Type-4808) ranging from 10 G peak-to-peak to 50 G peak-to-peak as measured by using a Bruel & Kjaer 4371 accelerometer as reference (Figure 5.3). This experiment is run conveniently by using the ZI-HF2LI lock-in amplifier.

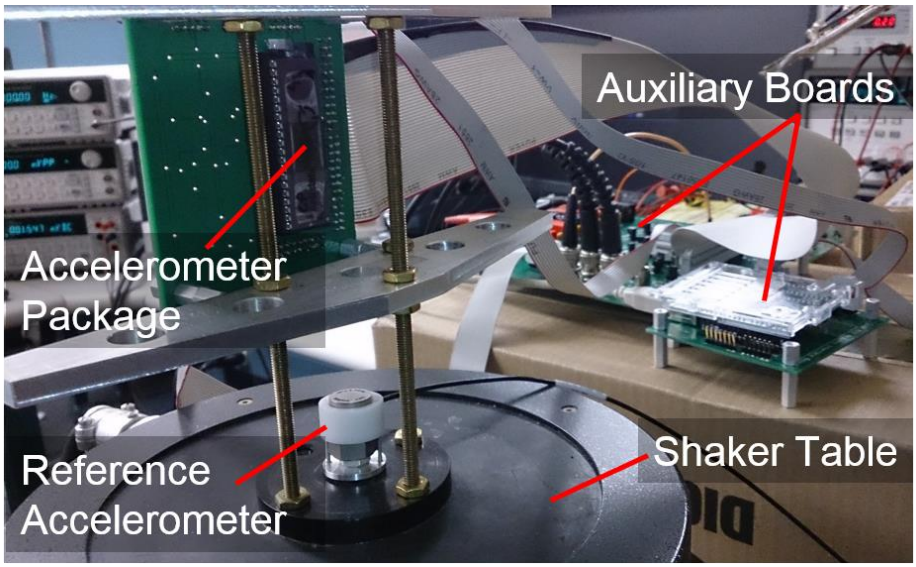


Figure 5.3. Shaker table testbed for characterizing the scale factor of the accelerometer.

The output signal data of the device under test (DUT) (Figure 5.4) fits to a sinusoidal function in order to determine the signal amplitude, which is verified by monitoring the power spectrum of the response. The transfer function of the readout circuit (Figure 5.5), measured with the HF2LI, provides the system gain that is used to refer the measurements to the transducer's capacitive bridge output. The data found by linear fitting across 10 to 50 G peak-to-peak acceleration range is shown in Figure 5.6 (a) and (b) for the chips "with re-deposition" and "without re-deposition" problem (both with top metal), respectively, where the voltages are referred to the output of the accelerometer capacitive bridge. The slope in each of these plots is the intrinsic transducer scale factor prior to circuit amplification. The transducer scale factor increases from 0.60 μV/G to 1.07 μV/G after the improvements in processing. The measured scale factor on the clean chips (1.07 μV/G) compares well with the estimated scale factor (1.18 μV/G) for the chips with top metal and 10 μm lateral undercut. However, the scale factors of two subsequently processed chips are found to be around 0.85 μV/G and one another chip having a scale factor around 0.6 μV/G even after the process improvements.

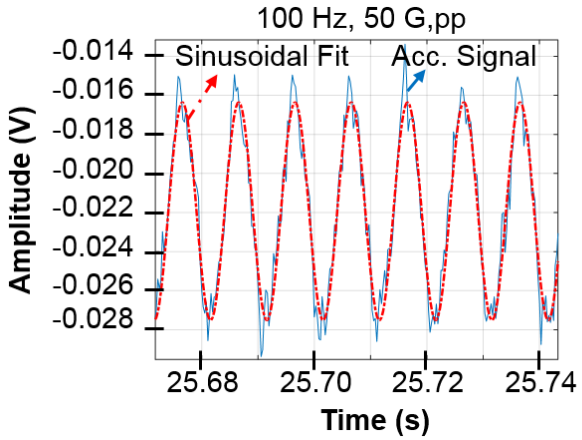


Figure 5.4. The blue trace is the measured acceleration signal at 50 G,pp, 100 Hz. The red trace is a sinusoidal function fitted on the acceleration signal in order to determine the signal amplitude.

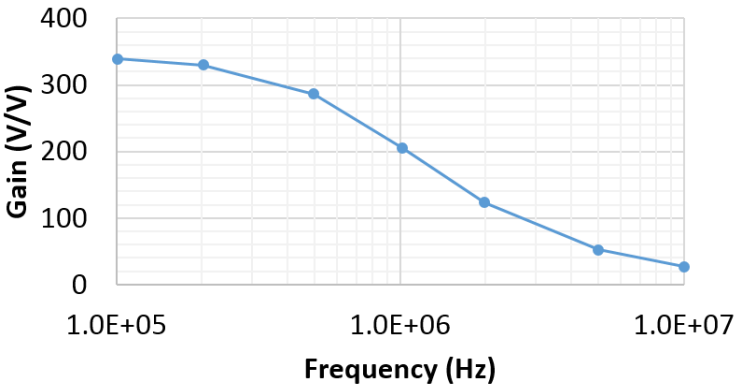
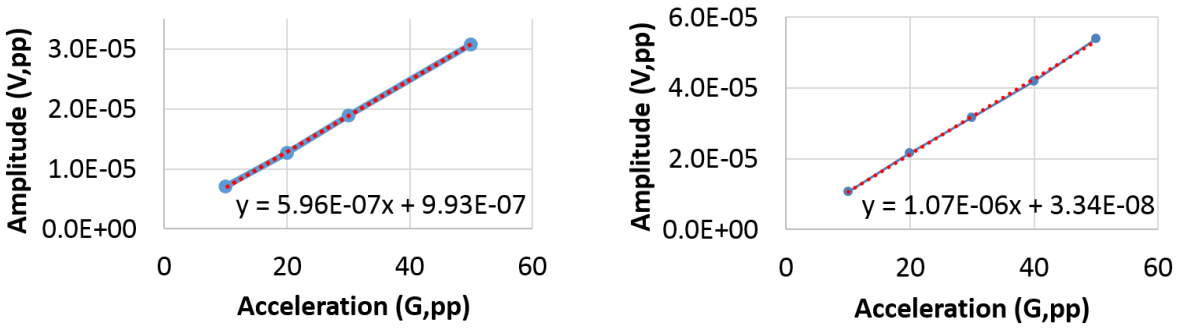


Figure 5.5. Transfer function of the signal path from the test inputs (V_{test}) to readout circuit output (V_{out}).



(a) (b)

Figure 5.6. Transducer scale factor measurement on chips (a) with re-deposition problem and (b) without re-deposition problem.

The accelerometer is also shown to function after the removal of the top metal. The estimated scale factor drops by only 1.7% (i.e., from 1.18 μV/G to 1.16 μV/G) upon top metal removal, thereby similar scale factor measurements are expected on the chips with and without top metal. The scale factor is measured as 0.87 μV/G (Figure 5.7) after top metal removal, which aligns well with the scale factor measurements taken on two of the chips with top metal (i.e., 0.85 μV/G). The measured scale factor is slightly lower than the estimated scale factor, which is believed to result from the additional parasitic capacitance loading at the input of the on-chip amplifier, such as the capacitance of the signal routing from the accelerometer array to on-chip

amplifier, the capacitance of the multiplexer that selects between transducer signal and test signals, and the capacitance of the biasing resistors. The chip-to-chip variation in measured scale factor remains to be investigated.

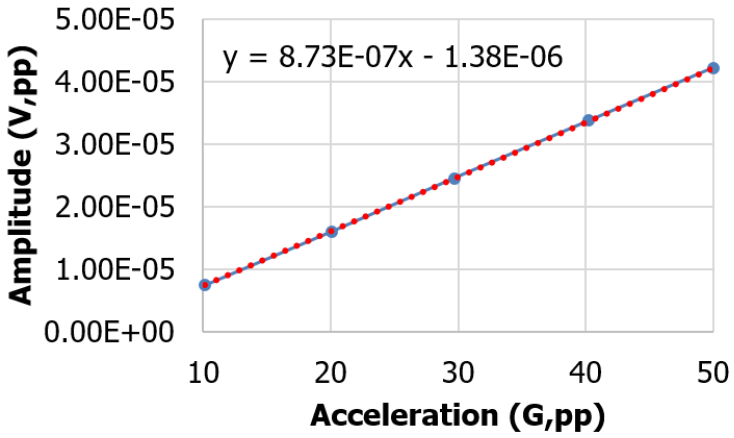


Figure 5.7. Transducer scale factor measurement after the removal of the top metal.

5.3 Shock Response

5.3.1 Split Hopkinson Bar Test Setup

The split Hopkinson bar test setup (Figure 5.8) is acquired from REL Inc. (REL Inc., Calumet, MI) for testing the shock response of the accelerometer. The system uses a gas gun that fires pressurized air (or nitrogen if higher pressures are desired) to put a striker bar into motion, which creates an impact on the incident bar and initiates a strain pulse. The generated strain is converted into shock loading on the accelerometer through the aluminum sled, which is designed in collaboration with REL. The device under test (DUT) mounts in a zero insertion force socket on a printed-circuit board and the board is screw mounted at the center of the sled. The 40-pin DIP package housing the accelerometer device under test is entrained by a set of aluminum blocks bolted into the sled. The sled contacts the incident bar prior to firing the gas gun. Located on the other side of the sled is a damper (i.e., shock absorber) to absorb the energy of the sled and stop

the motion. A high-G reference accelerometer (Meggitt 7270A-60KM4) is screw mounted directly on the sled and measures the generated acceleration and deceleration profile.

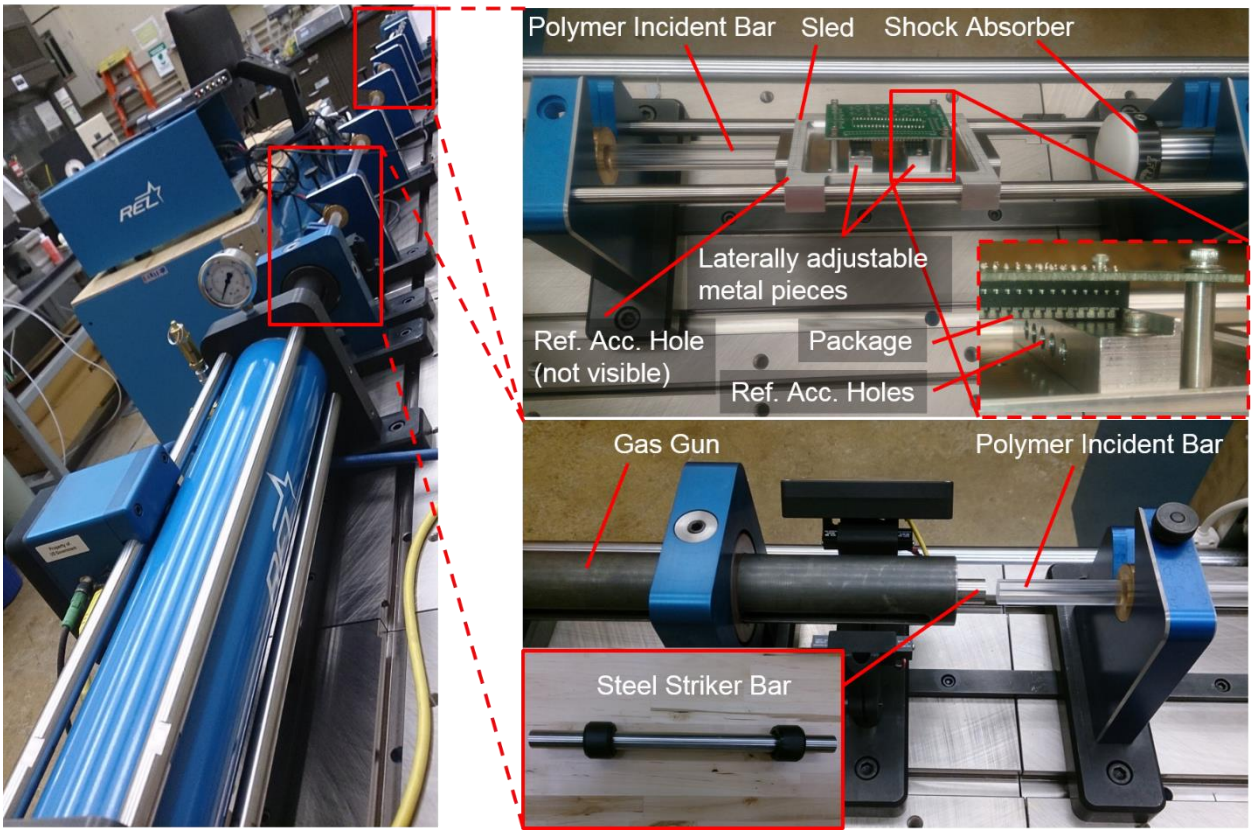


Figure 5.8. Split Hopkinson bar test setup to measure the shock response of the accelerometer.

Two custom, machined aluminum pieces create a trench for the accelerometer's ceramic DIP package (Figure 5.9). These pieces adjust to contact laterally to both sides of the ceramic package, thereby enhance the acceleration transfer between the sled and the DUT. They also prevent the package from detaching from the socket upon impact. The holes opened on these pieces are used for mounting the reference accelerometer adjacent to the DUT in order to ensure similar acceleration profiles for the two accelerometers when the impact on the sled is not completely transferred to the DUT. Aluminum screws break due to the shear stress exerted on them during shock events. Mounting the printed-circuit board with black-oxide alloy steel screws (with

170,000 psi tensile strength) and steel spacers improves the robustness. Soldering the ribbon cables permanently on the printed-circuit board prevents detachment of the cables during the experiments.

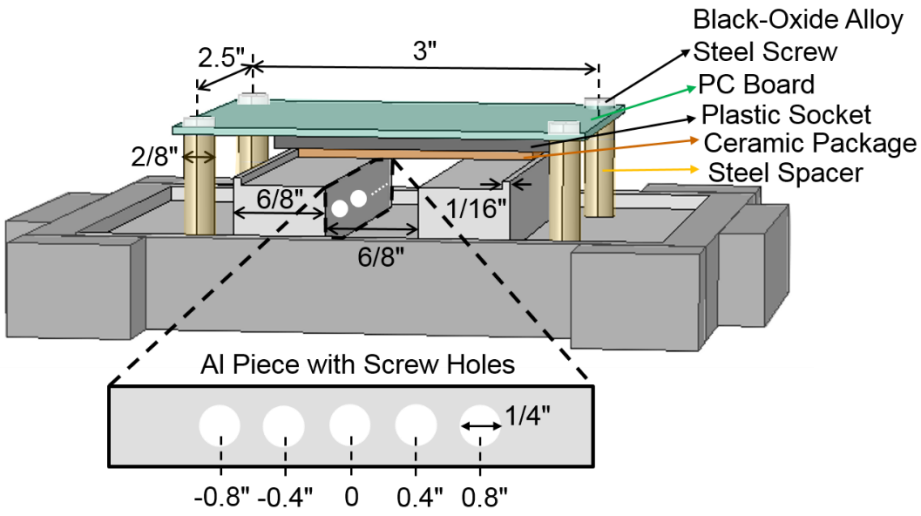


Figure 5.9. Printed-circuit board mounting on the sled of the split Hopkinson bar test setup.

The acceleration and deceleration profiles can be fine-tuned by using pulse shapers. In particular, soft materials can be used between the incident bar and sled or the sled and the shock absorber to increase the pulse duration at the expense of reduced pulse amplitude. However, the amplitude and duration of the acceleration and deceleration pulses are mostly determined by the striker bar weight, length and the gas gun pressure as well as the incident bar material. The pulse duration increases as the striker bar length is increased. On the other hand, a lighter striker bar can be accelerated to a higher velocity, which then leads to a higher amplitude acceleration pulse on the sled. The amplitude of the acceleration pulse also increases as the pressure of the gas gun is increased. However, the relationship between the pressure, the striker bar velocity, and the resultant acceleration pulse amplitude is not linear. For example, increasing the gas gun pressure from 20 psi to 80 psi increases the striker bar velocity from 36.5 fps (feet-per-second) to 80.8 fps and the acceleration pulse amplitude from 2.3 kG to 4.9 kG. The gas gun of the acquired system

cannot fire at pressures above 120 psi unless a pressurized nitrogen tank is used as gas supply, which was not available, and the firing is made through a manual firing valve (instead of firing with a remote control). Therefore, it is not possible to increase the pressure arbitrarily to obtain the desired acceleration and deceleration amplitude.

The longest available striker bar (i.e., a 12" long steel striker bar) is used in the shock tests in order to maximize the pulse duration. The pressure is kept at 20 psi, which leads to an acceleration pulse amplitude between 2.3 to 2.5 kG (with ~ 1 ms duration) and a deceleration pulse amplitude between 4.5 to 5.1 kG (with ~ 0.4 ms duration) when a polymer incident bar is used. The amplitude of the deceleration pulse depends on the velocity reached by the sled through the acceleration pulse duration, thereby the acceleration pulse amplitude and duration need to be improved simultaneously to get up to 50 kG deceleration amplitude with sub-ms (i.e., > 100 μs) pulse duration. Using a steel incident bar leads to an acceleration pulse with significantly higher amplitude (i.e., > 100 kG), albeit with much shorter duration (i.e., < 20 μs). Decreasing the acceleration pulse duration attenuates the transferred pulse to the DUT as described in the following sub-sections.

Both the DUT and the reference accelerometer exhibit ringing after a shock event. A modulation frequency value at or above 500 kHz is adequate to capture the ringing at the transducer resonance frequency of 118 kHz upon impact. A second-order Butterworth low-pass filter with 5 kHz cutoff frequency filters the transducer output signal when the pulse duration is above 0.4 ms (i.e., in the tests with the polymer incident bar). A larger 200 kHz filter bandwidth filters the signal when the pulse duration is below 20 μs (i.e., in the tests with the steel incident bar). The shock tests are run by using the ZI-HF2LI lock-in amplifier, which allows tuning the modulation frequency and the low-pass filter bandwidth over a wide range.

The scale factor measurements obtained by using the shaker table are taken as reference when calculating the amplitude of the impact based on the measured electrical signal during the shock tests. The scale factor is predicted to increase as the proof-mass displacement increases; however, in the measured acceleration range (i.e., < 5 kG) the nonlinearity of the accelerometer response is estimated as < 0.6% and the predicted change in scale factor is negligible.

5.3.2 Impact Profile with Polymer Incident Bar

The polymer incident bar accelerates the sled up to 2.4 kG amplitude in 1.1 ms (Figure 5.10 (a)), which subsequently is decelerated with 4.5 kG amplitude in 0.4 ms (Figure 5.10 (b)) upon collision with the shock absorber located at the end of the Hopkinson bar setup. The DUT successfully captures both the acceleration and deceleration events throughout the multiple trials in the experiment without experiencing failure. Figure 5.10 shows that the acceleration pulse exerted on the sled is transmitted to the DUT without significant distortion in the pulse shape, whereas the deceleration pulse is slightly attenuated during its transmission to the DUT due to the shorter pulse length. The fidelity of the transferred pulse shape decreases at shorter pulse durations, which is more significantly observed in the tests with the steel incident bar.

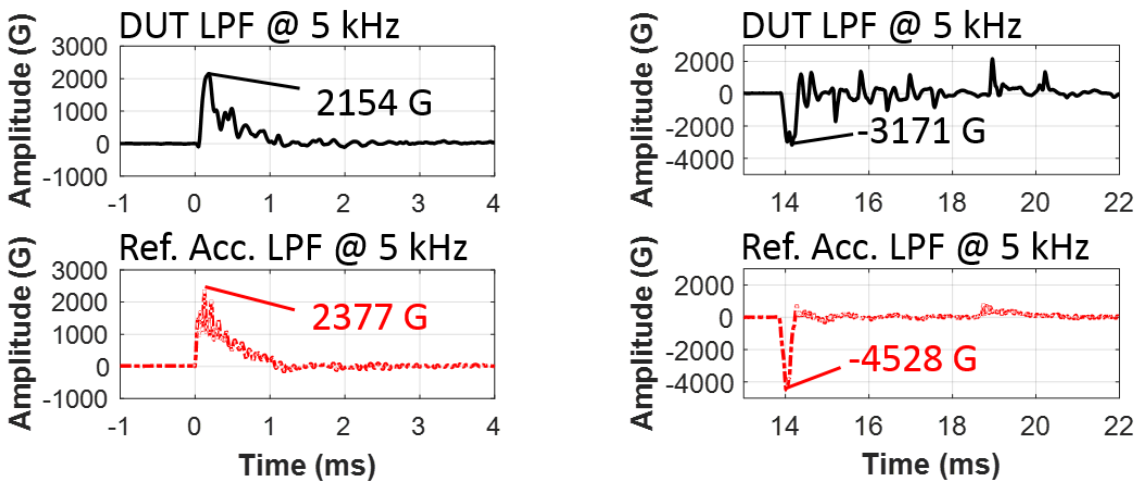


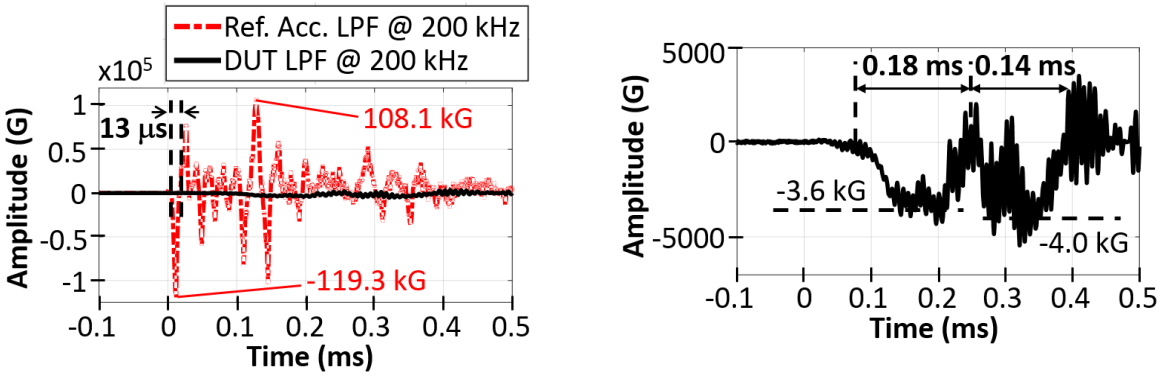
Figure 5.10. (a) Acceleration and (b) deceleration profile with polymer incident bar.

The difference in the measured pulse amplitudes and vibration profiles upon shock event results from having the reference accelerometer screw-mounted on the sled independent of the DUT board as discussed further in section 5.3.4. The reference accelerometer shows two types of oscillations upon impact. The inherent high frequency oscillations (~ 800 kHz) of the piezoresistive reference accelerometer attenuate upon filtering with a 5 kHz cut-off frequency. The low-frequency oscillations that persist after filtering result from the vibrations of the aluminum sled upon impact. Similarly, the oscillations of the DUT at resonance frequency are suppressed by the filter. However, the filtered response indicates that the DUT experiences higher amount of vibrations for a longer time compared to the reference accelerometer.

5.3.3 Impact Profile with Steel Incident Bar

Operation with the steel incident bar increases the shock amplitude beyond the target maximum acceleration input (50 kG). The reference accelerometer mounted on the sled indicates that the impact generated on the sled has more than 100 kG amplitude and 13 μs duration followed by lower amplitude oscillations (Figure 5.11 (a)). The DUT signal indicates that the acceleration

pulse transferred to device package is delayed in time, increased in duration and attenuated in amplitude to 4 kG (Figure 5.11 (b)). The finite stiffness of the printed-circuit board mounting and the DUT package mounting in its socket is believed to cause the difference between the impact profiles experienced by the two accelerometers. The signal is filtered at 200 kHz in this experiment in order to capture the high frequency components introduced by the short duration shock pulse. The ringing frequency of the DUT is approximately 126 kHz, which matches the designed resonance frequency (118 kHz) to within 7%.



(a) (b)

Figure 5.11. (a) Reference accelerometer output from sled impact of more than 100 kG amplitude and 13 µs duration followed by lower amplitude oscillations. (b) Corresponding DUT accelerometer output with an expanded y-axis scale.

5.3.4 Effect of Accelerometer Mount

The shock test with the steel incident bar is repeated after mounting the reference accelerometer on one of the holes on the laterally adjustable aluminum pieces (i.e., closer to the DUT). The measurements taken from the DUT and the reference accelerometer are filtered at 5 kHz and compared. Figure 5.12 shows that the DUT and the reference accelerometer measurements match better when mounted closely, thereby confirming the change in pulse shape as the force is transmitted throughout the sled assembly. The attenuation and dispersion of the

shock pulse become less significant as the pulse length increases; however, the current test setup cannot attain the 50 kG pulse amplitude and > 100 µs pulse duration simultaneously. This limitation prevents a comprehensive validation of the accelerometer operation at the designed input range. Reducing the mass of the sled and the striker bar should help reaching higher acceleration levels with the polymer incident bar at feasible pressure levels for the gas gun. This should allow the transfer of higher acceleration levels to the DUT, hence validation of the accelerometer operation at the designed input range.

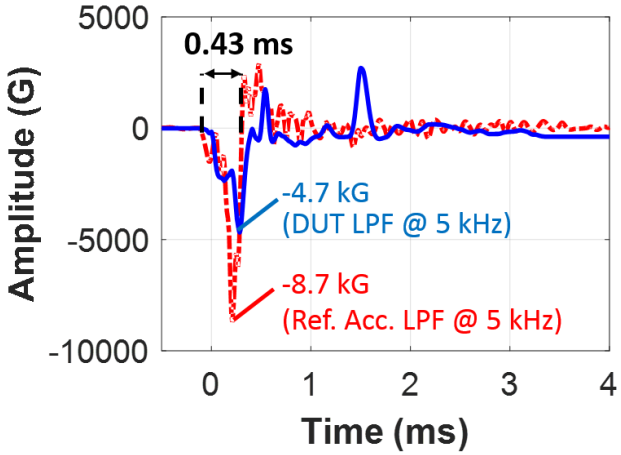


Figure 5.12. The reference accelerometer and DUT measurements match better when mounted closely.

5.4 Accelerometer and Circuit Noise Floor

Noise measurements are made at 100 kHz and 2 MHz modulation frequencies to observe the improvement in the noise floor when the noise is chopped at higher frequencies. The ZI-HF2LI lock-in amplifier is utilized for these noise tests. Both the equivalent acceleration noise floor of the readout circuit and the noise floor of the accelerometer (Figure 5.13) decrease as the modulation frequency is increased. The measured readout circuit noise is lower than simulated

when the circuit noise is chopped at 100 kHz; however, the reduction in circuit noise at 2 MHz modulation frequency is less than predicted by simulation.

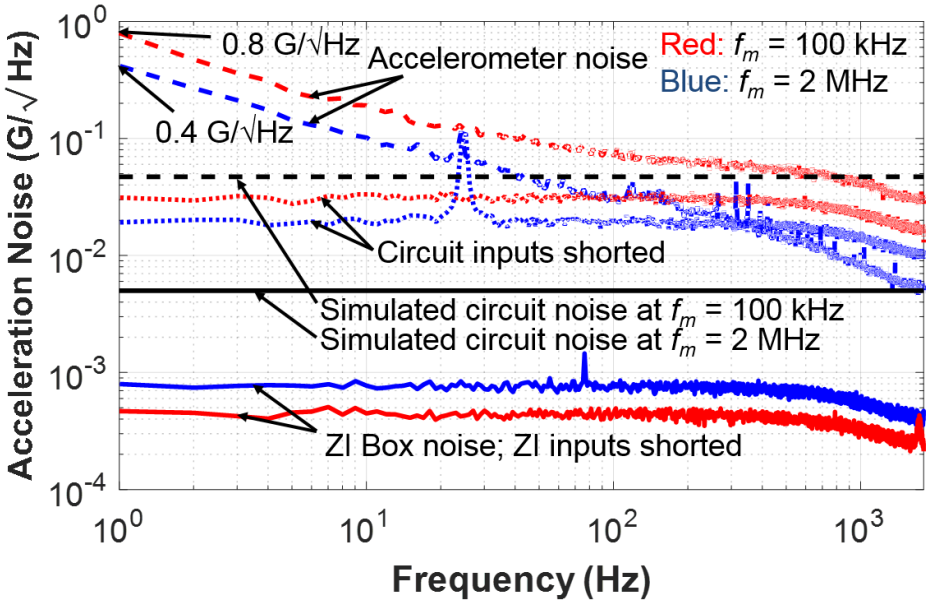


Figure 5.13. Comparison of equivalent acceleration noise density of accelerometer, readout circuit, ZI-HF2LI inputs and modulation waveform.

The contribution of the modulation voltage noise to the accelerometer noise floor is investigated. The flicker noise of the modulation waveform (generated at the output of ZI-HF2LI lock-in amplifier) is measured by shorting the modulation signals directly to ZI-HF2LI inputs (i.e., ZI-HF2LI outputs are shorted to its inputs through 30 cm long BNC cables), which get demodulated and filtered at 1 kHz (i.e., goes through the same signal processing steps as the accelerometer readout) by the internal electronics of HF2LI. Figure 5.14 shows the power spectral density of the modulation voltage waveform.

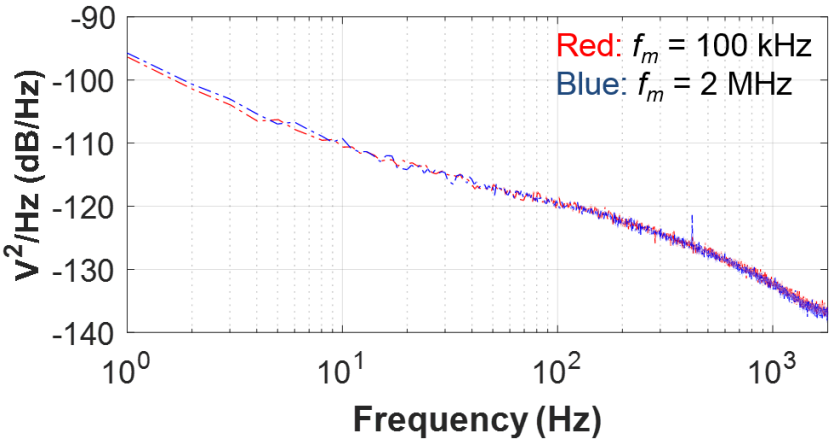


Figure 5.14. Power spectral density of the modulation waveform.

The modulation voltage noise is divided across the capacitive bridge when it is referred to the transducer output, thereby the lateral curl of the accelerometer cells (i.e., the offset acceleration) determines the contribution of modulation voltage noise to the acceleration noise floor as discussed in section 2.5.3. The equivalent acceleration noise floor is calculated by dividing the offset acceleration with the signal to noise ratio of the modulation voltage waveform. Assuming a linear relationship between acceleration and rotor displacement, the equivalent acceleration noise of the measured modulation voltage noise is calculated as:

$$\sqrt{\overline{a_{n,m}^2}/\Delta f} \cong \frac{x_{off}}{0.94\times10^{-6}} 50\times10^3 \frac{\sqrt{\overline{v_{n,m}^2}/\Delta f}}{V_{m0}} \tag{5.1}$$

where $\sqrt{\overline{v_{n,m}^2}/\Delta f}$ is the measured modulation voltage noise, V_{m0} is the modulation voltage amplitude (i.e., 0.9 V), x_{off} is the lateral offset, $\sqrt{\overline{a_{n,m}^2}/\Delta f}$ is the equivalent acceleration noise and 0.94 μm is the displacement at 50 kG acceleration as simulated in section 2.1.1. Figure 5.15 shows the equivalent acceleration noise floor of the modulation voltage waveform for different amounts of lateral curl. The difference between the measured accelerometer and circuit noise floor in Figure

5.13 can be explained by the modulation voltage noise when the lateral curl of the rotors is around 500 nm and the resultant offset is not cancelled. However, the lateral curl observed on scanning electron micrographs or measured as an offset signal at the accelerometer output is negligible. A more detailed investigation of the noise sources in the accelerometer system, including noise aliasing that explains the difference between the accelerometer and circuit noise measurements as well as the effect of environmental variations (i.e., temperature and stress variations) follows in the next section.

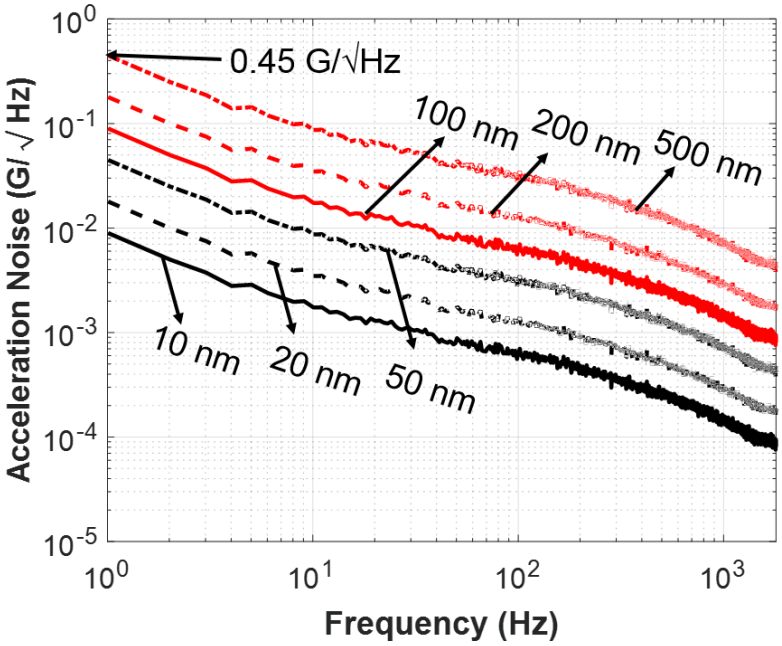


Figure 5.15. Equivalent acceleration noise floor of the modulation voltage waveform for different amounts of lateral curl.

5.5 Discussion of Noise Sources

The noise contribution of different signal processing steps performed by the ZI-HF2LI lock-in amplifier cannot be investigated, since the lock-in amplifier does not provide access to the signal output of individual steps (e.g., analog-to-digital conversion, demodulation, filtering). Therefore, on-board circuit components are utilized for the investigation of the noise sources. The modulation

frequency is set to 625 kHz by using the oven-controlled crystal oscillator employed on the board. The potential noise sources in the testbed are shown in Figure 5.16.

In order to ensure that the modulation voltage noise at each node of the capacitive bridge (i.e., $\sqrt{\overline{v_{n,m1}^2}/\Delta f}$ to $\sqrt{\overline{v_{n,m4}^2}/\Delta f}$) are completely correlated, all the modulation signals are generated by using a single voltage regulator and potentiometer (i.e., $V_{m1} = V_{m3} = -V_{m2} = -V_{m4}$). The noise contribution of the modulation signals (i.e., $V_{n,m1}$ to $V_{n,m4}$) are lumped together as $\sqrt{\overline{v_{n,m}^2}/\Delta f}$, the noise contribution of the biasing resistors (i.e., $\sqrt{\overline{v_{n,R1}^2}/\Delta f}$ and $\sqrt{\overline{v_{n,R2}^2}/\Delta f}$) and the on-chip circuits (i.e., $\sqrt{\overline{v_{n,A1}^2}/\Delta f}$) are lumped together as $\sqrt{\overline{v_{n,OC}^2}/\Delta f}$, the noise contribution of the on-board circuits (i.e., $\sqrt{\overline{v_{n,A2}^2}/\Delta f}$) including the low-pass filter are lumped together as $\sqrt{\overline{v_{n,OB}^2}/\Delta f}$ and the input noise of the data-acquisition card is represented as $\sqrt{\overline{v_{n,DAQ}^2}/\Delta f}$ in Figure 5.16. These lumped noise sources are investigated to identify the limiting noise source in the accelerometer system.

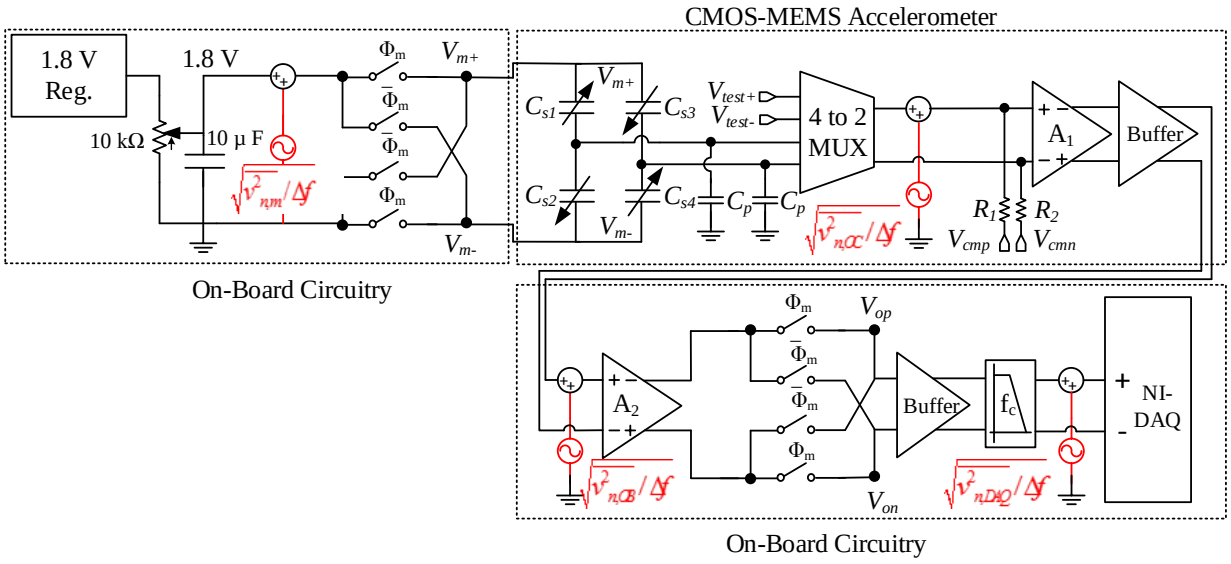
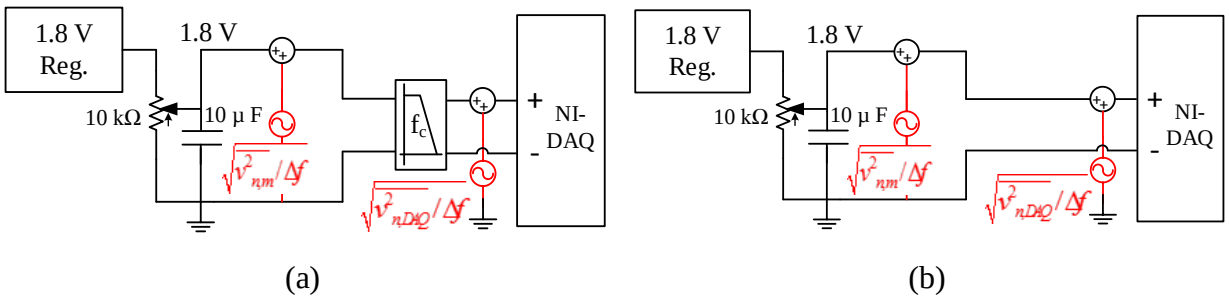


Figure 5.16. Schematic of the accelerometer readout circuit with modified modulation signal generation block and the lumped noise sources.

5.5.1 Testbed Noise Floor

In the first experiment, the noise floor of the dc voltage regulator (MAX 8887- low-dropout linear regulator with fixed 1.8 V output) in the testbed is measured with and without the low pass filter to see if the filter has a significant noise contribution. The regulator output directly connects to the on-board filter in one case (Figure 5.17 (a)) and without the intermediate filter in the other case (Figure 5.17 (b)), with resulting output voltages read by the NI-DAQ. Figure 5.18 compares the noise floor of the regulator to the noise floor of NI-DAQ (i.e., $\sqrt{\overline{v_{n,DAQ}^2}/\Delta f}$) obtained by shorting and grounding its inputs. The noise floor of the regulator does not change by the inclusion of the filter on the signal path, indicating that the filter does not introduce a significant amount of noise.



(a) (b)

Figure 5.17. Testbed connections for testing regulator noise floor (a) with and (b) without filter.

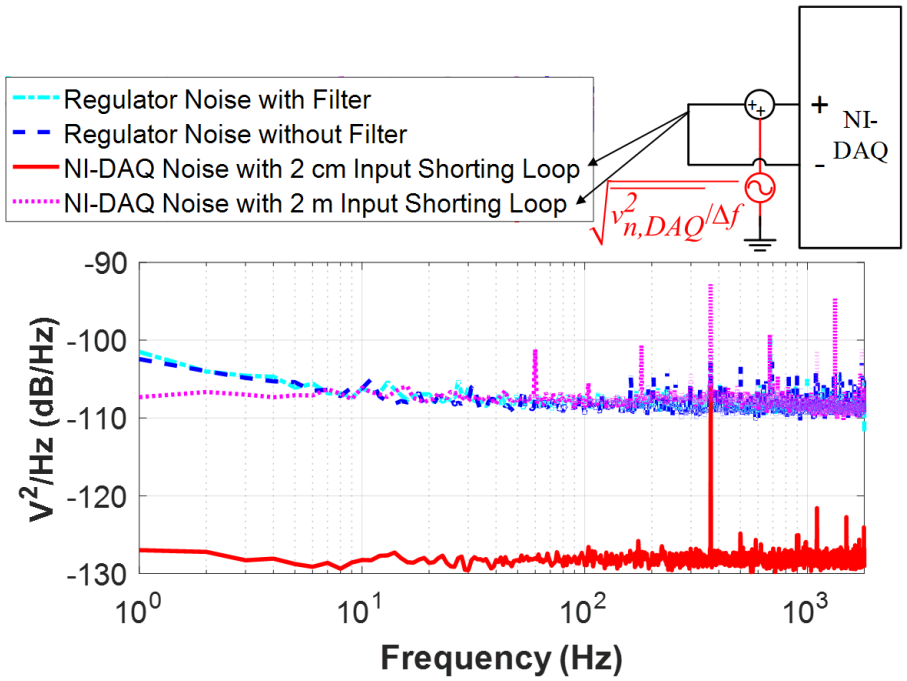


Figure 5.18. Noise floor of the regulator with and without low-pass filter compared to the noise floor of the NI-DAQ.

The noise floor of the NI-DAQ inputs are very low when a short jumper wire (i.e., ~ 2 cm) shorts the differential inputs. However, the noise floor increases significantly when a 2 m long wire loop shorts the two inputs (and the inputs connect to ground through another meter long cable). A compact testbed with minimum cable length and shielded cables is important for improvement of the noise floor.

The second experiment determines the noise contribution ($\sqrt{\overline{v_{n,m}^2}/\Delta f}$) of the on-board modulation and demodulation steps. The same 1.8 V regulator used in the previous experiment connects to the on-board modulator and the output of the modulation block directly connects to the demodulation switches (Figure 5.19). The transducer, on-chip circuits and the on-board amplifier stage A_2 are bypassed in this experiment to isolate the effect of modulation and demodulation steps on the noise floor. Figure 5.20 compares the noise floor of the regulator obtained in the previous experiment with the noise floor obtained after modulation and demodulation at 625 kHz. The noise with inclusion of the modulation and demodulation circuits increases by 2 dB; however, the dc voltage source (i.e., the on-board regulator) feeding the modulation switches sets the $\sqrt{\overline{v_{n,m}^2}/\Delta f}$ noise floor. The 2 dB difference is most likely due to the difference in cabling in the system rather than the additional circuits. The flicker noise of the modulation waveform (e.g., the noise density at 1 Hz) is 3.5 dB lower than that generated by ZI-HF2LI, implying that the modulation voltage noise is not expected to limit the acceleration noise floor.

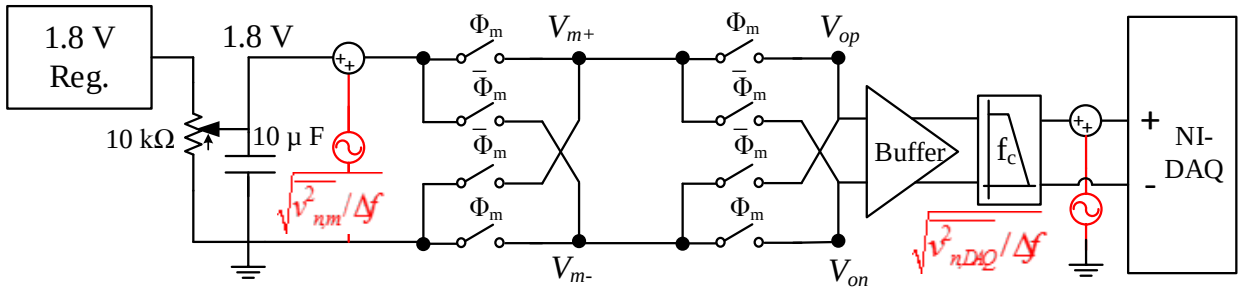


Figure 5.19. Testbed connections for testing noise injection from modulation and demodulation switches.

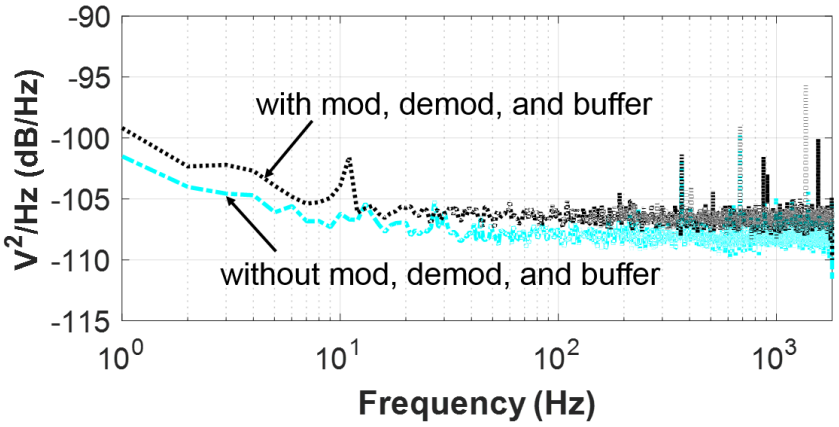


Figure 5.20. Noise floor of the regulator after modulation and demodulation at 625 kHz frequency.

The third experiment distinguishes between the noise contributions from the on-board circuits without the modulation switches (i.e., $\sqrt{\overline{v_{n,OB}^2}/\Delta f}$) and the on-chip circuits without the modulation switches (i.e., $\sqrt{\overline{v_{n,OC}^2}/\Delta f}$) . The noise floor of the on-board circuits is obtained by biasing the on-board circuit inputs at 1.65 V (Figure 5.21) to match the potential of the on-chip buffer output that is applied to the on-board circuit inputs when the amplifier stages are cascaded. The combined noise floor of the on-chip and on-board circuits is obtained similarly by shorting the on-chip circuit inputs when they are biased at 0.9 V (Figure 5.22) by the on-board regulators through the 10 MΩ on-chip resistors as in regular operation. The noise data is still collected by the NI-DAQ after filtering, therefore the observed noise floors include the noise contribution from the filter and the NI-DAQ. The demodulation switches are also active during both tests and clocked at 625 kHz, so that the on-chip (A_1) and on-board (A_2) amplifier circuit noise is chopped as in regular accelerometer operation. Figure 5.23 compares the equivalent acceleration noise floor of the on-board circuits with that of the whole amplifier chain. The on-chip amplifier dominates the readout circuit noise as expected and the measured white noise floor matches well with the estimated noise

floor by simulation. The flicker noise is believed to result from noise folding from higher frequencies as discussed in the next section. The readout circuit noise is filtered above 1 kHz by the second-order filter. The filtering effect is not as significant on the on-board circuit noise floor, indicating that the measured noise is limited by the NI-DAQ input noise floor (i.e., around 7 mG/√Hz equivalent acceleration noise floor with around 60 cm total length of unshielded cables used in this experiment). The equivalent noise floor of the NI-DAQ is 3 times lower when a ~ 2 cm jumper wire shorts the NI-DAQ differential inputs.

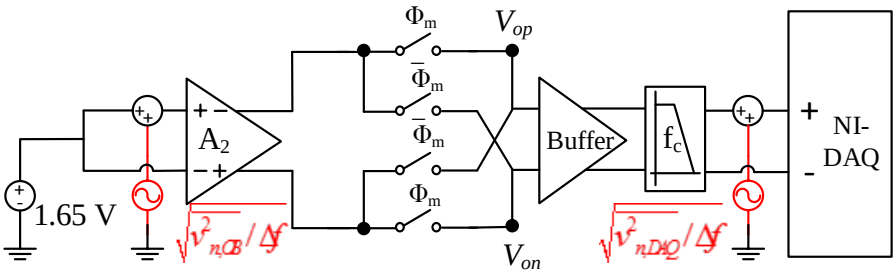


Figure 5.21. Testbed connections for testing the noise contributions from the on-board circuits without the modulation switches.

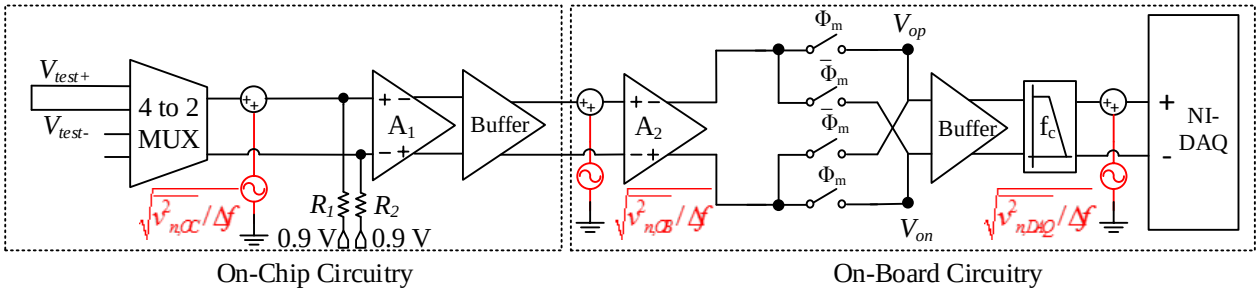


Figure 5.22. Testbed connections for testing the combined noise contributions from the on-chip and on-board circuits without the modulation switches.

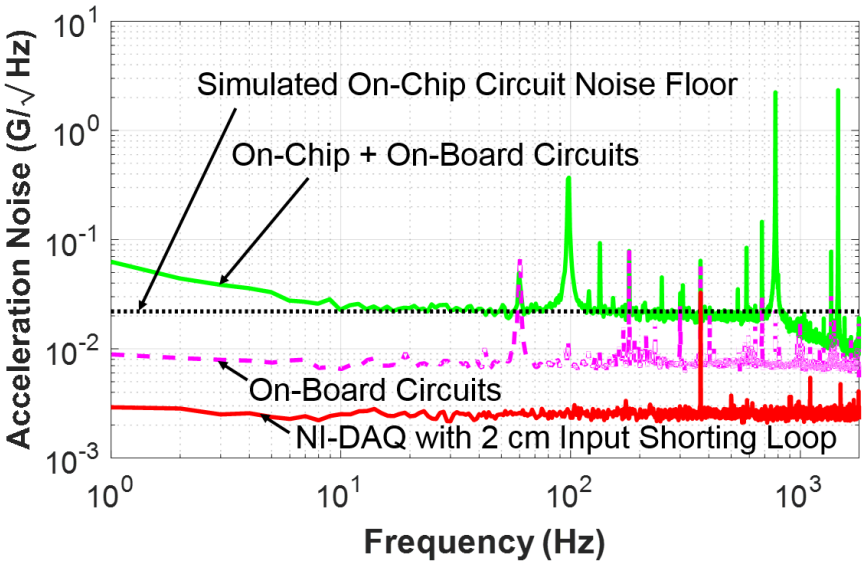


Figure 5.23. Equivalent acceleration noise floor of the on-board circuit compared to that of the whole amplifier chain.

5.5.2 Effect of Sampling Rate and Noise Folding

The DC offset voltage at the input of the readout circuit is amplified and up-converted to modulation frequency as it passes through amplifier stages and on-board demodulator. Varying the DC offset voltage is expected to lead to an observable change in the baseband signal if there is any significant aliasing from higher frequencies to baseband upon sampling and digitization of the signal through NI-DAQ. This hypothesis is tested by tuning the bias voltages at the two input nodes of the on-chip amplifier.

The high-impedance differential inputs to the preamp connect through 10 MΩ resistors to two independent bias voltages (Figure 5.24) that set the input offset and the common-mode input bias. An on-board voltage regulator and potentiometer-based dividers set the two input bias voltages. The intrinsic offset voltage of the preamp is observed at the output by switching the input multiplexer to the differential $V_{test\pm}$ inputs, shorting those inputs, turning off the modulation clock (i.e., by fixing the modulation and demodulation switches) and recording the signal with the NI-

DAQ. Shorting the $V_{test\pm}$ inputs averages any extrinsic residual offset from the on-board circuitry, while serving to set the common-mode bias. The common-mode bias is set to 0.9 V, i.e., midpoint between V_{dd} and V_{ss}. Small deviations from the midpoint do not alter the circuit performance, as validated by measurements (as will be discussed in conjunction with Figure 5.26). The measured intrinsic output-referred offset voltage is 330 mV, which translates to around 1.2 mV input offset voltage at the preamp.

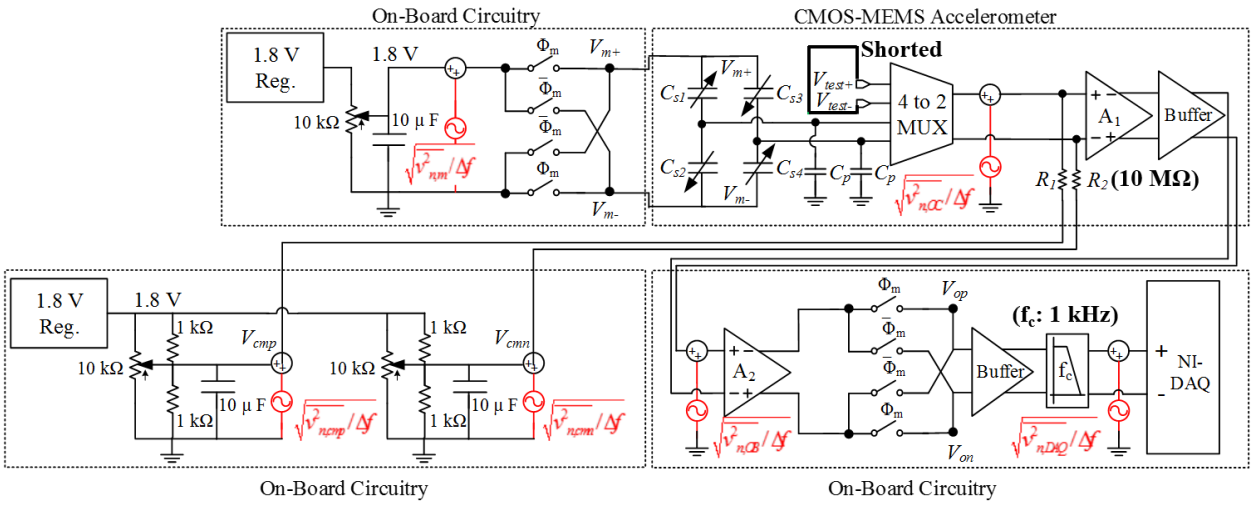


Figure 5.24. Testbed connections for tuning the DC offset voltage at the input of the readout circuit.

To set the preamp offset to other values (and ultimately to null it), the output DC offset voltage of the preamp is observed by switching the input multiplexer to the differential V_{test} inputs, opening those inputs, turning off the modulation clock and recording the signal with the NI-DAQ. Once the offset voltage is set, the modulation clock is turned on in order to activate the modulation and demodulation switches for regular operation. The resulting accelerometer noise spectral density measurements in Figure 5.25 indicate a significant dependence of noise on the DC offset voltage, such that both the white noise and the flicker noise drop by more than an order of magnitude as the output-referred offset voltage is reduced from 1.56 V to 4 mV on an aluminum-

etched chip. The accelerometer noise overlaps with the readout circuit noise when the output referred offset is minimized, showing that the noise is not inherent to the transducer.

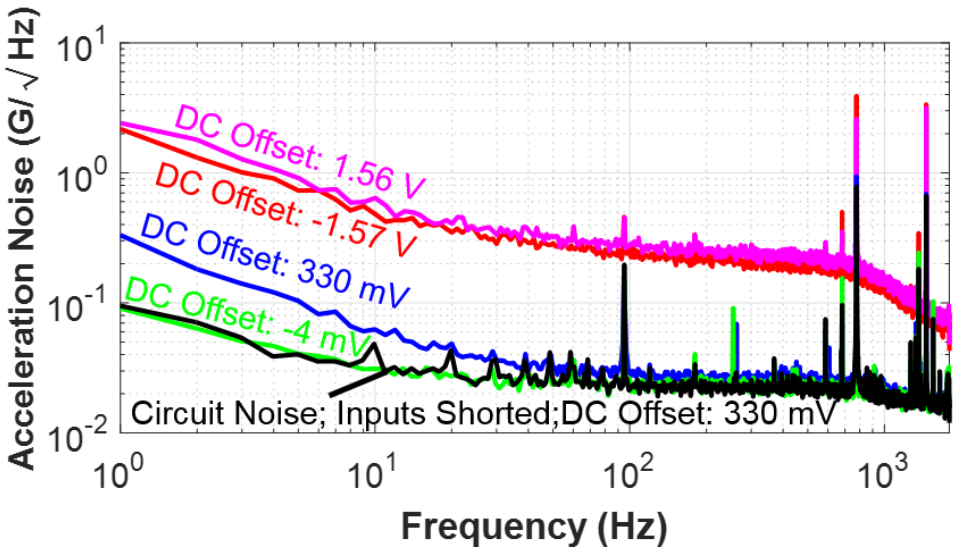


Figure 5.25. Effect of DC offset voltage on the accelerometer noise floor.

The effect of the common-mode input voltage on the accelerometer noise floor is illustrated in the measurement results in Figure 5.26, where the common-mode input bias is set to midpoint and to 50 mV above the midpoint. The noise of the accelerometer (transducer and circuit) and of only the readout circuit vary within the repeatability of the current testbed setup. The DC offset bias voltage is nulled to within 4 mV in these measurements.

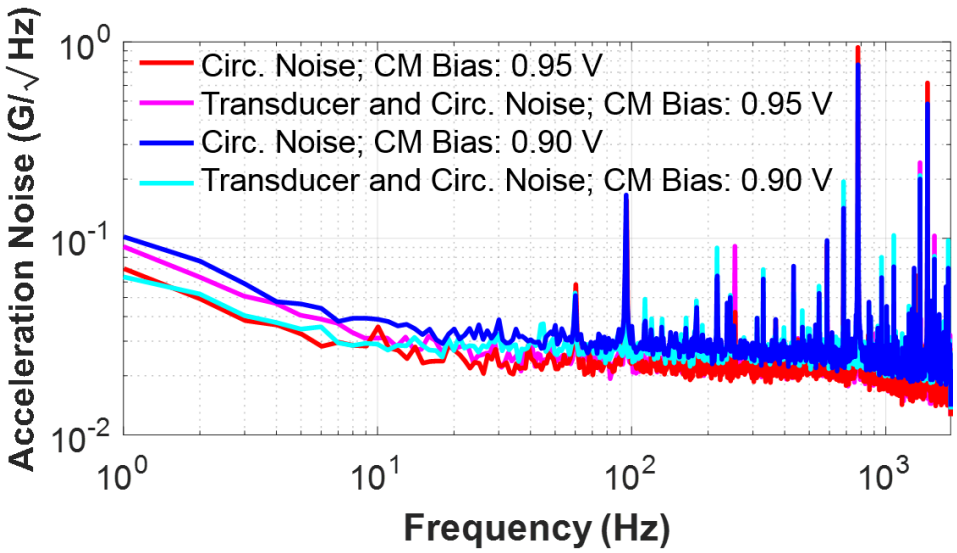


Figure 5.26. Effect of common-mode input voltage on the accelerometer noise floor.

The frequency tone disturbances seen at low frequencies are believed to result from noise folding from higher frequencies. The frequency and amplitude of the tones depends on the sampling rate, as observed in the measurements shown in Figure 5.27. Changing the sampling rate from 3.6 kHz (i.e., the sampling rate used in the prior experiments) to 50 kHz removes most tones between 70 Hz to 1800 Hz, generates new tones between 7 Hz and 50 Hz, decreases the white noise and increases the flicker noise. The white noise floor agrees well with the estimated equivalent acceleration noise floor of the readout circuit when the sampling rate is 50 kHz, whereas it increases by around 4 dB when the sampling rate is 3.6 kHz. The cutoff at 1 kHz in noise arises from the pole of the continuous-time second-order low-pass anti-aliasing filter (f_c = 1 kHz) in the testbed. The white noise above 2 kHz corresponds to the noise floor of the NI-DAQ. The measured acceleration noise power density at 1 Hz at the 3.6 kHz sampling rate translates to less than 50 nV/√Hz input referred noise at 1 Hz, which underscores the importance of having a stable input bias voltage and minimizing the noise coupling to the input nodes. Importantly, the dependence of

tone disturbances on the sampling rate indicate that these issues are not inherent to the transducer and should be reduced with further improvements to the testbed.

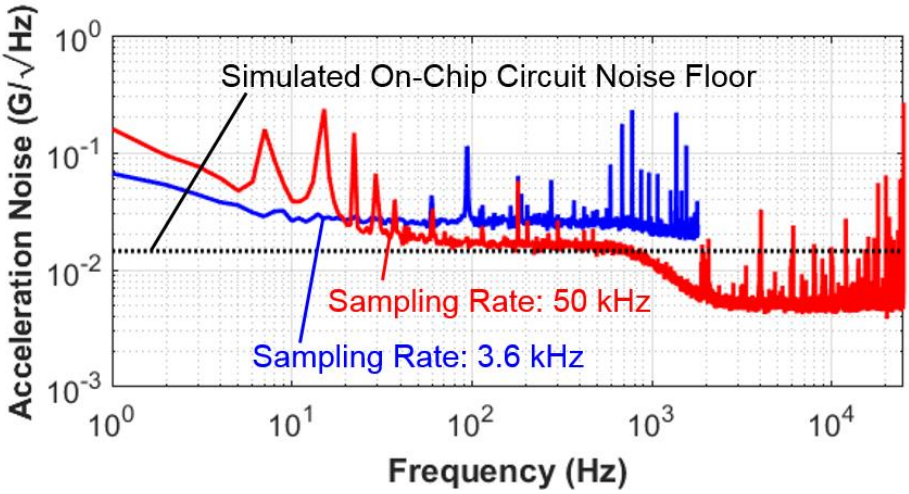


Figure 5.27. Effect of sampling rate on the accelerometer noise floor.

Figure 5.28 shows the Allan deviation of the aluminum-etched accelerometer after cancelling the DC offset (corresponding to blue curve in Figure 5.27). The estimated Allan deviation curve (i.e., the green curve) corresponds to the total acceleration noise floor at 625 kHz modulation frequency (i.e., 10.2 mG/√Hz) calculated in section 2.5.4, which is dominated by the combined noise floor of the on-chip amplifier and biasing resistors (i.e., $\sqrt{\overline{v_{n,OC}^2}/\Delta f}$). The Allan deviation is about two times higher than estimated at short integration times. The bias stability of the accelerometer is around 70 mG and limited by the flicker noise, which is believed to result from testbed noise and noise folding from higher frequencies. In future work, increasing the stability of the input bias voltages, improving the noise decoupling at the sensitive nodes (particularly, the input nodes) and using a higher order anti-aliasing filter before analog-to-digital conversion should help suppress the noise to reach the white noise limit set by the readout circuit and improve the bias stability up to the limit set by the environmental variations.

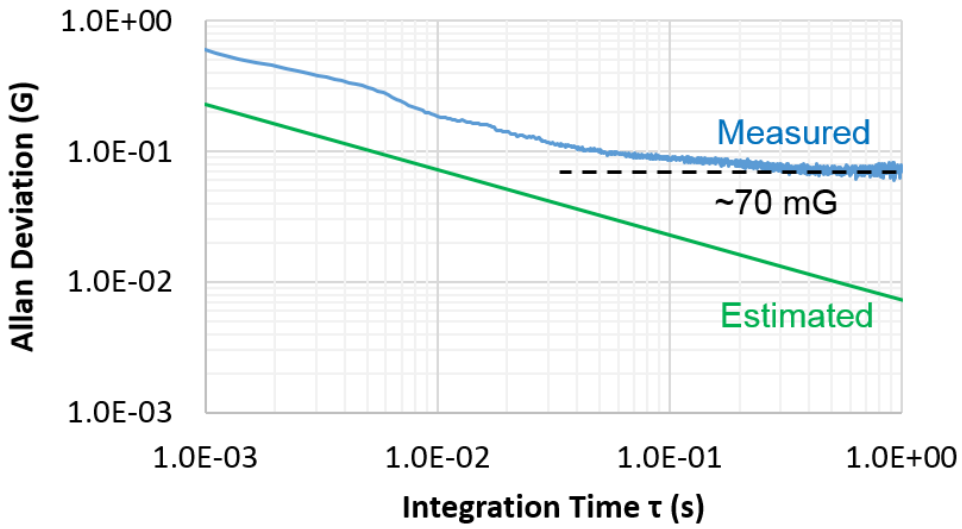


Figure 5.28. Allan deviation of the aluminum-etched accelerometer after cancelling the DC offset.

5.5.3 Effect of Environmental Variations

The contribution of environmental variations to the noise floor of the accelerometer is investigated to see if the compensation of these variations helps with the accelerometer resolution, given the existing noise floor. The temperature is varied with 20 ^{o}C steps over 20 ^{o}C to 80 ^{o}C range in a climatic chamber. Figure 5.29 (a) and (b) show the temperature and stress variations as measured by an on-chip PTAT temperature sensor and an n-type piezoresistive normal stress sensor. The temperature and stress sensors on the lower left corner of the accelerometer array (sensor area # 1 in Figure 4.19) are used for these measurements. The drift of the accelerometer output is saved simultaneously. Figure 5.30 shows the accelerometer signal after decimating by a factor of 5718 and subtracting the mean value. The decimation increases the sampling period of the accelerometer data to equal that of the environmental sensors (i.e., around 1.59 s sampling period).

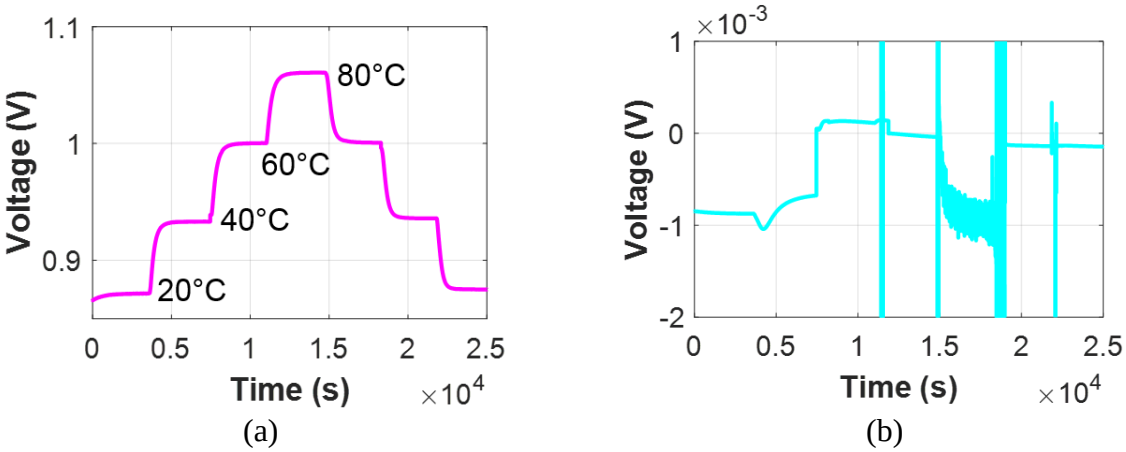


Figure 5.29. (a) On-chip temperature measured with the PTAT sensor over 20 °C to 80 °C temperature range, with 20 °C steps and (b) corresponding on-chip stress variations measured with an n-type piezoresistive bridge.

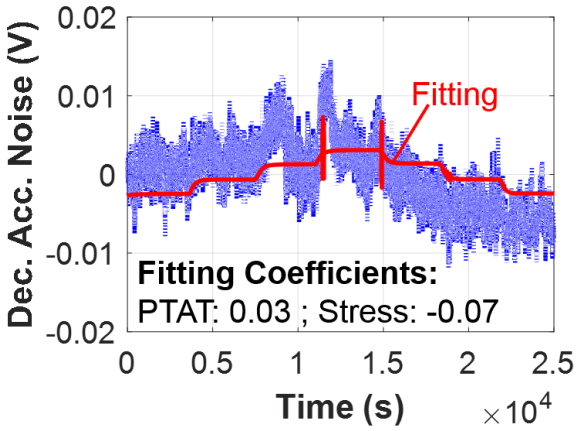


Figure 5.30. The linear fit on the decimated accelerometer bias drift.

The linear fitting in Figure 5.30 is performed by solving the following matrix equation by using the backslash operator in MATLAB:

$$A - \bar{A} = [c_T \quad c_\sigma] \begin{bmatrix} T - \bar{T} \\ \sigma - \bar{\sigma} \end{bmatrix} \tag{5.2}$$

where A is the measured acceleration signal (with mean value $\bar{A}$), T is the measured temperature (with mean value $\bar{T}$), σ is the measured stress (with mean value $\bar{\sigma}$), c_T is the fitting coefficient for temperature measurements and c_σ is the fitting coefficient for stress measurements. The best linear

fit on the accelerometer data is obtained by using 0.03 and –0.07 as the fitting coefficients for the PTAT temperature and piezoresistive stress sensor data, respectively. One of the peaks at the stress sensor output coincides with a sudden change in the accelerometer output, whereas the others do not seem to be reflected as significantly on the accelerometer output. Further experiments are needed to determine whether the peaks and the oscillations at the stress sensor output are triggered by sudden changes in the stress level or artifacts in the measurement. The drift in the accelerometer output due to varying temperature is clearly observed, although the accelerometer output does not return to the same level as the temperature is returned back to 20 ^{o}C. A hypothesized shifted on-chip stress level after thermal cycling helps explain the additional drift of the accelerometer output.

The accelerometer data is compensated for stress and temperature variations by subtracting the linear fit obtained in Figure 5.30 from the accelerometer readout:

$$A_{comp} = A - \left(0.03(T - \bar{T}) - 0.07(\sigma - \bar{\sigma})\right) \tag{5.3}$$

where A_{comp} is the compensated acceleration signal. The compensation provides an observable improvement in stability at longer integration times; however, does not help improving the drift at shorter integration times (Figure 5.31 (b)) as evident from the time domain data (Figure 5.31 (a)). An in-depth investigation is needed to improve the fitting results with more sophisticated algorithms.

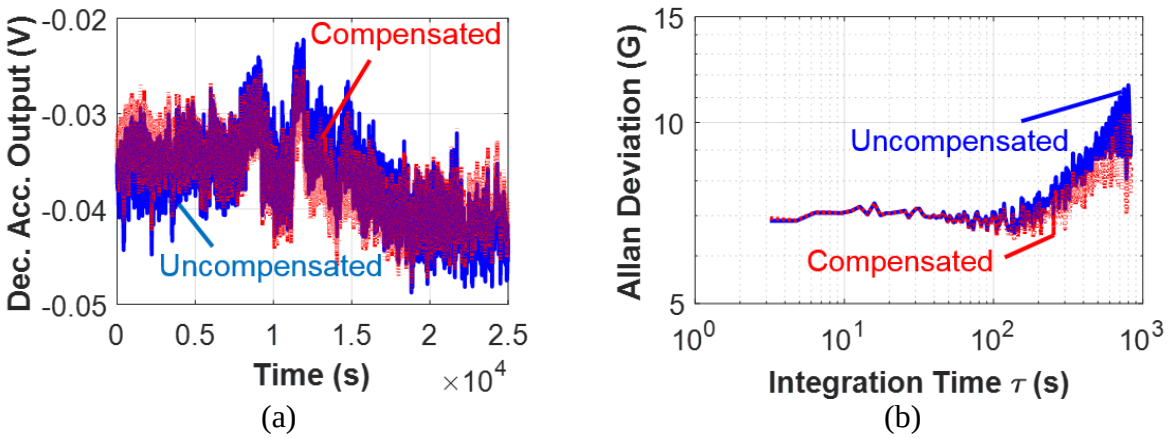


Figure 5.31. (a) Decimated accelerometer signal before and after compensation. (b) Allan deviation of the accelerometer signal before and after compensation.

The short-term bias drift of the accelerometer in the environmental chamber (Figure 5.31 (b)) is higher than that measured at ambient conditions (Figure 5.28). The short-term drift in temperature and stress on the chip during environmental chamber test is investigated by using 20 min of data (Figure 5.32) extracted from the PTAT temperature sensor and piezoresistive stress sensor measurements in Figure 5.29. The correlation between the short-term drift in temperature and stress measurements is clearly observed on the data.

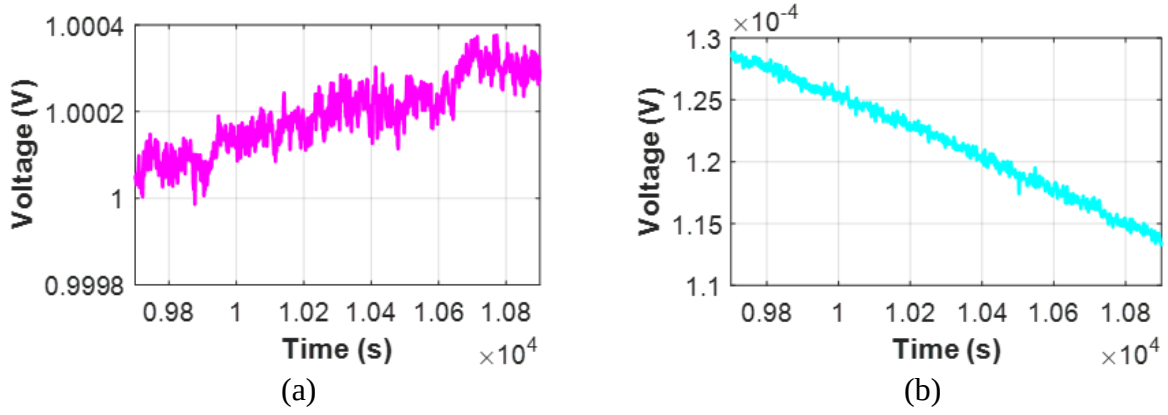


Figure 5.32. (a) PTAT temperature sensor and (b) n-type piezoresistive stress sensor measurements at 60 °C, obtained after the environmental chamber temperature is stabilized.

Figure 5.33 compares the short-term drift in the on-chip temperature and stress measurements obtained during the environmental chamber test to the bias drift of PTAT temperature and piezoresistive stress sensors under ambient conditions. The comparisons show that the temperature and stress drift on the chip during the environmental chamber test is less than that observed under ambient conditions. The comparisons also imply that the measured bias drift of the PTAT temperature and piezoresistive stress sensors under ambient conditions is a combination of the inherent drift of the sensor and the drift in ambient conditions. Further investigation is needed to understand the source of the additional noise in the system during environmental chamber tests. The effect of environmental variations on the accelerometer drift should become dominant once the flicker noise is suppressed, thereby allow modeling the correlations between the environmental sensor and accelerometer measurements with higher accuracy.

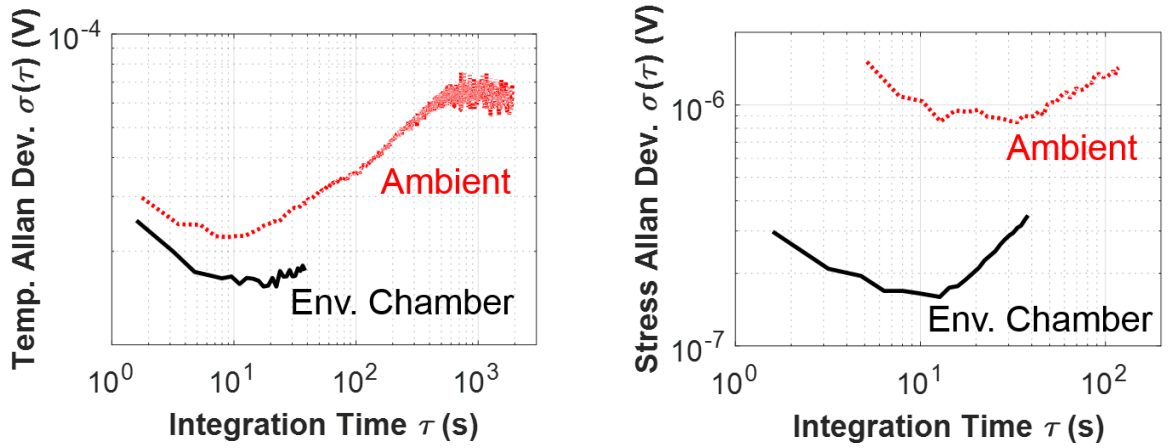


Figure 5.33. Short-term drift in the on-chip temperature and stress measurements obtained during the environmental chamber test compared to that obtained at ambient conditions.

5.6 Performance Summary of Accelerometer Array

Table 5.1. Comparison of designed and measured accelerometer specifications after Al-etch

	Designed (for 10 μm Undercut)	**Measured**
Transducer scale factor	1.16 μV/G	0.87 μV/G
White noise floor @ 625 kHz mod. freq.	10.8 mG/√Hz	23.7 mG/√Hz (SR: 3.6 kHz)
Resolution	1 mG (target)	70 mG (SR: 3.6 kHz)
Bandwidth	< 118 kHz	< 126 kHz
Input range	± 50 kG	± 4 kG (validated)
Dynamic range	154 dB	95.1 dB

The estimated performance parameters for the accelerometer design without top metal are compared to the measurement results in Table 5.1. The scale factor of the aluminum-etched accelerometer (0.87 μV/G) is slightly lower than the estimated scale factor (1.16 μV/G) when the lateral undercut length is 10 μm, implying that the parasitic capacitance is slightly higher in practice.

The white noise floor of the accelerometer overlaps with that of the readout circuit when the DC differential offset at the readout circuit input is nulled. The measured white noise floor when measured with a 50 kHz sampling rate matches the predicted noise floor by the circuit simulations. However, the white noise floor increases by 4 dB due to noise folding when measured with a 3.6 kHz sampling rate. The resolution (i.e., bias stability) is limited by the flicker noise of the accelerometer, which depends on the sampling rate and DC offset voltage. The target bias stability (1 mG) is not reached due to excessive flicker noise, which is believed to result from noise folding from higher frequencies.

The resonance frequency of the accelerometer cells sets a fundamental limit on the bandwidth of the accelerometer array. In practice, the measurement bandwidth is set by passing the accelerometer signal through a low-pass filter. The filter bandwidth is set to 1 kHz in scale factor and noise characterization experiments and is set to 5 kHz in shock tests with the polymer incident bar. When the filter bandwidth is set higher than the resonance frequency (e.g., set as 200 kHz in the shock tests with steel incident bar), the oscillations of the accelerometer cells at resonance frequency are captured in the response; however, the frequency components above the resonance frequency are still mechanically attenuated (i.e., the accelerometer cells act like a second-order mechanical filter). The ensemble resonance frequency of the accelerometer cells with top metal is extracted as 126 kHz by observing the ring-down profile in the experiments with a steel incident bar and 200 kHz filter bandwidth. The extracted resonance frequency matches the predicted resonance frequency (i.e., 118 kHz) by finite-element analysis to within 7%.

The target input range of 50 kG is not validated due to the difficulties with transferring 50 kG pulses to the DUT using our shock test setup. The input range is validated up to 4 kG on accelerometer cells with top metal by using the polymer incident bar. Assuming the same input range for the aluminum-etched devices, the dynamic range is calculated as 95.1 dB. Improvements in the test setup and successful transfer of accelerations above 50 kG to the DUT should readily lead to validation of dynamic range beyond 117 dB. In future work, the flicker noise should be suppressed and the environmental variations should be compensated to reach the targeted bias stability and dynamic range.

CHAPTER 6: CONCLUSIONS

A high dynamic range CMOS-MEMS capacitive accelerometer array is designed and characterized in this thesis. PTAT temperature sensors, piezoresistive stress sensors and resonator-oscillators are co-designed to provide resolution suitable for compensating the bias and scale factor stability of the accelerometer up to 1 ppm. Monolithic integration of the accelerometer array, the front-end amplifier and the auxiliary sensors forms a novel accelerometer system-on-chip that targets sub-mG bias stability, 50 kG input range and above 154 dB dynamic range as the first step towards inertial navigation under harsh environmental conditions. The capacitive sensing method and an open-loop accelerometer design are identified as the most suitable candidates for achieving low noise floor and high input range simultaneously to maximize the dynamic range. The small size and mass of individual accelerometer cells ensure high-G survivability. Running multiple accelerometer cells in parallel helps with increasing the sense capacitance as well as averaging the thermomechanical noise across the array, hence improving the signal to noise ratio.

Finite-element analysis captures the fringing electric fields when estimating the sense and parasitic capacitances, therefore improves the accuracy of the scale factor estimation. Finite-element analysis also captures the effect of accelerometer geometry when estimating the temperature and stress effects on the scale factor variation. Simulations reveal that temperature variations lead to a non-uniform expansion (or contraction) on the truss due to the constraint set by the spring beam connections. Bending on the truss leads to a non-uniform change in capacitive gaps with temperature. The average capacitive gap change with temperature is 1.4 times higher than a first-order estimation based on CTE of oxide and silicon. Simulations also show that the simulated stress dependent change in capacitive gaps is 3.8 times smaller than a first-order estimation based on the Young's modulus of silicon substrate when the substrate undercut is

30 µm. The substrate undercut isolates the rotor and stator anchors from the stress and strain on the substrate, hence reducing the effect of stress on the scale factor drift.

Removal of the top metal through the developed aluminum etch process reduces the sense capacitance and routing capacitance of the accelerometer cells simultaneously. The scale factor of the accelerometer increases only when the ratio of sense capacitance to parasitic capacitance increases, which is guaranteed when the circuit input capacitance is negligible. However, when the circuit input capacitance is comparable to the total sense and routing capacitance of the accelerometer, removal of the top metal does not improve the sensitivity significantly. For optimum performance after top metal removal, the circuit input capacitance should be set to maximize the signal to noise ratio given the estimated sense and routing capacitance without top metal. Matching the on-chip circuit input capacitance to the total sense and parasitic capacitance of a 336 cell accelerometer array after top metal removal and increasing the allowed modulation voltage amplitude from 1.8 V to 5 V peak-to-peak can increase the scale factor up to 7.25 µV/G. Assuming the same voltage noise floor for the 336 cell array, the corresponding acceleration noise floor and bias stability would be 6 times better than the existing design.

The shock tests are made by using a split Hopkinson bar test setup and a custom designed sled for housing a small printed-circuit board with the DUT. Shock pulses with ~ 300 µs duration and up to ~ 4 kG amplitude are repeatably generated and transferred to the DUT by using a polymer incident bar. Pulse duration is critical for the transfer of the impact to the DUT with minimum attenuation and dispersion. The high frequency content of the acceleration pulse is filtered through the accelerometer mount when the pulse duration is only around 10 µs. Longer pulses with > 100 µs duration are transferred with higher fidelity. Increasing the pulse length by using a polymer incident bar or a pulse shaper simultaneously decreases pulse amplitude, hence

making it challenging to reach 50 kG pulse amplitude with > 100 μs duration. In the measured acceleration range (i.e., up to ~ 4 kG), the die attach, wire bonds and printed-circuit board components are found to survive consistently. Attachment of ribbon cables to sockets on the DUT board leads to measurement artifacts and loss of contact during shock events. Soldering the cables directly on the board improves the measurement repeatability and prevents loos of contact. The large number of I/O connections of the accelerometer chip require a wide ribbon cable for board-to-board connections, which introduces additional mass loading to the system. The finite stiffness of the wide ribbon cable also increases the risk of cable failure after repeated exposure to impact. The number of required connections can be minimized by integrating more electronic components on the chip in order to reduce the printed-circuit board area and increase the testbed robustness.

Excessive flicker noise in the system limits the bias stability of the accelerometer to 70 mG. The white noise floor of the readout electronics agrees well with the design predictions. The accelerometer noise floor overlaps with the circuit noise floor when the DC offset voltage at the input of the on-chip amplifier is cancelled. The flicker noise and the low-frequency tones in the system are believed to result from noise folding from higher frequencies upon sampling the acceleration signal. Capacitive decoupling of high frequency noise in supply, bias and common-mode voltage sources is critical to reduce the noise in the system. A higher order anti-aliasing filter before analog-to-digital conversion should further suppress the high frequency noise and help mitigate noise aliasing. The bias and scale factor drift due to environmental variations can be investigated in further depth once the flicker noise is suppressed and the readout stability is limited by the transducer.

The temperature resolution of the PTAT temperature sensors and the resonance frequency stability of the resonator-oscillators are difficult to measure with high accuracy. The drift in

temperature sensor measurements at integration times above 100 s is on the order of 10 mK. Similarly, the drift in resonance frequency of the resonator-oscillator over 8 h corresponds to around 200 mK. Such small variations in ambient temperature are easily expected over the corresponding time frames. The intrinsic drift of these sensors can be estimated more accurately by running multiple sensors in parallel and compensating their output for the ambient temperature variations based on the correlation between their measurements.

The accuracy of the calculated stress sensor resolution depends on the accuracy of the measured stress sensitivity of the sensor. Finite-element analysis is used to predict the attenuation in stress as it gets transferred from the package to chip surface. However, attenuation depends on the adhesion layer thickness and the position of the sensor on the chip. The exact amount of attenuation may be more or less than predicted dependent on the adhesion layer uniformity, the chip dimensions and the distance of the etch areas on the chip to the particular stress sensor. Development of a die attachment method to obtain a uniform and repeatable adhesion layer thickness can improve the repeatability of the measurements. Running finite-element analysis on an exact chip model can increase the accuracy of the estimated stress attenuation, hence improving the accuracy of calibration. The raw measurement of stress resolution (i.e., not taking the stress attenuation into account) sets a lower bound on the stress resolution and corresponds to better than 2 ppm scale factor stability for the accelerometer.

The long wait-time needed for frequency stabilization prevents the practical use of resonator-oscillators for scale factor compensation. Reducing the polarization voltage can reduce the charging time; however, the high polarization voltage is needed to keep the sensor in oscillation unless the motional resistance of the resonator is reduced by operating it under vacuum. Vacuum packaging is not a preferred solution, since air damping is needed to minimize the ring-down time

of the accelerometer. Further research is needed to mitigate the dielectric charging problem in CMOS-MEMS resonators, such as investigating the efficiency of conductive thin-film coatings in reducing the effects of dielectric charging.

The correlation between the environmental sensor measurements and accelerometer readout is observed only when the temperature is varied over a wide range (e.g., from 20 °C to 80 °C) due to excessive flicker noise in the system. A low-noise testbed is needed to reach the noise floor set by the environmental variations. The stress and temperature can vary across the chip and can be different on the chip and on the package as indicated by the variations in the measured sensitivities of the stress sensors due to variations in stress attenuation. Therefore, the data collected from the distributed environmental sensors on the chip is expected to correlate with the accelerometer readout better compared to measurements taken from off-chip stress and temperature sensors. Bias drift compensation at room temperature remains to be investigated with an improved testbed design.

Table 6.1. Comparison of the designed accelerometer to other low-G and high-G accelerometers

	Honeywell Q-Flex® QA2000-030	**Wang, et. al. [92]**	**Bosch Sensortec, BMA 456**	**Meggit, 7270A-60K**	**CMOS-MEMS Acc. Array in this Thesis**
Type	Quartz, Macro-ElectroMech.	MEMS, Oscillating	MEMS, Open-Loop	MEMS, Piezoresistive	MEMS, Open-Loop
Scale factor	1.2 - 1.46 mA/G	280 Hz/G	0.49 mG/LSB	3 μV/G	0.87 μV/G
Noise floor	< 70 μG-rms (10-500 Hz)	1.2 μG/√Hz	120 μG/√Hz	-	23.7 mG/√Hz
Resolution	< 1 μG	0.4 μG	0.49 mG	-	70 mG
Bandwidth	> 300 Hz	< 190 Hz	< 684 Hz	100 kHz	20 kHz
Input range	± 60 G	± 20 G	± 16 G	± 60 kG	± 4 kG
Dynamic range	155.6 dB	154 dB	90.3 dB	-	95.1 dB
Linearity/VRE	< 20 μG/G^2-rms (50-500 Hz); < 60 μG/G^2-rms (500-2000 Hz)	-	0.5% of full range	-	< 1.2% in 10 kG range
Power	< 480 mW	4.37 mW	< 0.54 mW	-	20.4 mW*
Maximum shock	250 G	-	10000 G	180000 G	> 50000 G
Output	Analog	Analog/Dig.	Digital	Analog	Analog

* Simulated power consumption of the on-chip amplifier and buffer is reported.

The designed CMOS-MEMS capacitive accelerometer array is compared to other state of the art low-G and high-G accelerometer designs as well as a commercial grade accelerometer design from Bosch Sensortec in Table 6.1. The reported bandwidth in the comparison is assumed to be set by low-pass filtering the accelerometer signal. The resonance frequency of the accelerometer cells can be increased as described in the future work or the proposed frequency staggering method can be used to attenuate the ring-down oscillations faster in order to allow higher signal bandwidth. The input range is validated only up to around 4 kG due to test setup

constraints. Successful transfer of 50 kG shock pulses to the accelerometer should validate the designed input range, thereby increase the dynamic range of the existing chips to 117 dB. The accelerometer can potentially survive higher than 50 kG shock events; however, the maximum shock for the survival of the cells remains to be tested in a setup that can transfer the required pulse amplitudes to the accelerometer. The linearity of the accelerometer in ±10 kG input range is acceptable for high-G measurements; however, the estimated nonlinearity increases to 3.4% in ±20 kG input range, and to 19.0% of the full range when the design is used in ±50 kG acceleration range. The sensitivity can be increased up to 7.25 μV/G in a future design, which decreases the acceleration noise floor to 2.8 mG/√Hz and the bias stability to 8.4 mG as long as the voltage noise floor is preserved. Suppressing the flicker noise in the system and compensating the readout for environmental effects should help improve the bias stability another order of magnitude, leading to sub-mG acceleration resolution and above 154 dB dynamic range.

6.1 Future Work

6.1.1 Frequency Staggered Array Tests

Staggering the resonance frequencies of the accelerometer cells in the array and introducing incoherence between the ring-down oscillations of accelerometer cells reduce the ring-down time of the accelerometer array. Increasing the resonance frequencies of groups of accelerometer cells for decreasing the ring-down time simultaneously decreases the sensitivity of the accelerometer array. The ratio of mean-square (m/k) to energy under the ring-down curve is defined as a figure of merit for the comparison of different array designs and an example array is designed with 312 accelerometer cells. This array is planned as 12 columns of accelerometer cells with 26 cells per column. A similar array design with 336 accelerometer cells is laid out as 14 columns with 24 cells per column. The designed array remains to be fabricated and tested with the

split Hopkinson bar setup. A comparison between the output signals of the frequency staggered array and the existing array should confirm that the transient oscillations generated by the shock event attenuate much faster at the frequency staggered array output.

6.1.2 Additional Design Improvements

The capacitive gap size of the accelerometer does not have a direct effect on the transducer scale factor as long as the resonance frequency is adjusted such that the ratio of the proof mass displacement to the capacitive gap remains unchanged for a given acceleration input. Reducing the gap size makes the oxide etch more difficult, typically leading to a longer etch time and higher amount of polymer deposition on the capacitance sidewalls. However, these difficulties are not likely to occur when the oxide etch is performed by using STS-Aspect AOE instead of Plasma-Therm 790 RIE. In this case, the capacitive gaps can be reduced while simultaneously increasing the resonance frequency of the accelerometer cells such that 50 kG target maximum acceleration closes half of the capacitive gap. Increasing the sense capacitance reduces the effect of parasitic capacitance due to the signal routing and also allows using a larger input transistor for the readout circuit to drive down the circuit noise floor. Furthermore, the increased resonance frequency simplifies the filter design for the attenuation of ring-down oscillations in the bandwidth of interest while increasing the fundamental limit on the bandwidth of the system.

The front-end circuits implemented on the chip include an open-loop amplifier and an open-loop buffer. The open-loop circuit gain is prone to drift with environmental variations, hence contributing to the scale factor drift of the accelerometer. The drift in the circuit gain can be compensated based on the stress and temperature measurements obtained from the on-chip sensors; however, higher sensor resolution may be needed to improve the scale factor stability to a target level. Substituting the open-loop circuits with closed-loop circuits should minimize the

environmental effects on the circuit gain. An alternative circuit design would implement charge-rebalance for acceleration signal readout, which can also help reducing the effect of parasitic capacitances.

6.1.3 Additional Testbed Improvements

The split Hopkinson bar test setup should be amended for generating the target maximum 50 kG acceleration amplitude without sacrificing the pulse duration. To that end, the striker bar weight can be reduced without reducing the length of the bar (e.g., using a lighter bar material) to accelerate the striker bar to higher velocities by using feasible pressure levels for the gas gun. Using a lighter sled should also help with accelerating the sled to a higher velocity with the impact of the incident bar. The polymer incident bar is better than the steel incident bar as it increases the duration of the impact, hence leading to a longer acceleration pulse. Finally, the reference accelerometer can be mounted directly on the printed-circuit board and adjacent to the DUT in order to ensure that the same acceleration profile is experienced by the two accelerometers.

The bias drift is shown to vary with stress and temperature and is compensated to some extent by using the measurements obtained from one PTAT temperature sensor and one n-type piezoresistive stress sensor on the chip. However, the distributed stress and temperature sensors across the chip are not fully utilized in the performed experiments. The 60-bit scan chains implemented on the chip can be completely loaded in less than 20 ms, hence allowing data acquisition from different sensor areas with less than 20 ms intervals. The data can be acquired with a data acquisition card and subsequently processed to obtain the stress and temperature map of the chip. If the measurements from multiple sensors are used for the least-squares fitting on the accelerometer drift, the fitting coefficients should inform the relative effect of the stress and temperature variations in a certain area of the chip on the accelerometer scale factor and bias drift.

Finally, more elaborate fitting algorithms can be tried to see if the correlation between the auxiliary sensor measurements and accelerometer drift can be modeled with higher accuracy to improve the compensated accelerometer system performance.

6.1.4 Mitigation of Dielectric Charging

The frequency drift of the resonator-oscillator upon start-up is believed to result from charging in the oxide and sidewall polymer. The charging effects should be investigated in more detail through controlled experiments. Coating the capacitance sidewalls with a conductive material through atomic layer deposition should provide a conductive interface between the residual sidewall polymer or oxide and air, hence reducing the fluctuations in potential due to charge traps. The frequency drift of the resonator-oscillators can be taken as reference when tuning the processing steps to reduce the dielectric charging. The resonance frequency of the resonator-oscillator should stabilize faster once the dielectric charging is minimized, thereby allow the practical use of the oscillators for scale factor compensation.

The stress and temperature variations affect the scale factor of the accelerometer by changing the capacitive gaps and resonance frequency. However, the measurement of the accelerometer drift as a function of temperature and stress cannot inform whether the drift is dominated by the changes in the capacitive gaps or the resonance frequency. If the dielectric charging problem of the resonator-oscillators is resolved, the frequency measurements taken from the oscillators can be used to inform the stress and temperature effects on the resonance frequency and distinguish between the capacitive gap and resonance frequency dependent variations in the scale factor and bias, thereby verify the finite-element analysis based estimations in this study.

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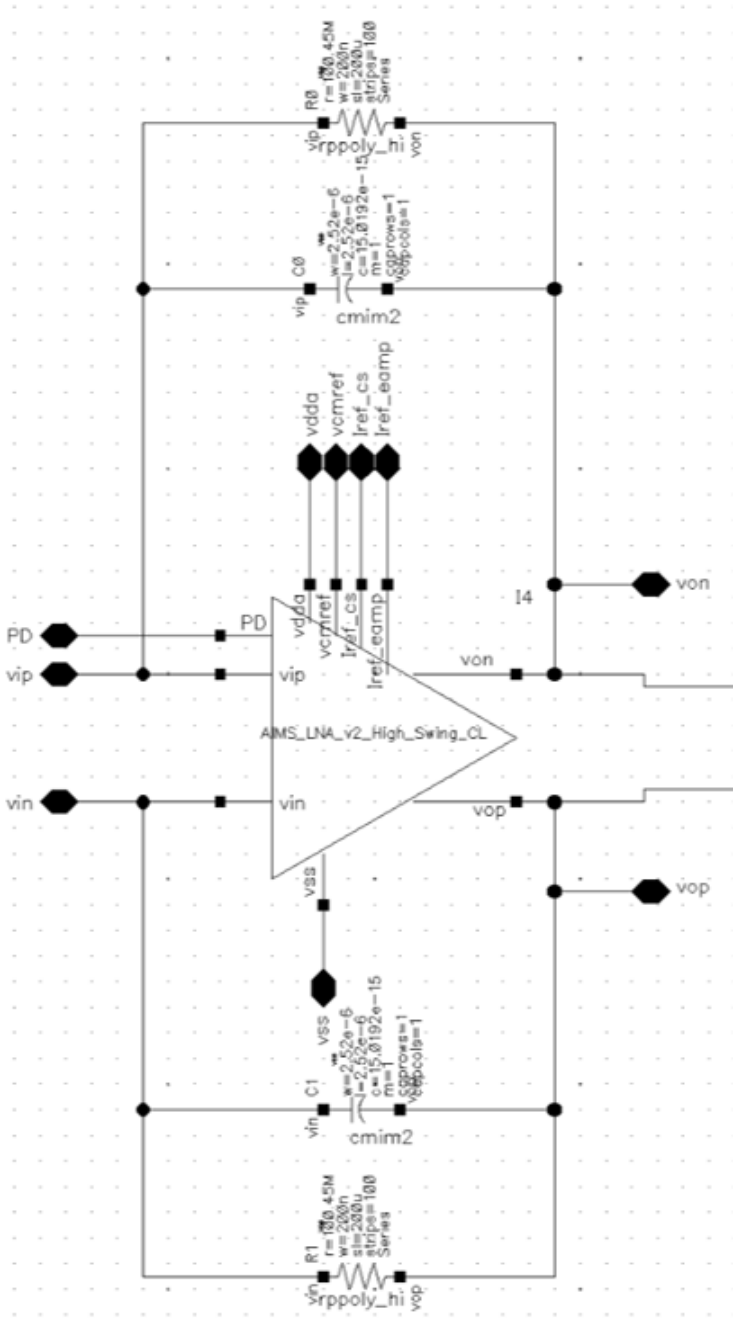
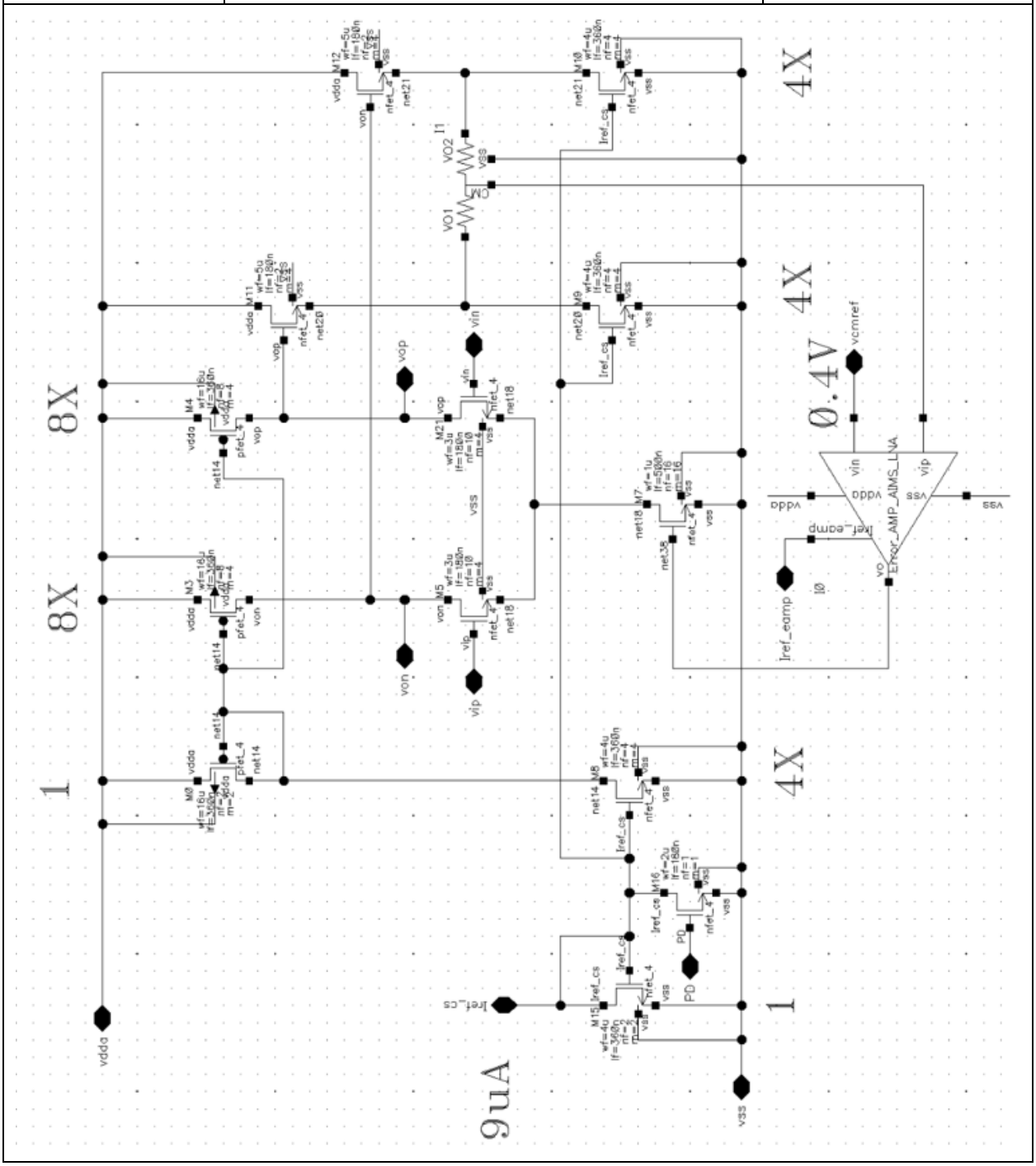
APPENDIX A: SCHEMATICS OF ON-CHIP AMPLIFIERS

A.1 Frontend Amplifier for Acceleration Signal Readout

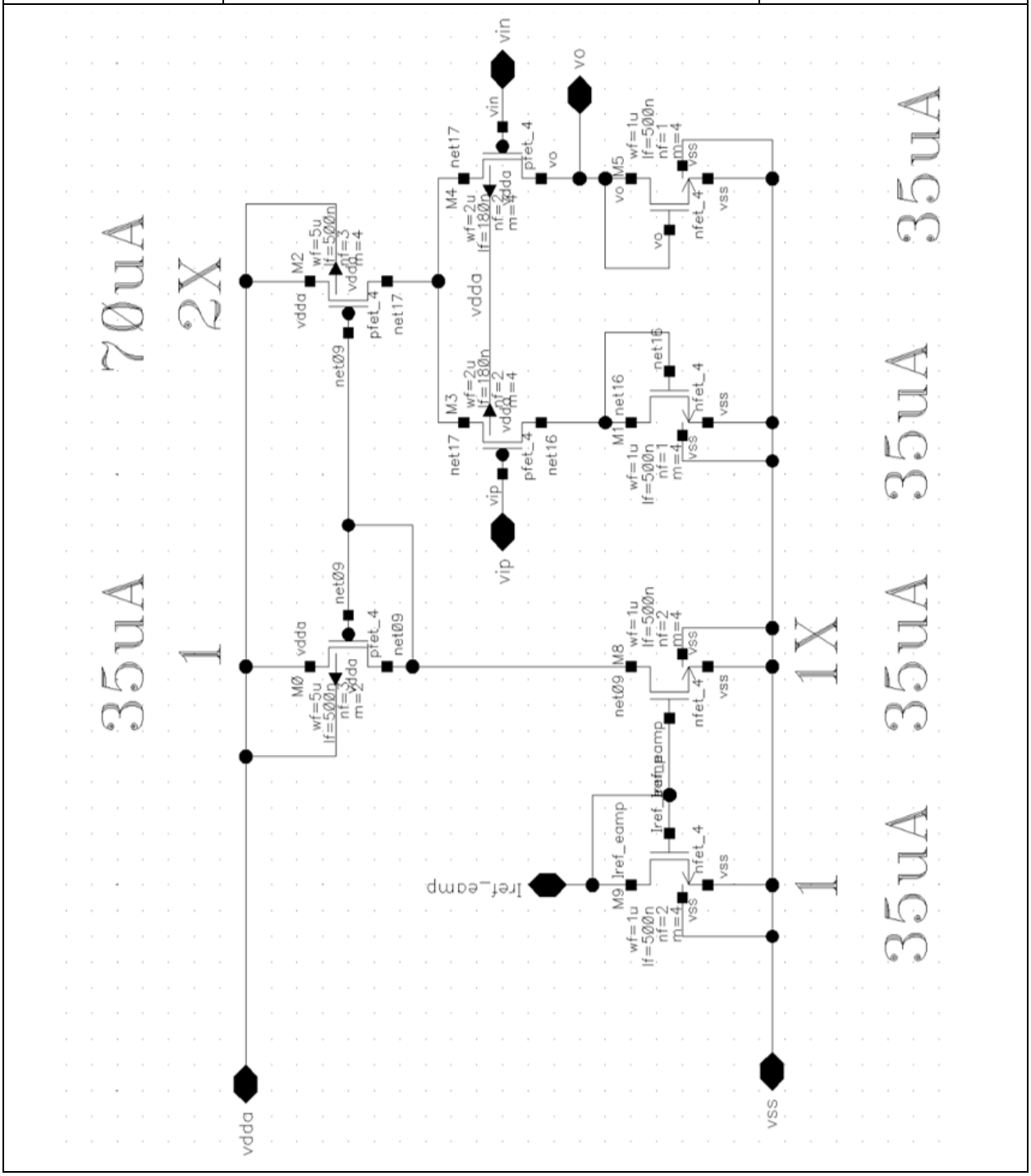
Library Name	Cell Name	Notes
jzc18_009	Simplified_Readout	Amplifier; Top Level



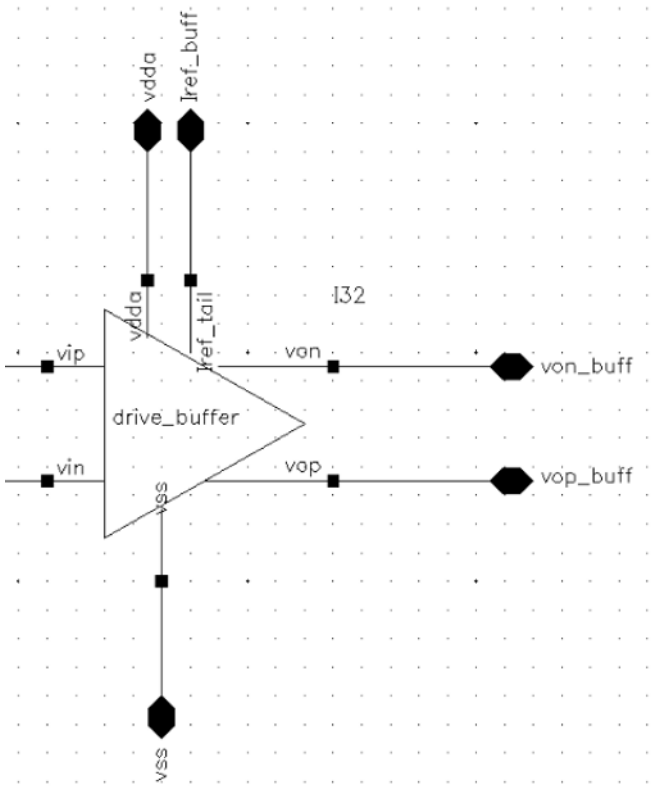
Library Name	Cell Name	Notes
jzc18_009	AIMS_LNA_v2_High_Swing_CL	Amplifier; Transistor Level



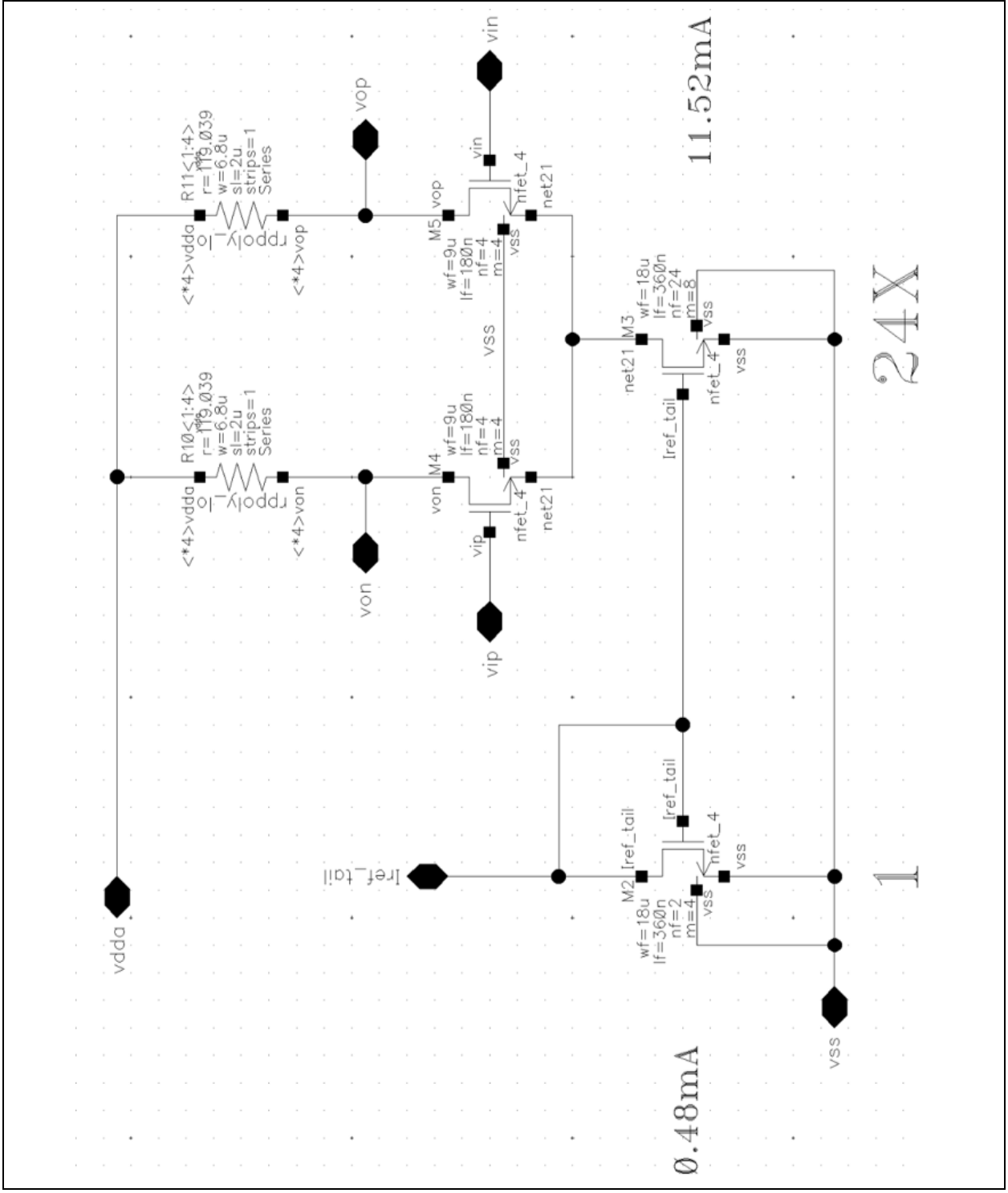
Library Name	Cell Name	Notes
jzc18_009	Error_Amp_AIMS_LNA_v1_jzc18_009_Li_02	Error Amplifier in Common-Mode Feedback; Transistor Level



Library Name	Cell Name	Notes
jzc18_009	Simplified_Readout	Buffer; Top Level

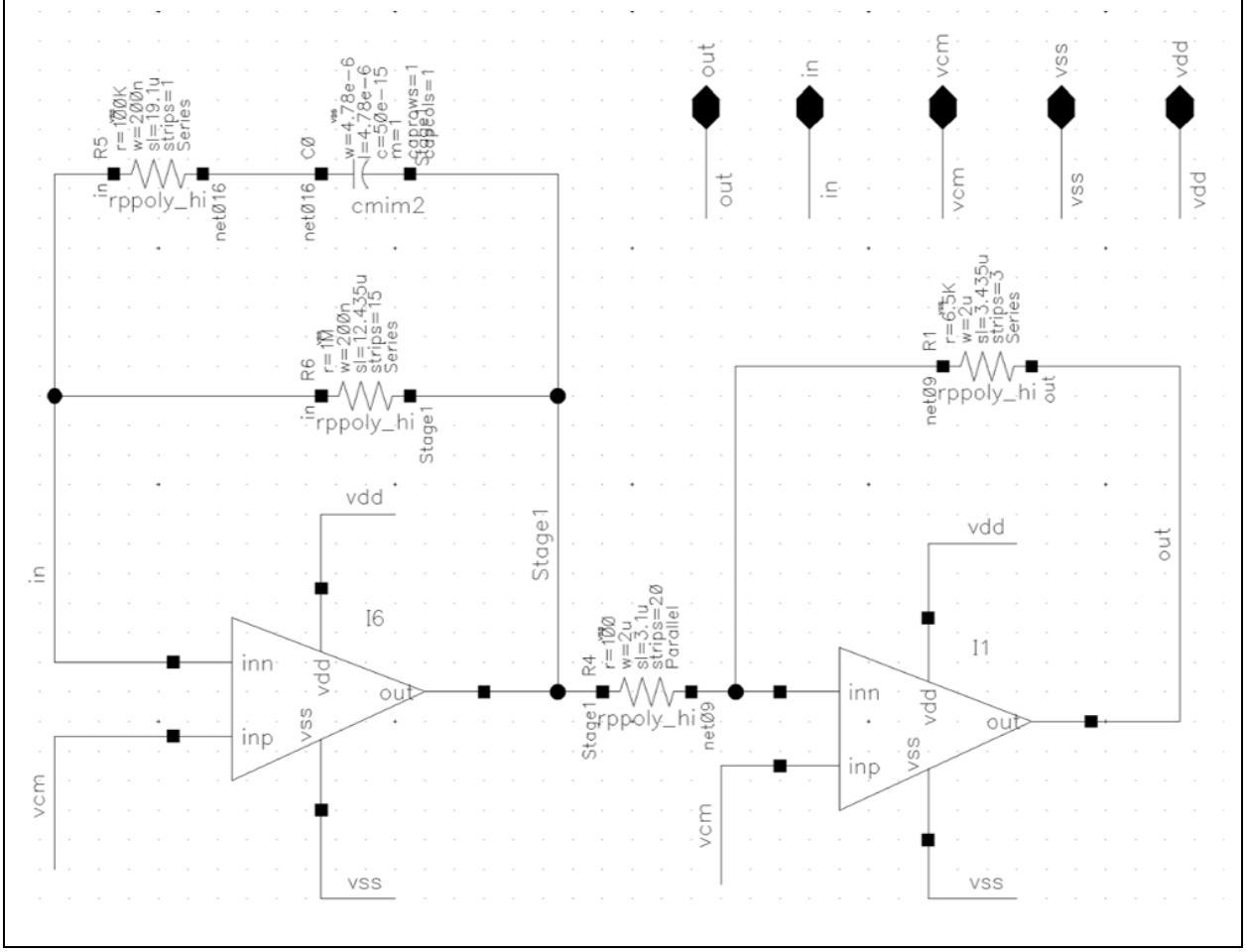


Library Name	Cell Name	Notes
jzc18_009	drive_buffer	Buffer; Transistor Level

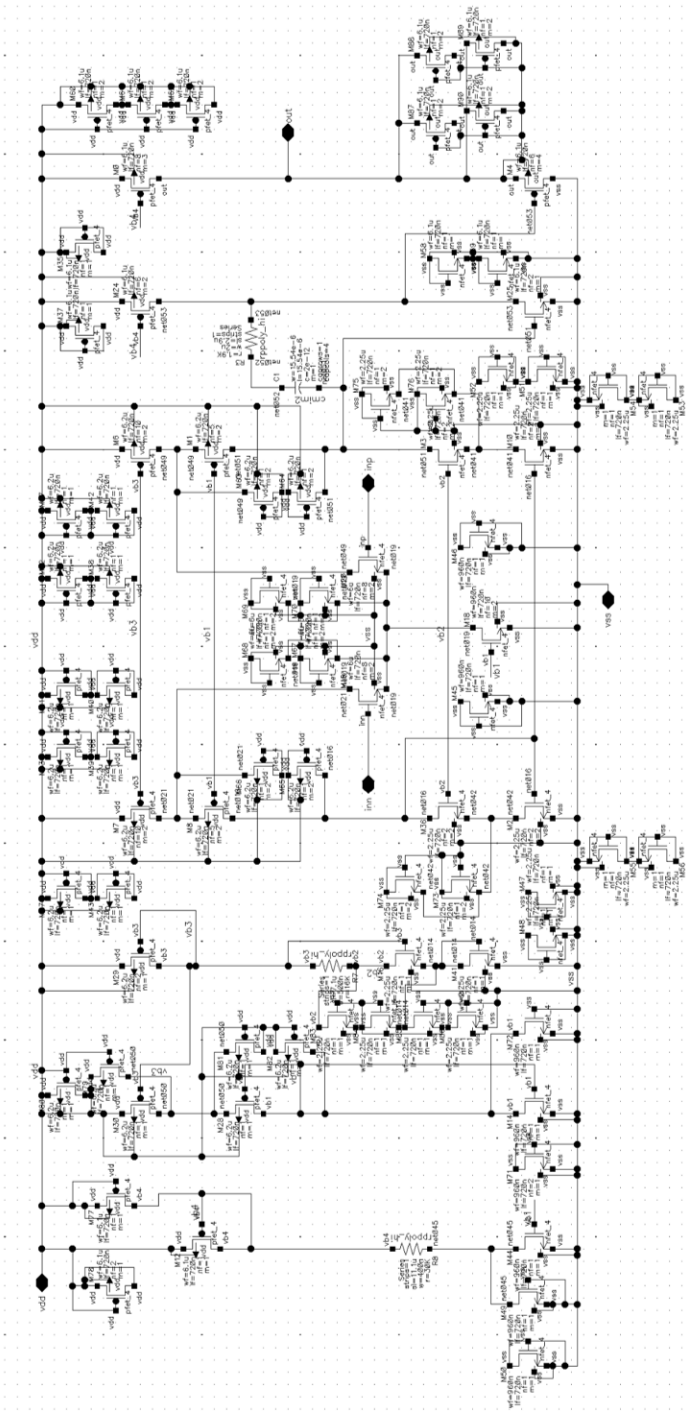


A.2 Sustaining Amplifier for Resonator-Oscillator

Library Name	Cell Name	Notes
jzc18_009	Sust_Amp_mod_circ	Sustaining Amplifier; Top Level



Library Name	Cell Name	Notes
jzc18_009	opamp_gen_metin	Op-Amp in Sustaining Amlifier; Transistor Level; w/ Dummy Transistors



APPENDIX B: TESTBED DESCRIPTION AND SCHEMATICS

B.1 Description of Printed-Circuit Boards

The testbed for the characterization of the 56 cell accelerometer array and the environmental sensors in the accelerometer system includes three custom printed-circuit boards: the “connector” board, the “Arduino interface” board, and the “accelerometer” board.

The connector board (Figure B.1) interfaces the accelerometer and the environmental sensors with power supplies and measurement instruments through various connectors. Voltage regulators and resistive dividers generate the bias voltages and currents for flexible debugging and operation of the chip. Unity-gain buffers act as an additional stage of isolation for the accelerometer and resonator-oscillator signals from the large capacitive loading introduced by the coaxial cables, which shield signals from external disturbances. The board includes analog CMOS switches for generating modulation signals and demodulating the acceleration signal. The board also allows bypassing the switches, so that the modulation signals can be generated by using Zurich Instruments® HF2LI lock-in amplifier and the demodulation can be performed in the HF2LI after digitization. The schematic design of the connector board is provided in Appendix B.2 along with the component models used in the design.

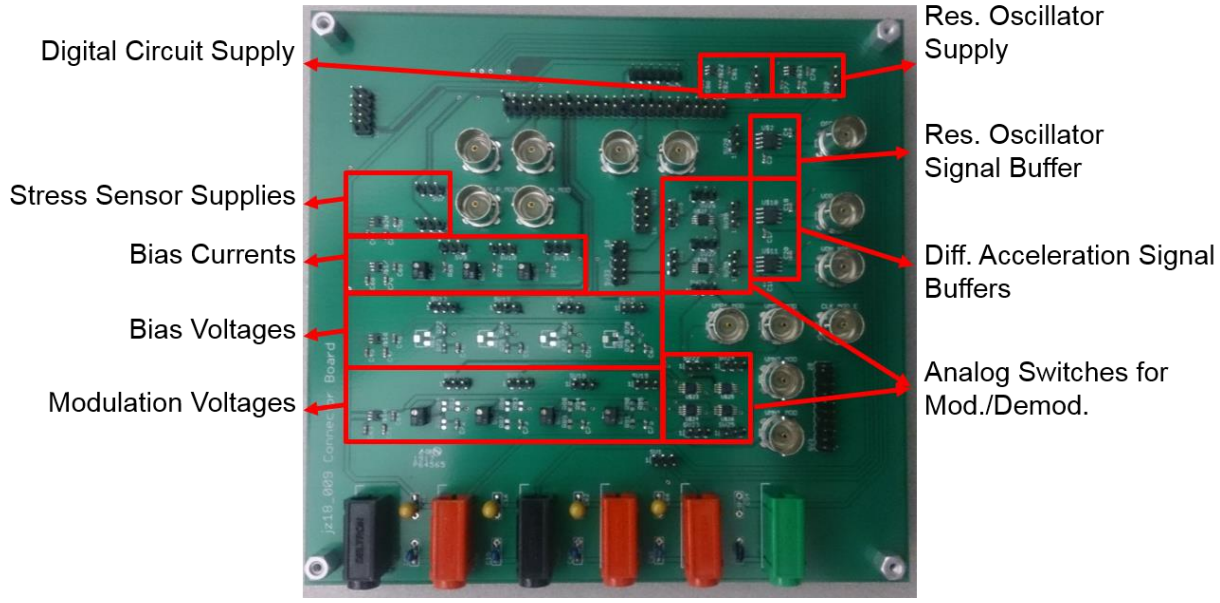


Figure B.1. Connector board for interfacing the accelerometer and environmental sensors with power supplies and measurement instruments.

The Arduino interface board (Figure B.2) carries the Arduino® UNO microcontroller board and provides voltage translation between the Arduino I/O voltage level (5 V) and CMOS voltage limit (1.8 V). The Arduino board supplies a flexible way to program the on-chip scan chains and to apply various select bits for on-chip multiplexers. The schematic design of the Arduino interface board is provided in Appendix B.3.

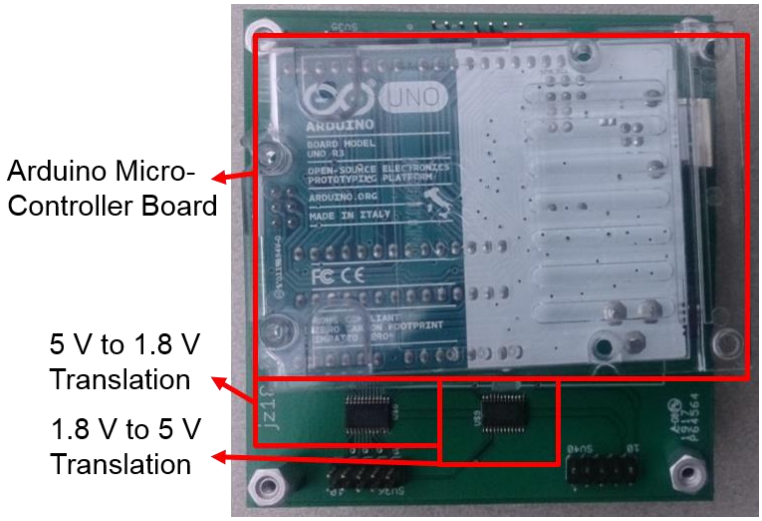


Figure B.2. Arduino interface board for voltage translation between the Arduino® UNO microcontroller and the on-chip digital circuits.

The accelerometer board, connector board, and Arduino interface board are separated in order to keep the accelerometer board (Figure B.3) dimensions small so that it can be mounted on the sled of the Hopkinson Bar setup for acceleration shock tests. The ribbon cables are rigidly soldered on this board in order to prevent loss of contact during shock tests. Two op-amps on the accelerometer board form the first stage of an instrumentation amplifier with 21 V/V DC gain. The differential output signals from this first stage are buffered on the connector board and used for differential readout. However, the readout circuit on the accelerometer board can also be converted to a differential instrumentation amplifier with higher gain and DC offset control by soldering an additional four op-amps in case the on-chip gain stage fails to satisfy design expectations. The schematic design of the accelerometer board is provided in Appendix B.4 along with the component models used in the design.

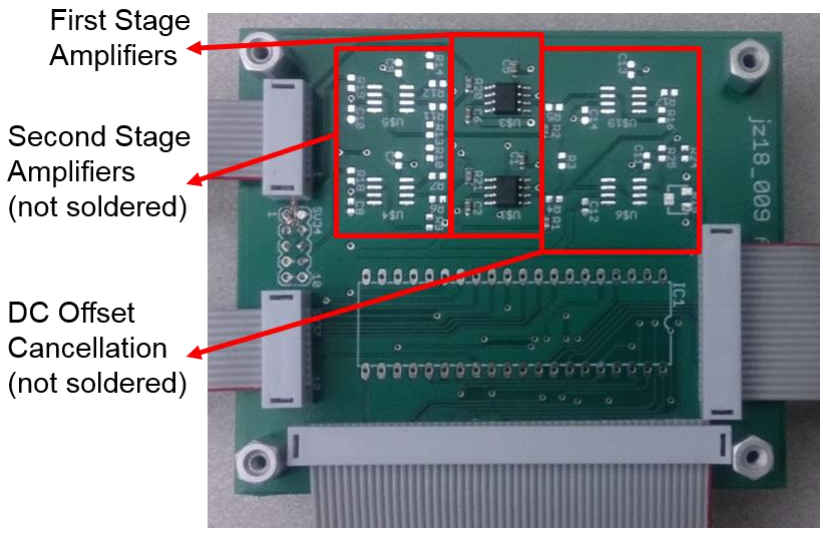


Figure B.3. Accelerometer board for housing the device package and further signal amplification.

Finally, a clock-generation board is designed and fabricated (Figure B.4) for clocking the analog CMOS switches on the connector board. This board is designed to substitute a benchtop signal generator and provide a highly stable clock signal. An oven controlled crystal oscillator (OCXO) generates a 10 MHz square-wave signal with 5 V amplitude, and D-flip flops perform frequency division to obtain 5 MHz, 2.5 MHz, 1.25 MHz and 625 kHz clocks. The analog CMOS switches on the connector board use 5 V logic, hence not requiring voltage translation. However, a separate clock signal path is implemented with voltage translation to 1.8 V so that the board can also be used for clocking the on-chip switches when testing the larger array. The schematic design of the clock-generation board is provided in Appendix B.5 along with the component models used in the design.

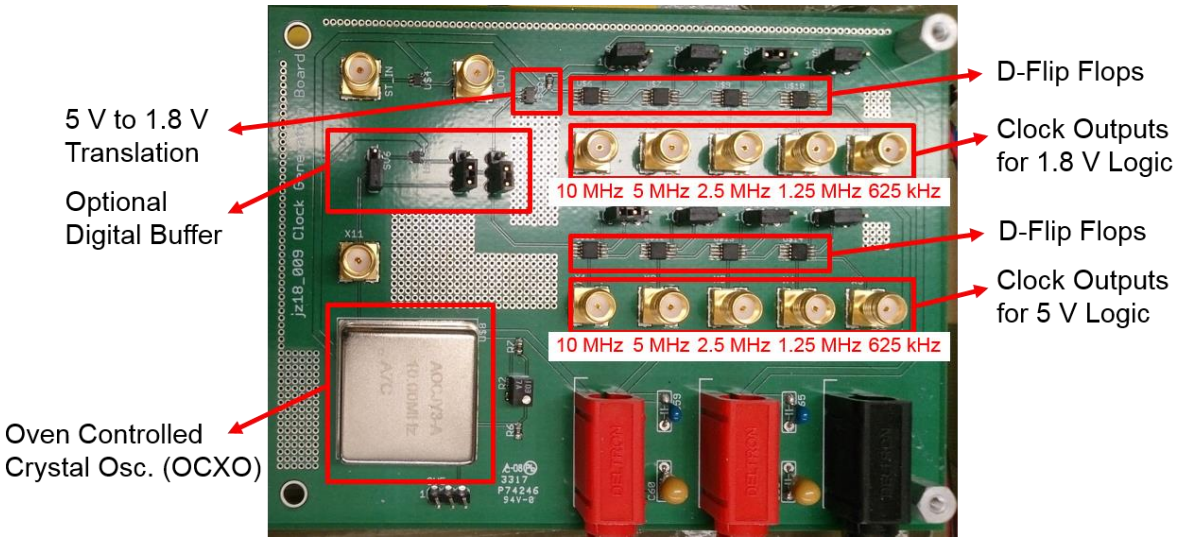
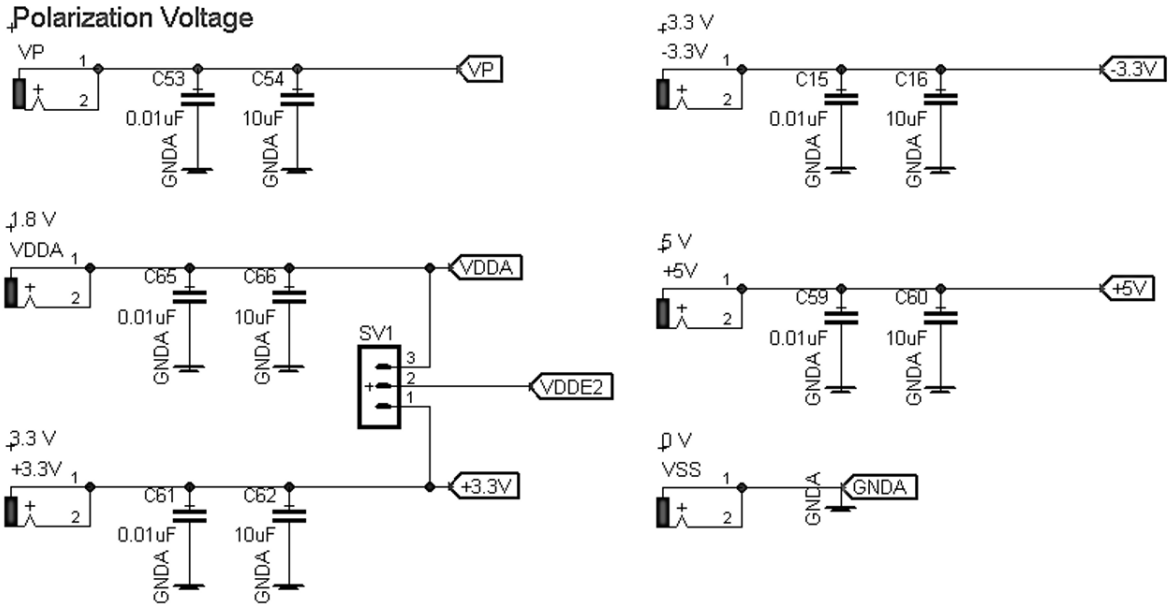


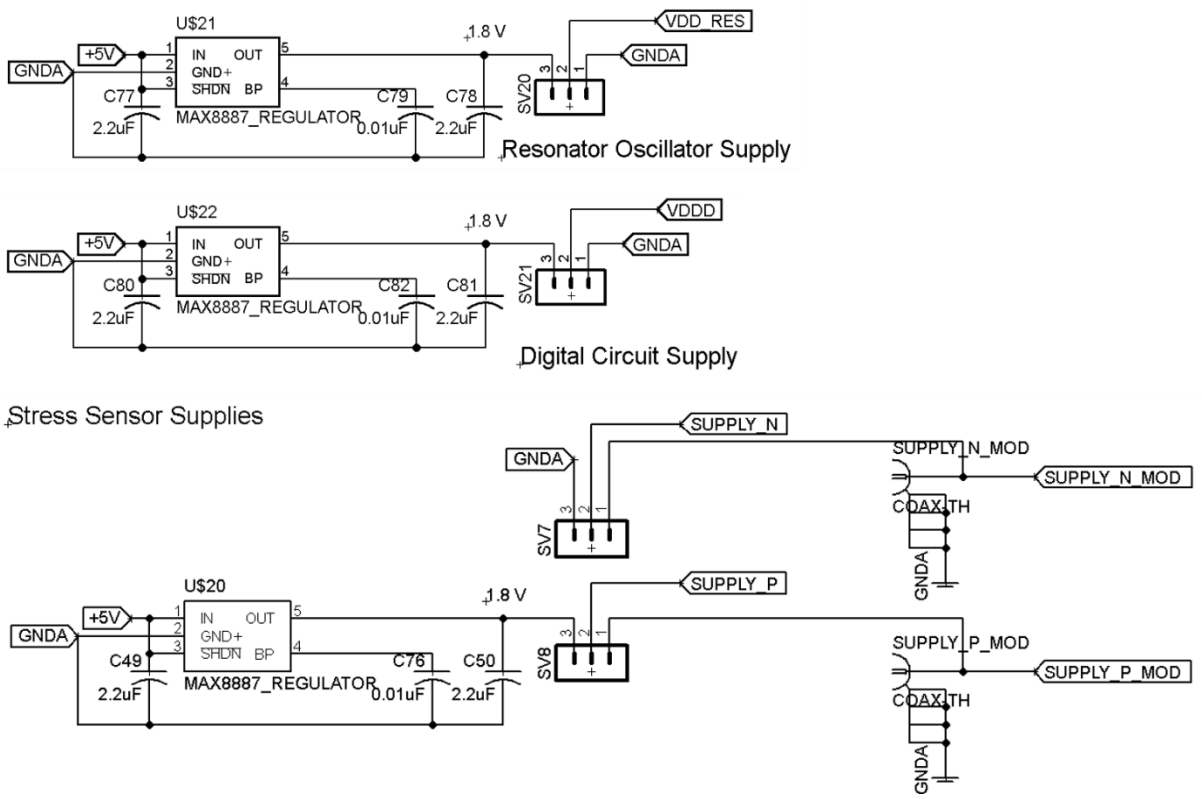
Figure B.4. Clock-generation board for high stability clock signal generation.

B.2 Connector Board

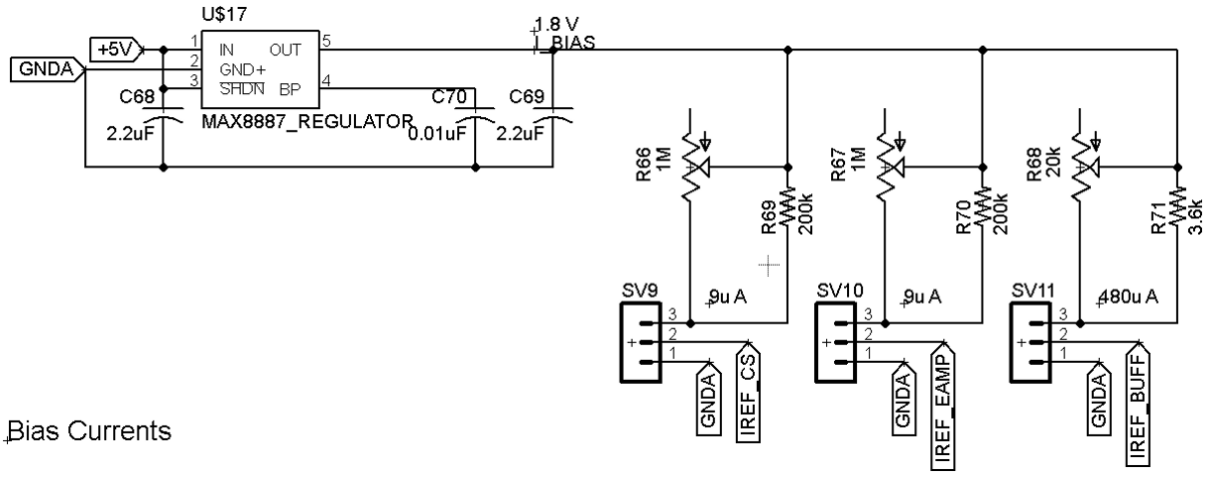
Power Supply Connections



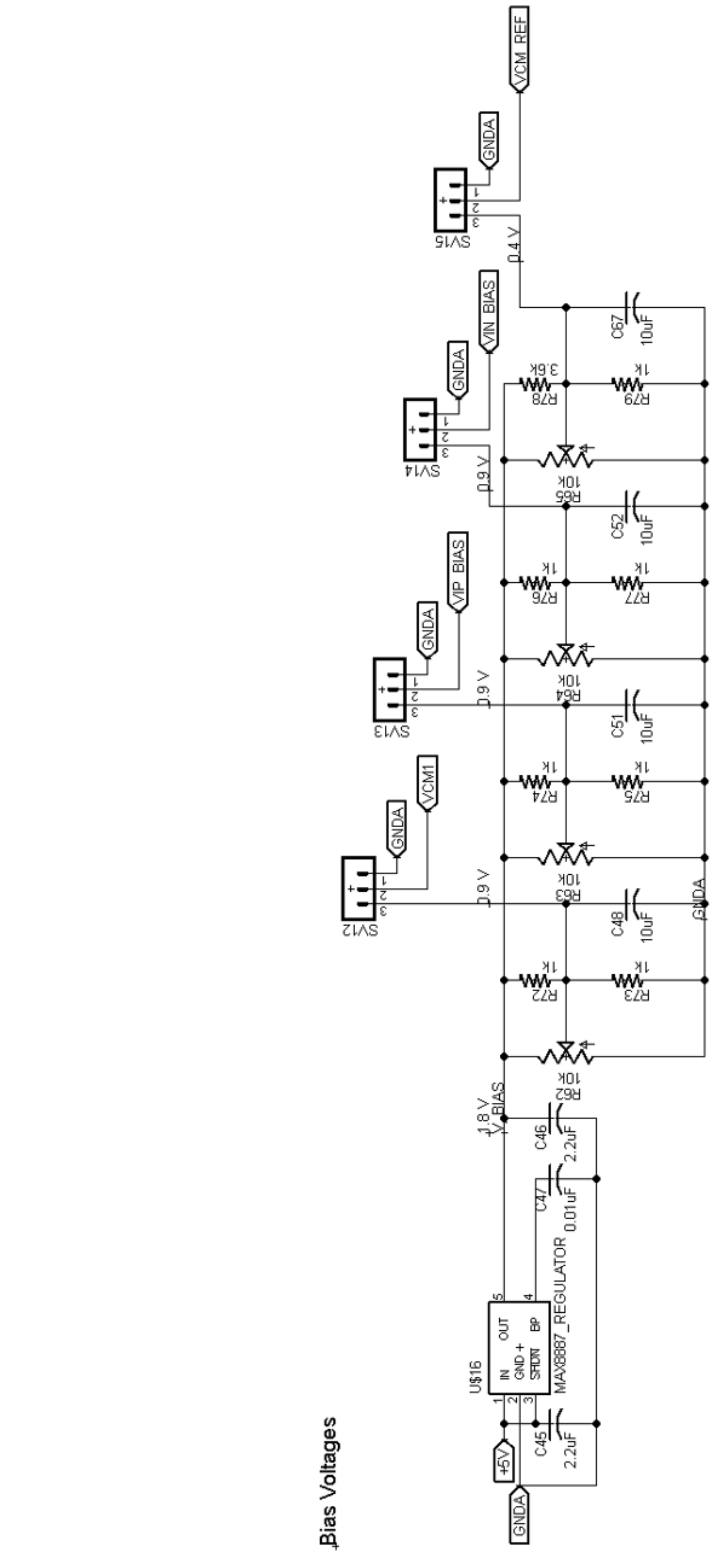
Regulated Supplies



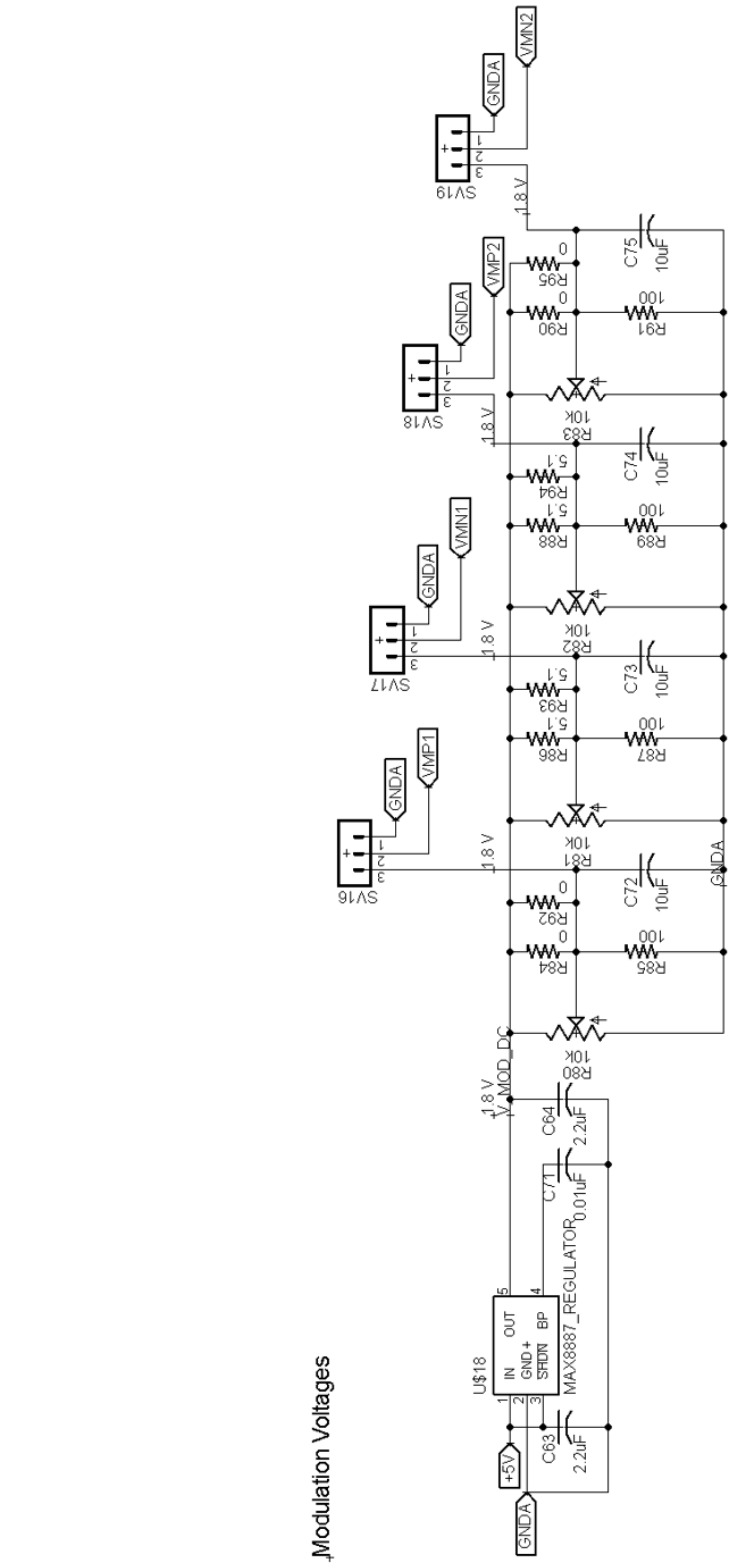
Bias Currents



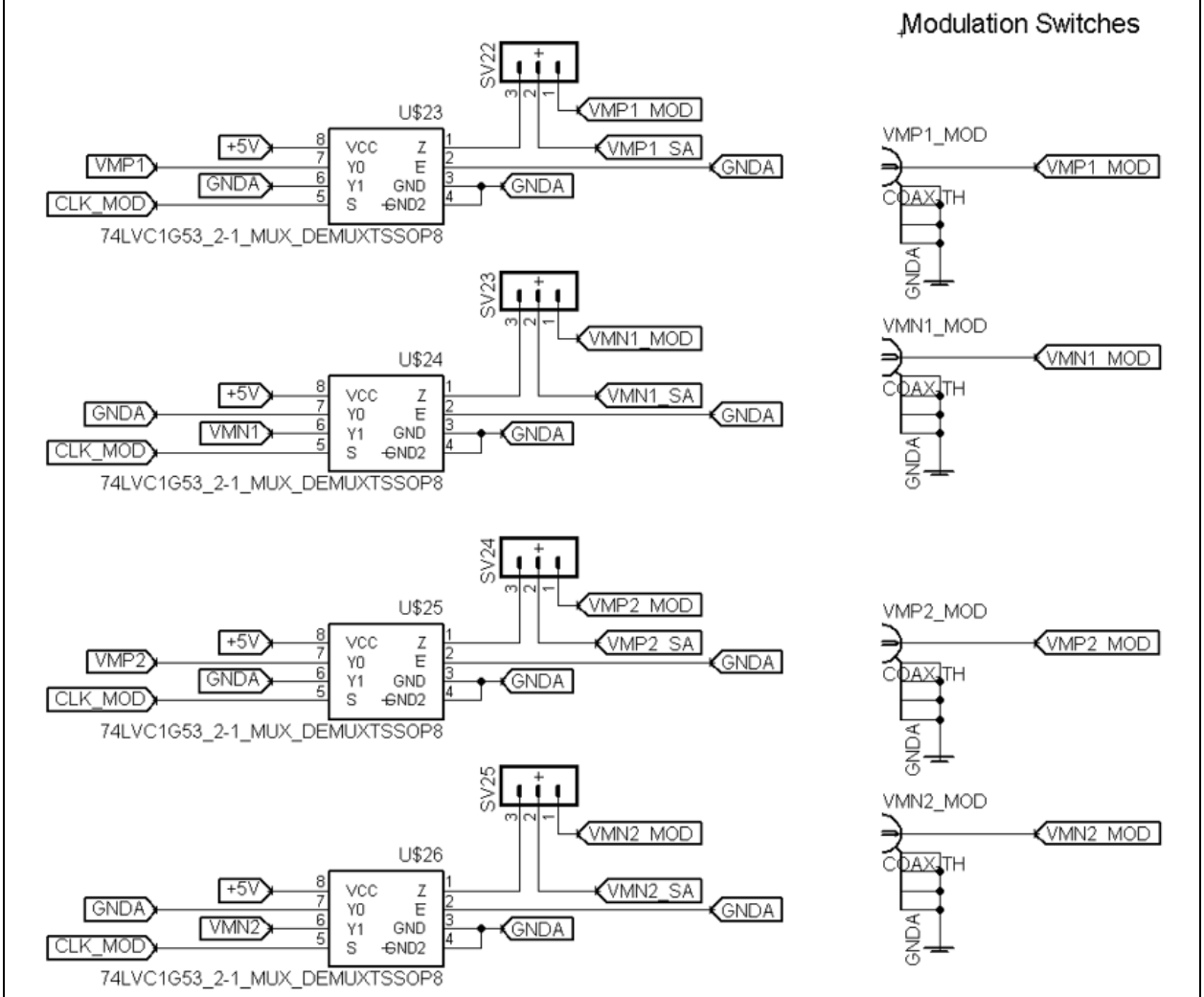
Bias Voltages



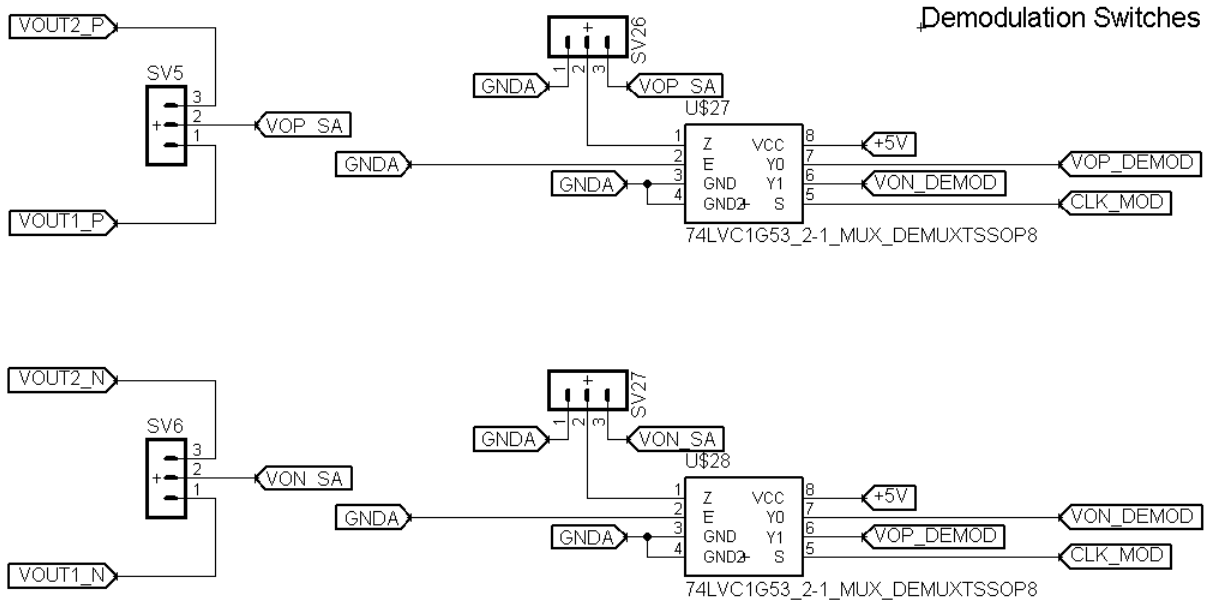
Modulation Voltages



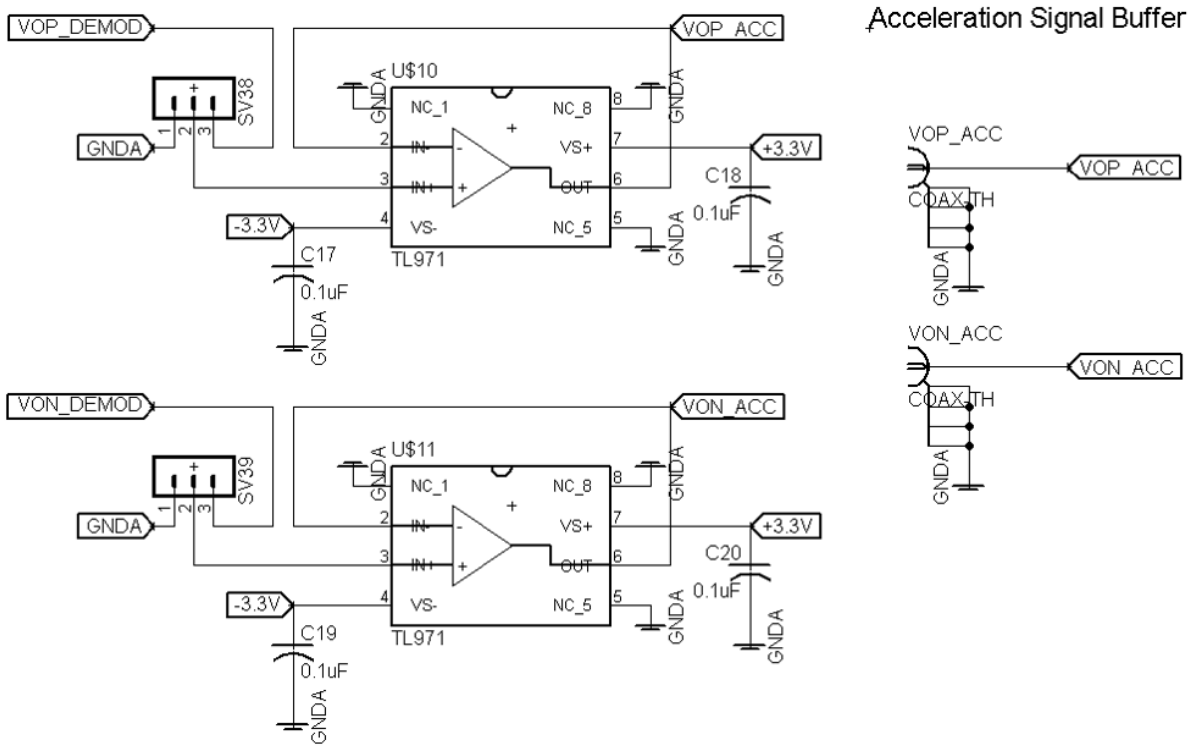
Modulation Switches



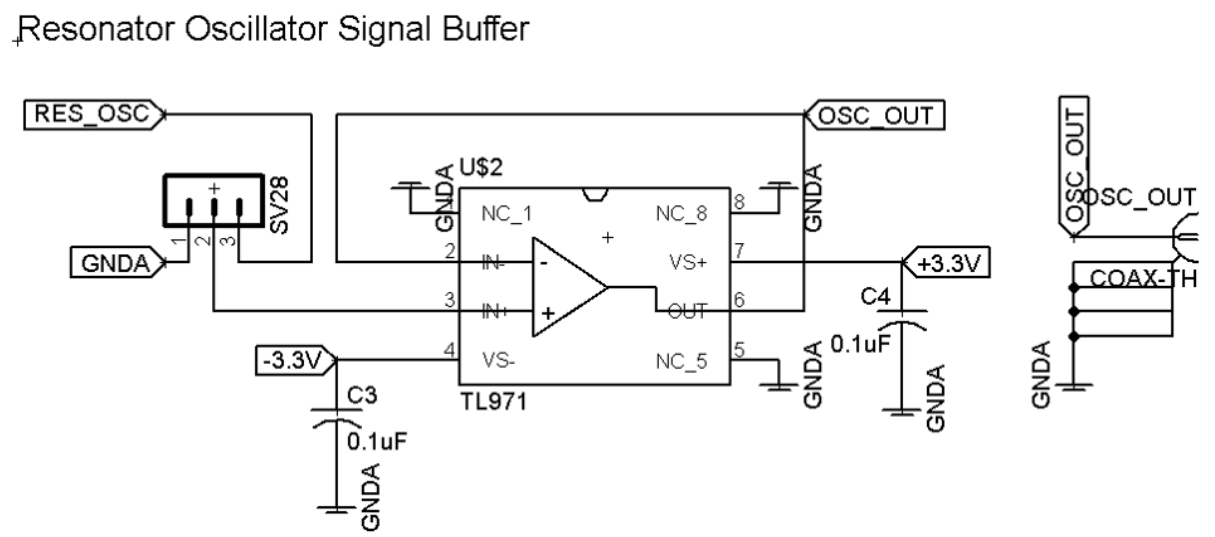
Demodulation Switches



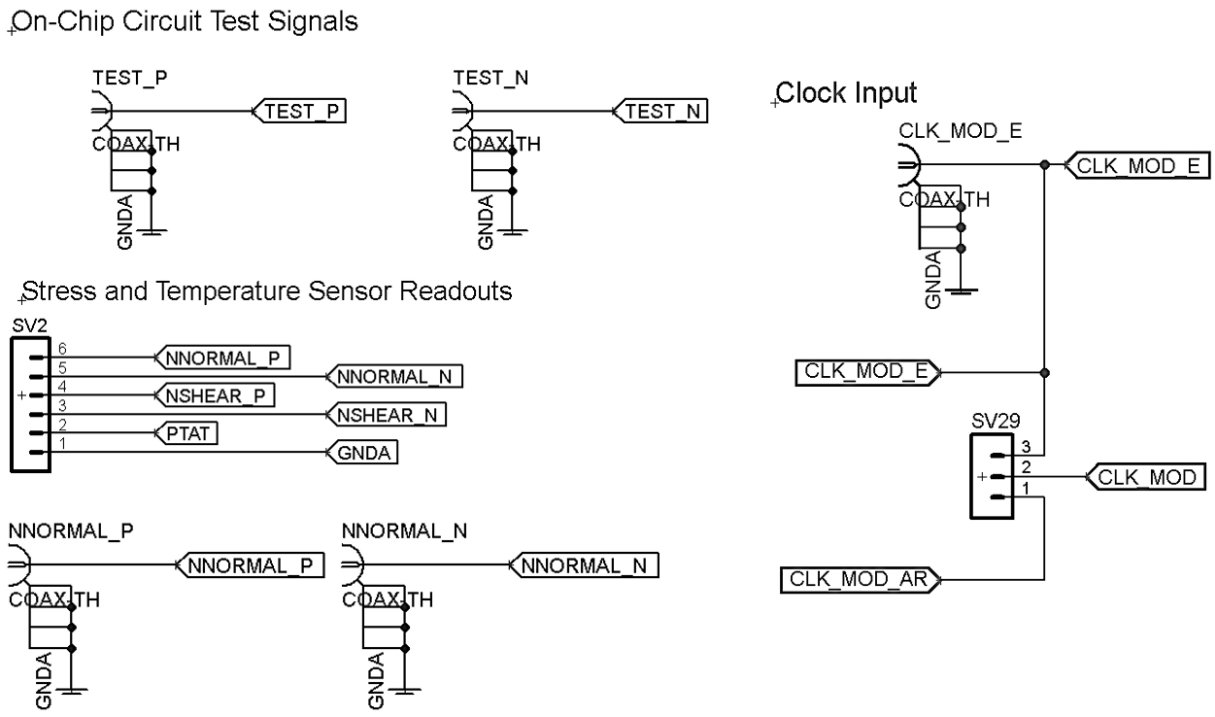
Acceleration Signal Buffer



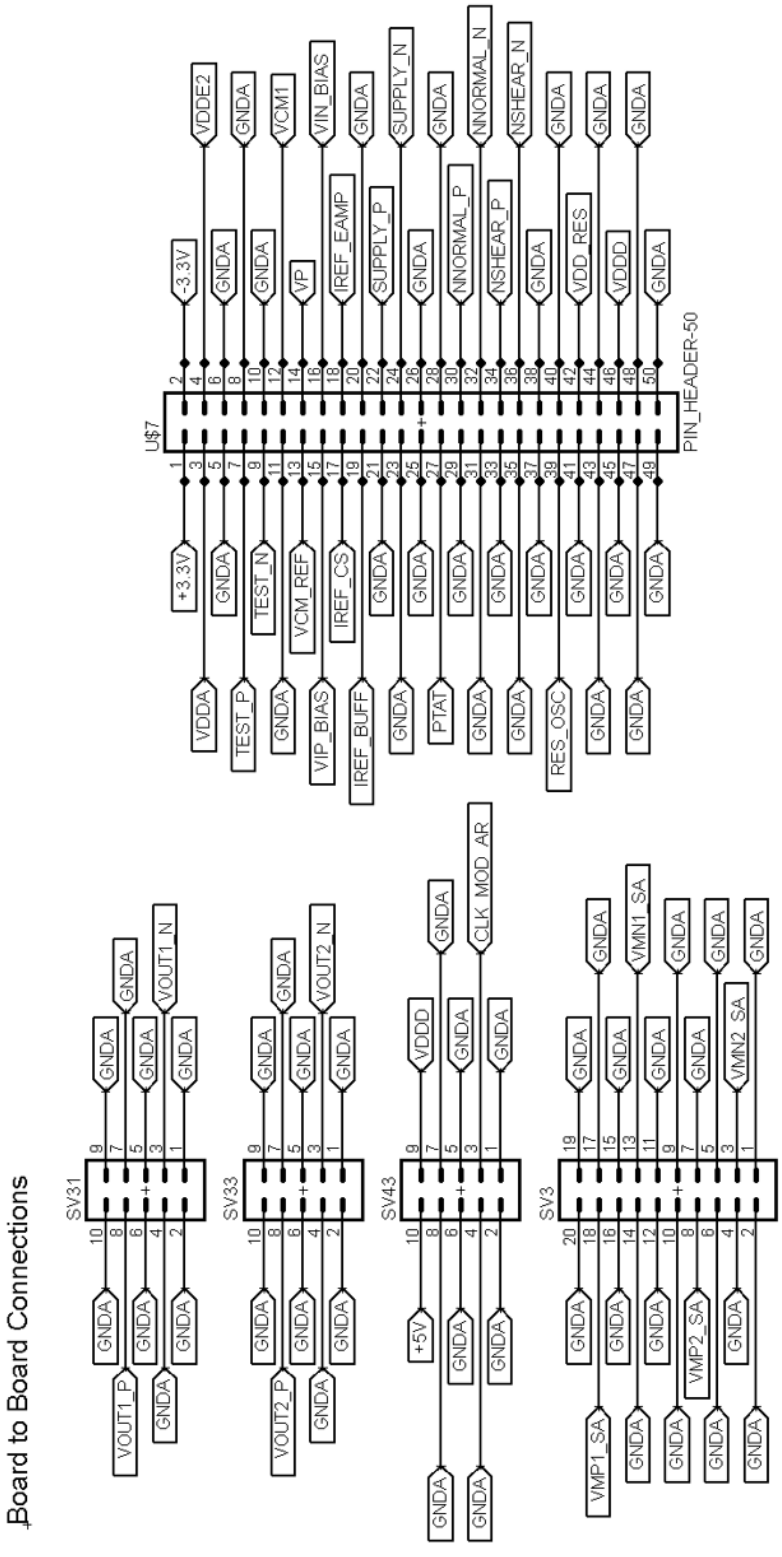
Resonator-Oscillator Signal Buffer



Other Input and Output Connections

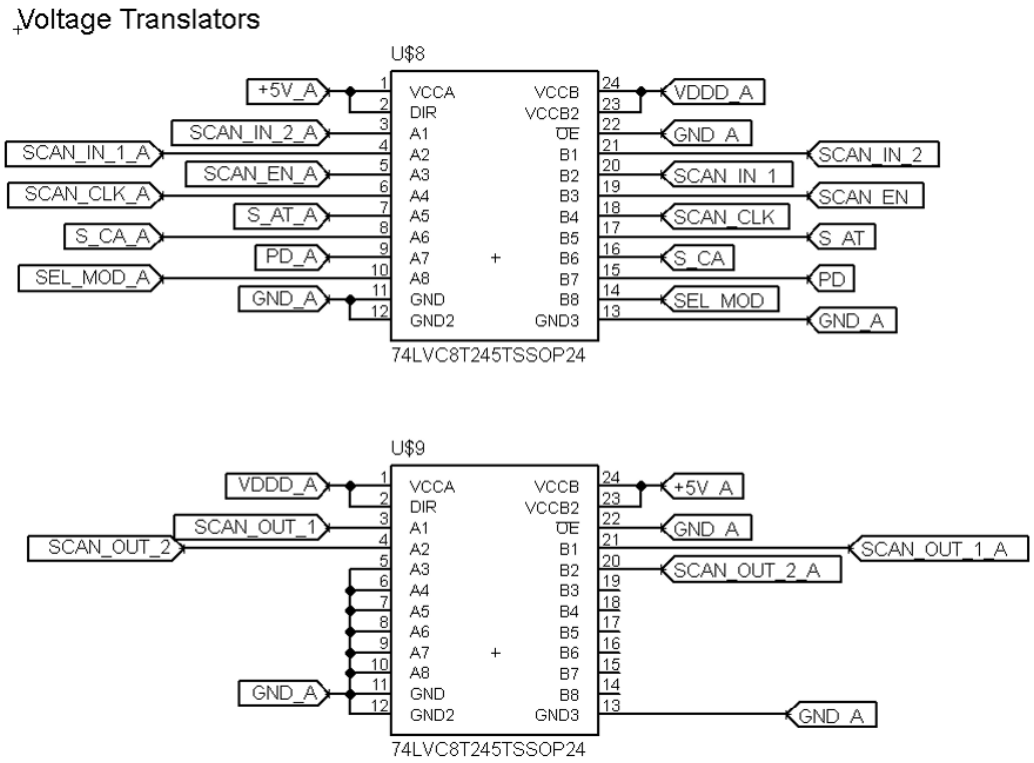


Board to Board Connections

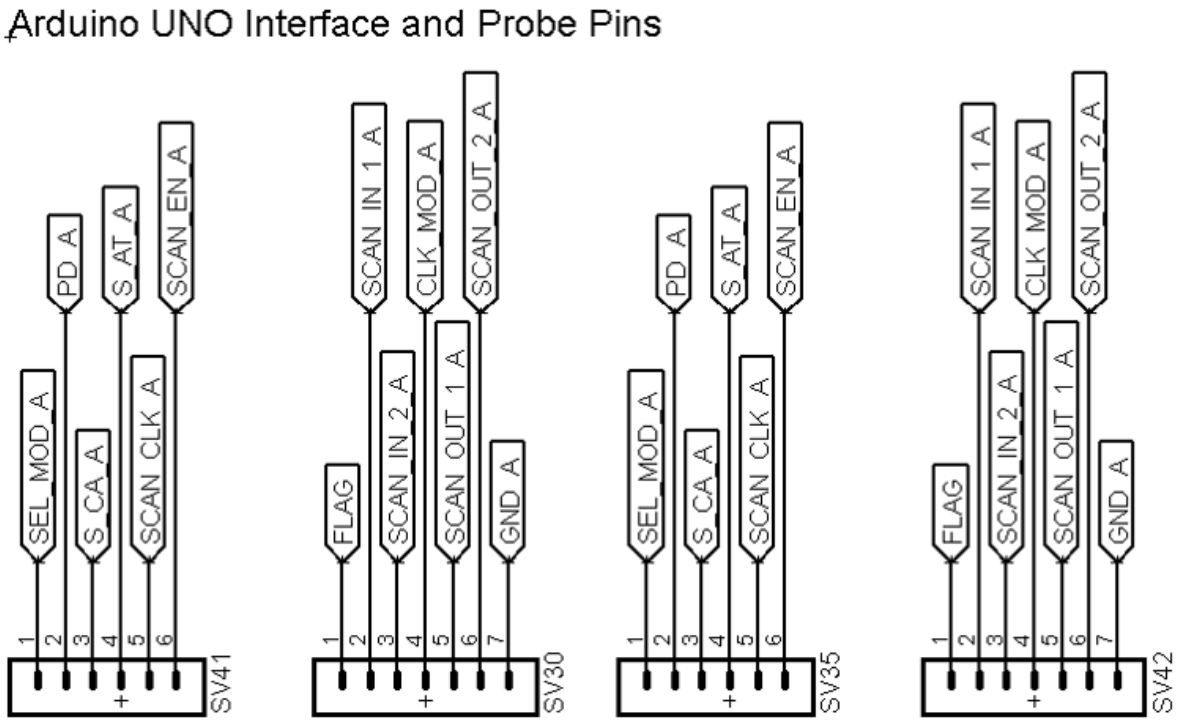


B.3 Arduino Interface Board

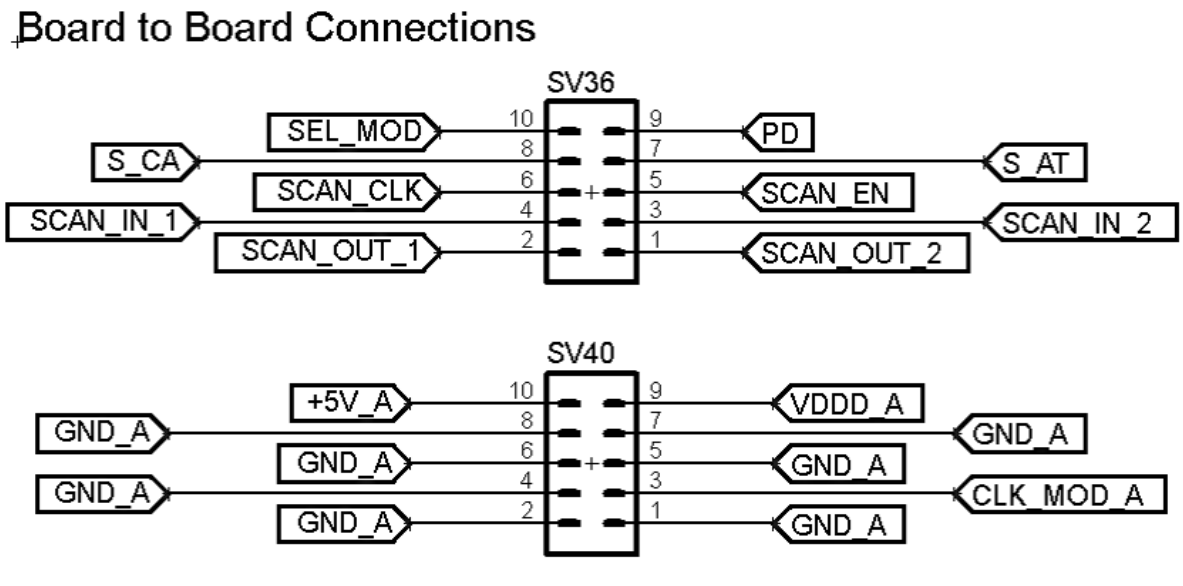
Voltage Translators between 1.8 V and 5 V



Arduino UNO Interface and Probe Pins

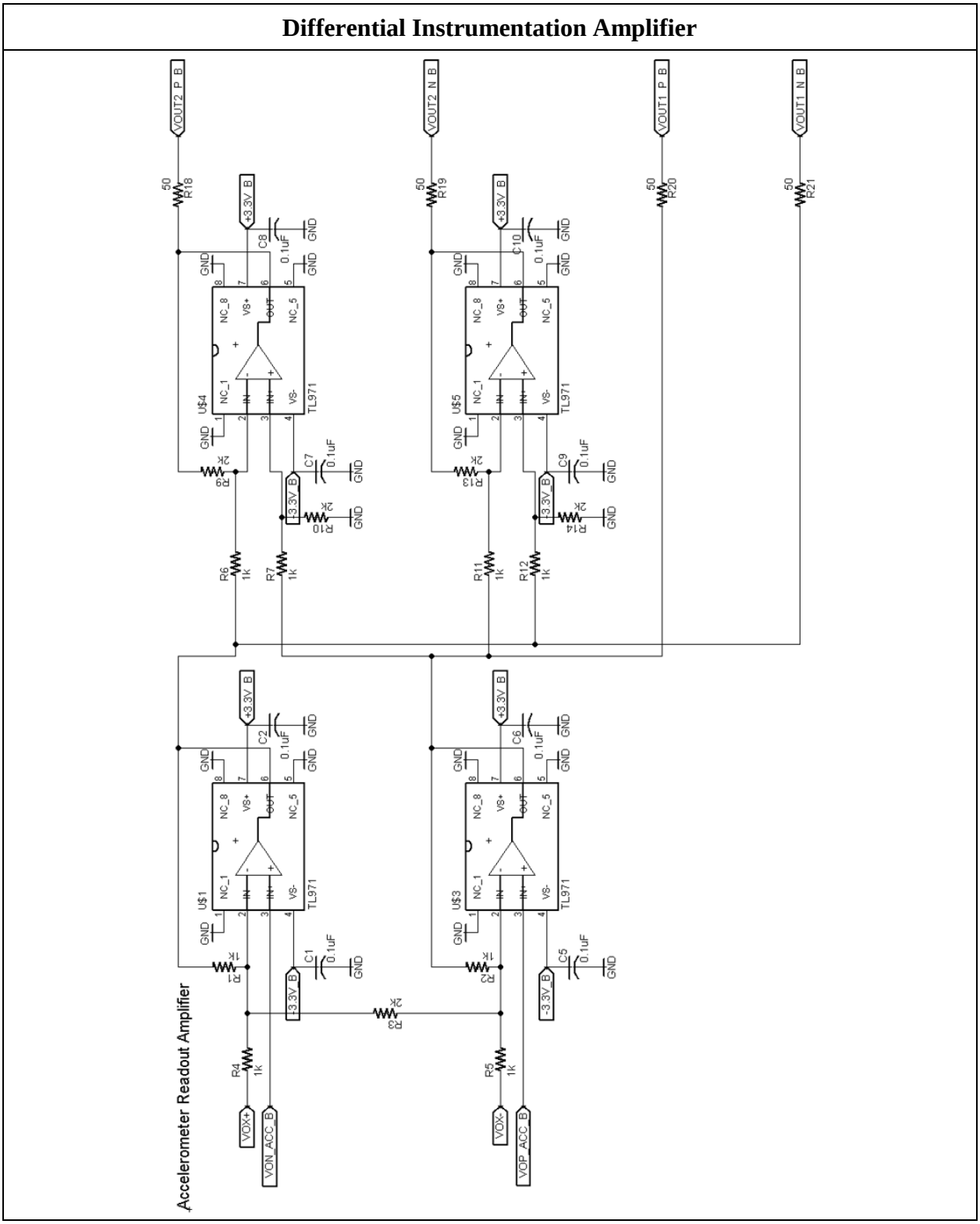


Board to Board Connections

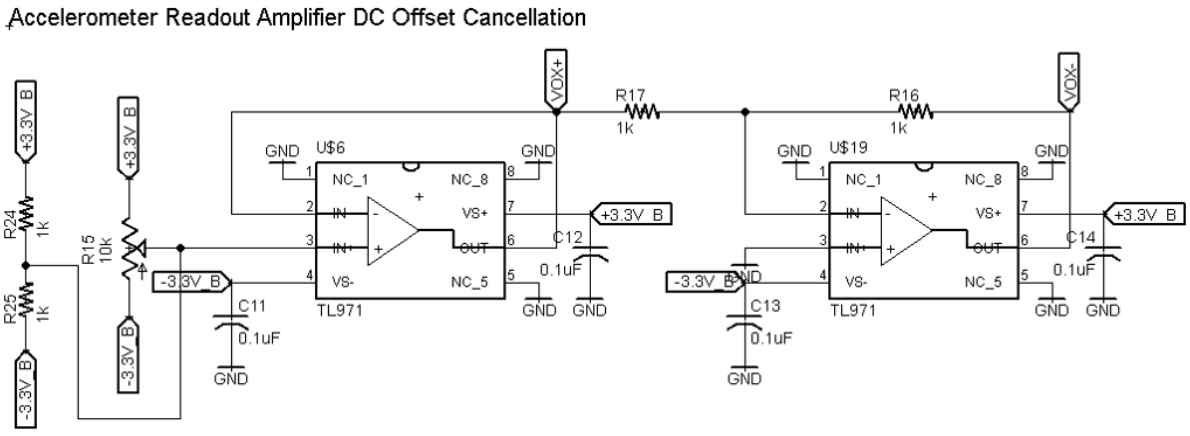


B.4 Accelerometer Board

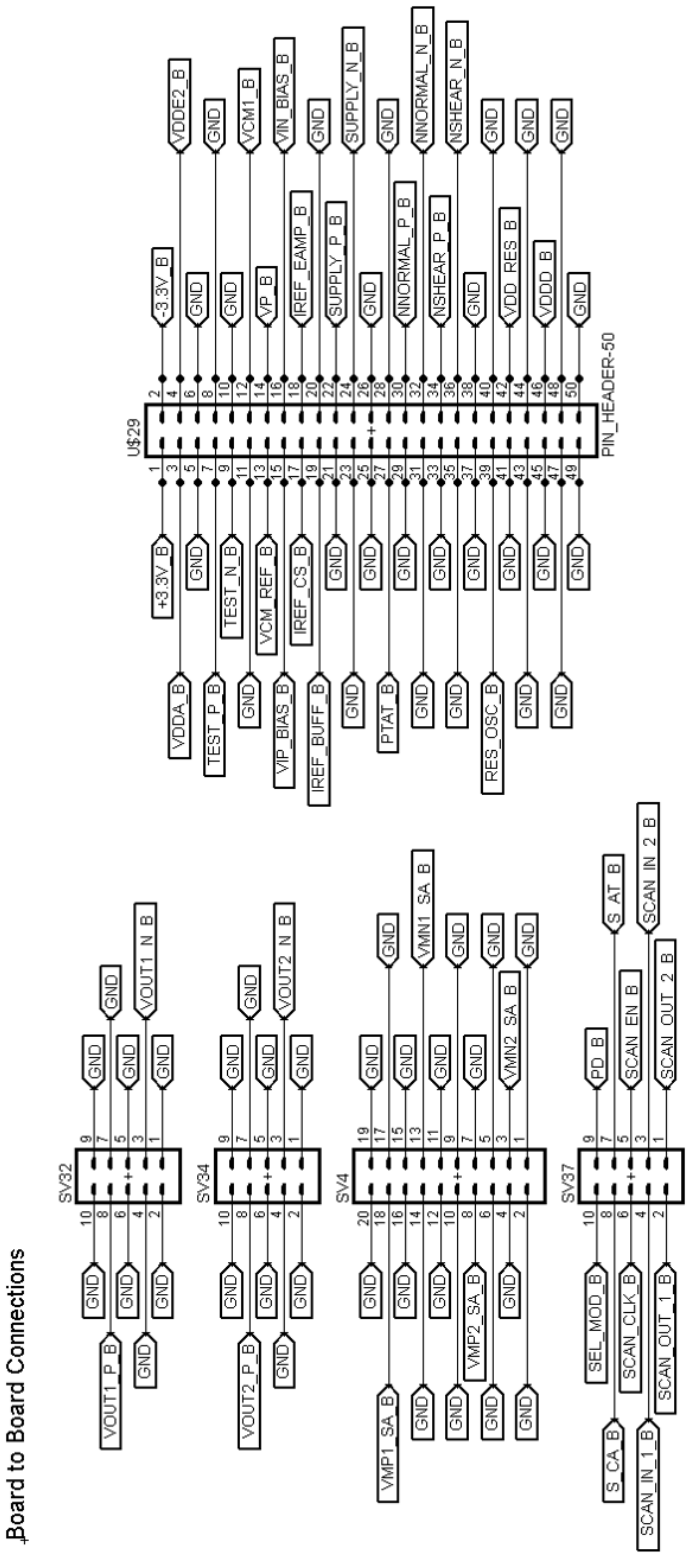
Differential Instrumentation Amplifier



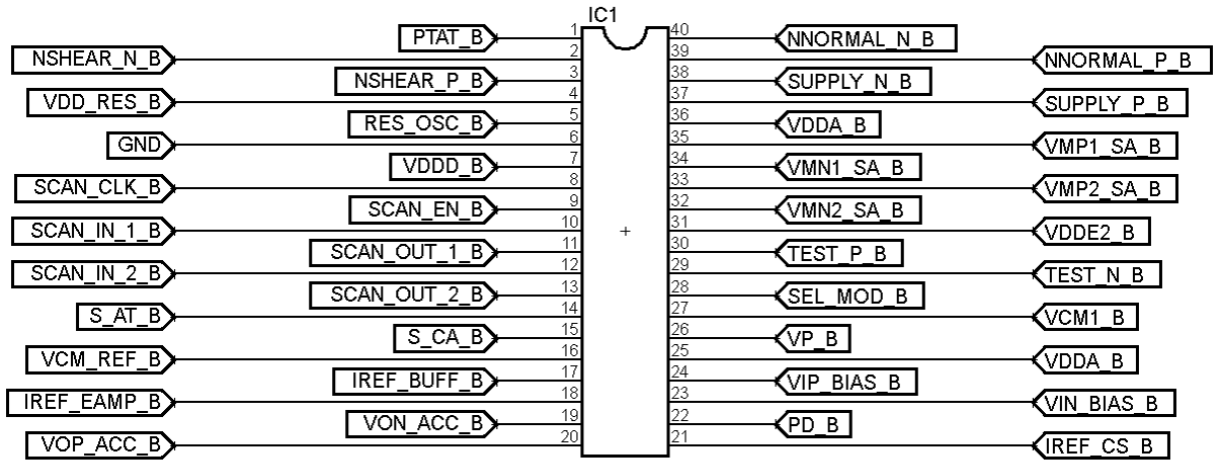
DC Offset Control for Differential Instrumentation Amplifier



Board to Board Connections

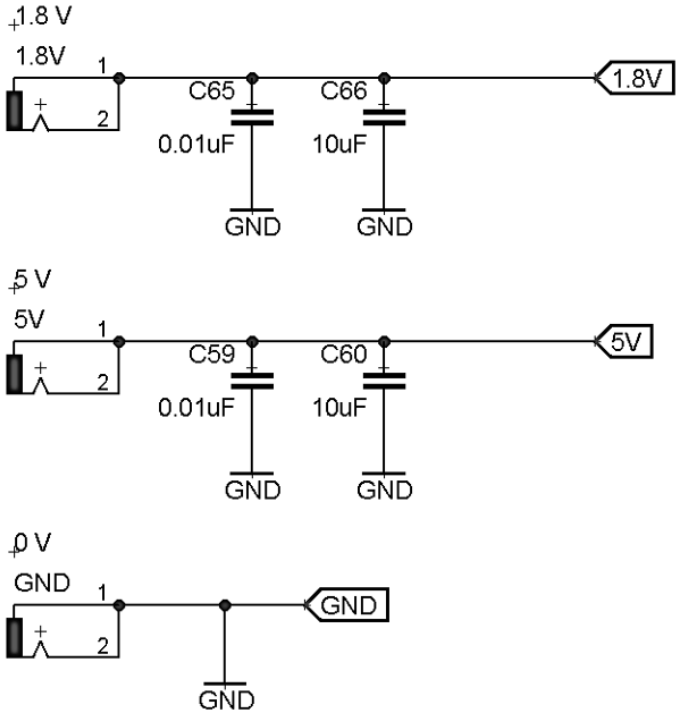


Accelerometer Package Connections

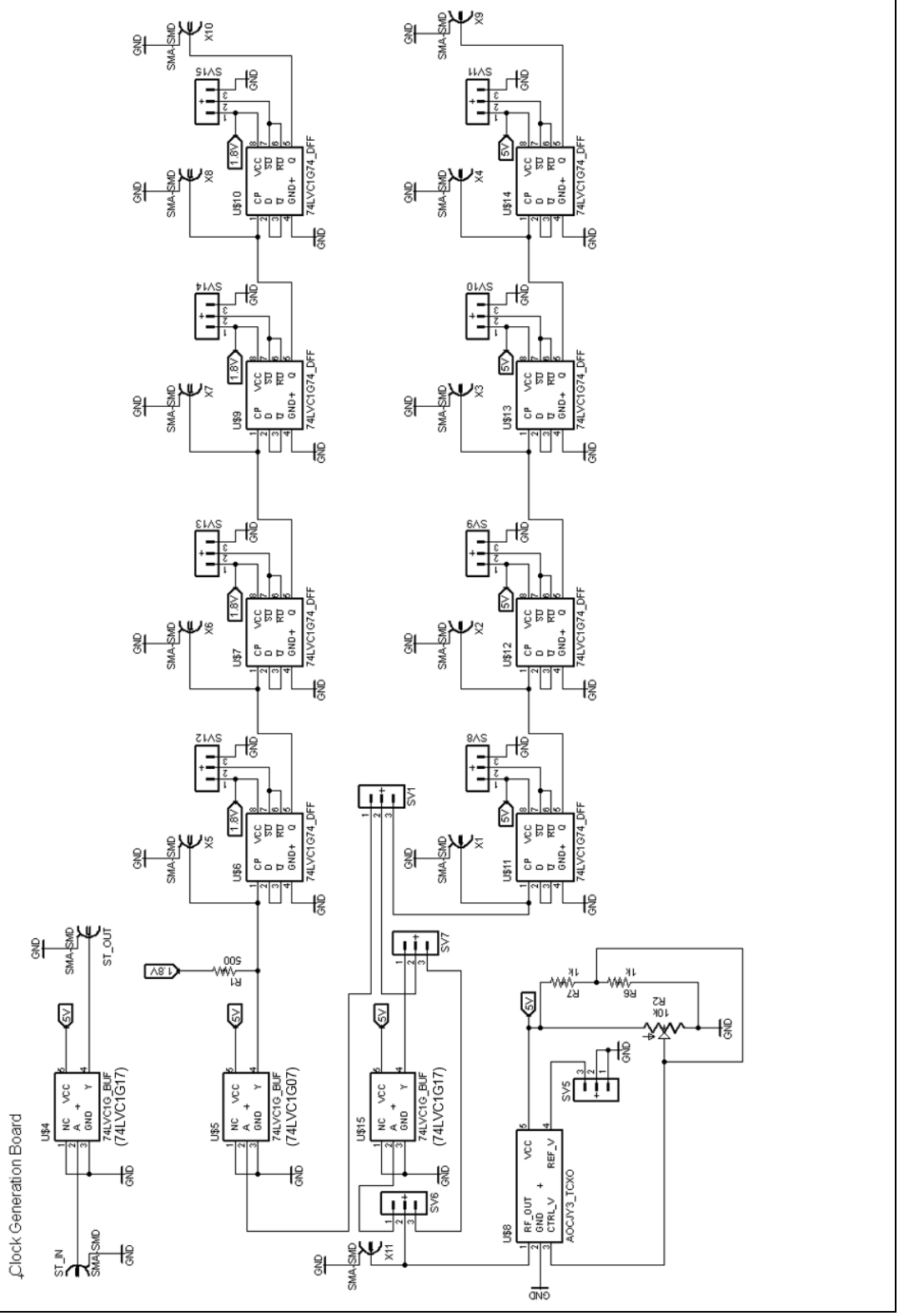


B.5 Clock Generation Board

Power Supply Connections

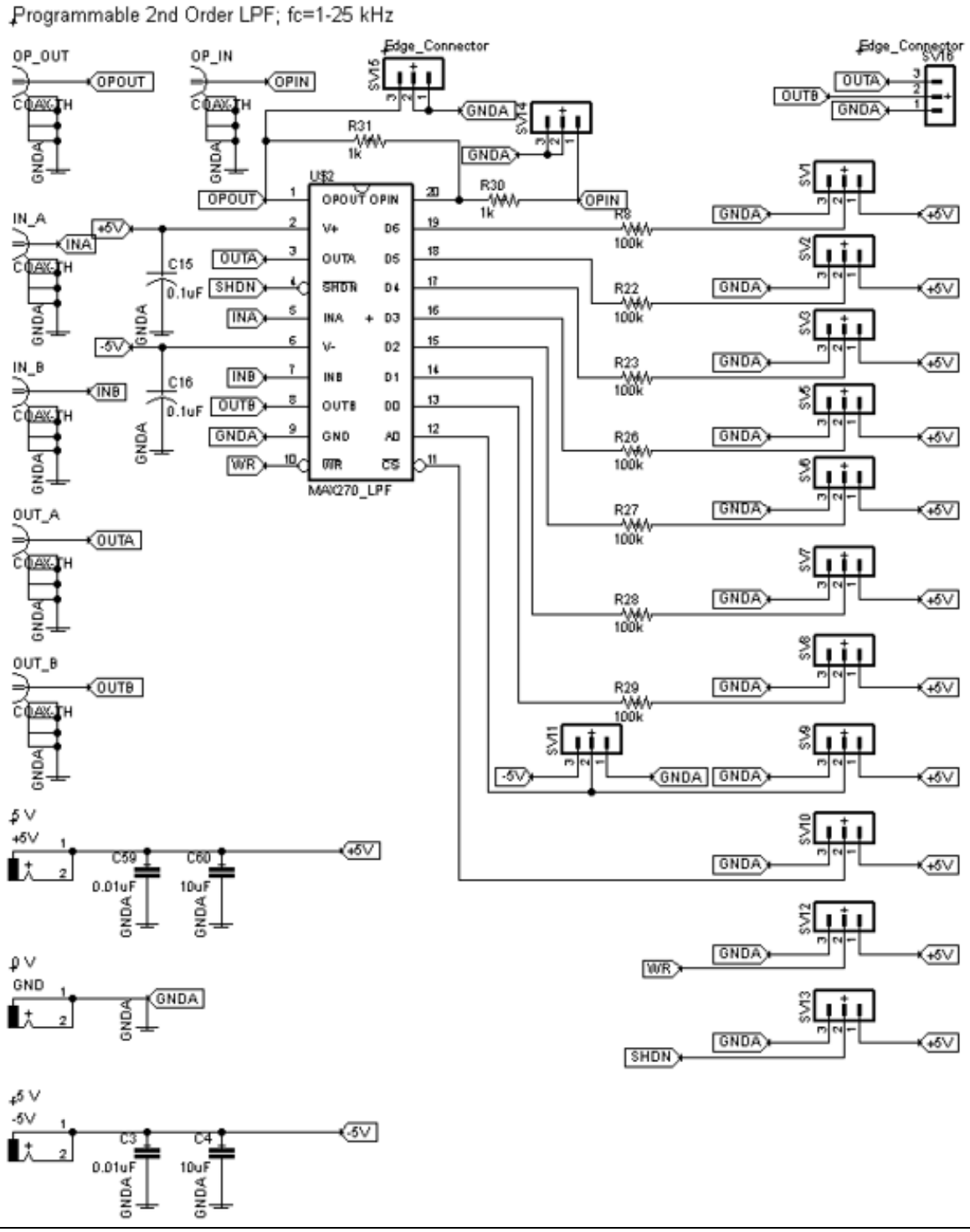


Clock Generation



B.6 Low-Pass Filter Board

Low-Pass Filter Board- Optional
(can be combined with the Connector Board or the filter can be used on a breadboard)



APPENDIX C: TABLE OF CMOS TAPEOUTS

Table C.1. Table of CMOS tapeouts

Run	Tapeout Library	Tapeout Process	Tapeout Content	Notes
1	jz18_006	TowerJazz CA18HD 0.18 µm CMOS	First non-curl matched accelerometer design and crude interface circuit	Accelerometer functional with 1 µV/G sensitivity affected by adverse biasing of interface circuit
2	jz18_007a	TowerJazz SBC18H2 0.18 µm Bi-CMOS	Same accelerometer cell design and interface circuit, accompanied by PTAT circuit, stress sensors, and a resonator-oscillator design	PTAT, piezoresistive stress sensors and resonator-oscillator function and perform as intended
3	jzc18_008	TowerJazz CA18HA 0.18 µm CMOS	Curl matched accelerometer cell design; crude interface circuit	Curl matching successful; accelerometer interface circuit same as Run 1 and 2 and with same bias issue
4	tsmc018_007	TSMC 0.18 µm CMOS	CMOS MEMS test structures to validate process for micromechanical devices	Excessive metal milling and excessive MEMS curl relative to the TowerJazz processes
5	jzc18_009	TowerJazz CA18HA 0.18 µm CMOS	Full accelerometer system design, with updated CMOS interface circuits, and with piezoresistive stress sensors, piezo-FET sensors, PTAT, and resonator-oscillators	All system components function and perform as intended; electronics and noise folding limit accelerometer noise floor

APPENDIX D: POST-CMOS MEMS PROCESSING RESULTS FOR TSMC 0.18 μm CMOS PROCESS

The TSMC 0.18 μm CMOS process is a potential alternate CMOS foundry for making the CMOS-MEMS accelerometer system. Various test structures, a small accelerometer array and resonator-oscillator designs (Figure D.1) were taped-out in early February 2017 in order to explore the applicability of the CMOS-MEMS post-processing steps on the devices built in the TSMC 0.18 μm CMOS process. Most of the test structures were taken from the legacy CMOS-MEMS tape-outs of the MEMS Laboratory research group at Carnegie Mellon University. The etch rate and substrate undercut test structures help determine the post-processing times. Bimorph, vertical curl, lateral curl and axial-stress test structures are used to evaluate the curling due to the stress built in the structures during CMOS fabrication. Young's modulus test beams enable nano-indentation based measurement of the Young's modulus of various beam designs, which would inform the spring constant calculations for the beams fabricated in this process. The thickness test structure is designed to confirm the layer thicknesses in the process through a simple profilometer measurement. Finally, the accelerometer and resonator-oscillator designs used in this study directly inform the fidelity of the mechanical structures upon post-processing. The accelerometer and resonator-oscillator designs in this tape-out can also potentially be tested with off-the-shelf circuits in order to explore their standalone performance.

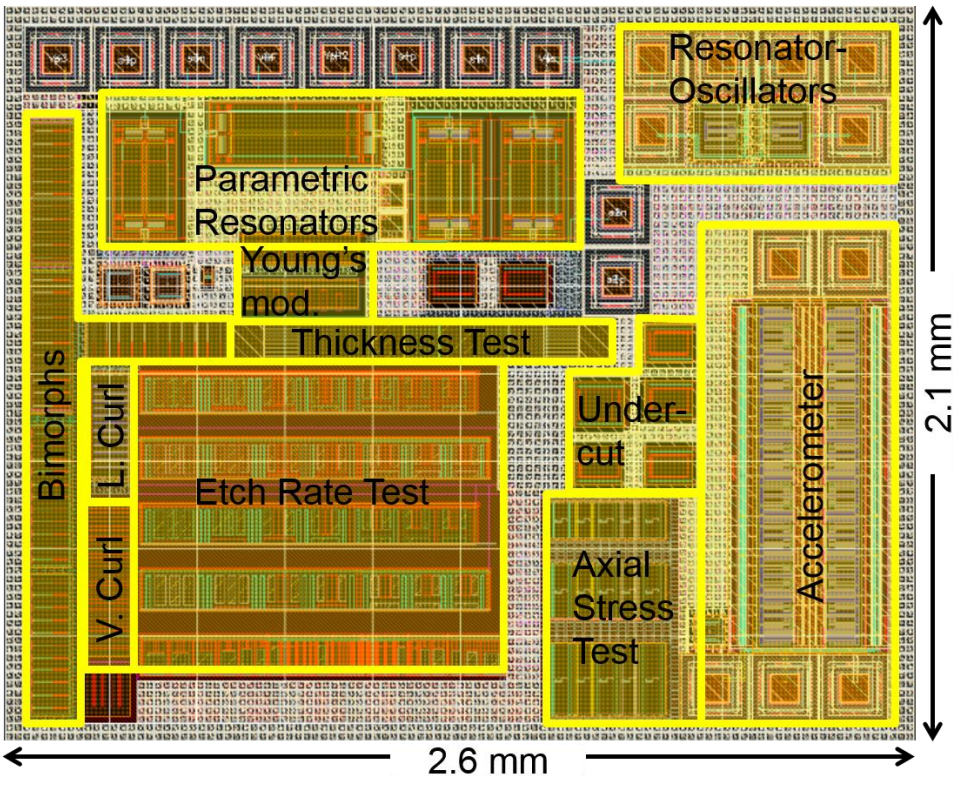
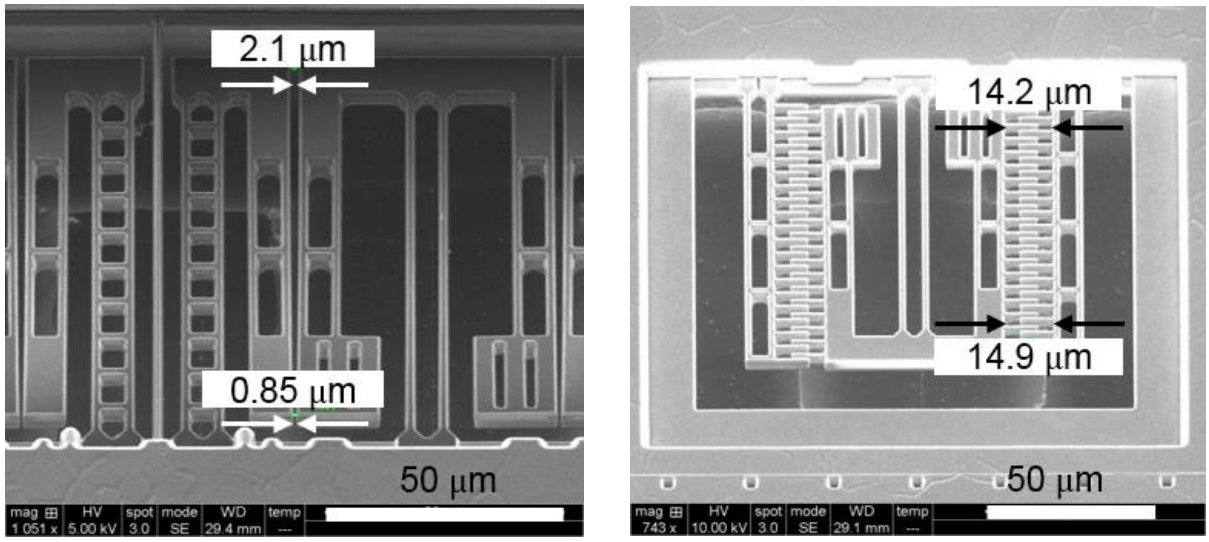


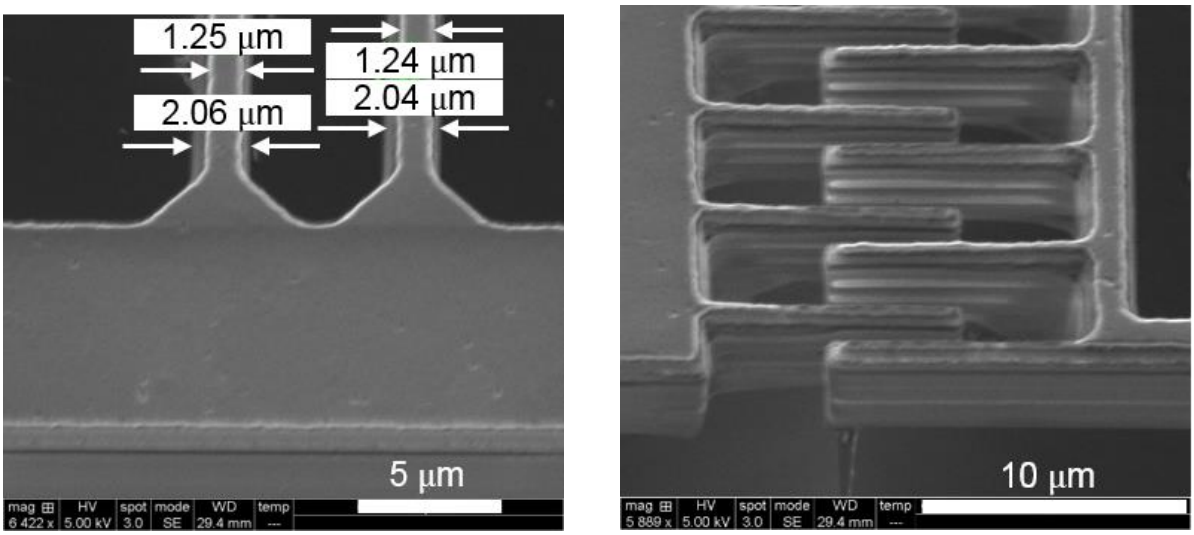
Figure D.1. Various test structures, a small accelerometer array and two resonator-oscillators were taped out in the TSMC 0.18 µm CMOS process.

The CMOS-MEMS post-processing steps are completed successfully on the TSMC chips. The accelerometer array and the resonator-oscillators release through 420 min reactive-ion etch (RIE) of oxide in a Plasma-Therm 790 RIE followed by 20 min (60 cycles) anisotropic and 7 min isotropic Si etch in STS Multiplex ICP RIE. The inherent stress in the structures is higher compared to TowerJazz processes such that the accelerometer (Figure D.2 (a)) and resonator-oscillator electrodes (Figure D.2 (b)) undergo ~ 0.7 µm lateral curl due to relatively large internal bimorph residual stress effects upon release. The top metal of the process is less robust as an etch mask in the Plasma-Therm chamber. Significant milling is observed on the top metal after oxide RIE (Figure D.3), even though the top metal is 1.6 times thicker in the TSMC process compared to the TowerJazz processes.



(a) (b)

Figure D.2. (a) The lateral curl of the accelerometer and (b) resonator-oscillator electrodes due to internal bimorph residual stress in the TSMC process.



(a) (b)

Figure D.3. (a) The milling on the top metal of the spring beams and (b) comb fingers of the resonator-oscillators on the TSMC chips after oxide reactive ion etch.

The vertical curl of the stator and rotor springs of the accelerometer cells matches with 20 nm maximum mismatch at the truss ends (Figure D.4). The maximum vertical curl in the TSMC

process (0.54 μm) is larger than that in the TowerJazz process (0.2 μm), which is another indicator of relatively high residual stress gradients in the TSMC process.

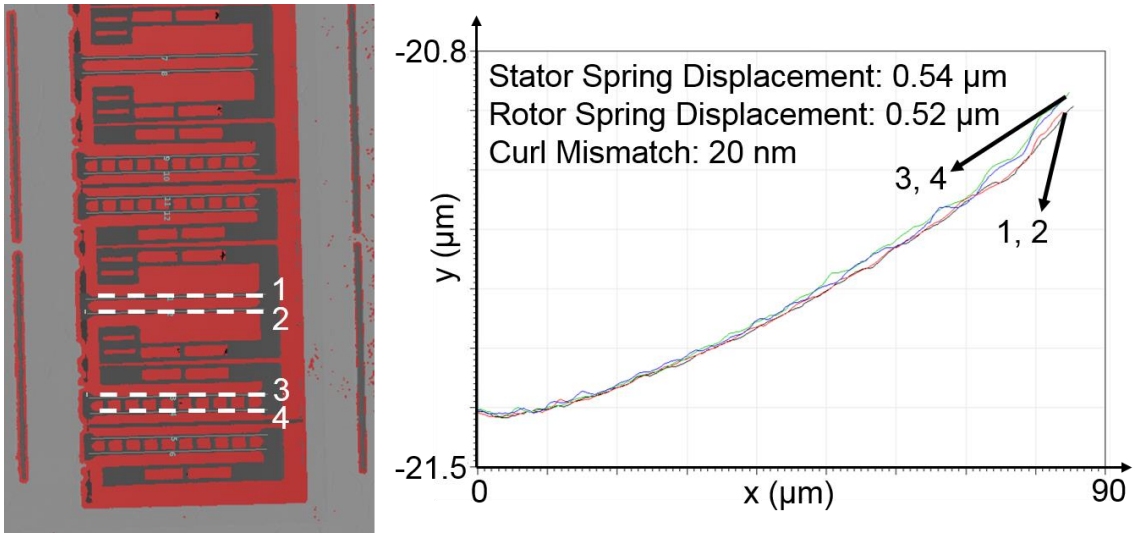


Figure D.4. The vertical curl of the springs and curl matching between the accelerometer rotor and stators in the TSMC process.