In the name of God

Material gradients in thin stretchable substrates for wearable electronics

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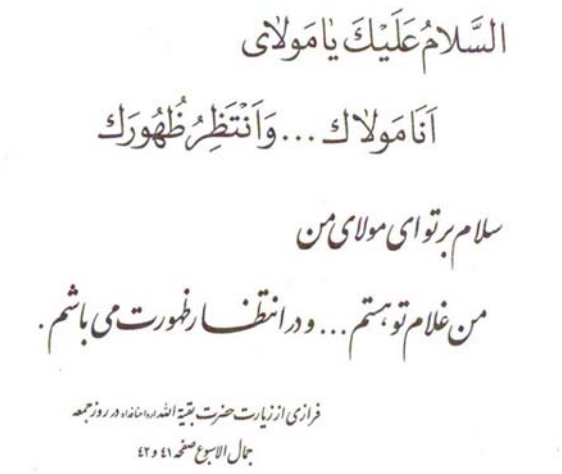
Dedication



Peace be on you, my Master

I'm your servant … and waiting for your re-appearance.

Acknowledgments

I would like to thank who has brought me into being and has endowed me with hearing, and sight, and wisdom to discover the mystery of life. Thank God; I found out you are that mystery.

I could not have been where I am in my life without the help of so many people. This thesis is a sample product of the collective contributions of my family, friends, peers and mentors. I want to acknowledge a few of them here with the full knowledge that this list is incomplete.

I wish to warmly thank my family, my father, my mother and my wife for constantly following my life journey, being supportive in difficult moments, and serving as such inspiring examples for my life.

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Abstract

Stretchable electronics garners attention for its promise in unobtrusive wearable systems for health monitoring and potentially for medical therapy. One significant question though is whether to develop holistic stretchable electronics where the process steps for electronic and mechanical functions are interwoven, or to integrate mature CMOS into stretchable electronic substrates where the CMOS process is separate from mechanical process steps. A major limitation with integrating CMOS is the interface between the soft and hard materials when introduced into functional systems. To address this, we have developed a new platform for stretchable electronics with the ability to embed hard CMOS based substrates that are prevalent in electronic and sensing devices. Through integrating and connecting small CMOS chips spread through an elastomeric substrate, the final system will have highly functional electronic attributes, while being stretchable because of the high percentage of low modulus elastomers. However, in general, delamination readily occurs when a stretchable substrate with embedded thinned chips is strained. We have developed an approach to control the elasticity of the polymer layers around the hard materials associated with CMOS electronic parts to create a controllable material stiffness gradient interfacing a highly rigid material to the soft stretchable system. This approach enables a thin stretchable system that adheres to the skin, but has hard CMOS based materials distributed through its matrix. Our coupled computational and experimental approach reveals that adding just one controlled layer in the material gradient results in a 5.5 times increase in the strain failure threshold. This huge increase in strain failure threshold decreases the risk of delamination. Also, we have developed an approach to pattern an elastomeric polymer layer with spatially varying mechanical properties around CMOS electronics to create a controllable material stiffness gradient. Our experimental approach reveals that modifying the interfaces can increase the strain failure threshold up to 30% and subsequently decreases delamination. The stiffness gradient in the

polymer layer provides a safe region for electronic chips to function under a substrate tensile strain up to 150%. These results will have impacts in diverse applications including skin sensors and wearable health monitoring systems.

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Chapter 1

1. Introduction

This chapter introduces the thesis subject of thin stretchable substrates for wearable electronics. Section 1.1 presents the background of flexible and stretchable electronics design and fabrication; then the motivation of this work along with the advantages and disadvantages of other works are offered in section 1.2. Section 1.3 gives the thesis statement and the contribution of this work.

1.1. Flexible and stretchable electronics background

Flexible and stretchable electronics have emerged in a pallet of new technologies for realizing smart sensors and actuators for biomedical applications [1–4]. Such systems have been evolving at a rapid rate with the promise of being able to be integrated on areas such as the human body, while providing tremendous amounts of sensory data [5,6]. There are several ways to design and fabricate these interesting structures. These approaches investigate building flexible and stretchable electronics through exploiting new materials, new designs and new fabrication techniques or combination of them. In this section, some of these approaches are briefly discussed.

1.1.1. Organic materials (conductive polymers)

Organic semiconductors are carbon-rich compounds in which the structure is modified in a way to optimize specific properties like charge mobility or luminescent properties. This type of organic material can be divided into three specific categories: small molecules, polymers and biological materials (Figure 1.1). Each of these categories can be exploited in various applications, such as organic light-emitting devices (OLEDs) [7–9]. Organic electronics can be deposit on a variety of substrates such as metal, plastic and glass. They are also lighter, cheaper and more flexible compared to inorganic materials. These specific properties of organic electronics have increased interest in employing organic electronics in different applications [10].

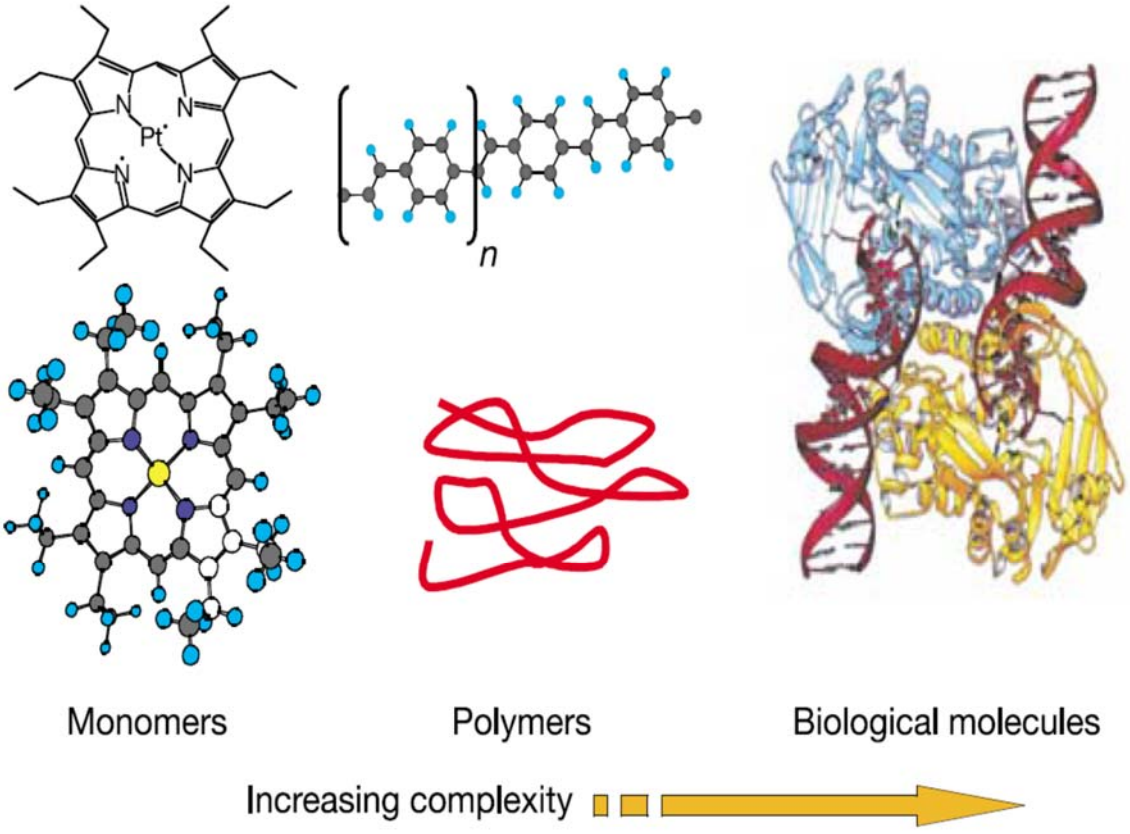

Figure 1.1. Different types of organic electronic materials, ranged in order of increasing complexity from left (simplest, Monomers) to right (most complex, biological molecules) [10].

1.1.2. Nanowires and nanotubes

Nanowires (NWs) and nanotubes are nanometer-scale structures that show highly flexible behavior due to sub-micrometer diameters. These materials can offer promises for high-performance electronics because of their high carrier mobility [11]. The synthetic semiconductor nanowires (GaAs NWs [12–14], InAs NWs [15–17] and etc.) are highly attractive for large scale printable electronics (Figure 1.2) with requirements on performance, since they can be easily grown using bottom-up chemical methods and their material properties (like shape, size, atomic composition, and doping concentration) are adaptable. Nanotubes are excellent candidates for flexible electronics. They are strong and flexible, however the precise control of doping and reproducibility should be addressed [18].

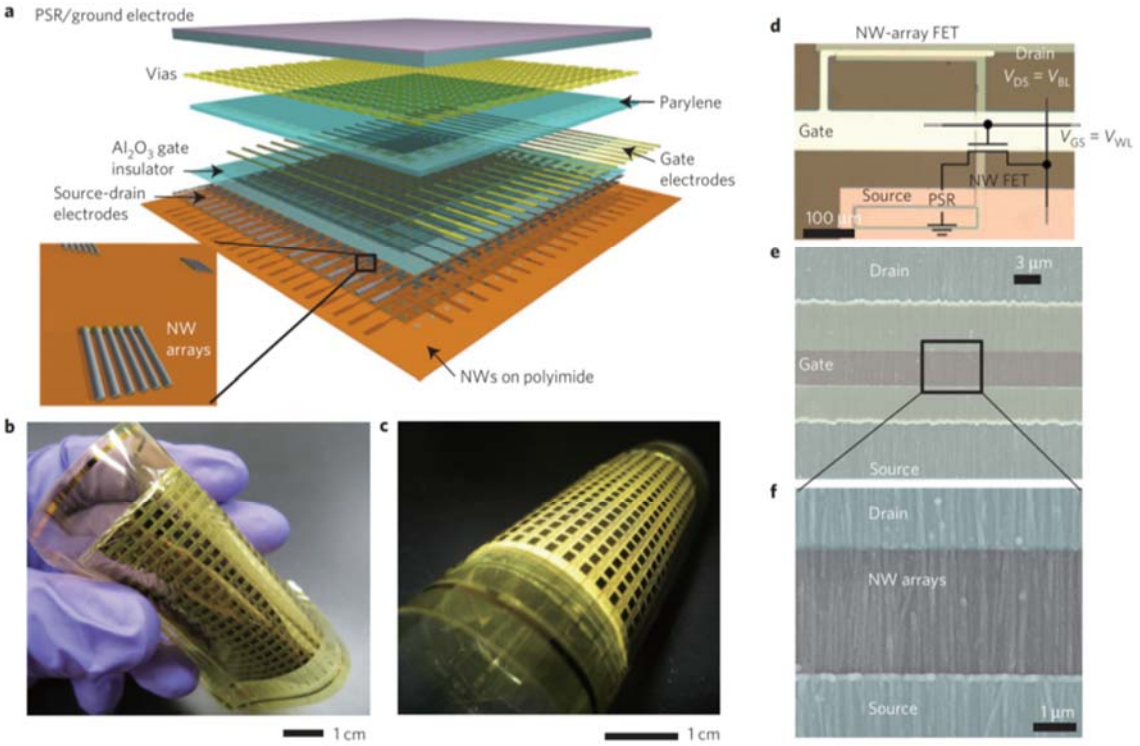

Figure 1.2. Macro-scale flexible devices using Nanowire-based approach. a, Passive and active schematic of the NW e-skin layers. **b, c,** Optical photographs of a fully fabricated e-skin device under bending **(b)** and rolling **(c)** conditions. **d,** A single sensor pixel in the array. **e, f**, Scanning electron micrographs of a NW-array FET [19]

1.1.3. Nanomaterials (thin inorganic films)

Another way of making flexible electronics is based on using design strategies and fabrication techniques [6]. In this approach, by using different fabrication techniques, a very thin layer of inorganic materials is patterned into a substrate. Sub-micron layers of inorganic material show flexible and stretchable properties. These characteristics are enhanced by embedding these layers into the soft elastomeric substrates [20]. These structures can be used for various biological and biomedical applications like health monitoring, improving surgical procedures [21,22] and establishing human-machine interfaces [23]. Some of these applications ranging from epidermal electronics to stretchable batteries are shown Figure 1.3.

Figure 1.3 Nanomaterial applications. a, b, Epidermal electronics with advanced capabilities in near-Field Communication [24]. **c, d,** Stretchable batteries with integrated wireless recharging systems [25]. **e,** Multifunctional inflatable balloon catheters with capabilities in cardiac electrophysiological mapping and ablation therapy [26]. **f,g,** Stretchable silicon circuit with a mesh design, wrapped onto a model of a fingertip [27]. **h,** Conformal silk-supported neural electrode arrays [28]. **i,** Electronics on glove fingertip [29]. **j,** Multifunctional epidermal electronics [30].

1.1.4. Conductive liquid materials

Conductive liquid materials can also provide a base for making flexible and stretchable electronic systems. Eutectic Gallium-Indium (eGaIn) is an example of the conductive liquid materials. eGaIn is a gallium and indium alloy which maintains liquid at room temperature and its high surface tension and high electrical conductivity make it an ideal conductor for a soft sensor [31]. Conductive liquid materials can be employed in applications like soft wearable robots [32] and stretchable sensors [33] (Figure 1.4).

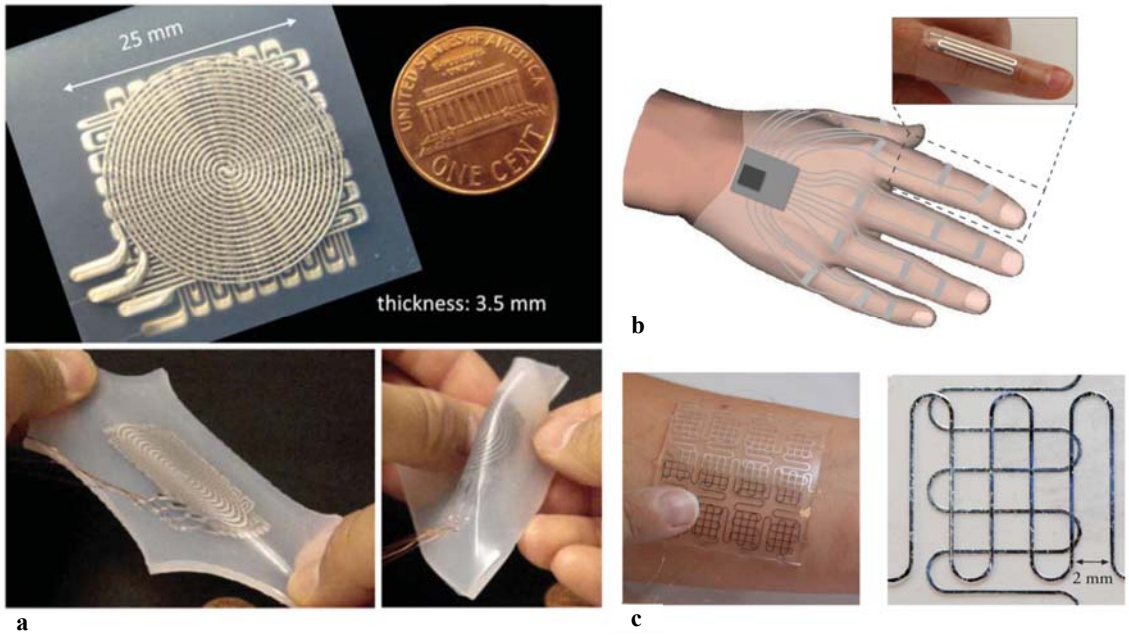

Figure 1.4. Some application of Conductive liquid material (eGaIn). **a**, Soft artificial skin [31], **b,** An illustration of a human hand covered with curvature sensors at every joint [32]. **c,** Flexible and stretchable tactile keypad devices [33].

1.2. Motivation

Flexible and stretchable electronics have been pursued through a wide variety of avenues including different methods and materials like organic electronic materials (conductive polymers) [34], inorganic semiconductors (nanotubes [35–37] and nanowires [38–40]), conductive liquid materials [33] and embedding extremely thin inorganic materials (nanomaterial) like Si and GaAs in soft polymers [41–43]. These approaches have advantages and disadvantages for the goal of simultaneously achieving the performance and reliability of established foundry electronics processes, but in a stretchable electronics platform.

Organic semiconductors are flexible but not necessarily stretchable as they have relatively poor transistor density and performance as well as uncertain reliability [44]. Nanowires and nanotubes hold remarkable promise for making flexible electronics, however they are not stretchable and they still remain in the first stage of development with unknown reliability [6,11]. Conductive liquid materials show some promises for making stretchable and flexible systems but like other new materials, the reliability of manufactured devices is an issue.

On the other hand, inorganic materials have been used in electronic devices for decades and embedding inorganic materials in soft materials is a promising approach for making stretchable and flexible structures, however delamination of rigid materials from soft materials has inhibited the abilities to use this approach [45]. In this direction, using sub-micron layers of inorganic materials (nanomaterial) in the structure of an electronic device has shown promise for making flexible and stretchable electronics [46] as this thinning (thickness < 1 μm) allows rigid materials to have a higher degree of flexibility [47]. However, thinning the devices causes significant challenges for integrating silicon-based electronics (i.e., CMOS) as the interconnect stack for these is over 1μm in thickness and can often be over 10 μm thick. Along with the thickness of these silicon based electronics is the mechanical response if they are embedded in flexible materials. In this composite system, one major challenge is the significant mismatch

in mechanical properties of silicon-based electronics (Young's modulus, E = 170 GPa) and the human body (Young's modulus, E = 100 kPa); this mismatch causes difficulties in the attachment, stretching and functioning for wearable biomedical instruments [48]. In contrast to silicon-based electronics that are rigid and planar (fracture strain < 2%) [20,49,50], flexible and stretchable electronics can be bent, stretched and twisted (elongation at failure > 10 %) [51].

To address these challenges and take the advantage of CMOS chips in stretchable structures, a stretchable platform that allows us to employ "thick" electronic chips (thickness > 10 μm) into soft material is needed. This platform can be used for applications that integrate in biomedical applications on the skin where large deformation occurs.

1.3. Thesis statement and contributions

In this thesis, the feasibility of making stretchable and flexible wearable electronic systems through embedding thick inorganic materials into soft organic materials is explored. Towards this objective, a stretchable platform is designed, fabricated and tested.

In order to make stretchable electronics with a tremendous amount of functionality, we have investigated fundamentals in interfacing CMOS technology, which already has advanced functionality, with flexible materials. The goal is to prevent delamination occurring between electronic chips and soft materials, which is a major challenge in designing stretchable electronics with already highly functional CMOS systems. This delamination issue is addressed by engineering polymer layers around the electronic parts in order to gradually change material properties from a highly rigid material to a highly soft material.

To increase the effect of engineered layers on the delamination, a series of computational optimization using finite-element analysis was performed. Materials and dimensions of the engineered platform were subjected to this optimization.

To validate the design achievements, the design phase was followed by fabrication process of stretchable and flexible platform. Several samples of engineered platform and non-engineered structure using silicon chips and polymers were built. The samples were subjected to fixed-displacement tensile tests. In each test, the strain which caused delamination of layers was recorded.

Designing reliable interconnections between CMOS chips which increase the reliability of the whole system is another goal of this work. These interconnections must pass through several layers with different material properties. These interconnections are the most vulnerable part of the structure where passing the interfaces of the materials. In order to protect these interconnections from breaking, two approaches for interface modification were used. The behavior of wires on these modified interfaces were examined and the results were compared.

A safe region area, a region with low strain, in a stretchable system was introduced through interface modification approach, and a LED mimicking a CMOS chip was embedded in the safe area of structure. The behavior of the LED under strain was studied.

The methodology of this work, including design principals and quantification of delamination in fracture mechanics, are presented in Chapter 2. In Chapter 3, design parameters are introduced and fabrication process of engineered platform is discussed. In Chapter 4, the parameters optimizations and delamination test results are provided and compared. Chapter 5 discusses the interface modification approaches including design and fabrication of interconnections between CMOS islands and design, fabrication and test of built-in LEDs in a wearable platform.

Chapter 2

2. Methodology

In this section, the methodology for design, experiments and computational modeling of engineered platform is discussed.

2.1. Stretchable and flexible platform

As discussed in the previous chapter, several approaches exist for making stretchable and flexible electronics. Among these approaches, exploiting inorganic semiconductors in the structure of stretchable electronics is the most promising approach to gain stretchability and reliability at once. However, there are some challenges in implementation of this approach which should be addressed. One of these challenges is delamination of soft material from stiff material under strain conditions. As the thickness of electronic device goes up, the delamination challenge will increase. A thin layer of rigid material can be used as stretchable component when it is patterned in a meandering shape [51–55]. To address both challenges (delamination and device thickness) we designed a platform with capability of employing thick electronic devices. This platform can survive under high strain conditions without delamination. The delamination issue is caused by mismatch in properties of the soft and rigid materials while the bounding adhesion of these materials is low. When the structure is under load condition, in

contrast to the rigid material, the soft material wants to expand. So, the soft-rigid interface experiences high amount of strain and stress. This stress at the interfaces breaks weak van der Waals link between soft materials (polymers) and rigid materials.

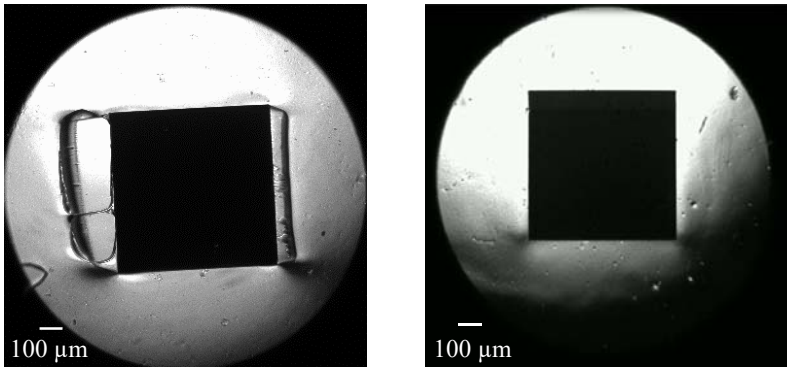

Figure 2.1. Stretchable integrated system under experimental strain examining the **(a)** delamination of the polymer from the silicon chip under 20% strain for a sample without the intermediate material and **(b)** the lack of delamination of our two-polymer approach even up to 140% strain.

Eliminating delamination between the soft and rigid material (i.e. CMOS components) is required for designing stretchable systems. To quantify the delamination characteristic of the interface, the 'energy release rate', G from the field of fracture mechanics [56], in units of J/m^2 is needed, which guides the fabrication of these integrated flexible electronic systems. The energy introduced to an initiated crack causing it to increase in size must be balanced by the amount of energy lost due to the formation of new surfaces and other dissipative processes, such as plasticity. When the energy release rate equals a critical value, the fracture energy denoted as Γ, the crack size increases (G concept is discussed is next section in more detail). The risk of delamination at the interface of a soft material and rigid material is significant and this risk increases when the system is subjected to mechanical strain (i.e., stretched). Therefore, if the structure has high stress at the interface between the two materials, delamination occurs at this interface (Figure 2.1a). To address this challenge, the amount of strain and strain energy

in the soft material at the interface needs to be minimized to prevent delamination. This was accomplished using a combined computational and experimental approach where we created a material gradient such that the mechanical stiffness properties between the soft and rigid materials were changed gradually, creating an intermediate gradient (Figure 2.1b and Figure 2.2). For simplicity, the material gradient is assumed as a step function (Figure 2.2), however in reality the material gradient is not a pure step function because of the material diffusion through another material [57]. Adding a single intermediate soft material has a significant effect in reducing delamination while allowing for the addition of small rigid components, as in functional CMOS systems.

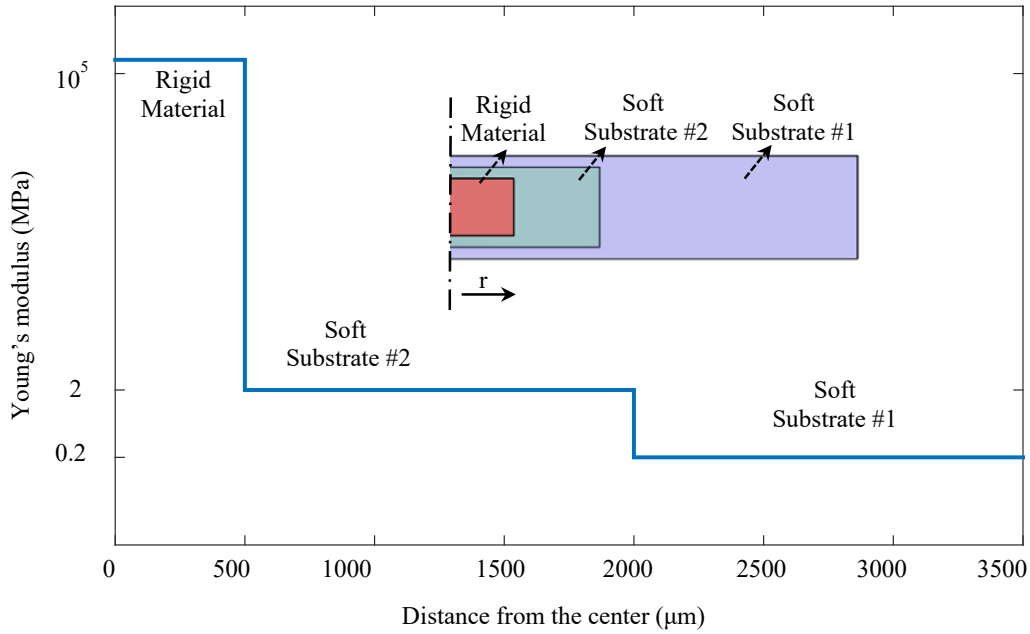

Figure 2.2. Schematic of the material gradient approach for one intermediate material between hard silicon and soft substrate materials, with Young's modulus of the materials based on location in the system along the length.

In our approach, the substrate, which surrounds the electric device, is made of two soft polymers with different Young's modulus, E_1 and E_2 ($E_2 > E_1$). The stiffer polymer (Young's Modulus E_2) is in contact with the silicon while the softer material (Young's Modulus E_1) occupies the outer domain (Figure 2.2). When the composite substrate is strained, the outer

polymer has a higher strain when compared to the intermediate inner polymer. Using this approach will allow us to make highly stretchable electronic devices (Figure 2.3). To analyze this we will discuss the design, fabrication and test process of wearable electronic systems in the next chapter.

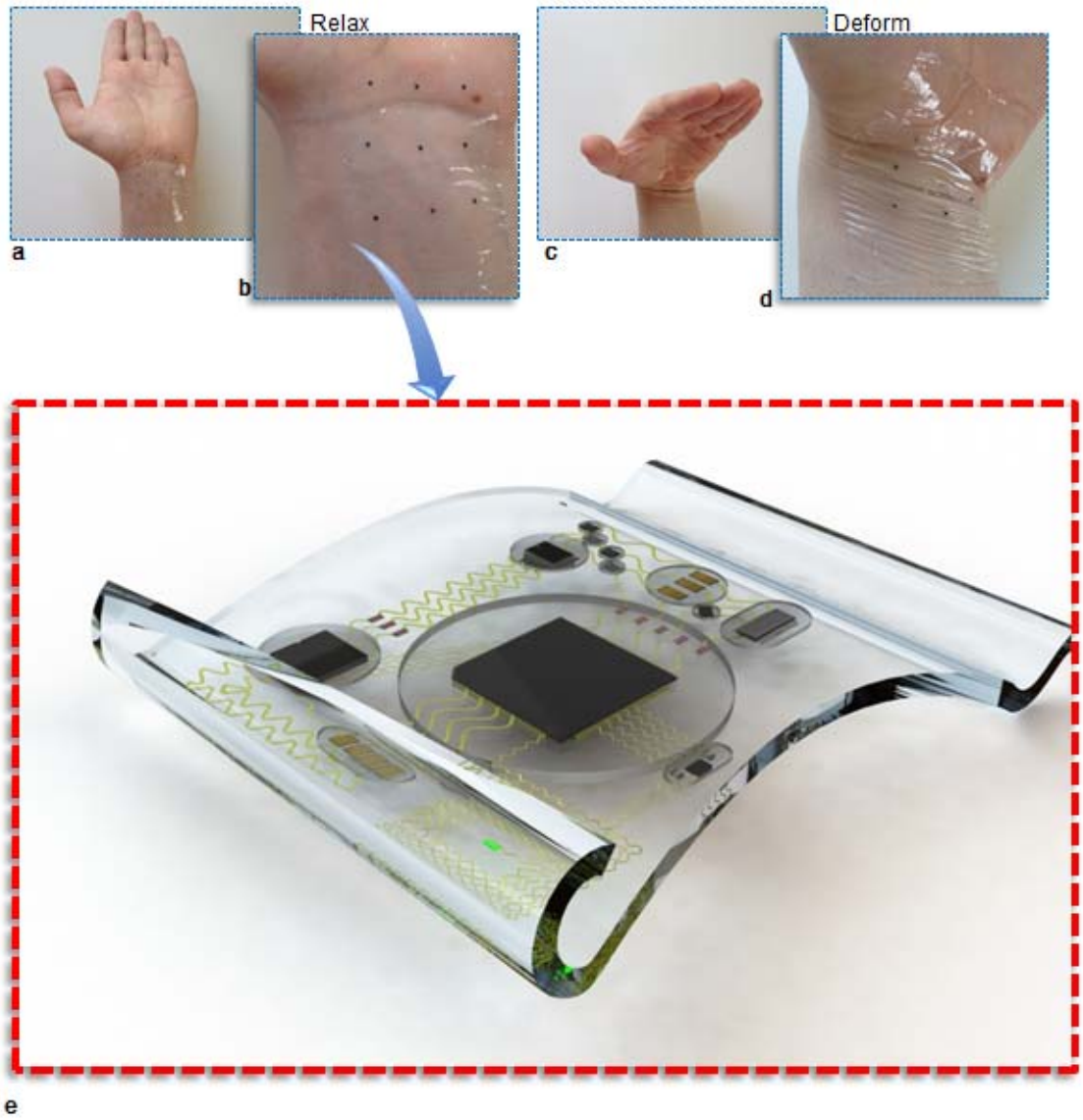

Figure 2.3. **Material gradients in stretchable electronics for integrated functionality. a, b, c, d,** Embedded rigid silicon chips similar to CMOS material in a PDMS stretchable system under controlled strain conditions with no strain **(a)** and a magnified image **(b)** and then under highly strained conditions **(c)** and a magnified image **(d)**. **e,** Schematic concept for embedded, distributed, and interconnected electronics chips in stretchable systems.

2.2. Energy release rate

The crack energy release rate quantifies the potential energy change rate of a cracked elastic solid when the crack propagates [58]. An elastic cantilever beam, Figure 2.4, is subjected to a load [59]. Assume the cantilever beam contains a crack with length of *a,* and crack area, A. Energy balance for this case when crack does not extend can be noted as:

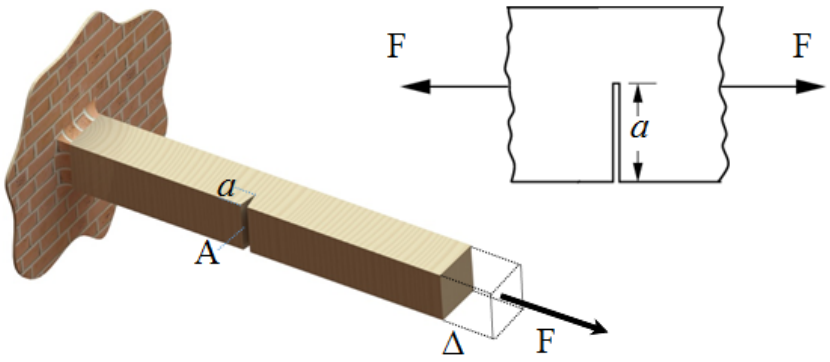

Figure 2.4. Schematic of a cantilever beam with a crack.

$$U - W = 0 \qquad Eq.(2-1)$$

where U is the elastic energy contained in the beam and W is the work performed by the external force. When the crack extends the energy balance becomes:

$$\frac{dU}{dA} - \frac{dW}{dA} + \frac{dQ}{dA} = 0 \qquad Eq.(2-2)$$

where $\frac{dU}{dA}$ shows change in the strain energy, $\frac{dW}{dA}$ is the performed work on the body as the crack extends and $\frac{dQ}{dA}$ is the required energy to tear apart the material to form dA. The above equation can also be written as:

$$G = \frac{dQ}{dA} = \frac{dW}{dA} - \frac{dU}{dA} = \frac{d}{dA}(W - U) \qquad Eq.(2-3)$$

where G is the energy release rate. This equation for a beam with constant thickness of B becomes:

$$G = \frac{1}{B}\left(\frac{dW}{da} - \frac{dU}{da}\right) \qquad Eq.(2-4)$$

Let F represent the magnitude of the applied load, and Δ the displacement. When the crack increases in size by an amount of da, the displacement, Δ, will increase by an amount $d\Delta$, so the load does work $Fd\Delta$ to the body and energy release rate becomes:

$$G = \frac{1}{B}\left(\frac{Fd\Delta}{da} - \frac{dU}{da}\right) \qquad Eq.(2-5)$$

The energy release rate can be calculated in two conditions; fixed displacement condition in which Δ is held constant and fixed load condition in which F is held constant. In this thesis, we considered fixed displacement for both theoretical and experimental G extractions. For this condition, $\frac{d\Delta}{da} = 0$ and by substituting this term in the last equation:

$$G = -\frac{1}{B}\left(\frac{dU}{da}\right) \qquad Eq.(2-6)$$

The crack propagation involves energy dissipation regardless of the applied load conditions. To tear apart material, a small amount of energy is required. Also, there are a complex process zone at the tip of crack that requires energy dissipation like plastic zone and chemical reaction zone (Figure 2.5). The energy rate dissipation will stay at a constant rate if the process zones remains identical while the crack propagates. The amount of this energy dissipation can be measured experimentally [59]. This value is known as critical energy release rate, Γ, and is a property of the material. The crack size can only increase if the energy release rate exceeds the critical value [58]:

$$G \geq \Gamma \qquad Eq.(2-7)$$

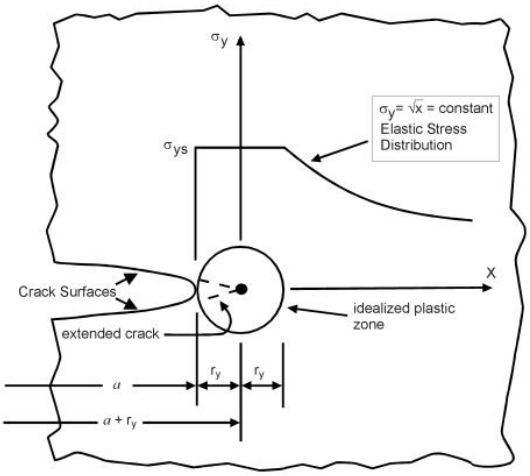

Figure 2.5. Crack propagation plastic zone Small-Scale Yield Model [60]

2.3. Extracting G from numerical Models

Energy release rate can be extracted from numerical models in different ways. Some of these methods are; Fundamental definition of *G*, local stress fitting, local displacement fitting, virtual crack closure technique (VCCT) and *J* integral [61–63]. In this work, "fundamental definition of *G*" is used for energy release rate calculation. This approach is simple and accurate since the basic *G* formula (Eq. 2-8) without any simplifications and approximation is used in energy release rate extraction.

$$G = \frac{1}{B}\lim_{\Delta a \to \infty}\left(\frac{1}{\Delta a}(\Delta W - \Delta U)\right) \qquad Eq.(2-8)$$

where ΔW is the change in work, ΔU is the change in strain energy, B is the film thickness and Δa is the crack length.

In order to calculate *G*, we need to first identify the interfaces where delamination is predicted or observed. The delamination typically happens at sharp edges and corners or at regions with high strains. Strain analysis of the model can help to find these regions.

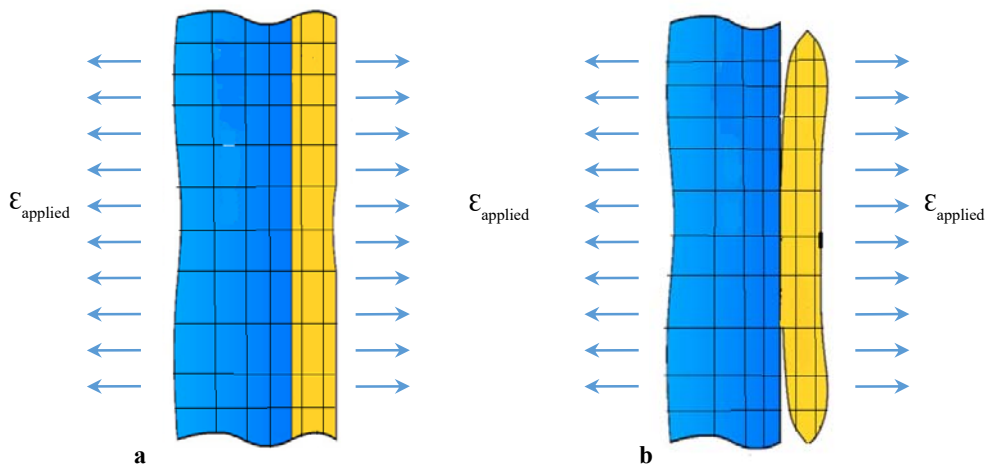

Figure 2.6. Extracting energy release rate from numerical models **(a)** before crack propagation and **(b)** after crack propagation.

After identifying the delamination regions, two strain analysis, one with full bonding layers (Figure 2.6a) and the other with a substantial delamination between layers (Figure 2.6b) are needed. For each case, the strain energy for the whole model is calculated. The average energy release rate for delamination can be extracted by taking the difference between the strain energies and work terms in the delaminated vs. fully bonded cases and divided by delamination area. The "work" term in *G* equation is zero if the strain is applied under strict fixed displacement conditions. By changing geometry, materials and applied strains, we can see how much this quantity is changed, and that can be the fracture mechanics-based design metric.

Chapter 3

3. Stretchable and flexible platform: Design, fabrication and test

In this chapter the platform design is discussed in more details. The effect of some parameters on energy release rate is investigated. The general idea of the platform design is mentioned in the previous chapter. In this platform the rigid component is surrounded by several polymer layers. In this chapter the simplest platform structure which has two polymer layers is studied (Figure 3.1). As it can be seen in Figure 3.1b the design parameters are; electronic chip thickness, h_3, intermediate layer thickness, h_2, primary layer thickness, h_1, electronic chip Young's modulus, E_3, intermediate layer Young's modulus, E_2, primary layer Young's modulus, E_1, electronic chip length, L_3, intermediate layer length, L_2, primary layer length, L_1, period of electronic chips, S, and intermediate layer shape. The material properties effect (Young's modulus) on delamination of layers is discussed in this chapter and in the next chapter the dimensions effect will be mentioned.

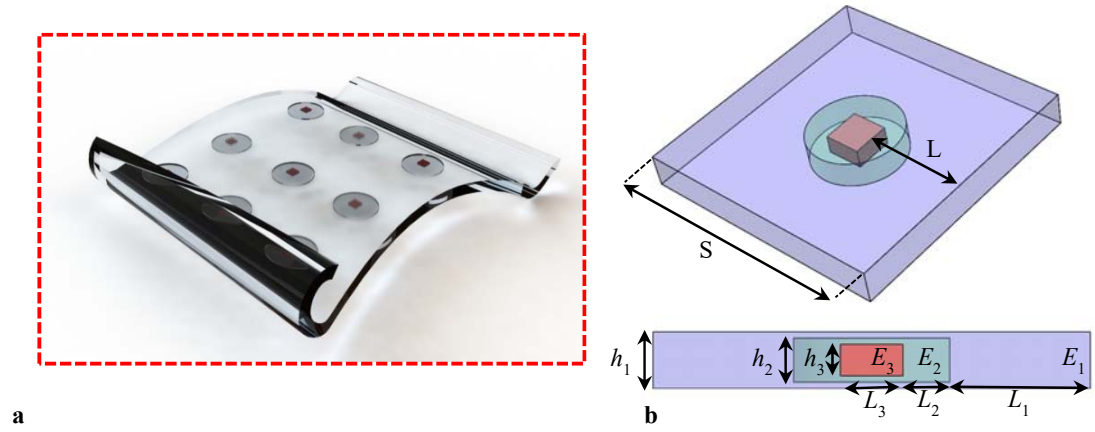

Figure 3.1. Material gradients for integrated functionality in stretchable electronics. a, Schematic concept for embedded and distributed electronics chips in stretchable systems. **b,** Schematic of the material gradient approach for one intermediate material between the hard silicon and soft substrate material

3.1. Materials Effect

The Young's modulus of the intermediate material, E_2, which is fabricated adjacent to the primary soft substrate material, E_1, plays an important role in minimizing the delamination in the stretchable and flexible system. Calculation of the energy release rate for interfaces with different materials with different Young's modulus along with stress and strain analysis of the structure will provide us comprehensive perspective for structure design.

3.1.1. Energy release rate analysis

To analyze Young's modulus role on delamination, we examined the factor (E_2/E_1) by calculating the energy release rates using Finite Element Analysis focusing on two arbitrary conditions E_2/E_1=10 and E_2/E_1=100 while also controlling the length of the intermediate material, L_2, with the total length of the soft material, $L= L_1 + L_2$ being held constant. External strain as a boundary condition is held constant at 5% for all cases. The system having the higher Young's modulus ratio has the lower energy release rate for all values of L_2 (Figure 3.2). The energy release rate characteristic rises with external strain, the system with the higher Young's modulus ratio would result in a larger safe region under high strains. Importantly, for any case where an intermediate material is utilized, the energy release rate is lower when compared to

just a single soft material having either Young's modulus E_1 or E_2. The energy release rate values for additional ratios are provided in Figure 3.3**.** As the ratio increases the energy release rate approaches lower value and consequently lower risk of delamination at interfaces can be achieved.

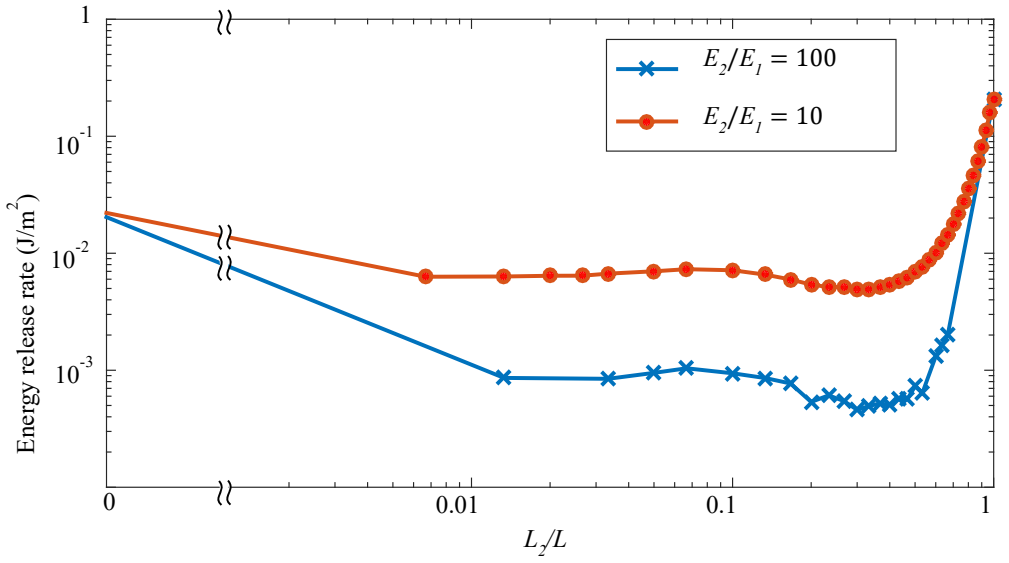

Figure 3.2. Young's modulus effect on energy release rate under 5% strain.

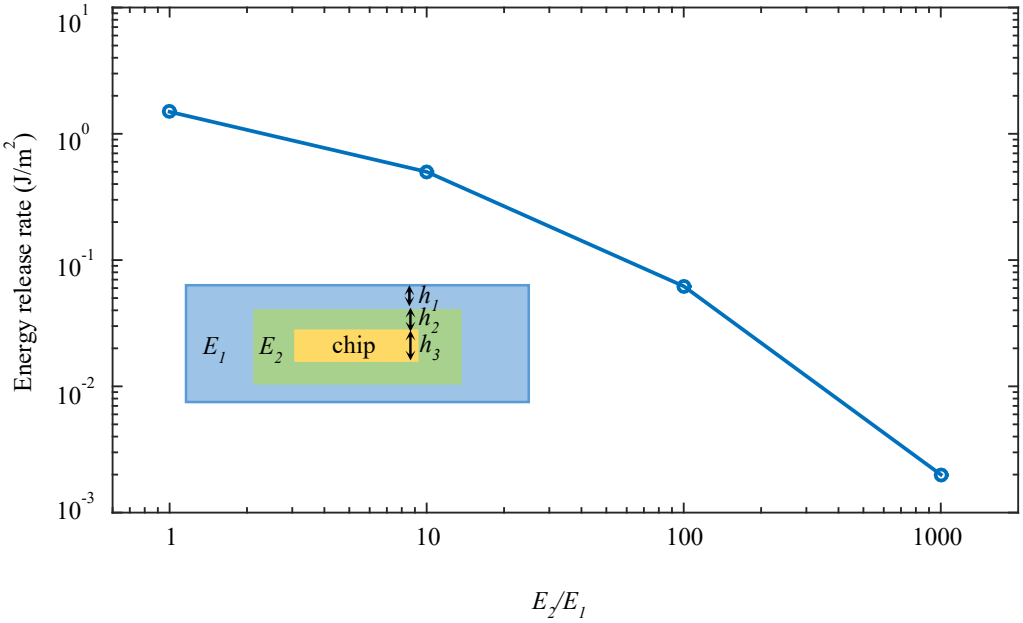

Figure 3.3. Energy release rate of silicon-PDMS interface debonding as function of E_2/E_1. ($h_1/h_2 = 1$, $L_2/L = 0.15$, $\varepsilon_{applied} = 20\%$)

3.1.2. Maximum principal elastic strain and stress analysis

A finite-element analysis (FEA, ANSYS) model was developed to calculate the maximum principal elastic strain. Figure 3.4a and Figure 3.4b show the maximum principal elastic strain for two structures without and with the engineered substrate, respectively. The graphs indicate the amount of strain along the top surface of the electronic device with the length of the intermediate soft material measured from the silicon interface being L_2, and the length of the primary soft material being L_1. The strain at the interface between the silicon and the intermediate soft material in the engineered substrate is approximately six times smaller than in the substrate having only a primary soft material. In other words, the intermediate material experiences approximately 250% lower strain compared to the single soft material substrate shown in Figure 3.4a. This lower strain region at the silicon interface reduces the delamination between the electronic part and the soft material. In this case, the higher strain occurs at the interface between the primary and intermediate soft materials. This region is likely the most susceptible region to delamination. If two materials with strong bonding ability are used, the delamination would occur at a higher strain at this interface. Finding two soft elastomeric materials with strong bonding is accomplished experimentally though using Polydimethylsiloxane (PDMS, Sylgard 184 Dow Corning) with different mix ratio.

The maximum principal stress was calculated for the structure without (Figure 3.5a) and with (Figure 3.5b) the engineered substrate. There is a stress concentration at the PDMS-PDMS interface in the structure with the engineered substrate. This interface is the most vulnerable to delamination, however this interface form strong covalent bond between polymer-polymer materials and because of that the delamination for this interface happens at higher level. The strain failure threshold for all interfaces of the structures are studied in the chapter 4.

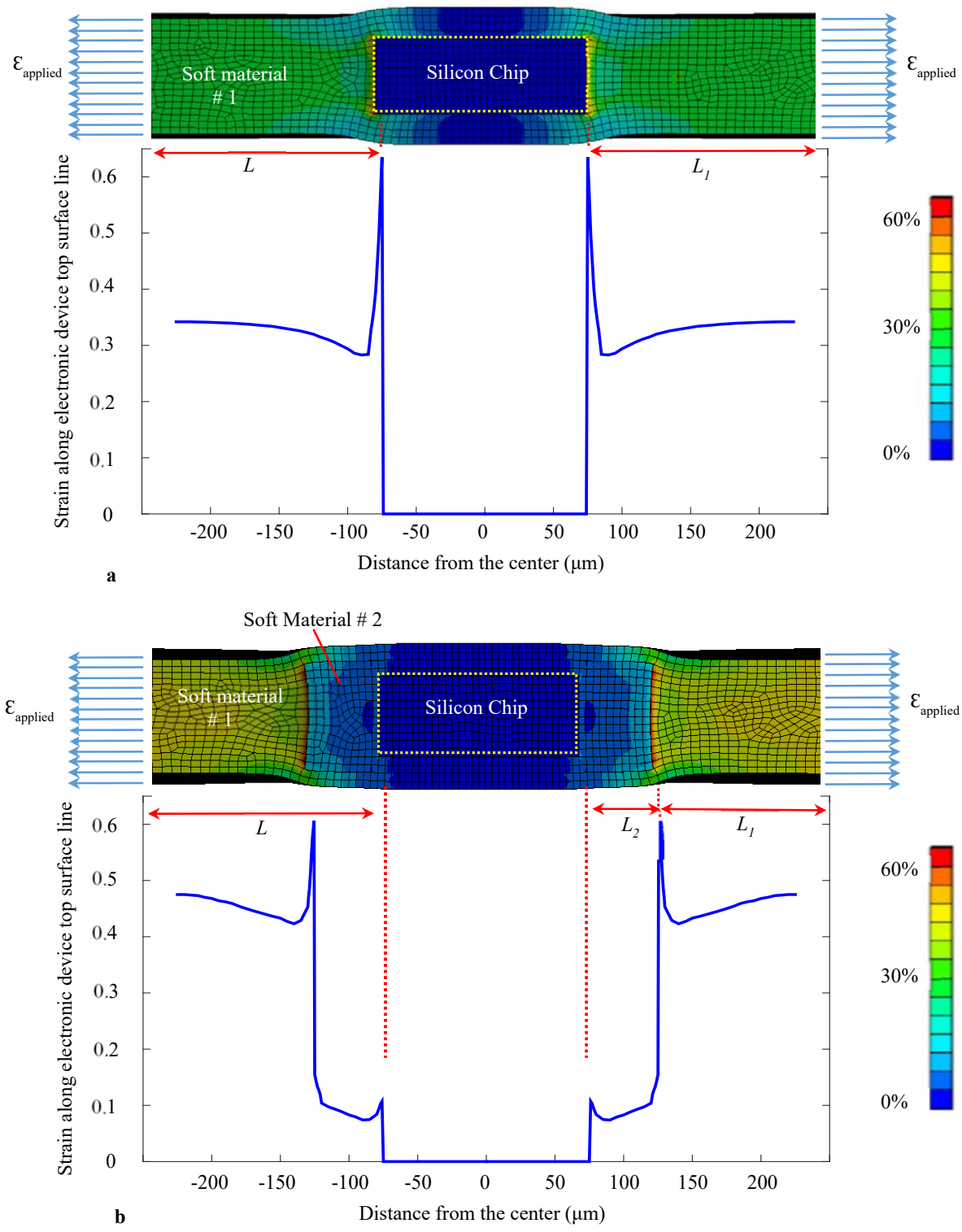

Figure 3.4. Finite-element modeling of strain associated with the two material stretchable system. Maximum principal elastic strain analysis for **(a)** an embedded silicon chip in a soft material without intermediate material ($E_1 = 0.26$ *MPa*, $L_2 = 0$, $L = 175$ μm, $\varepsilon_{applied} = 50\%$, elastic substrate thickness = 90 μm) and **(b)** embedded silicon chip in the two-material gradient stretchable system $E_2/E_1 = 7.6$, $L_2 = 50$ μm, $L = 175$ μm, $\varepsilon_{applied} = 50\%$, elastic substrate thickness = 90 μm).

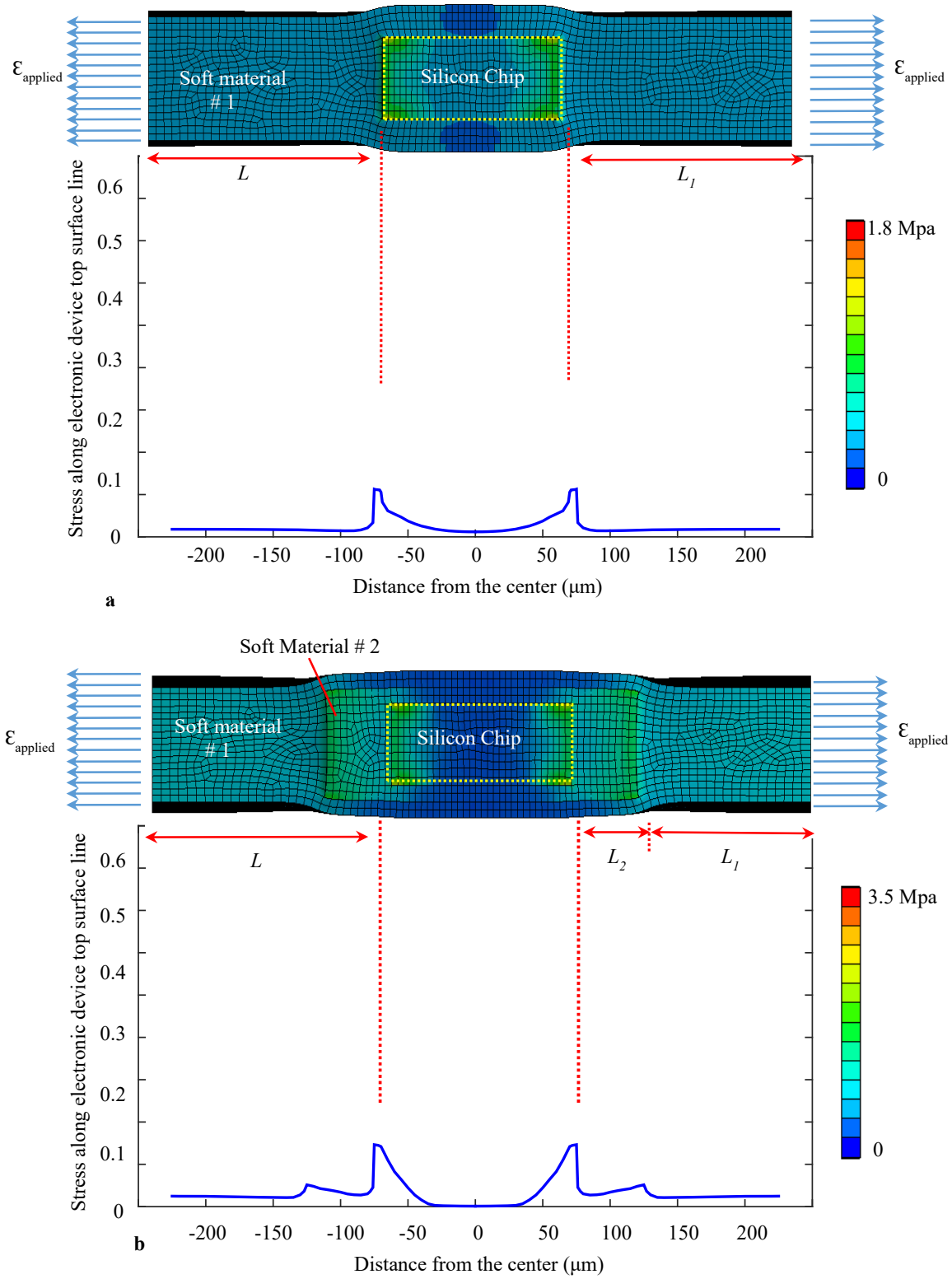

Figure 3.5. Finite-element modeling of stress associated with the two material stretchable system. Maximum principal stress analysis for **(a)** an embedded silicon chip in a soft material without intermediate material (E_1 = *0.26 MPa*, L_2 = 0, L = 175 μm, $\varepsilon_{applied}$ = 50%, elastic substrate thickness = 90 μm) and **(b)** embedded silicon chip in the two-material gradient stretchable system E_2/E_1 = 7.6, L_2 = 50 μm, L = 175 μm, $\varepsilon_{applied}$ = 50%, elastic substrate thickness = 90 μm).

3.2. Platform Fabrication

In order to validate the intermediate soft material approach, three types of structures are designed and fabricated. In all of these structures PDMS with different mixing ratio are used as soft materials. Also, 1mm×1mm×50 μm silicon chips are used as surrogate electronic devices (Figure 3.7 and Figure 3.8). PDMS is widely used in micro fabrication and flexible electronics [64–66]. Using PDMS with different ratios of base and curing agent for the primary and intermediate materials allow us to select the desired Young's modulus values, which also exhibit strong bonding at their interface.

The Si-PDMS flexible substrate was created using PDMS with mix ratio of (5:1) and (20:1). PDMS Young's modulus ratio of 5:1, E= 1.98 MPa, 20:1, E= 0.26 MPa, were measured using an Instron 5940 system (Appendix B, Figure B1 and Figure B2). The stretchable substrates correspond to the circled point in Figure 3.2 were made by embedding a 1 mm × 1 mm × 50 μm Si chip (Appendix A, Figure A1) (E = 170 GPa) into a 90 μm-thick PDMS sheet. The PDMS ratio for structure #1 is (5:1), for structure #2 is (20:1), and structure #3 is made by a combination of PDMS (5:1) as the intermediate soft material and PDMS (20:1) as the primary soft material (Figure 3.8). To accomplish this, the Si chip (Appendix C, thin si chips fabrication process) was coated with a 70 μm thick PDMS (5:1) layer and then cured at 80 ºC for 4 hr. This composite structure was then cut into a 1 mm diameter circle and subsequently embedded into a 90 μm thick PDMS with the PDMS ratio of (20:1) followed by 4 hr. curing at 80 ºC. The softer material (PDMS (20:1)) covered the intermediate structure (Appendix A, Figure A1).

3.3. Platform analysis and delamination test

The fabricated structures in the previous section were subjected to analysis and test. For each sample, tensile test and finite-element analysis were performed. The results from both experimental and computational analysis were compared.

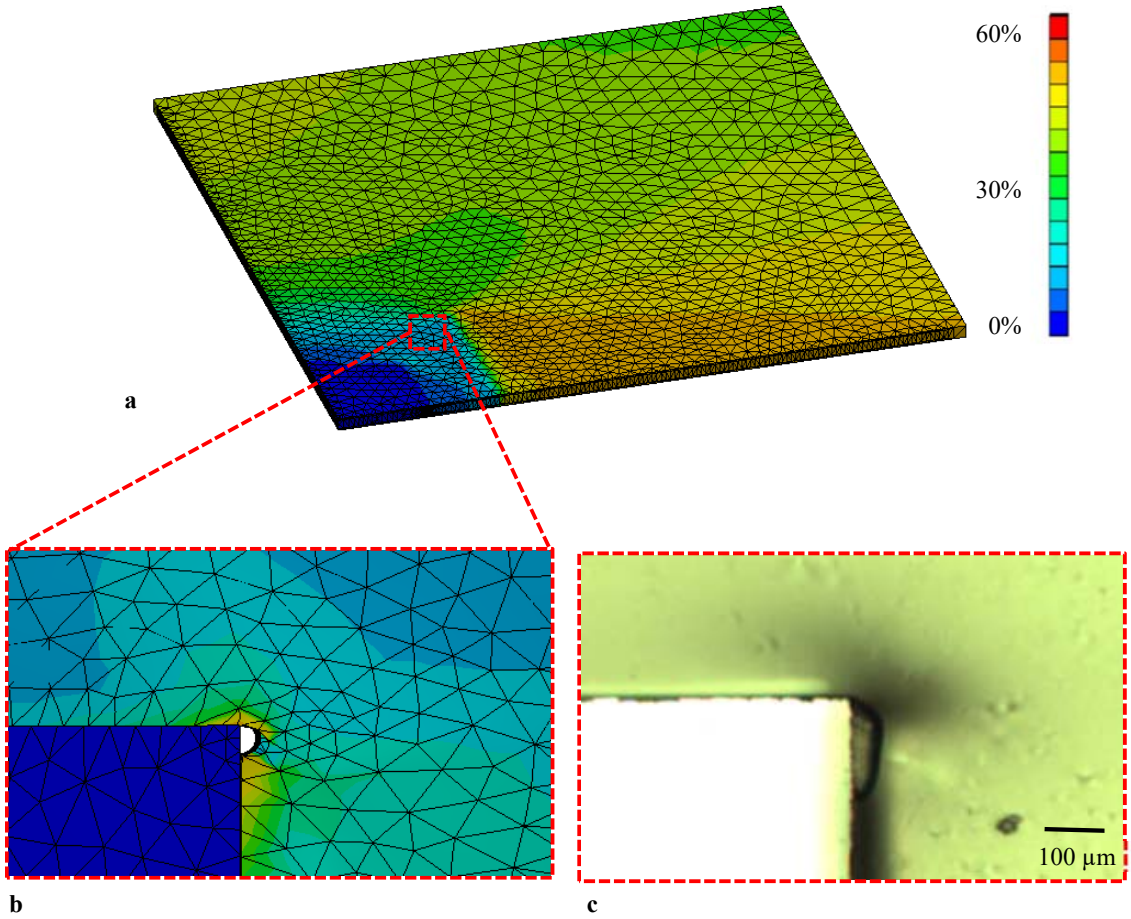

Figure 3.6. Finite-element modeling of strain associated with an embedded silicon chip in a soft material without intermediate material (E_1 = 0.26 MPa, L_2 = 0, L = 175 µm, $\varepsilon_{applied}$ = 50%, elastic substrate thickness = 90 µm). a, Maximum principal elastic strain analysis. **b,** Crack initiation in the FEA model. **c,** Delamination at the edges of a rigid and soft material interface without a material gradient under 20% strain**.**

3.3.1. Energy release rate calculation

To examine the delamination at the boundary, we examine the energy release rate. The energy release rate is determined using a finite-element analysis with a symmetric quarter model of the entire substrate (Figure 3.6a). A fine mesh is placed on an initial 10-µm wide separation (i.e., the crack) located at the interface between the sidewall of the Si chip and the surrounding PDMS. The crack with the worst-case stress is at the corner of the chip (Figure 3.6b). The energy release rate is determined by subtracting the strain energy before and after crack growth, while dividing by the crack area. Mesh refinements are used to verify numerical convergence. In the ANSYS simulations, linear isotropic materials with tetrahedron

SOLID187 elements were used to calculate strain fields and energy release rates. The energy release rate for structure #3 is approximately two times lower than the next best structure #2 (Table 3.1). When the energy release rate exceeds the critical value, the crack propagates and PDMS delaminates from the Si chips (Figure 3.6c). Since, the energy release rate for structure #3 is lower, the risk of delamination at the interface of Si-PDMS is very low and the delamination for this interface does not occur at these low strains.

Table 3.1 Energy release rate results through our ANSYS analysis for 3 material gradient stretchable Si-PDMS systems (a =10 μm, $E_{PDMS(20:1)}$=0.26 MPa, $E_{PDMS(5:1)}$=1.98 MPa, ε=20%, Si (1mm×1mm×50 μm))

Sample	Primary Material	Intermediate Material	Energy release rate
#1	PDMS (5:1), $L = L_2 = 3$ mm	none	10.99 J/m^2
#2	PDMS (20:1), $L = L_1 = 3$ mm	none	1.493 J/m^2
#3	PDMS (20:1), $L_1 = 2$ mm	PDMS (5:1), $L_2 = 1$ mm	0.689 J/m^2

3.3.2. Platform delamination test

To compare experimental response to our FEA predictions, we use tensile tests for all three structure types. This approach also allows us to determine the strain failure. Fixed displacement is applied at the edges of the substrates and the strain loading is applied as a series of smaller incremental step functions. The system is strained at low strain rates (0.001 s^{-1}) for mimicking steady-state and the strain failure is examined through optical microscopy imaging. For example, the delamination for structure # 1 occurs at 20% strain indicated by the crack and growth (Figure 3.7a). The strain for delamination for structure # 2 is higher than structure # 1, which occurs at 30% strain (Figure 3.7b); this is supported by the FEA predictions (Table 3.1). For structure #3 (Figure 3.8), the Si-PDMS (5:1) interface showed significant improvements for resisting delamination as crack growth does not occur until 140% strain. Comparing this strain to delamination to structure #1 (with the Si-PDMS(5:1) interface) a 5.5 times increase in

the strain failure threshold is found. At even high strains, the high stress leads to delamination at the PDMS (20:1)-PDMS (5:1) interface not at Si-PDMS (5:1) interface.

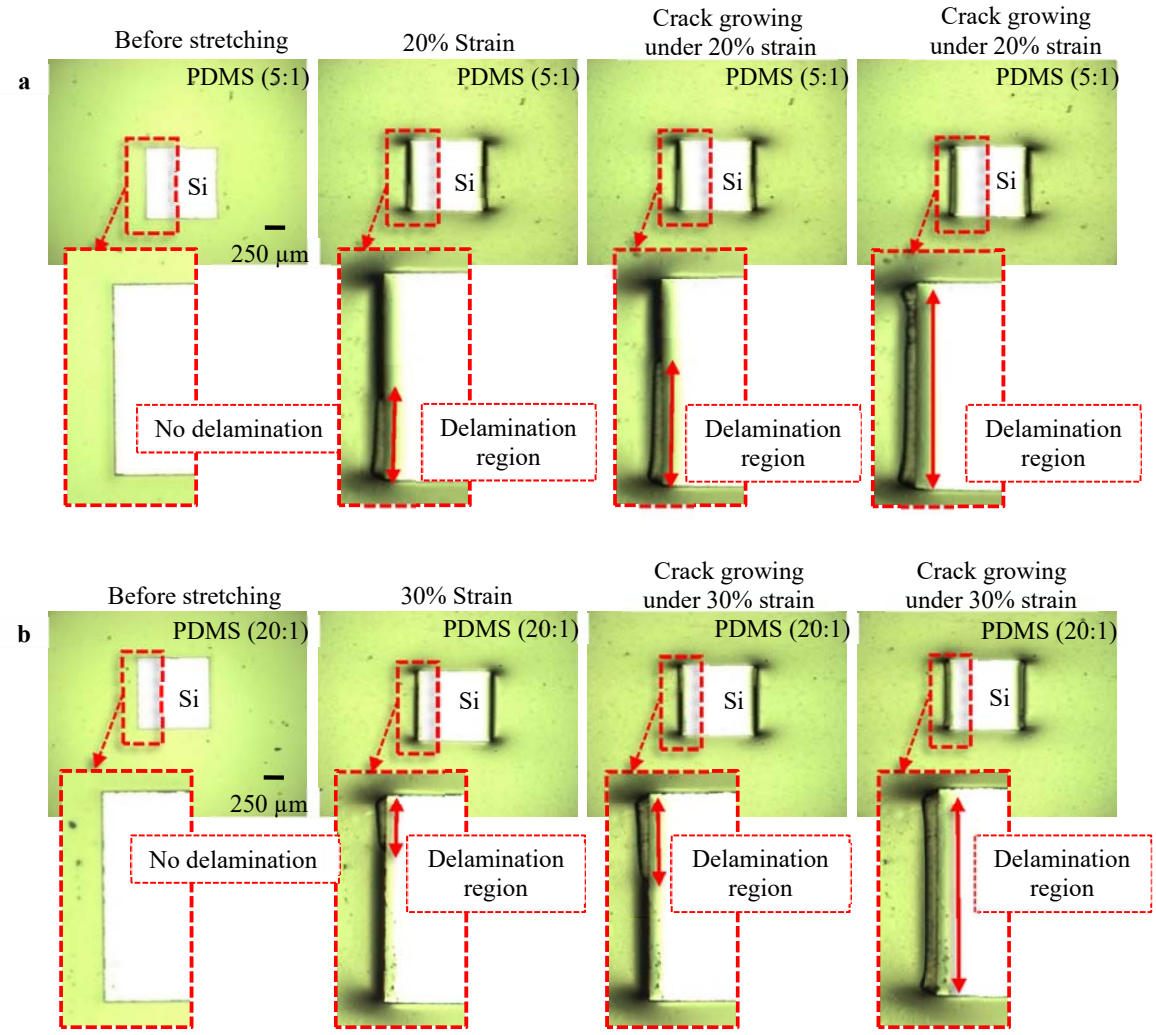

Figure 3.7. Experimental results of delamination at the interface of the silicon and PDMS interface without intermediate material. a, The silicon-PDMS (5:1) stretchable substrate, sample #1, when placed under a ramped strain test and fails at 20% strain and displays a subsequent increase in the delamination area. **b,** The Si-PDMS (20:1) stretchable substrate, sample #2, is similarly tested and fails at 30% strain.

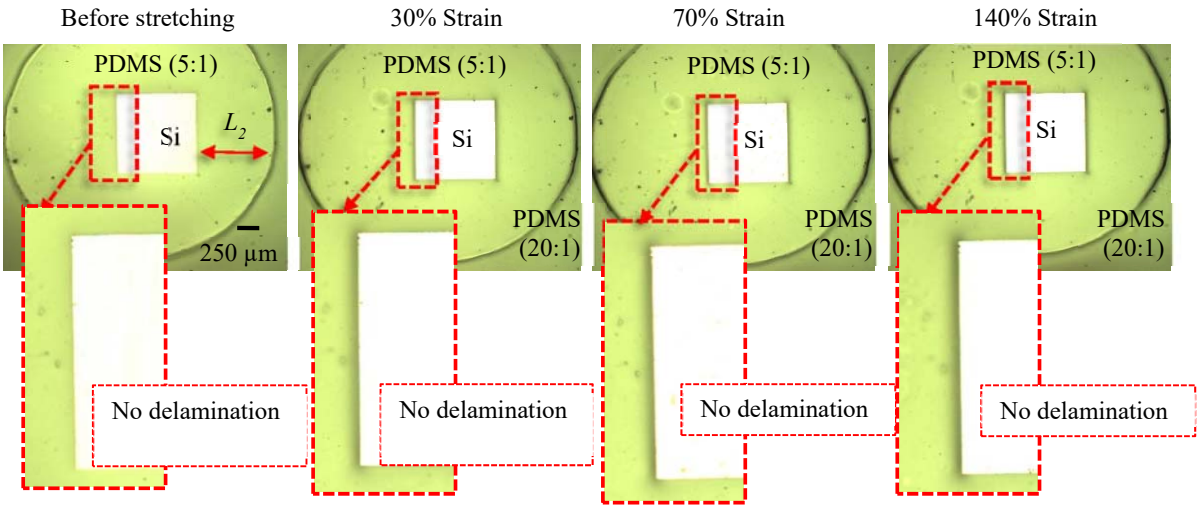

Figure 3.8. The silicon-PDMS stretchable substrate, sample #3, with the intermediate soft material (L_2 = 1 mm) withstands a significantly higher strain before failure. Delamination does not occur under this ramped strain test at the silicon-PDMS interface up to 140%. At 140% strain, failure occurs at the PDMS-PDMS interface.

Chapter 4

4. Stretchable and flexible platform: Optimization

As discussed in the previous chapter, there are several design parameters which should be considered in the design of stretchable and flexible electronics platform, including geometry and material properties. Investigating the best characteristics of the primary-intermediate soft material platform would help decrease the risk of delamination at the PDMS-PDMS interface even further. In this chapter, the effect of geometry parameters on delamination and the strain failure threshold for interfaces using delamination test has been investigated.

4.1. Intermediate length effect

4.1.1. Intermediate length optimization

To minimize delamination risk, we analyzed our structure based on the ratio of the length of intermediate polymer (L_2) to the total substrate length ($L=L_1+L_2$). The energy release rates for different L_2/L ratio at the interface of silicon-PDMS (5:1) and at the interface of PDMS (5:1)-PDMS (20:1) are calculated; respective representative crack regions are shown in Figure 4.1a and Figure 4.2. The energy release rates at these interfaces are a function of crack length, a, Young's modulus of the PDMS materials, E_1 and E_2, the applied strain, ε, and the geometry of the components, L_1 and L_2:

$$G = f(a, E_i, L_i, h_i, \varepsilon) \quad i = 1{:}3 \qquad\qquad Eq.(4-1)$$

To determine the best characteristics, all parameters except L_2 are assumed to be fixed. The energy release rate increases with increasing applied strain (Figure 4.3). The energy release rate between the primary PDMS, the intermediate PDMS interface, and the Si to PDMS interface at 20% strain indicates that the PDMS-Si is two times higher than PDMS-PDMS (Figure 4.4 blue and red curves, respectively). In this graph, L_2/L=0 represents the substrate #1 case and L_2/L=1 represents the substrate #2 case. The energy release rate for substrate #2 (1.493 J/m^2) is approximately 7 times larger than the substrate #1 value of 10.99 J/m^2.

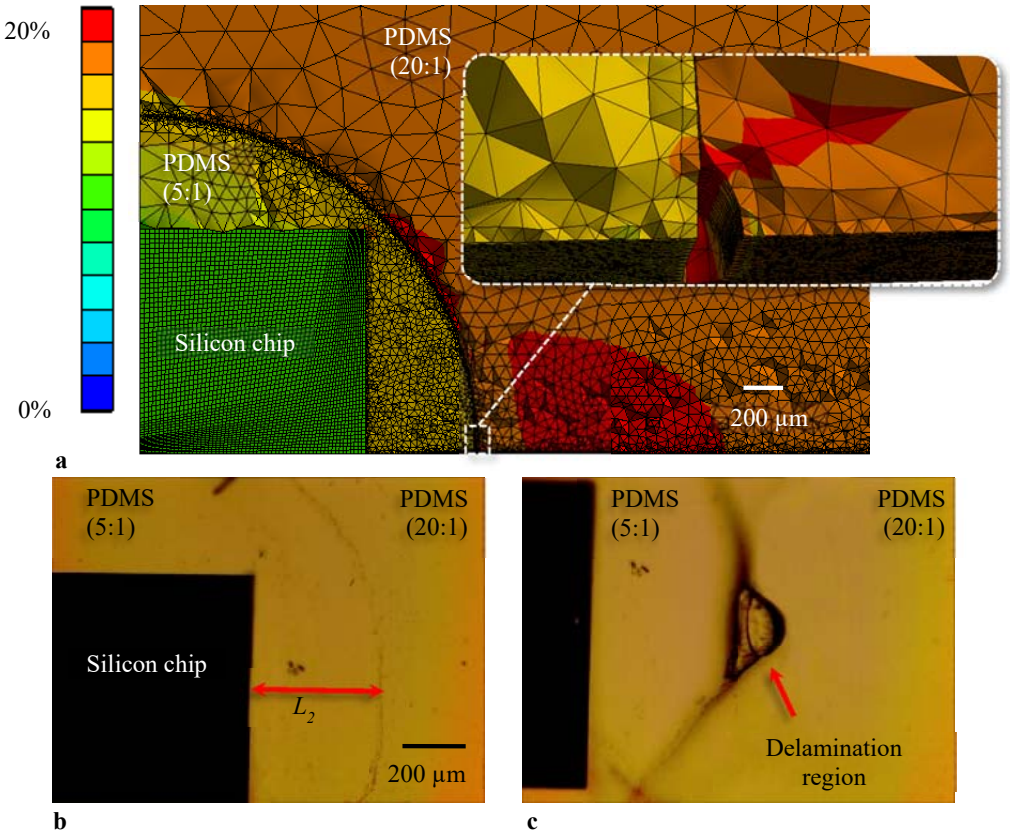

Figure 4.1. a, Maximum principal elastic strain analysis for structure #3, **(b)** which is then experimentally tested. **c,** initiation of the crack at interface of PDMS-PDMS.

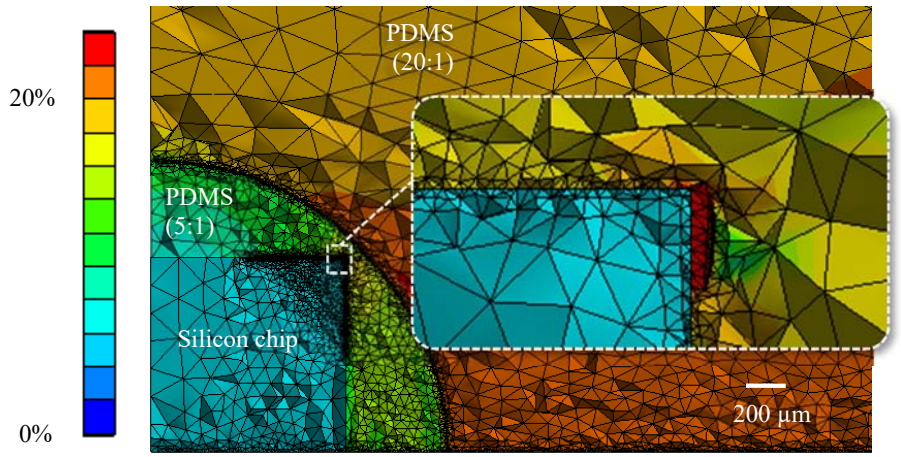

Figure 4.2. Maximum principal elastic strain analysis for structure #3, initiation of the crack at interface of silicon-PDMS.

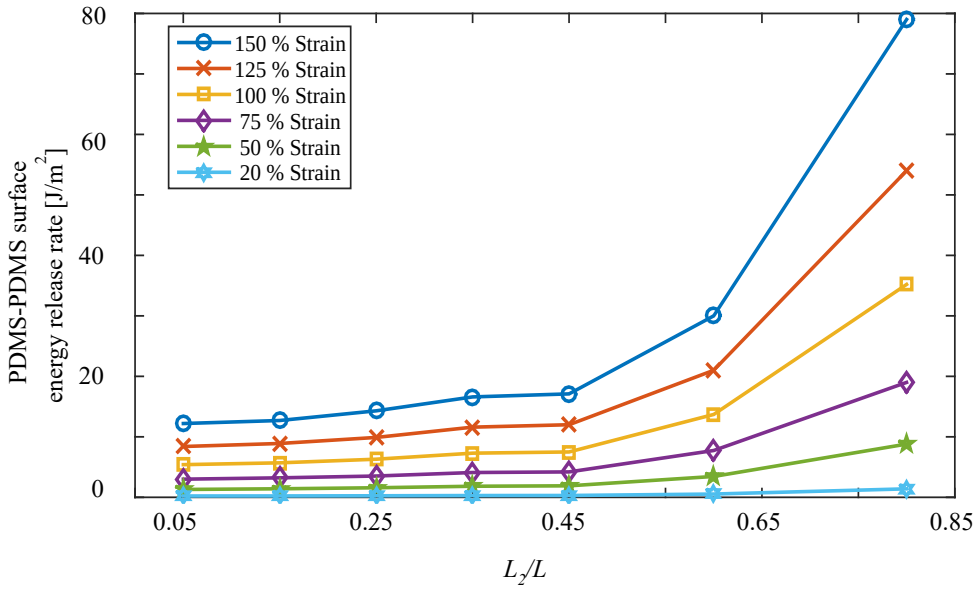

Figure 4.3. Determining the optimal geometry for the stretchable material gradient system. The energy release rate for the PDMS-PDMS interface, structure #3, (a =10 µm, $E_{PDMS(20:1)}$ = 0.26 MPa, $E_{PDMS(5:1)}$ = 1.98 MPa) under increasing strains.

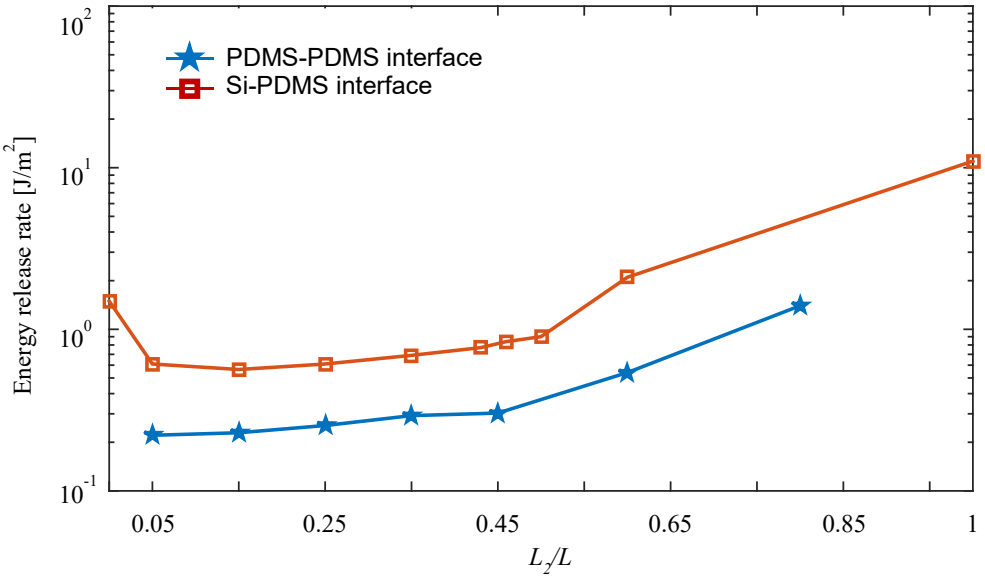

Figure 4.4. An energy release rate comparison between silicon-PDMS and PDMS-PDMS interfaces for structures with different L_2 and a strain of 20%.

4.1.2. Delamination strain test

For intermediate values of L_2/L, the energy release rate at the Si-PDMS interface decreases significantly. Due to the challenge of determining which interface (Si-PDMS or PDMS-PDMS) fails first due to different reported critical energy release rate value, Γ, for these materials [67], a delamination strain test is implemented for these interfaces. Tensile responses of the material gradient systems are examined on structures with different L_2/L (0.05, 0.15, 0.25, 0.35, 0.45 mm) and L=10 mm, while keeping the other dimensions, materials and loading conditions constant. These systems examine the strain level that causes delamination; for all cases the PDMS-PDMS interface fails first. The system with L_2/L = 0.05 had the highest failure strain of 140% (Figure 4.5; blue dots). The response of this structure during crack growth is shown in Figure 4.6 along with the failure strain value for the structures without intermediate material, L_2/L=0 and L_2/L=1, indicated by the red dots.

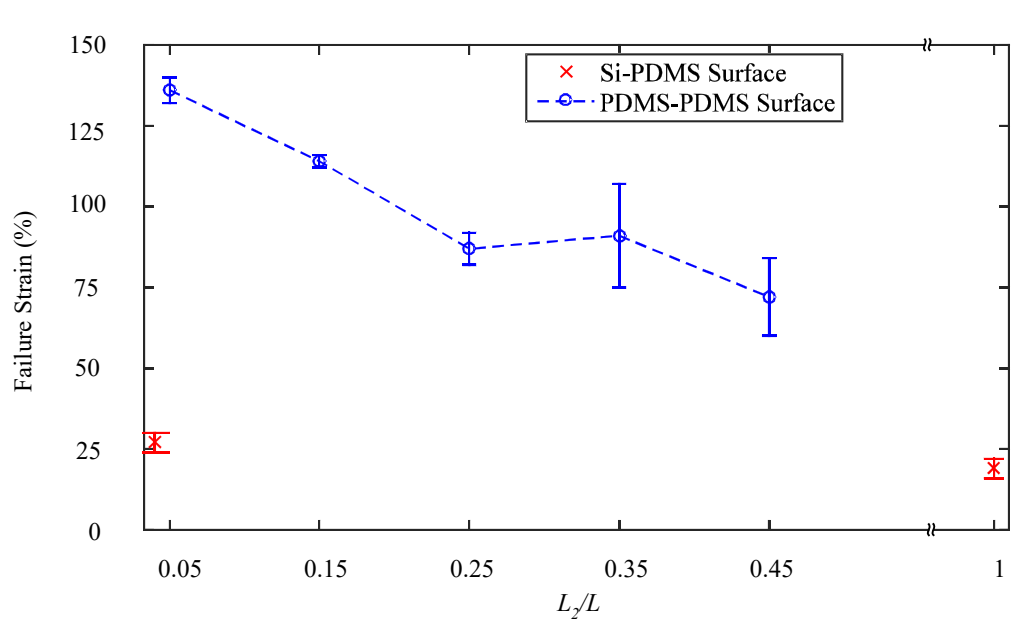

Figure 4.5. Delamination strain values for structures with different L_2 at the silicon-PDMS and PDMS-PDMS interfaces.

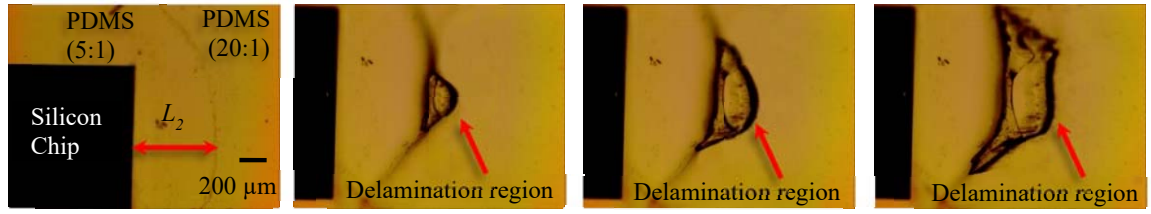

Figure 4.6 . Response of the material gradient substrate with L_2/L = 0.05 before and after applying strain up to 140%.

Investigators have reported values in the range of 0.05–0.4 J m^{-2} for the adhesion energy of Si–PDMS interfaces [68]. The work of adhesion for a PDMS–PDMS interface is reported in the range of 250−300 J m^{-2} [69].Therefore, the PDMS–PDMS bonding is stronger than Si–PDMS bonding by four orders of magnitude. While the Si–PDMS adhesion could possibly be enhanced through a geometric interlock design or through use of adhesion promoters, the presented method of moving the critical interface to the PDMS–PDMS interface enables exploitation of the natural adhesion between similar polymers.

4.1.3. Cyclic tensile test

A cyclic tensile test is a type of test in which a material, or object of interest is subjected to repeated tensile testing, instead of a single test cycle. The goal of such testing is to confirm that the structure will perform reliably, and to get an opportunity to subject it to simulations of many different real world conditions. The strain cycling performance of sample #3 up to 100 cycles under maximum 50% strain is studied. The strain is applied at the structure edges and the sample interfaces are observed using camera equipped microscope (Olympus MX-80) after 1, 10, 20, 30, 50, 70, 90 and 100 cycles (Figure 4.7). Delamination is not detected at either interface.

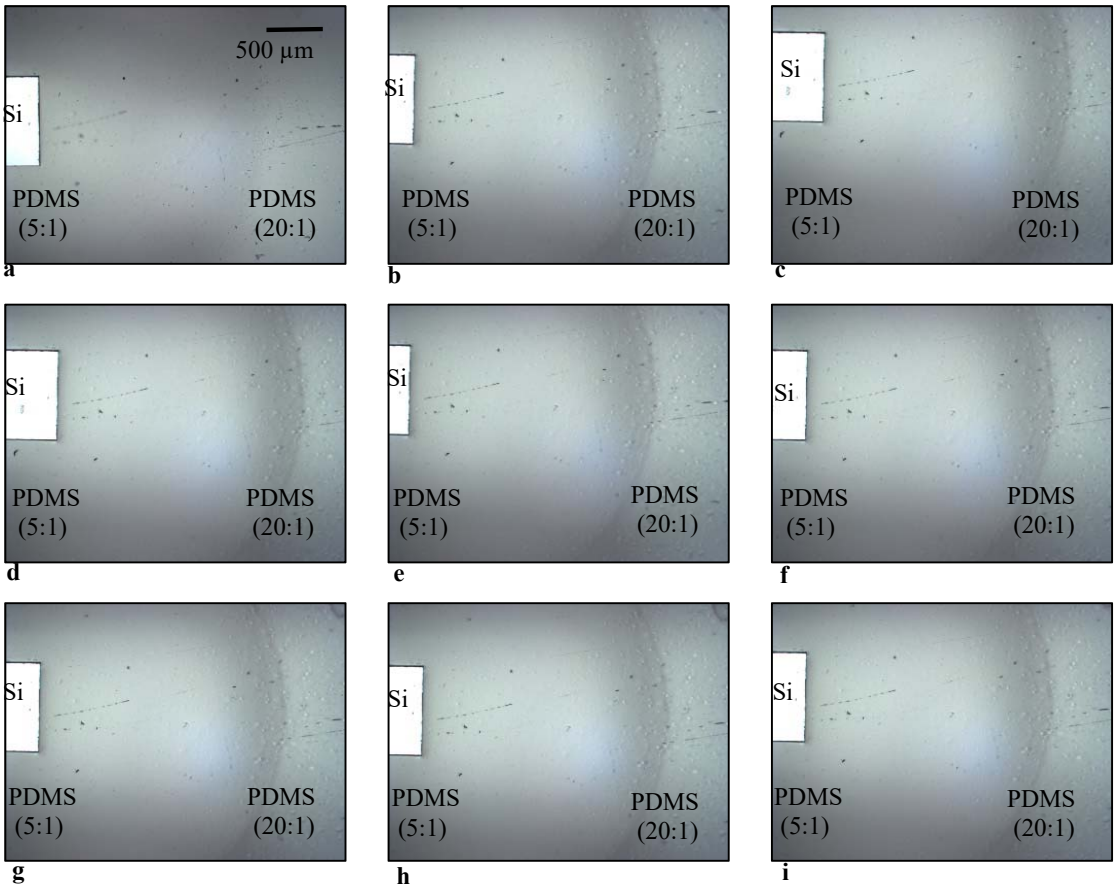

Figure 4.7. Cyclic stretch test for 100 cycles ($E_1/E_2 = 7.6$, $h_3/h_2 = 5$, $h_1/h_2 = 1$, $L_2/L = 0.2$, $\varepsilon_{applied} = 50\%$). a, Before starting test. After **(b)** 1 cycle, **(c)** 10 cycles, **(d)** 20 cycles, **(e)** 30 cycles, **(f)** 50 cycles, **(g)** 70 cycles, **(h)** 90 cycles and **(i)** 100 cycles.

4.2. Layers thickness effect

The silicon chip thickness and polymer layers thickness effect on delamination of layers were investigated. For this purpose, the energy release rate for Si-PDMS interface was calculated as function of h_3/h_2 and h_1/h_2 where h_3 is the electronic chip thickness, h_2 is the intermediate layer thickness on top of the electronic chip and h_1 is the primary layer thickness on top of the silicon chip. As the ratio of h_3/h_2 increases the energy release rate decreases (Figure 4.8). In order to avoid delamination, the lowest possible thickness for the electronic chips should be considered. The energy release rate has direct relationship with ratio of h_1/h_2. As this ratio raises the energy release rate increases (Figure 4.9). To minimize the risk of delamination the thinnest possible thickness for the primary layer should be considered.

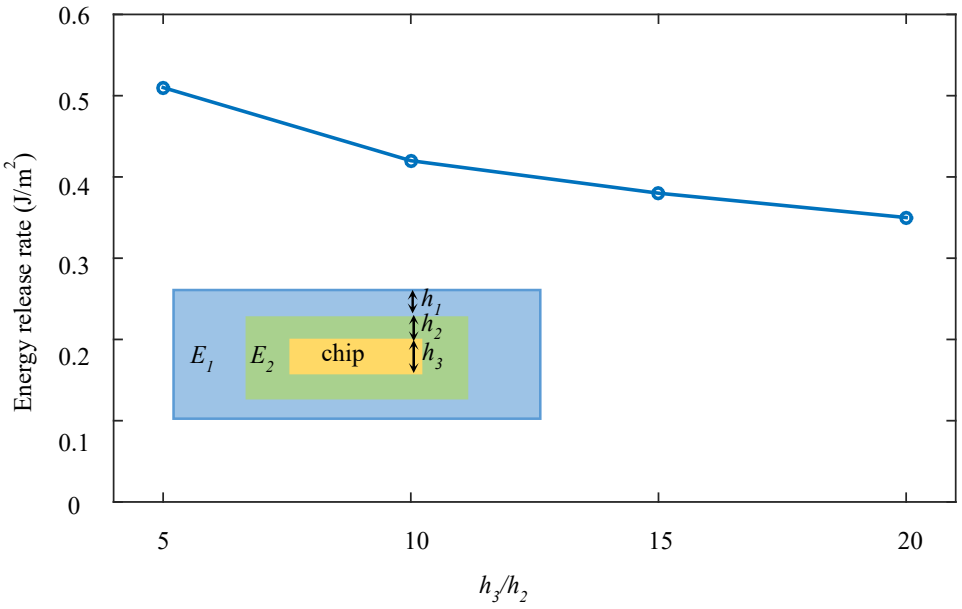

Figure 4.8. Energy release rate of silicon-PDMS interface debonding as function of h_3/h_2, ($E_1/E_2 = 7.6$, $h_1/h_2 = 1$, $L_2/L = 0.05$, $\varepsilon_{applied} = 20\%$).

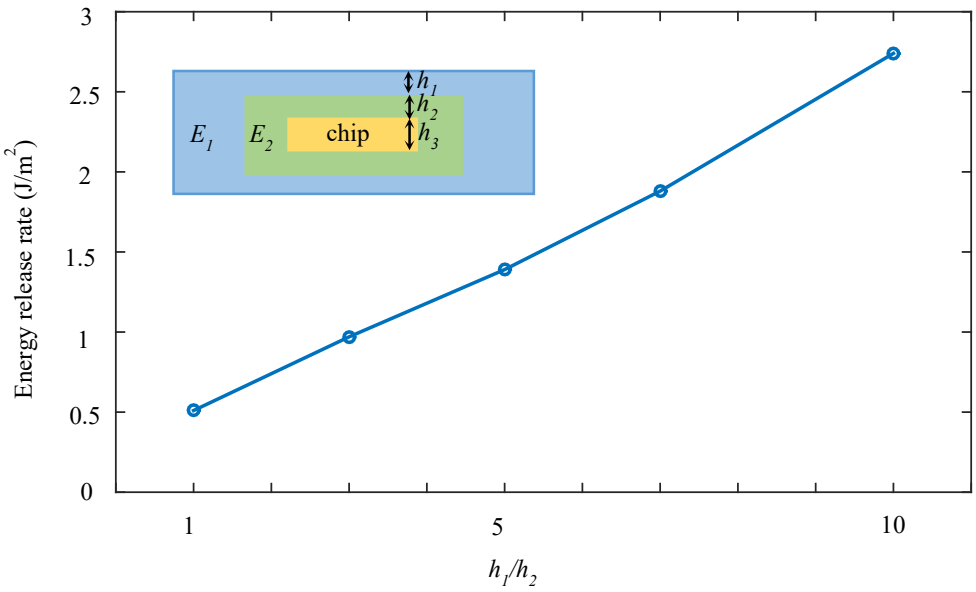

Figure 4.9. Energy release rate of silicon-PDMS interface debonding as function of h_1/h_2, ($E_1/E_2 = 7.6$, $h_3/h_2 = 5$, $L_2/L = 0.05$, $\varepsilon_{applied} = 20\%$).

4.3. Intermediate shape effect

Delamination typically happens at sharp edges and corners or at regions with high strains. This means the shape of electronic chips plays an important role in delamination of layers. In order to study this effect two structures with two types of electronic chips, square and circular, are investigated. These two electronic chips are embedded in engineered substrate platforms with the same geometry and material properties. 20% strain applied to the structures and the energy release rate for the Si-PDMS interfaces are calculated. Having rounded corners or circular chips can reduce the energy release rate. As an indication of this effect, the strain fields around a circular chip and a square chip are compared in Figure 4.10**.** The energy release rate for the square chip is seven times bigger than the circular chips.

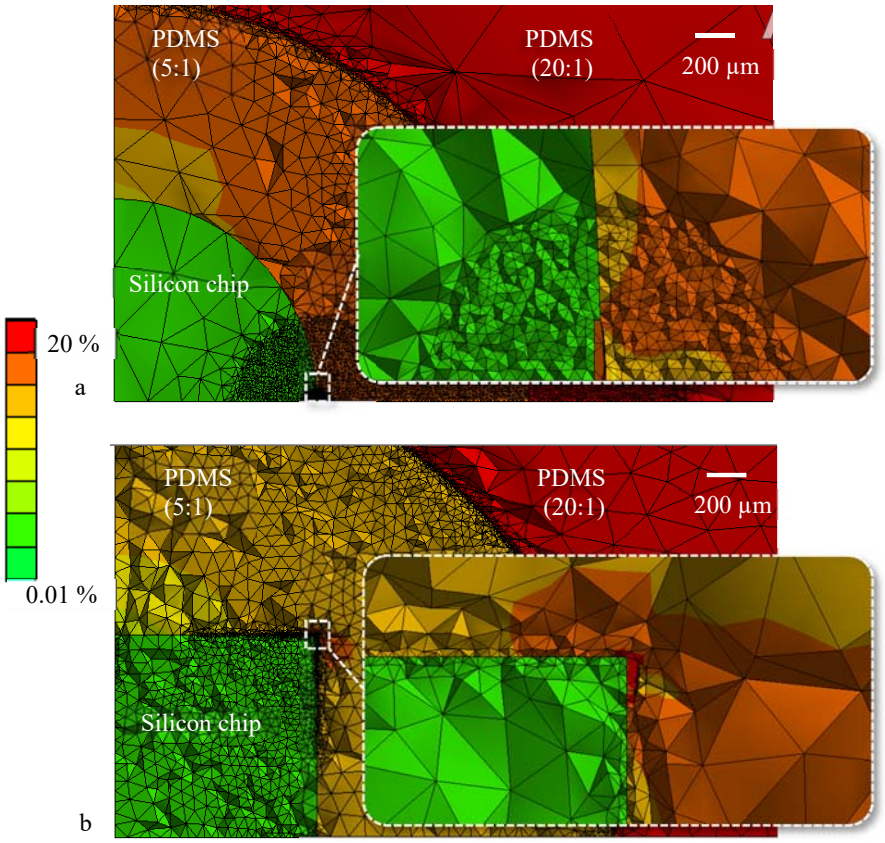

Figure 4.10. Maximum principal elastic strain analysis and energy release rate calculation ($E_1/E_2 = 7.6$, $L_2/L = 0.05$, $\varepsilon_{applied} = 20\%$) for **(a)** circular chip, G= 0.07 [J/m^2] and **(b)** square chip, G= 0.51 [J/m^2].

4.4. Applied load effect

There is a direct relationship between applied load and delamination of the layers. The energy release rate increases (Figure 4.11) with increasing applied strain with approximately quadratic dependence (Figure 4.12).

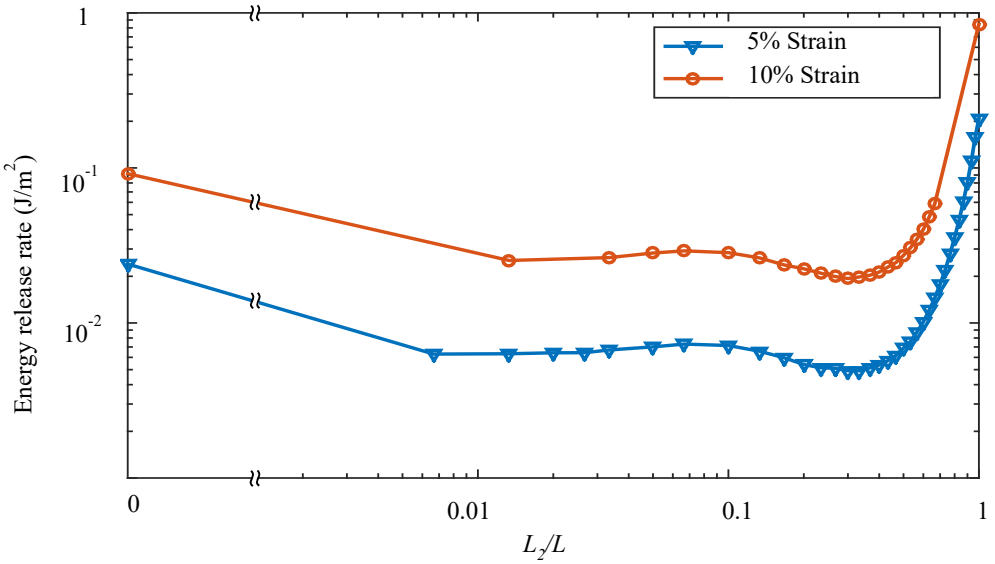

Figure 4.11. Applied load effect on energy release rate. ($E_1/E_2 = 10$, $h_3/h_2 = 5$, $h_1/h_2 = 1$) for Si-PDMS interface

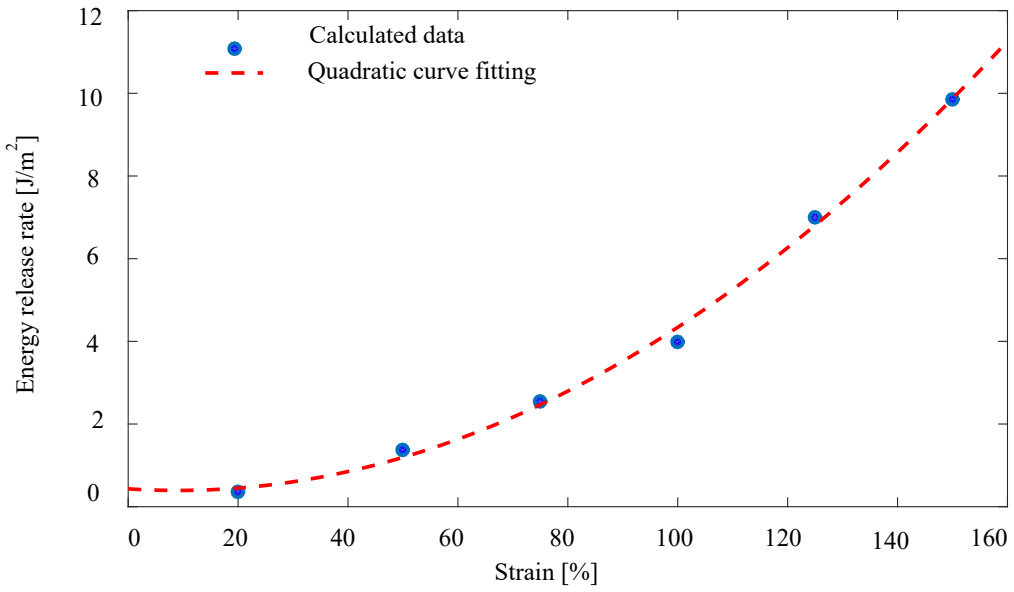

Figure 4.12. Energy release rate quadratic dependence to the applied strain. ($E_1/E_2 = 7.6$, $h_3/h_2 = 5$, $h_1/h_2 = 1$, $L_2/L = 0.45$, $\varepsilon_{applied} = 20\%$) for PDMS-PDMS interface.

Chapter 5

5. Interface modification

5.1. Introduction:

As discussed before, stretchable electronics are devices that can operate under high strain ($\varepsilon > 2$ %) and are useful for applications that require stretchability while they are functioning. Combinations of thin film inorganic and organic materials have shown promises for making stretchable and flexible electronics. The approach of thinning inorganic materials to nanoscale dimensions enhances flexibility properties and patterning inorganic materials in meander shape raises their stretchability properties. However, thinning electronic chips is one of the main challenges of this approach. Thinning electronic chips to sub-micro dimensions is not always possible since the functionality of the chips may be affected. For example, the interconnect stack in most CMOS chips is well over 10 μm thick. So, embedding "thick" electronic chips (e.g., with a thickness ≥ 20 μm) into soft materials is needed. Delamination of electronic chips from soft material and non-reliable connectivity are two main challenges for embedding thick electronic chips into soft materials.

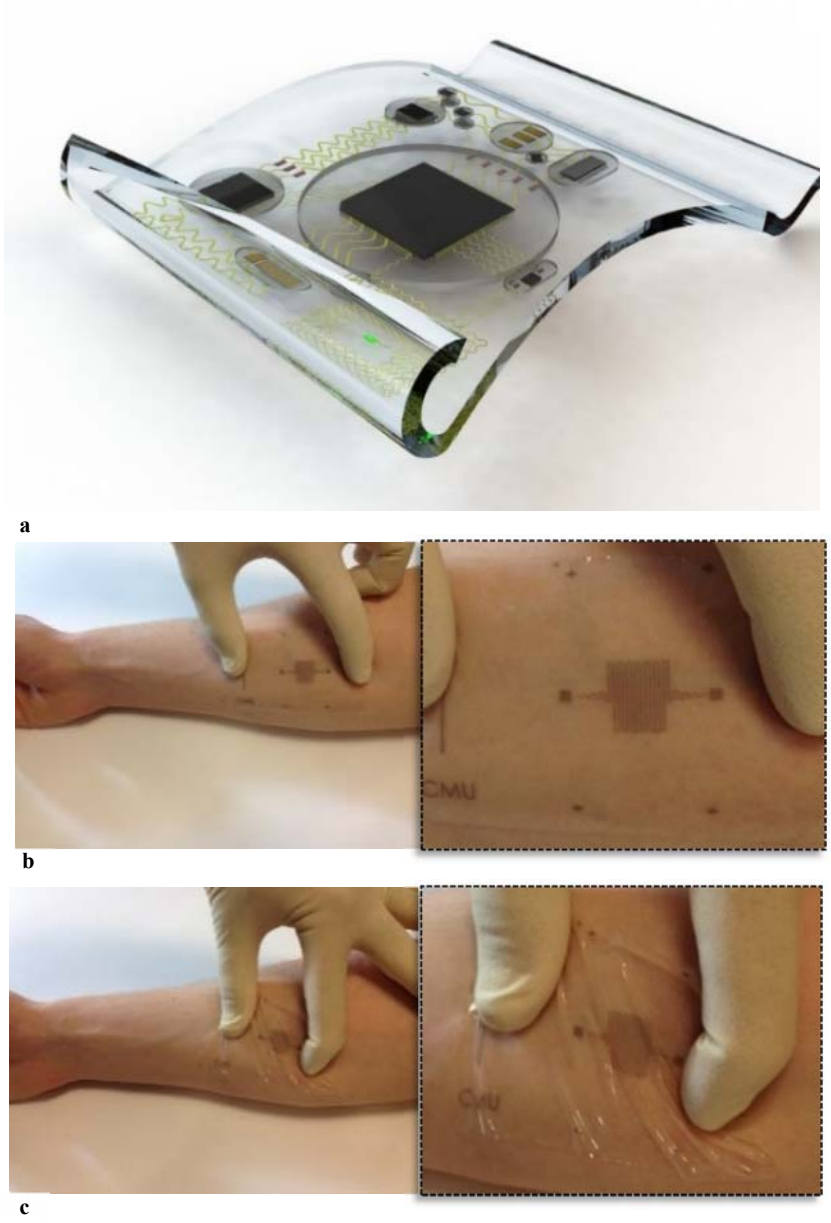

Figure 5.1. Thin stretchable substrate for integrated electronics. a, Schematic concept for embedded, distributed, and interconnected electronics chips in stretchable systems. **b, c,** Embedded wires in a PDMS stretchable system under controlled strain conditions with no strain **(b)** and then under highly strained conditions **(c).** See Appendix E for embedded wires fabrication process.

In the previous chapters, an "engineered substrate" was proposed to address the delamination issue[70]. The engineered substrate, which will be called substrate approach #1, is composed of several soft organic regions with different values of Young's modulus and located around electronic chips. The role of our multiple regions approach is to control strain

and stress contours at the interface to the chips when the surrounding substrate is stretched. For example, silicon chips with high Young's modulus (E ~ 169 GPa) are surrounded by polymer substrate regions that act as an intermediate region between the chip and the rest of the soft elastomeric substrate. The stiffness of the substrate material decreases from the chip to the edges of the substrate and the majority of strain will be accommodated in outer regions. Because of this, the substrate material near the chip interface experiences relatively low strain and stress (Figure 5.1). Our coupled computational and experimental approach revealed that adding just one discrete intermediate region results in a 5.5 times increase in the strain failure threshold and subsequently decreases delamination.

The second challenge of making stretchable electronics is wiring electronic components in soft substrates. Wires are made of conducting materials having a different Young's modulus from the substrate; therefore, these connections experience levels of strain and stress that also require soft substrate engineering. The interfaces between the soft materials are the most critical regions in a composite structure where the wires break. A composite structure of two soft material regions having different values of Young's modulus causes a step in the strain level at the interface (Figure 5.2a). This step in strain induces wire breakage. One approach to solve this issue is using liquid metal Galinstan which provides mechanical stability under deformation [71]. Another way to address the wiring problem is to embed the wires into a liquid form of the substrate. The suspended wires in the liquid substrate experience low stress [45,72]. In the current chapter, the effect of modifying the soft material interfaces on embedded wiring, without using liquid materials, is studied. Three distinct material interfaces are investigated and delamination tests along with strain mapping are performed. The results are compared and the behavior of thin-film wiring that passes across the interfaces is studied.

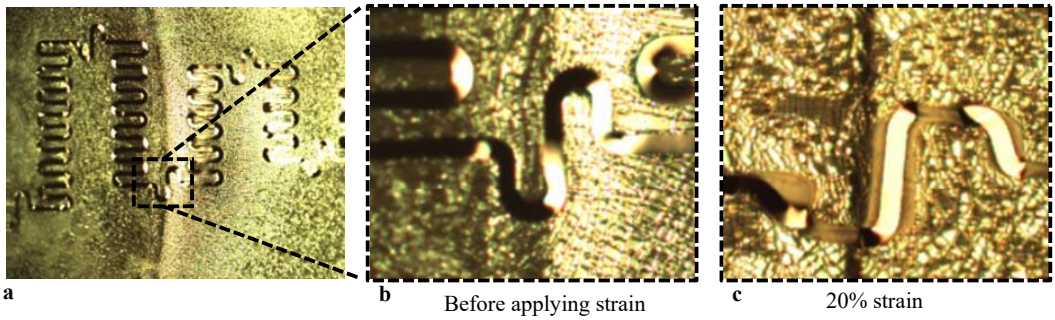

Figure 5.2. Behavior of interconnection wires on composite layer **(a),** before **(b)** and after applying strain **(c).**

5.2. Interface modification

Three methods of making soft substrates for stretchable electronics are studied. The goal of these approaches is to address wiring failure that can happen where the wire passes across the soft substrate regions having different stiffness values. Regions in a composite structure experience different levels of expansion and contraction in the direction perpendicular to the applied load. Shear stress at the edges of the interfaces can break the wires (Figure 5.2). In order to solve this issue, the substrate material stiffness needs to be smoothly transitioned from one region to another. This material gradient reduces the sharp shear stress at the interface between regions. In this work, two approaches (Figure 5.3b, c) for smoothing the transition between regions of engineered substrate, approach#1, (Figure 5.3a) are studied. In the approach #2 (Figure 5.3b), the transition region starts exactly at the edge of the chip. In the approach #3 (Figure 5.3c), the smooth change in material properties starts from the edge of a soft intermediate layer that surrounds the chip.

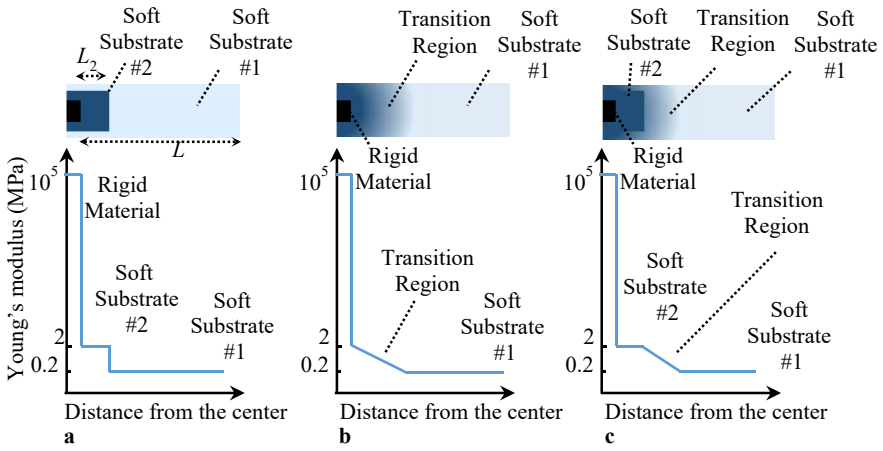

Figure 5.3. Interface modification approaches. Schematics of the Young's modulus of the materials as a function of location along the length of the stretchable substrate: **a,** Approach #1 of one intermediate soft material between the chip and soft substrate; **b,** Approach #2 of the chip embedded into the stretchable substrate with a gradient of stiffness around the chip; **c,** Approach #3 of the engineered substrate with one intermediate soft material between the chip and the soft stretchable substrate, and augmented with a gradient of stiffness around the intermediate soft region.

The fabrication processes for making thin stretchable substrates using the three approaches are illustrated in Figure 5.4. The fabrication process for approach #1 has two general stages: First, embedding an electronic chip into an intermediate material (Figure 5.4a-f) and next, embedding the manufactured structure into a primary substrate (Figure 5.4g-g1). In the first stage, a bare silicon wafer (Figure 5.4a) is coated with a submicron layer of gelatin (1%) as a sacrificial layer and then a 10 µm polydimethylsiloxane (PDMS) (5:1) film is coated on the gelatin layer (Figure 5.4b). The coating step is followed by partial curing at 80ºC for 20 min. This heat treatment allows the PDMS (5:1) film to solidify without losing its adherent nature. Therefore, the electronic chips (Figure 5.4c) and upper coating layer sticks to this surface well. A 60 µm-thick PDMS (5:1) layer is coated on the silicon chip and then cured at 80ºC for 4 h. (Figure 5.4d). Using a hard mask and through reactive-ion etching (SF_6/O_2 plasma) for 3 h (Figure 5.4e), the composite structure is patterned into a circular shape; then the patterned structure is transferred onto a second handle wafer that is covered with a 10 µm-thick coated and partially cured PDMS (20:1) film (Figure 5.4g). The fabrication process is

followed by coating the composite shaped structure with the intermediate material with a 80 µm-thick PDMS (20:1) layer and then curing it at 80ºC for 4 h (Figure 5.4g1). The substrate is released in hot water (70ºC) since gelatin is highly soluble at this temperature.

The fabrication process for approach #2 is similar to steps (a-d) of the approach #1 except that 20 µm PDMS (20:1) in step (b) and 70 µm PDMS (20:1) in step (d) are coated. In the next step, PDMS (5:1) droplets are injected around electronic chips (Figure 5.4d1) before curing PDMS (20:1). The injected PDMS (5:1) diffuses into the surrounding PDMS (20:1). Since the PDMS (5:1) droplets are injected to the center of the structure and PDMS flows from the center to the sides, the concentration of PDMS (5:1) at the center is higher than the edges. In other words, there is a concentration gradient of PDMS (5:1) across the soft substrate. Therefore, the mixture of PDMS (20:1) and (5:1) forms PDMS (*x*:1), where *x* varies between 5 and 20 across the substrate (Figure 5.3b).

In approach #3, the gradient in stiffness starts at the edge of an intermediate region (Figure 5.3c). The fabrication process of this approach is the same as the approach #1 (Figure 5.4a-h) except that for the formation of the gradient in stiffness, where PDMS (5:1) droplets are injected (Figure 5.4h1) to the center of the structure at the end of process before curing of PDMS (20:1).

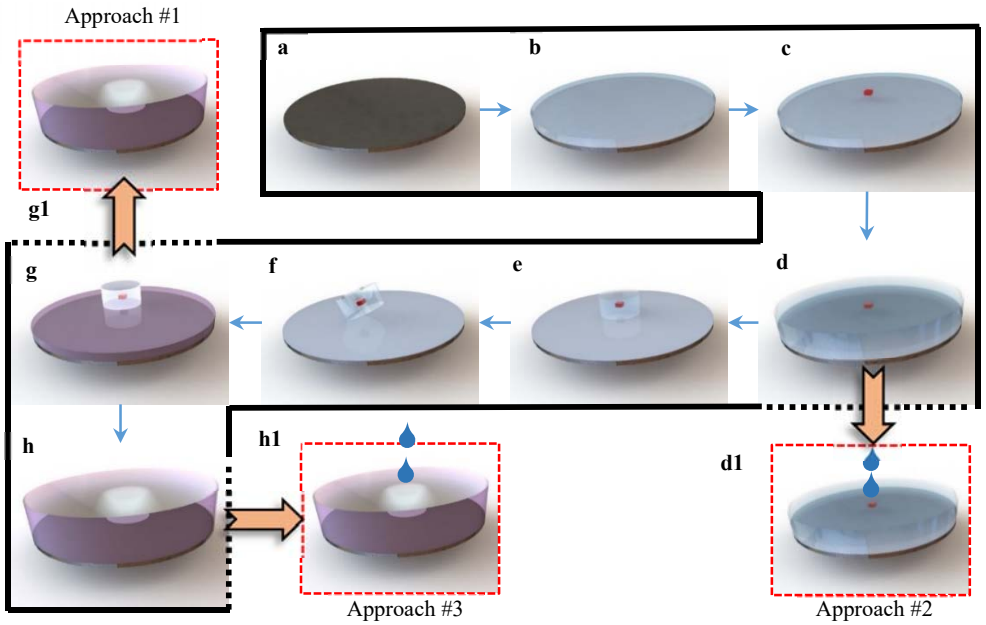

Figure 5.4. Fabrication process of our thin stretchable substrate. Approach #1 ("engineered substrate") a-g1, (a) Cleaning a bare silicon handle wafer, **(b)** Coating a thin layer of gelatin (1%) to aid in release and coating 10 µm-thick PDMS (5:1), **(c)** Silicon chip transfer **(d)** Coating 60 µm-thick PDMS (5:1) **(e)** Reactive ion etching using SF_6 and O_2 plasma, **(f-g)** Intermediate structure transfer onto handle wafer with 10 µm-thick PDMS (20:1), **(g1)** Coating 80 µm-thick PDMS (20:1). **Approach #2, a-d1, (a)** Cleaning a bare silicon handle wafer, **(b)** Coating a thin layer of gelatin (1%) to aid in release and coating 20 µm-thick PDMS (20:1), **(c)** Silicon chip transfer **(d)** Coating 70 µm-thick PDMS (20:1), **(d1)** injecting PDMS (5:1). **Approach #3, a-h1, (a-g),** the same as approach #1, followed by **(h)** coating 80 µm-thick PDMS (20:1), **(h1)** injecting PDMS (5:1) before curing.

5.3. Delamination test

In order to investigate the effect of these approaches on delamination at interfaces, three types of samples, shown in Figure 5.5a-c, are designed and fabricated. For the rigid components, 1 mm × 1 mm × 50 µm silicon chips are used as surrogate electronic devices. The silicon chips are embedded in a 20 mm × 20 mm × 90 µm soft substrate. For the compliant region of these structures, two mixtures of PDMS are used as soft materials (base-to-curing ratios 5:1 and 20:1). Samples of the approach #1 and the substrate using approach # 3 are examined with different ratios of L_2/L (0.05, 0.15, 0.25, 0.35, and 0.45) and a fixed L = 10 mm, while keeping the other dimensions, materials and loading conditions constant. In approach #2,

the same sample size with different droplet volumes (1 μL, 2 μL, 3 μL, 5 μL, 10 μL) are examined.

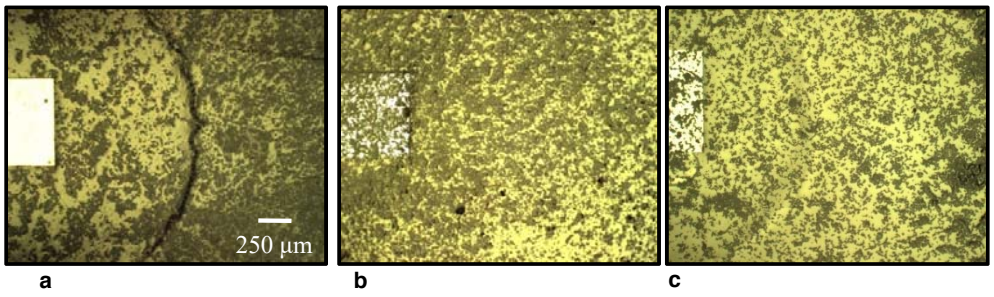

Figure 5.5. Three approaches samples. **a,** Approach #1 with different L_2/L (0.05, 0.15, 0.25, 0.35,0.45). **b,** approach #2 with different injected droplet **(**1 μL, 2 μL, 3 μL, 5 μL, 10 μL**)**. **c,** Approach #3 with different L_2/L ratios (0.05, 0.15, 0.25, 0.35, 0.45) and 10 μL PDMS (5:1) droplet.

To quantify the onset of strain failure, we performed tensile tests for all three sample types. Tensile strain loading at each end of the substrate is applied as a series of small incremental step functions. The system is elongated at a low strain rate (0.001 s^{-1}) to achieve a pseudo steady-state behavior and the strain failure is examined through optical microscopy imaging.

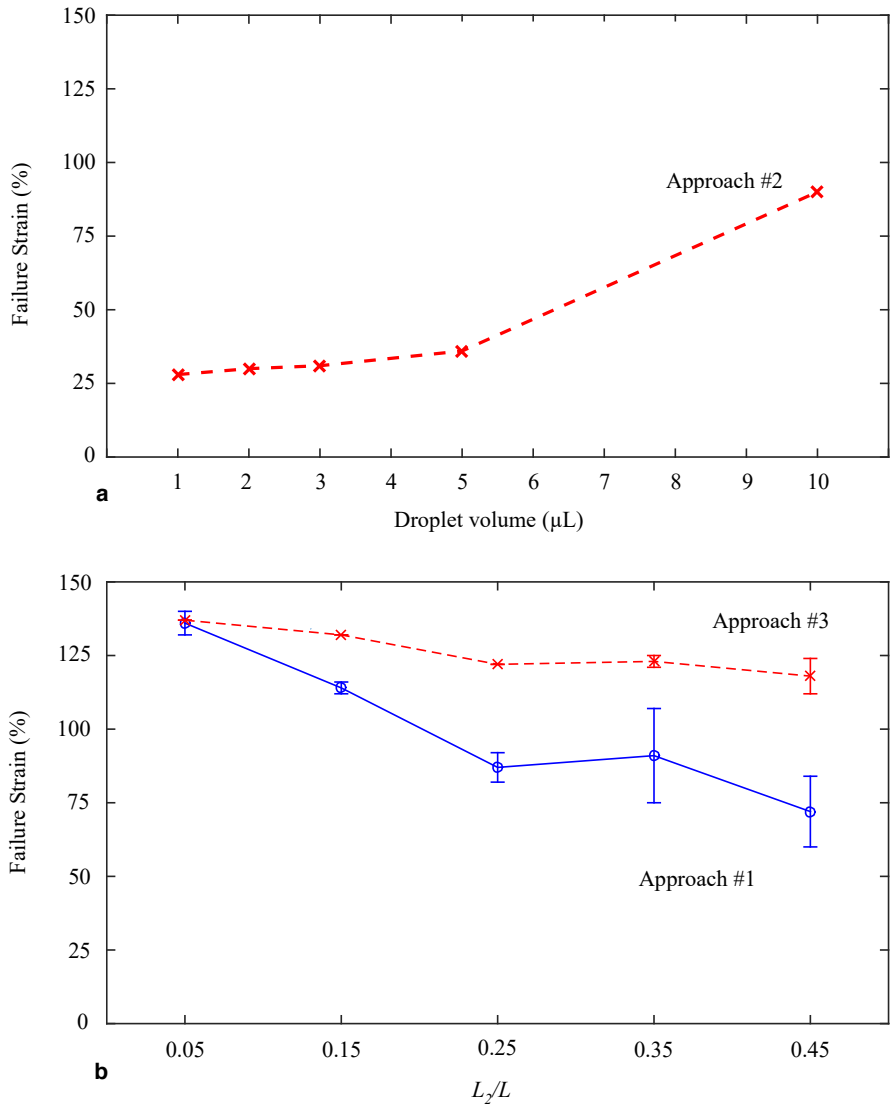

Figure 5.6. . Delamination strain values. **a,** Delamination strain values for approach #2 structures with different droplet volumes. **b,** Delamination strain values for the approach #1 and approach #3 structures as a function of intermediate region radius L_2.

Delamination for approach #2 occurs at the Si-PDMS interface in all cases. The strain failure threshold rises as the volume of droplets around the silicon chips increases (Figure 5.6a). A 90% strain failure threshold is achieved for the sample with a 10 μL droplet of PDMS (5:1) around the silicon chip. Delamination for the approach #1 occurs at the PDMS-PDMS interface. The strain failure value for this interface decreases as the radius of the intermediate region (L_2) increases. The delamination test results for approach #3, which is the combination

of approach #2 (with a 10 µL drop) onto the approach #1, show a higher strain failure threshold compared to the other approaches. For these samples, delamination occurs at the Si-PDMS interface and strain failure threshold stays above 125% strain for all samples (Figure 5.6b). Using approach #3 for modification of the interfaces increases strain threshold by 30% on average, compared to the engineered substrate approach.

5.4. Strain mapping

In order to investigate the effect of each approach on the distribution of strain in the structures, experimental strain mapping is performed for all approaches. To accomplish this, a sample with an intermediate region radius of 3 mm with the approach #1 (Figure 5.7a), a sample with a 10 µL intermediate droplet for approach #2 (Figure 5.7b), and a sample with intermediate region radius of 3 mm with a 10 µL droplet for approach #3 (Figure 5.7c) are measured. The strain across the surface of the samples is mapped with uniaxial stretching (20% strain) using Digital Image Correlation software [73] (see Appendix F for more information). In order to increase the performance of Digital Image Correlation in capturing surface behavior, 8.74 µm-diameter beads (Carboxyl Ferromagnetic Particles (CFM-80-5)) are scattered on the surface of the samples. Pictures are captured using a camera equipped microscope (Olympus MX-80) after applying the load and then are imported into the software. The strain mapping for the approach #1 shows a step in strain contour between PDMS regions (Figure 5.7d). For approach #2 and #3 this step does not exist and the strain contour is smoother (Figure 5.7e-f). Approach #3 results in a smoother strain contour with a lower strain around the silicon chip compared to other approaches

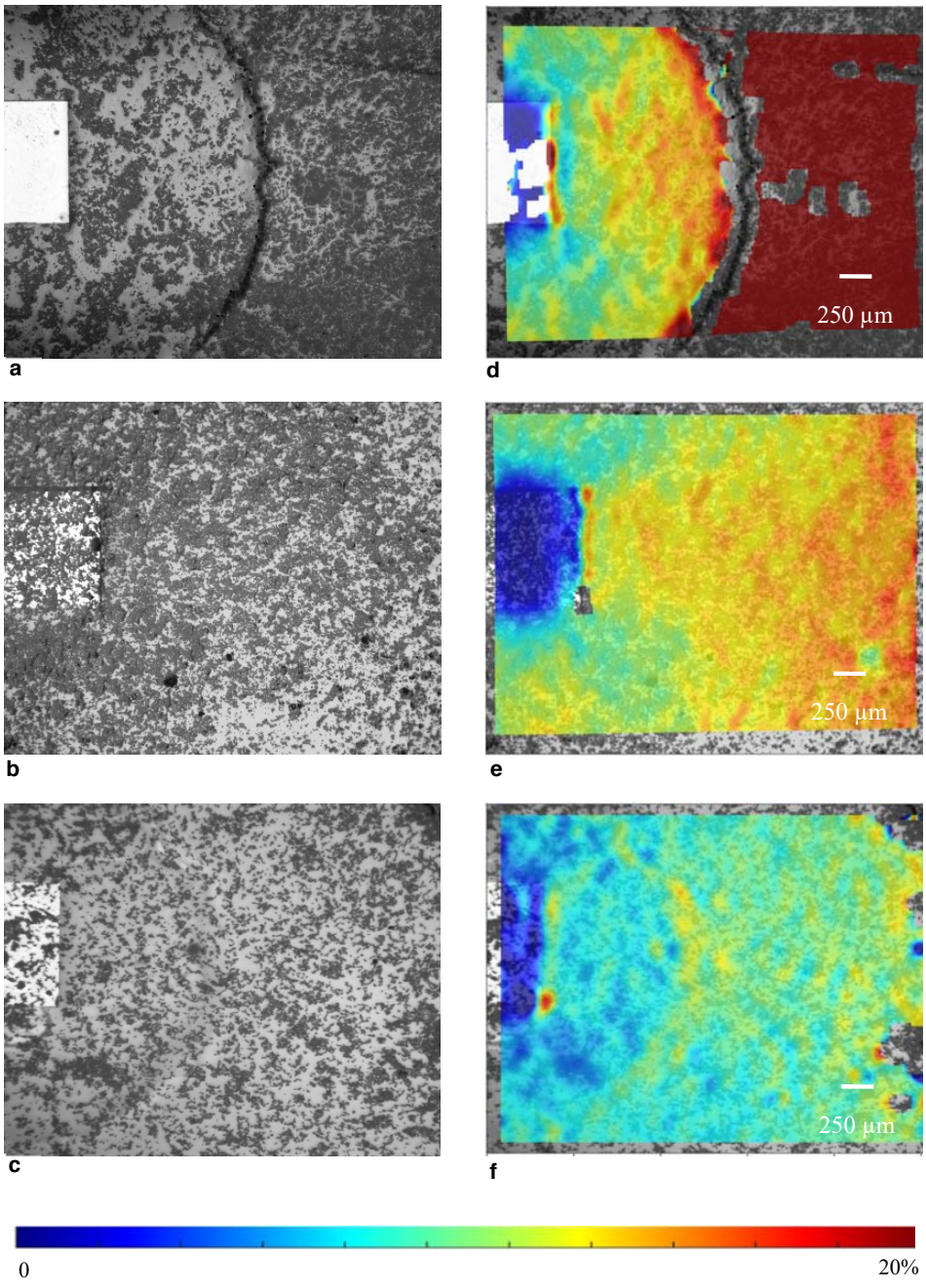

Figure 5.7. Strain contour mapping for. a, d, Approach #1. **b, e**, Approach #2. **c, f,** Approach #3 under 20% strain tensile test.

5.5. Interconnections behavior test

The behavior of thin-film wires on the surface of these composite substrates is also investigated. A 600 nm-thick sputtered copper film is deposited on a handle wafer. A submicron PMMA-A7 film is used as a sacrificial layer underneath of copper layer. Copper film is patterned in horseshoe shape [49,74] with photoresist (AZ 4210), exposed to copper etchant (AL etchant type a, Transene) for 1 min, and then the photoresist is removed with acetone. For the approach #1 sample, a PDMS (5:1) cylinder with thickness of 50 μm and diameter of 3 mm is placed on the middle of the structure above the wires. Then, the structure is coated with 70 μm PDMS (20:1) and cured at 80 ºC for 30 min (Figure 5.8a). For the approach #2 sample, the wires are coated with 70 μm PDMS (20:1). Before curing the PDMS (20:1), a 10 μL PDMS (5:1) droplet is injected in the middle of the structure (Figure 5.8b). The fabrication process of approach #3 is the same as approach #1 except that before curing step, a 10 μL PDMS (5:1) droplet is injected in the middle of the structure (Figure 5.8c). The full fabrication process is provided in Appendix D. Wire movement under tensile test is observed. As expected, the approach #1 interfaces lead to the worst breakage of wiring. The wires break at 15% strain due to the existence of the step in strain (Figure 5.8a1-a3). The corresponding critical strain value for approach #2 is 20% (Figure 5.8b1-b3). For approach #3, the wire remains intact without failure up to 135% strain (Figure 5.8c1-c3). The combination of the 3 mm intermediate layer and 10 μL volume of PDMS droplets results in a much larger operational regime. Electronic circuits and electronic chips function under high strain when they are embedded using approach #3. The integrated wires using this approach do not experience a pass across interfaces with discrete steps in strain.

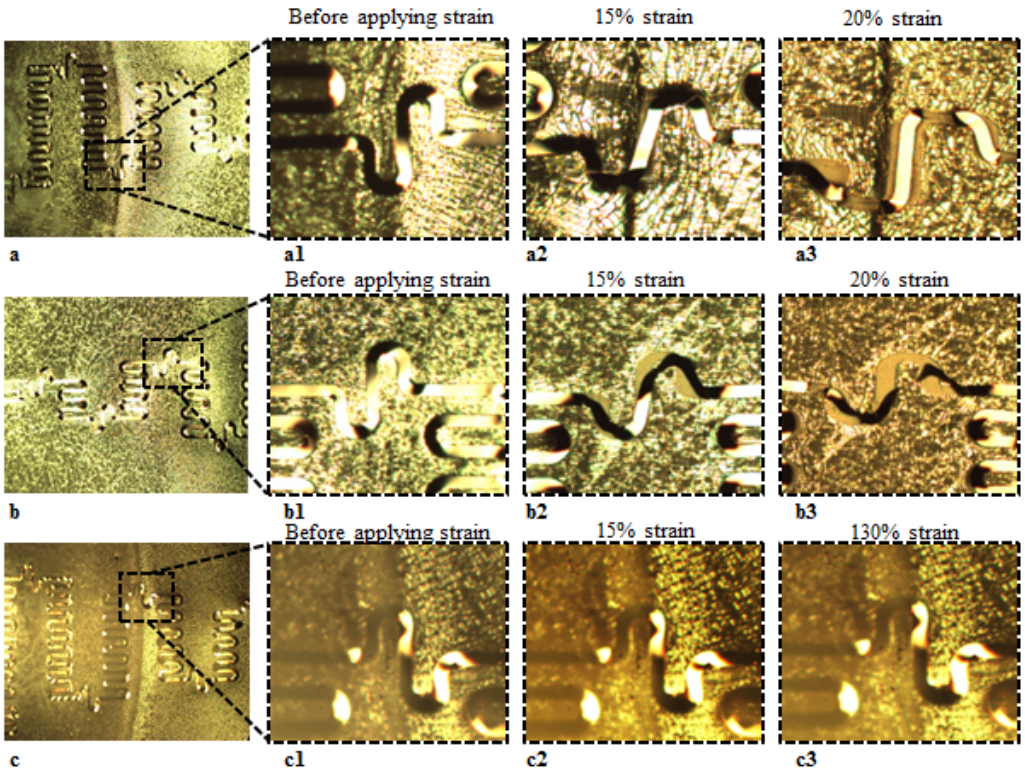

Figure 5.8. Behavior of interconnection wires on **(a)** approach #1 **(b)** approach #2 and **(c)** approach #3 structures under tensile test**.**

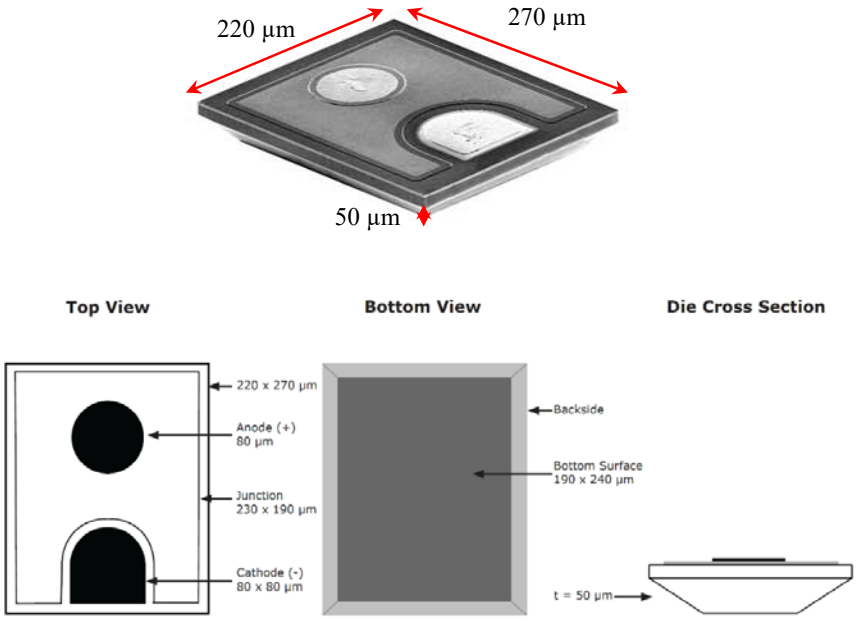

Figure 5.9. Cree® TR2227™ LED. InGaN Junction on Thermally Conductive SiC Substrate.

5.6. Built-in LEDs in a wearable platform

In order to demonstrate the ability of approach #3 to operate with embedded electronic chips, a light emitting diode (LED), Cree® TR2227™, (Figure 5.9) is embedded in the center of the substrate using approach #3. Its function is monitored while increasing the strain (Figure 5). The LED is electrically connected to 9V external DC power using gold wire bonding. The gold wires directly come out from the safe region and are connected to the DC power (Figure 5.10). The structure remains functional up to 150% strain (Figure 5.11).

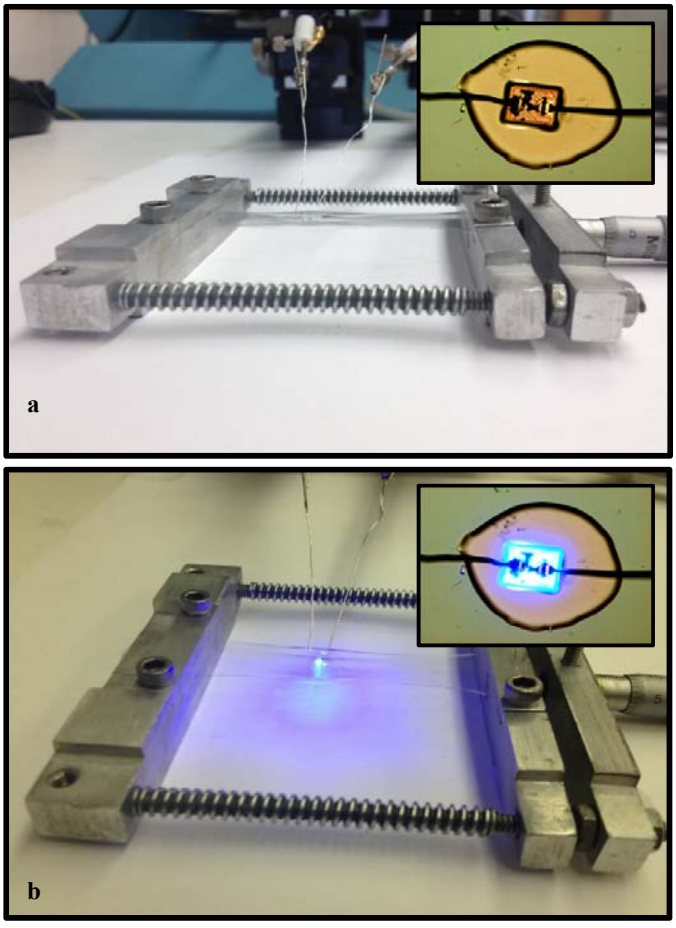

Figure 5.10. LED test setup. Embedded LED in a soft substrate using approach #3 under tensile test **(a)** before and **(b)** after connecting to a DC power.

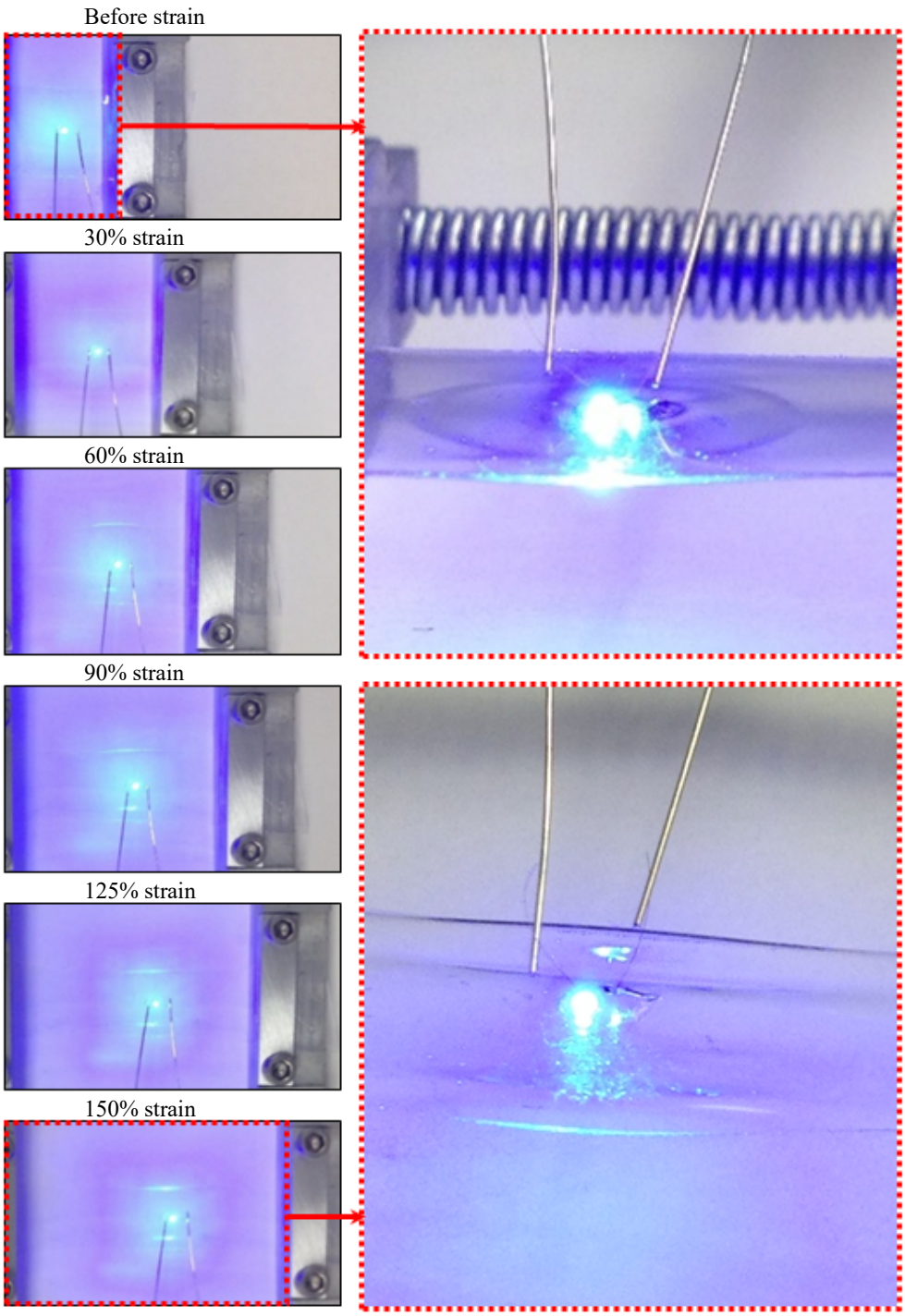

Figure 5.11. Embedded LED in safe region under steady-state tensile test.

Chapter 6

6. Conclusion

6.1. Engineered platform

The ability to create a material gradient interface can open up new avenues for the area of flexible electronics. By combining the more mature field of CMOS with the tremendous current functional capabilities of soft materials, tremendous advances will be made. The challenge of interfacing these material systems has been shown here to have advantages in using an intermediate gradient material. Comparing the value of failure strain using our approach increases the strain possible to 140% while the structures having no intermediate soft material fail at 20%. Our coupled computational and experimental findings demonstrate quantitatively the promise of this approach to reduce delamination under high external strain levels. The presence of the intermediate soft material with a Young's modulus between that of the primary soft material and the silicon substrate decreases the risk of delamination of the soft material from embedded silicon chips. The very significant increase in failure strain of 550% through employing an intermediate material layer is an important basis for the next generation of flexible and stretchable electronics, which will likely require functioning in high value strain environments such as in skin sensors.

6.2. Spatial varying mechanical properties

Stretchable composite structures having a smooth distribution of strain contours can provide a base for making new flexible and stretchable electronics with the ability to accommodate a high level of strain. Discrete composite structures show uneven changes in the level of strain when they are loaded and thus delamination occurs at interfaces between discrete regions and corresponding failure in connectivity at these locations are inevitable. In this work, these issues are addressed by adding a smooth transition in the elastomeric substrate stiffness between regions. For example, a 30% increase in strain failure threshold at the Si-PDMS interface is achieved through this approach. Also, this interface modification protects wires from breaking, to up to 135% applied strain while similar wires without the smoothing of the substrate stiffness fail at 15-20% strain. By selecting softer material for soft substrate #1 (Ecoflex, Smooth-On, Inc., Macungie, PA), the maximum level of applied strain can be enhanced even further. Using this approach provides a safe region for electronic components and electronic circuits to be embedded within in a stretchable substrate. However, since the strain within the stretchable substrate varies as a function of location, wiring design strategies need to come into play so that wires located anywhere on the substrate are able to function under high levels of strain.

Chapter 7

7. Future work

Research presented in this thesis provided the foundation for the design and fabrication stretchable and flexible electronics. Many applications can be made by using the proposed approach in this work. As an interesting application, making a stretchable display may be considered.

7.1. Stretchable display

Stretchable and foldable displays are one of the most interesting applications of stretchable electronics that researchers are investigating to achieve. A display is generally consist of LEDs, interconnection (electrodes) and covering glass. In a display, LEDs are placed in the matrix order with interconnections. In order to achieve a stretchable display using our proposed approach in this research, each LED (or combination of red, green and blue LEDs) should be embedded in an intermediate layer and the interfaces of layers should be modified using the proposed approach in this research (Figure 7.1). The design and fabrication process of such a system are challenging and should be addressed.

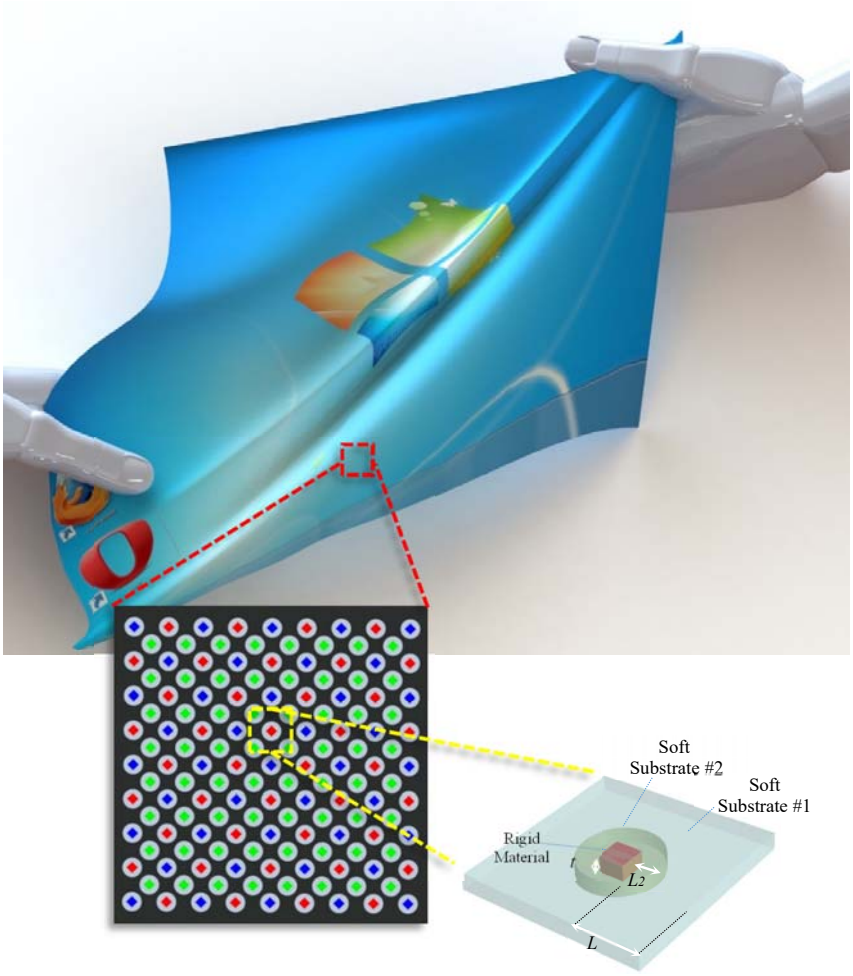

Figure 7.1. Schematic of stretchable display using the engineered platform approach

7.2. Design challenges

The actual size of a pixel in a display is approximately 2 μm. This value is significantly lower than the Si chips that we used in our design in this work. Intermediate layer parameters design, including intermediate layer thickness, primary layer thickness, intermediate layer Young's modulus, primary layer Young's modulus, intermediate layer length, primary layer length, period of electronic LEDs, should be redesign for this size.

LEDs interconnection stretchability defines the maximum amount of stretchability of the whole structure, since the LEDs and intermediate layer can function under high amount of

strain (150%). Therefore designing of reliable stretchable interconnection should be taken into account.

7.3. Fabrication challenges

A display is composed of several layers of different materials. The nature of fabrication process of each layer is different from another layer. Besides that, for the fabrication of huge amount of LEDs on a substrate, an automatic pick and place technique should be used. Fragile LEDs should be attached on an elastic substrate. So, controlling the applied load on LEDs to adhere them on the elastic substrate should be considered. In addition, adding material for interface modification should be precisely controlled, otherwise intermediate layers of LEDs will be mixed.

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Appendix A: Stretchable platform fabrication

Process flow for stretchable platform fabrication:

The fabrication process of our platform is illustrated in figure A1. This fabrication process has two general stages: First, embedding a silicon chip into an intermediate material (Figure A1a-g) and the second, embedding the manufactured structure into a primary substrate (Figure A1h-K).

First stage.

A bare silicon wafer (Figure A1a) is coated with a submicron layer of gelatin (1%). Gelatin has been used as a sacrificial layer since it is soluble in water and it aids in release of the structure. PDMS (5:1) is selected as an intermediate material since it adheres well to PDMS (20:1). For the next step, 10 µm PDMS (5:1) film is coated on the gelatin layer (Figure A1c). The thickness versus spin-speed graph for PDMS (20:1) and PDMS (5:1) is provided in Figure A2. Different film thicknesses are achieved at lower spin speeds due to the difference in viscosity of these polymers. The coating step is followed by partial curing at 80ºC for 20 min. This heat treatment helps the PDMS (5:1) film solidify without losing its adherent nature completely. Therefore, the silicon chip (Figure A1d) and upper coating layer sticks to this surface very well. The silicon chip is coated with a 60 µm-thick PDMS (5:1) layer and then

cured at 80ºC for 4 hr (Figure A1e). The composite structure is patterned into a circular shape by performing reactive-ion etching using SF_6/O_2 plasma for 3 hr (Figure A1f) and using circular PDMS with different diameter as masks; then the remaining structure is transferred on a second handle wafer that is covered with a 10 μm-thick coated and partial cured PDMS (20:1) film (Figure A1g-i). The etching process changes the mechanical properties of the PDMS surface because of chemical reactions (Figure A3a-b). Before the etching process the PDMS surface is smooth and sticky, but after the etching process it becomes uneven and less sticky. However, this uneven surface does not affect the adhesion between PDMS (5:1) and PDMS (20:1). In the second stage of the processing, the partially cured PDMS (20:1) is very sticky and the lower adhesion from the previous step can be compensated. The Young's modulus measurement before and after etching process reveals that the elasticity modulus is not changed (Figure A3c).

Process details:

1. Gelatin solution preparation.
    a. Gelatin powder (250 bloom, Modernist Pantry) is mixed with DI water (gelatin: water 1:99 w/w).
    b. The mixture is then heated in the oven at 60 ºC for 1 hour to dissolve.
2. PDMS solution preparation.
    a. PDMS solution (Sylgard 184, Dow Corning) is created by mixing pre-polymer gel and the cross linker in a 5:1 (w/w) and 20:1 ratio.
    b. The solution is agitated for 2 min for better mixing.
    c. The solution is placed in a vacuum chamber (Gast vacuum pump) for half of an hour to remove bubbles.
3. Spinning gelatin sacrificial layer.
    a. 4'' Si wafer is cleaned with acetone and IPA.

b. The heated gelatin mixture is spun at 1000 rpm for 10 seconds (Laurell WS-650Mz).

c. The sample is then dried in at room temperature to form a submicron sacrificial gelatin layer.

4. Spinning the first layer of PDMS (5:1).

   a. The PDMS (5:1) solution is spun on the gelatin at 3500 rpm for 60 s to form 10 μm thick PDMS (5:1) layer.

   b. The sample is then partially cured at 80ºC for 20 min.

5. Si chip placement

   a. A silicon chip (1 mm×1 mm×50 μm) is placed on the PDMS (5:1) surface by vacuum tweezers.

6. Spinning the second layer of PDMS (5:1).

   a. The PDMS (5:1) solution is spun on the silicon chip at 700 rpm for 60 s to form 60 μm thick PDMS (5:1) layer.

   b. The sample is then fully cured at 80ºC for 4 h.

7. Pattering the intermediate layer using RIE

   a. A circular PDMS (5:1) with thickness of 1 cm is used as a mask.

   b. The PDMS (5:1) is etched into circular pattern using Trion Phantom II RIE with the below recipe :

Etch					
SF_6 flow (sccm)	O_2 flow (sccm)	Etch time (sec)	CF_4 flow (sccm)	Press (mT)	Forward Power (W)
22.5	9	1100	0.0	25	170

Second stage:

The fabrication process is followed by coating an intermediate material with a 80 μm-thick PDMS (20:1) layer and curing it at 80ºC for 4 hr (Figure A1j). The resulting 90 μm-thick structure is cut into a rectangular shape (Figure A1k) for the subsequent experimental test procedures. The rectangular elastic substrate is released in hot water (70ºC) since gelatin is highly soluble at this temperature level.

8. Intermediate layer placement
    a. The patterned intermediate layer is placed on a 10 μm thick PDMS (20:1) surface by tweezers.
9. Spinning the second layer of PDMS (20:1).
    a. The PDMS (20:1) solution is spun on the silicon chip at 750 rpm for 60 s to form 70 μm thick PDMS (20:1) layer.
    b. The sample is then fully cured at 80ºC for 4 h.
10. Releasing the structure
    a. The sample is released in hot water (50 ºC, 10 min).

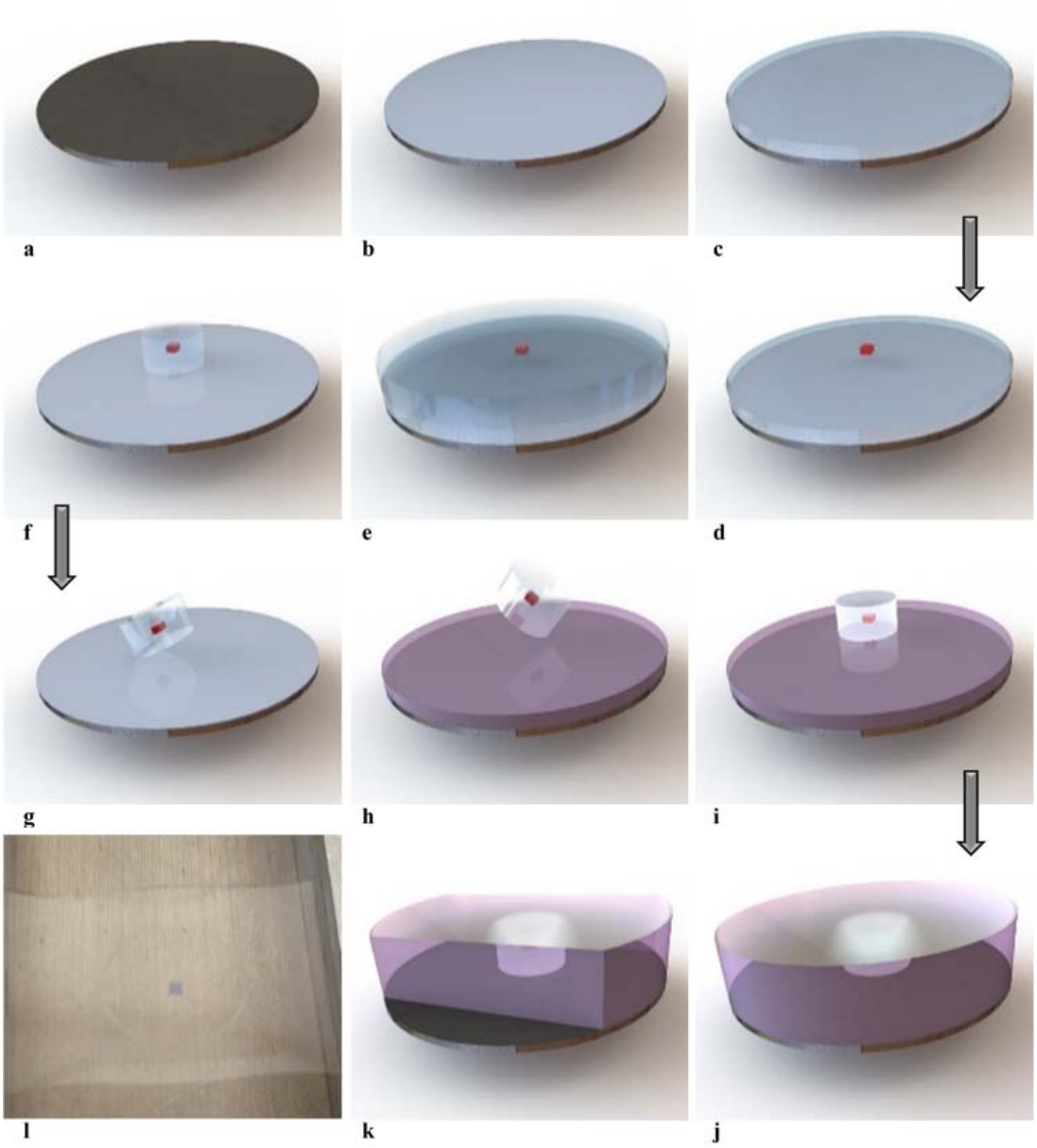

Figure A1. Fabrication process of stretchable platform. **a,** Cleaning a bare silicon handle wafer. **b,** Coating a thin layer of gelatin (1%) to aid in release. **c,** Coating 10 µm-thick PDMS (5:1). **d,** Si chip transfer. **e,** Coating 60 µm-thick PDMS (5:1). **f,** reactive ion etching using SF_6 and O_2 plasma. **g-i,** Intermediate structure transfer onto handle wafer with 10 µm-thick PDMS (20:1). **j,** Coating 80 µm-thick PDMS (20:1). **k,** Cutting structure in rectangular shape for stretch test. **l,** Real sample after release from handle substrate.

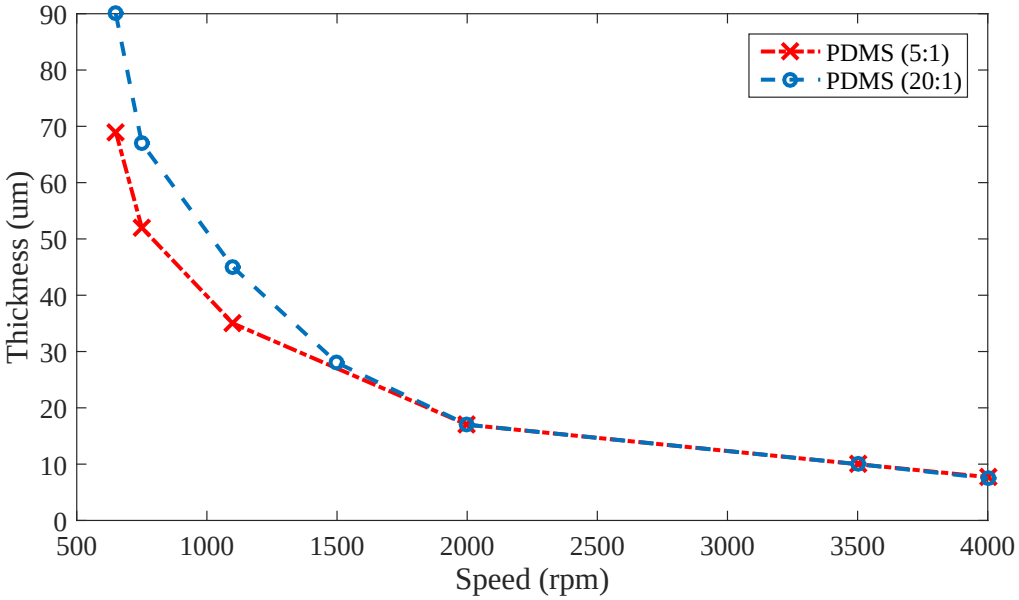

Figure A2. Thickness of PDMS (20:1) and PDMS (5:1) film under a range of spin speeds.

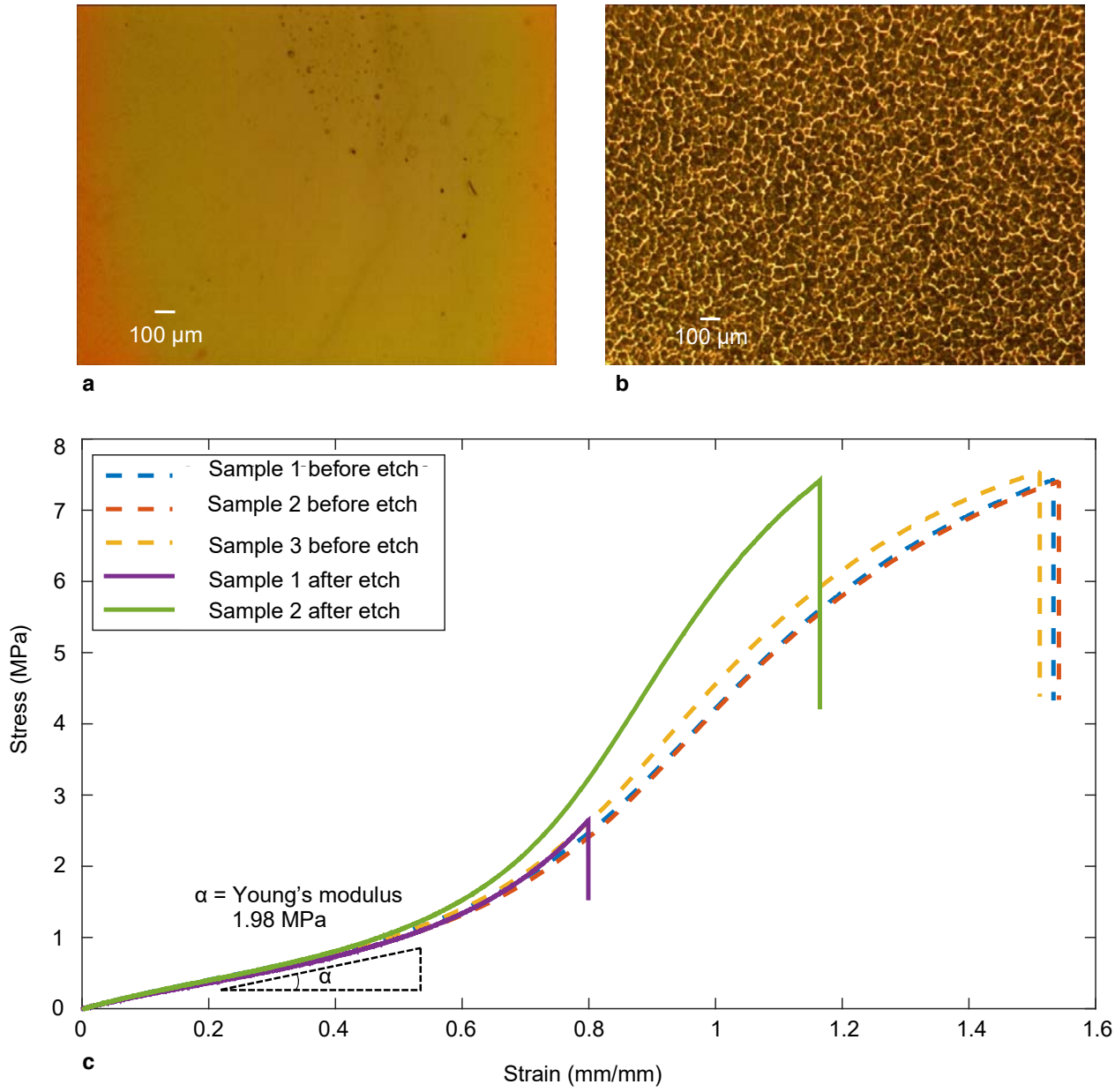

Figure A3. PDMS (5:1) surface before **(a)** and after **(b)** etch process (SF_6/O_2 plasma), **c,** Young's modulus comparison before and after etch process.

Appendix B: Young's modulus extraction test

Test process:

Our platform is composed of a Si chip and two polymers with different values of Young's modulus. One of these polymers used as an intermediate (PDMS (5:1)) and another one as a primary (PDMS (20:1)) material. These polymers should have different elasticity properties in order to accommodate the applied strain. Young's modulus of PDMS (5:1) and PDMS (20:1) are measured by an Instron 5940 testing machine. For each polymer, three samples are tested and the Young's modulus calculation is performed by using stress-strain curves that are shown in Figure B1 and B2. The Young's modulus of PDMS (20:1) and PDMS (5:1) for strains less than 100% are 1.98 MPa and 0.26 MPa, respectively.

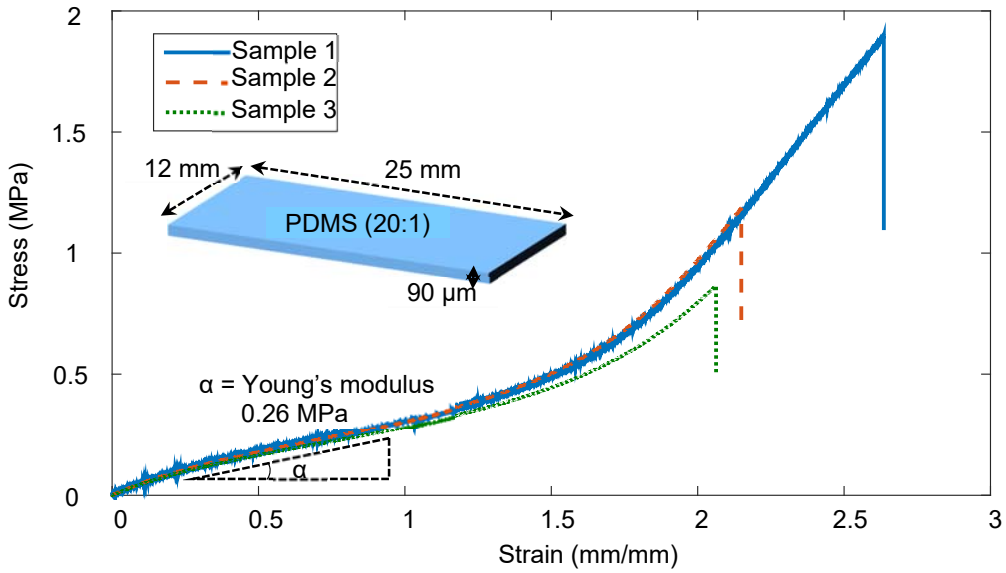

Figure B1. Young's modulus measurement for PDMS (20:1) film.

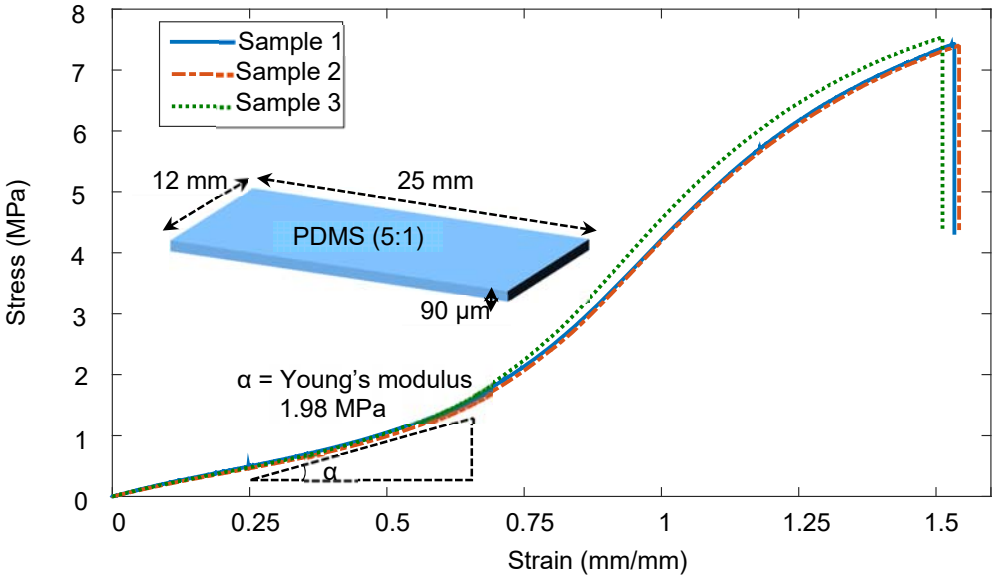

Figure B2. Young's modulus measurement for PDMS (5:1) film.

Appendix C: Thin silicon chip fabrication

Process details:

1. In this project thin Silicon chips were used as electronic chips in the test procedures. 50 µm thick silicon chips were fabricated using a 220 µm thick silicon 4" wafer (Figure C1a).
2. The wafer was scribed into 1mm×1mm squares (Figure C1b),
3. Then the scribed wafer was mounted on a substrate using a 70ºC heat release tape (Figure C1c).
4. The thickness of the 4" wafer was decreased to 50 µm using anisotropic etch process (SF_6 + C_4F_8). The recipe for deep reactive ion etching (DRIE) using Surface Technology Systems (STS) etcher process is provided in Table C1 and Table C2.

Table C1. DRIE recipe (Etch step)

Etch						
SF_6 flow (sccm)	O_2 flow (sccm)	Cycle time (sec)	Press (mT) APC	Coil power (W) (L %/T%)	Platen power (W) (L%/T%)	V_{pp} V_{dc}
130	13	12	19 58	600	12	265 62

Table C2. DRIE recipe (Passivation)

Passivation					
CF_6 flow (sccm)	Cycle time (sec)	Press (mT) APC	Coil power (W) (L %/T%)	Platen power (W) (L%/T%)	V_{pp} V_{dc}
85	8	12 58	600	--	--

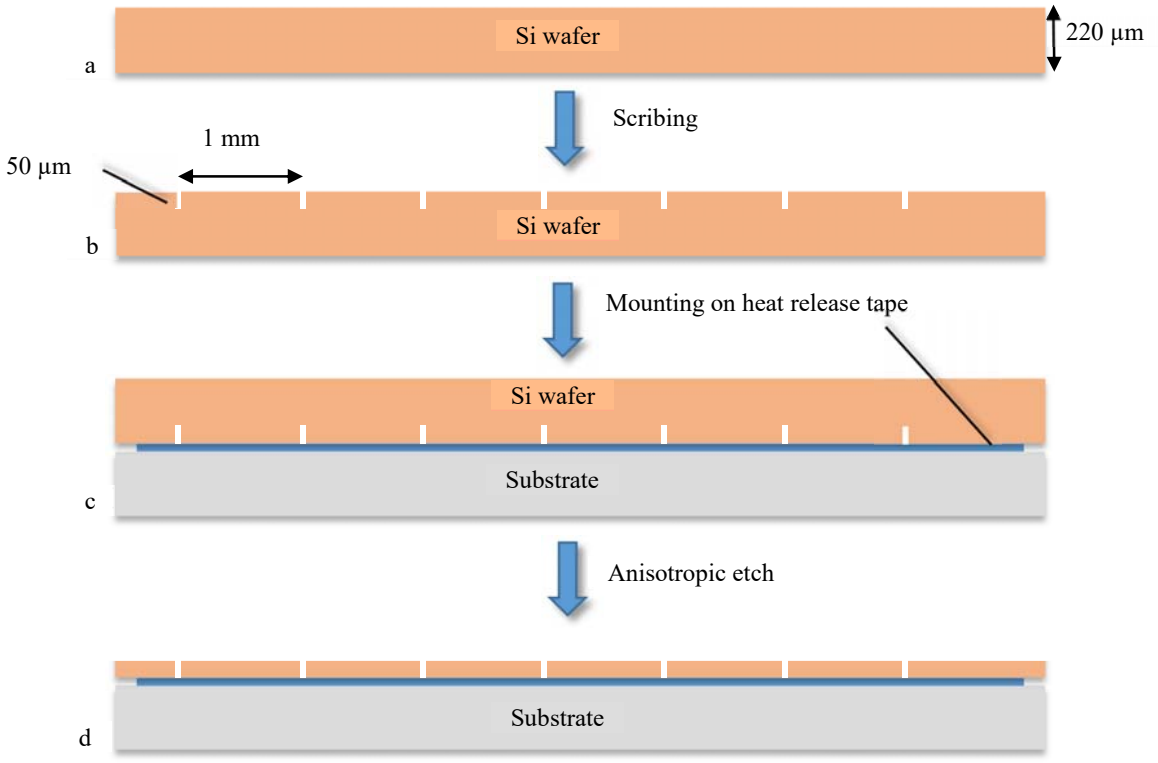

Figure C1. Thin silicon fabrication process. **a,** Preparing a silicon wafer. **b,** Scribing 50 µm deep trenches. **c,** Mounting the silicon wafer on a substrate using heat release tape. **d,** STS (anisotropic etch)

Appendix D: Interconnections fabrication

In this section the fabrication process of wires and structures with modified interfaces are discussed.

Process details:

5. PDMS solution preparation
    a. PDMS solution (Sylgard 184, Dow Corning) is created by mixing pre-polymer gel and the cross linker in a 5:1 (w/w) and 20:1 (w/w) ratio.
    b. The solution is agitated for 1 min for better mixing.
    c. The solution is placed in a vacuum chamber (Gast vacuum pump) for half of an hour to remove bubbles.
6. Spinning PMMA-A7 sacrificial layer
    a. 3'' Si wafer is cleaned with acetone and IPA.
    b. PMMA-A7 is spun at 3500 rpm for 45 seconds (Laurell WS-650Mz).
    c. The sample is then cured at 190 ºC for 2 min.
7. Metal sputtering
    a. 10 nm Cr is first sputtered on the PMMA layer (Perkin Elmer 8L) as an adhesion layer. The recipe is:

	Time (min)	DC power (W)	DC Current (A)	Target volts (V)	Chamber Pressure (Torr)
Pre sputter	10	100	0.353	282	20.07
sputter	1.5	30	0.110	270	20.03

b. 600 nm Cu is then sputtered on the Cr. The recipe is

	Time (min)	DC power (W)	DC Current (A)	Target volts (V)	Chamber Pressure (Torr)
Pre sputter	10	100	0.218	457	5.01
sputter	20	30	0.080	366	5.01

8. Lithography
    a. HDMS is spun on the wafer at 4000 rpm for 30 s as adhesion layer.
    b. AZ 4210 photoresist is then spun at 4000 rpm for 30 s to create 2.1 μm thick layer.
    c. It is then heated on the hot plate at 100 ºC for 1 min.
    d. The photoresist is exposed (Karl Suss MA6) at 5 mW/cm^2 for 200 s in vacuum mode.
    e. The exposed sample is developed in AZ developer for 1 min.
    f. After developing, it is rinsed with DI water and dried.
    g. The developed resist is flood exposed at 5 mW/cm^2 for 200 s. This is for photoresist removal after wet etching.
9. Wet etching
    a. The sample is placed on a 95 ºC hot plate for 1 min to increase the adhesion between the resist and film.

b. After baking, it is immersed in AL etchant for 60 s to pattern the top Cu layer and Cr layer.

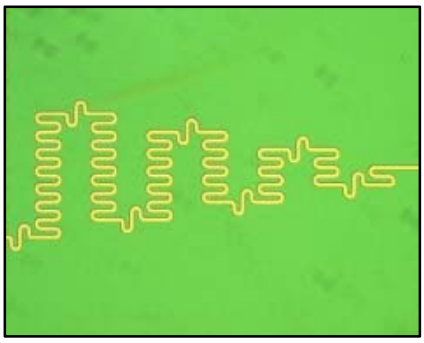

Figure D1. Patterned Cu/Cr layer on the PMMA layer.

c. The film is rinsed with DI water and dried.

d. The sample is immersed in AZ developer for 2 min to remove the photoresist.

e. The sample is rinsed with DI water and dried.

10. Spinning PDMS

a. Approach #1(Figure D2)

i. Intermediate PDMS (5:1) cylinder (thickness = 50 µm and Diameter = 3 mm) is placed on the middle of structure on top of wires. 1 µL PDMS (5:1) is used underneath of the cylinder as an adhesion layer.

ii. PDMS (20:1) is spun at 750 rpm for 1 min to get 70 µm film on the sample

iii. The sample is cured at 80 ºC for 30 min.

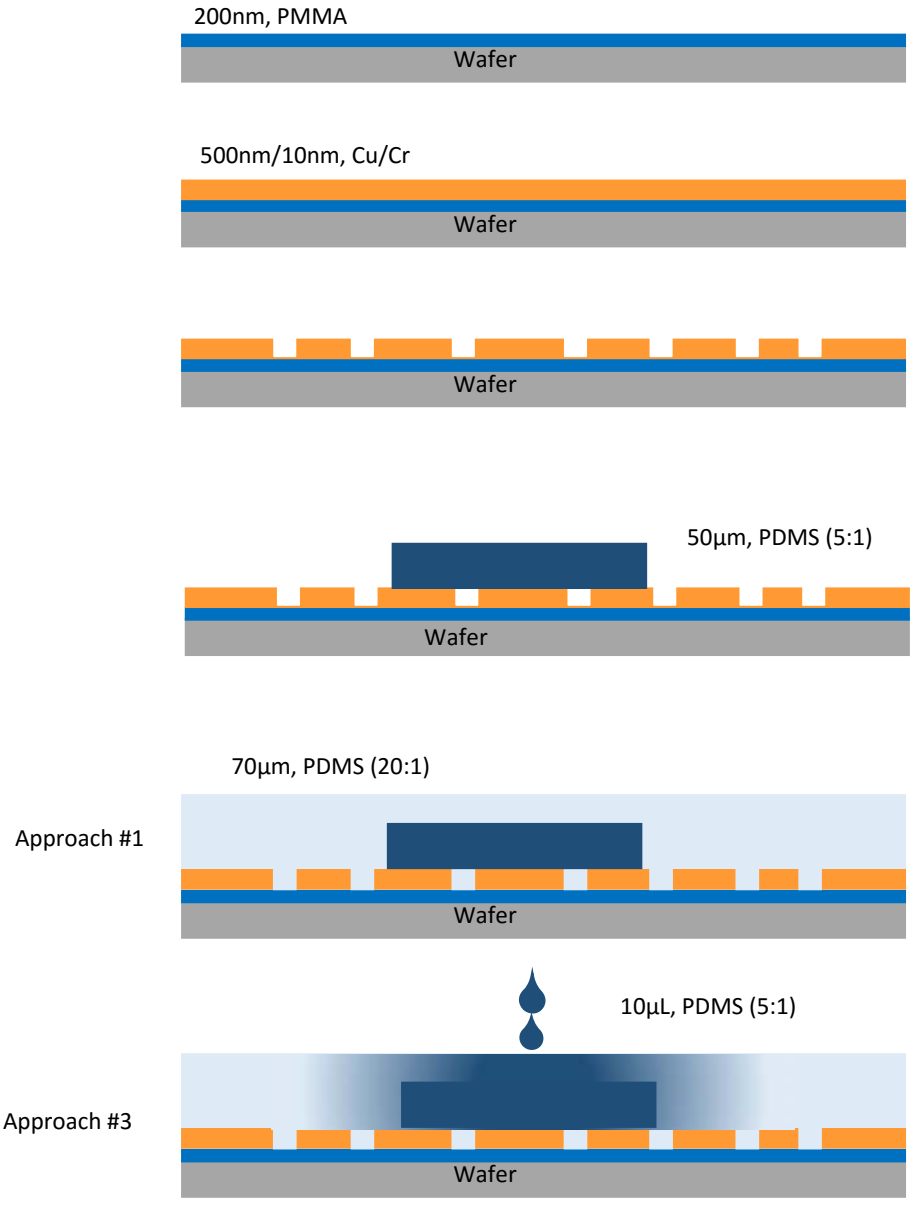

Figure D2. Approach #1 and #3 fabrication processes.

a. Approach #2 (Figure D3)

iv. PDMS (20:1) is spun at 750 rpm for 1 min to get 70 µm film on the sample

v. 10 µL, PDMS (5:1) droplet injected in the middle of the structure.

vi. The sample is cured at 80 ºC for 30 min.

b. Approach #3 (Figure D2)

vii. Intermediate PDMS (5:1) cylinder (thickness = 50 µm and Diameter = 3 mm) is placed on the middle of structure on top of wires. 1 µL PDMS (5:1) is used underneath of the cylinder as an adhesion layer.

viii. PDMS (20:1) is spun at 750 rpm for 1 min to get 70 µm film on the sample

ix. 10 µL, PDMS (5:1) droplet injected in the middle of the structure.

x. The sample is cured at 80 ºC for 30 min.

11. Releasing the structure

a. The structure is released by immersing it in acetone for 30 min

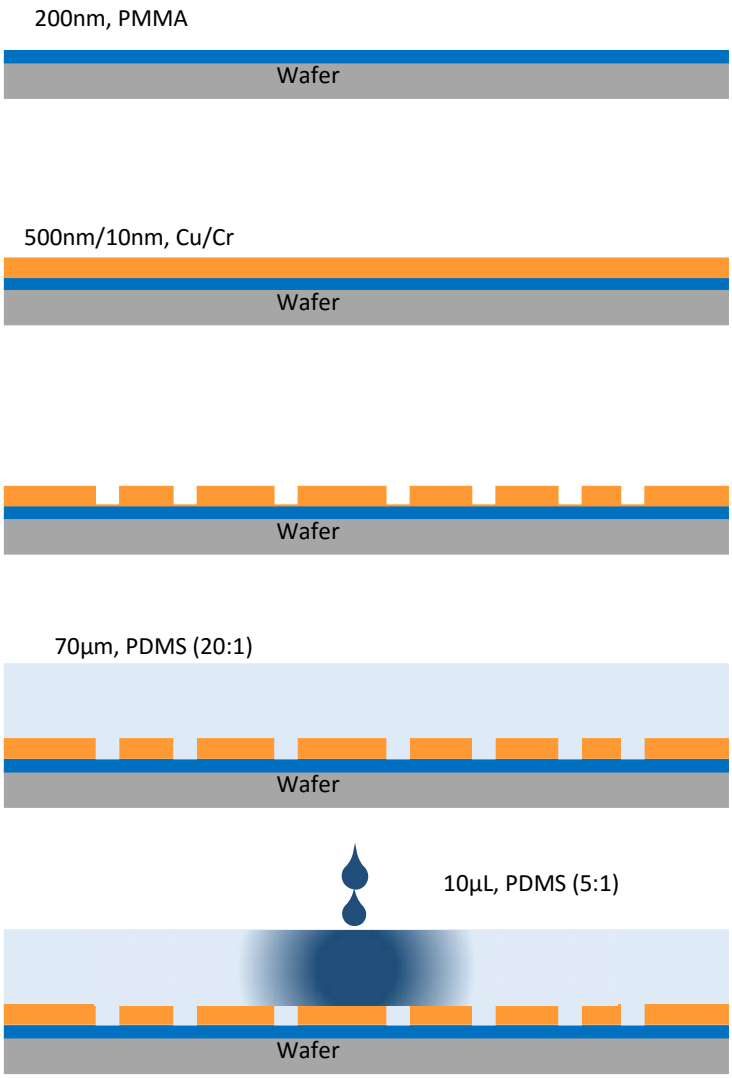

Figure D3. Approach #2 fabrication processes.

Appendix E: Embedded wires fabrication

Process details:

1. Gelatin solution preparation.
    a. Gelatin powder (250 bloom, Modernist Pantry) is mixed with DI water (gelatin: water 1:99 w/w).
    b. The mixture is then heated in the oven at 60 ºC for 1 hour to dissolve.
2. PDMS solution preparation.
    a. PDMS solution (Sylgard 184, Dow Corning) is created by mixing pre-polymer gel and the cross linker in a 20:1 (w/w) ratio.
    b. The solution is agitated for 1 min for better mixing.
    c. The solution is placed in a vacuum chamber (Gast vacuum pump) for half of an hour to remove bubbles.
3. Spinning gelatin sacrificial layer.
    d. 4'' Si wafer is cleaned with acetone and IPA.
    e. The heated gelatin mixture is spun at 1000 rpm for 10 seconds (Laurell WS-650Mz).

f. The sample is then dried in at room temperature to form a submicron sacrificial gelatin layer.

4. Spinning the first layer of PDMS (20:1).
    a. The PDMS (20:1) solution is spun on the gelatin at 3500 rpm for 60 s to form 10 μm thick PDMS (5:1) layer.
    b. The sample is then cured at 80ºC for 40 min.
5. Metal evaporation.
    a. 5 nm Cr is first evaporated on the PDMS (Ultek E-Beam Evaporator) as an adhesion layer. The recipe is:

Voltage (V)	Current (mA)	Pressure (T)	Deposition Rate (Å/s)
6000	40-50	1e-6 to 2e-6	1

    b. 200 nm Al is then evaporated on the Cr . The recipe is

Voltage (V)	Current (mA)	Pressure (T)	Deposition Rate (Å/s)
6000	60-100	1e-6 to 2e-6	1

    c. Another 5 nm Cr is evaporated on the Al to create the sandwich structure.
6. Lithography.
    a. HDMS is spun on the wafer at 4000 rpm for 30 s as adhesion layer.
    b. AZ 4210 photoresist is then spun at 4000 rpm for 30 s to create 2.1 μm thick layer.
    c. It is then heated on the hot plate at 80 ºC for 5 min. The initial temperate is 20 ºC and the ramping rate is 5 ºC/min.
    d. The photoresist is exposed (Karl Suss MA6) at 5 mW/cm^2 for 120 s.

e. The exposed sample is developed in AZ developer (AZ developer: water 1:1) for 2 min.

f. After developing, it is rinsed with DI water and dried.

g. The developed resist is flood exposed at 5 mW/cm^2 for 200 s. This is for photoresist removal after wet etching.

7. Wet etching.

   a. The sample is placed on a 50 ºC hot place for 10 min to increase the adhesion between the resist and film.

   b. After baking, it is first immersed in Cr etchant for 20 s to pattern the top Cr layer.

   c. After etching, the film is rinsed with DI water and dried. Then, it should be placed back on the 50 ºC hot place for 10 min.

   d. The sample is immersed in the Al etchant for 300 s to pattern the Al layer.

   e. The film is rinsed with DI water and dried. Then, it should be placed back on the 50 ºC hot place for 10 min.

   f. The sample is then immersed in the Cr etchant for 20 s to pattern the bottom Cr layer.

   g. The film is rinsed with DI water and dried. Then, it should be placed back on the 50 ºC hot place for 10 min.

   h. The sample is immersed in AZ developer for 2 min to remove the photoresist.

   i. The sample is rinsed with DI water and dried (Figure E1).

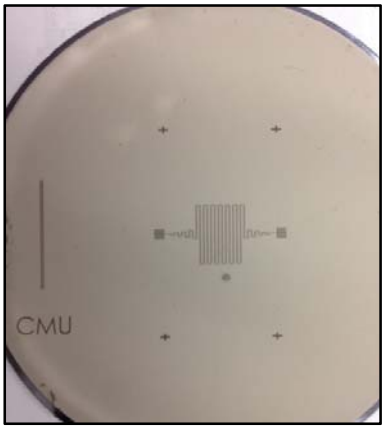

Figure E1. Patterned AL wires on PDMS after wet etching

8. Spinning the second layer of PDMS.
    a. The PDMS (20:1) solution is spun on the gelatin at 750 rpm for 60 s to form 60~70 μm thick PDMS layer.
    b. The sample is then cured at 80ºC for 40 min.
9. Releasing the structure
    a. The sample is released in hot water (50 ºC, 10 min), (Figure E2).

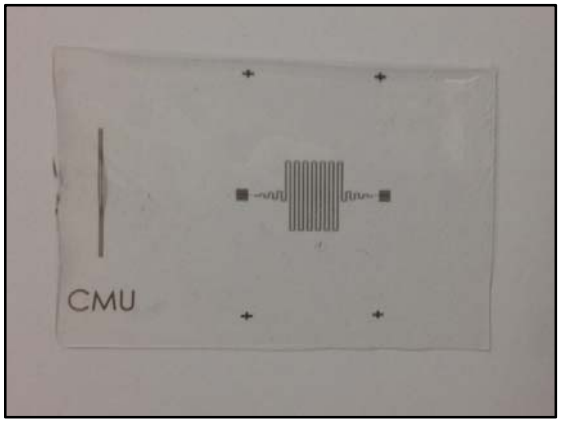

Figure E2. Embedded wires in PDMS after releasing stage

Figure E3. Embedded wires in a PDMS stretchable system under controlled strain conditions with no strain (a) and then under highly strained conditions (b).

Appendix F: Digital image correlation

Digital Image Correlation (DIC) is an innovative optical technique for accurate 2D and 3D measurements of changes in images. This is often used to measure deformation, displacement, strain, and optical flow. DIC is cost effective and simple to use approach compared to other techniques, and subjective than manual measurement methods. Digital image correlation (DIC) techniques have been increasing in popularity, especially in micro- and nano-scale mechanical testing applications due to its relative ease of implementation and use [75].

By comparing digital photographs of a component before and after a test at different stages of deformation (Figure F1), DIC can measure deformation. By tracking blocks of pixels, the system can measure surface displacement and build up full field 2D and 3D deformation vector fields and strain maps. The pixel blocks need to be random and unique with a range of contrast and intensity levels to get an efficient performance.

In this work, Matlab-based DIC code, which is an online DIC software for measuring deformation, strain and displacement was used [73].

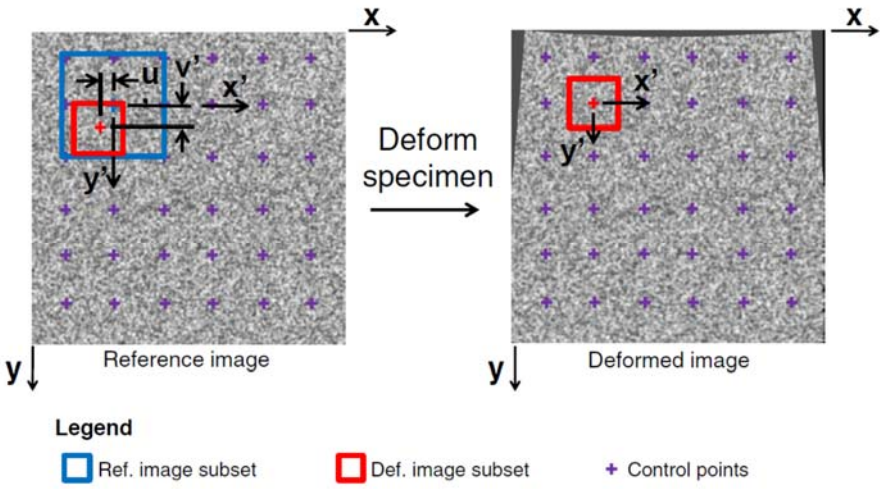

Figure F1. Schematic of digital image correlation methodology. A grid of control points (purple crosses) is defined over the region of interest. The normalized cross-correlation coefficient is computed by convolving a subset in the deformed image (red box) with the corresponding larger subset in the reference image (blue box). The actual displacement (u, v) is the displacement that maximized the correlation coefficient [73].