SAR ADCs Design and Calibration in Nano-scaled Technologies

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Shaolong Liu

B.S., Electrical Engineering, Beijing University of Technology, Beijing, China

M.S., Electrical Engineering, Peking University, Beijing, China

Carnegie Mellon University

Pittsburgh, PA

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ABSTRACT

The rapid progress of scaling and integration of modern complimentary metal oxide semiconductor (CMOS) technology motivates the replacement of traditional analog signal processing by digital alternatives. Thus, analog-to-digital converters (ADCs), as the interfaces between the analog world and the digital one, are driven to enhance their performance in terms of speed, resolution and power efficiency. However, in the presence of imperfections of device mismatch, thermal noise and reduced voltage headroom, efficient ADC design demands new strategies for design, calibration and optimization.

Among various ADC architectures, successive-approximation-register (SAR) ADCs have received renewed interest from the design community due to their low hardware complexity and scaling-friendly property. However, the conventional SAR architecture has many limitations for high-speed, high-resolution applications. Many modified SAR architectures and hybrid SAR architectures have been reported to break the inherent constraints in the conventional SAR architecture. Loop-unrolled (LU) SAR ADCs have been recognized as a promising architecture for high-speed applications. However, mismatched comparator offsets introduce input-level dependent errors to the conversion result, which deteriorates the linearity and limits the resolution and the resolution of most reported SAR ADCs of this kind are limited to 6 bits. Also, for high-resolution SAR ADCs, the comparator noise specification is very stringent, which imposes a limitation on ADC speed and power-efficiency. Lastly, capacitor mismatch is an important limiting factor for SAR ADC linearity, and generally requires dedicated calibration to achieve efficient designs in terms of power and area.

In this work, we investigate the impacts of offset mismatch, comparator noise and capacitor mismatch on high-speed SAR ADCs. An analytical model is proposed to estimate the resolution and predict the yield of LU-SAR ADCs with presence of comparator offset mismatch. A background calibration technique is proposed for resolving the comparator mismatch issue. A 150-

MS/s 8-bit LU-SAR ADC is fabricated in a 130-nm CMOS technology to validate the concept. The measured result shows that the calibration improves the SNDR from 33.7-dB to 42.9-dB. The ADC consumes 640 μW from a 1.2 V supply with a Figure-of-Merit (FoM) of 37.5-fJ/conv-step. Moreover, the bit-wise impact of comparator noise is studied for LU-SAR ADCs. Lastly, an extended statistical element selection (SES) calibration technique is proposed to calibrate the capacitor mismatch in SAR ADCs. Based on these techniques, a high-resolution, asynchronous SAR architecture employing multiple comparators with different speed and noise specifications to optimize speed and power efficiency. A 12-bit prototype ADC is fabricated in a 1P9M 65nm CMOS technology, and fits into an active area of 500 μm × 200 μm. At 125 MS/s, the ADC achieves a signal-to-noise-and-distortion ratio (SNDR) of 64.4 dB and a spurious-free-dynamic-range (SFDR) of 75.1 dB at the Nyquist input frequency while consuming 1.7 mW from a 1.2 V supply. The resultant figure-of-merit (FoM) is 10.3 fJ/conv-step.

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Chapter 1 : INTRODUCTION

1.1 Motivation

The fast evolvement in scaling and integration of modern complimentary metal oxide semiconductor (CMOS) technology motivates the replacement of traditional analog signal processing by digital alternatives in nano-scale technologies. Thus, analog-to-digital converters (ADCs), as the interfaces bridging the analog world and the digital one, are driven to enhance their performance in terms of speed, resolution and power efficiency.

Among various ADC topologies, successive approximation register (SAR) ADCs have particularly attracted extensive attention from the scientific community. The motivation is basically threefold. First, SAR ADCs, which consist of comparators, capacitors, and logic circuits, can maintain a large voltage input range without resorting to static circuits such as amplifiers. This is a very desirable feature, especially for ADCs realized in nano-scaled processes that present reduced supply voltage and limited intrinsic transistor gain. Second, the absence of static circuitry and switching-intensive operation enables SAR ADCs to attain excellent power efficiency compared to amplifier-based ADCs. Finally, the linearity of a SAR ADC relies mainly on the matching property of capacitors, which has benefited from advances in lithography. Consequently, the SAR ADC topologies have been recently employed in designs with specifications that used to be met with other topologies such as delta-sigma and pipeline, e.g. resolution ≥12 bits [1]- [12] and multi-GHz operation speed [4]- [8].

However, in nano-scale technologies device mismatch, such as capacitor mismatch and comparator offset mismatch, drastically brings down the performance and yields of the SAR ADCs. There are basically two approaches to solve this problem. First, according to Pelgrom scaling rule [33], the device mismatch issue can be alleviated by increasing its dimensions, which, however, inevitably compromises the power efficiency and performance. Second, various calibration

techniques can be applied to counter the mismatch issue by inserting redundancy in the design to cover the technology variations and/or post-processing the raw output. The second approach is more appealing as it is able to minimize the overhead and preserve the advantages of technology scaling. Furthermore, the scaled technologies render cheap implementations for calibration circuits, especially if they are digital-extensive.

1.2 ADC architectures and performance review

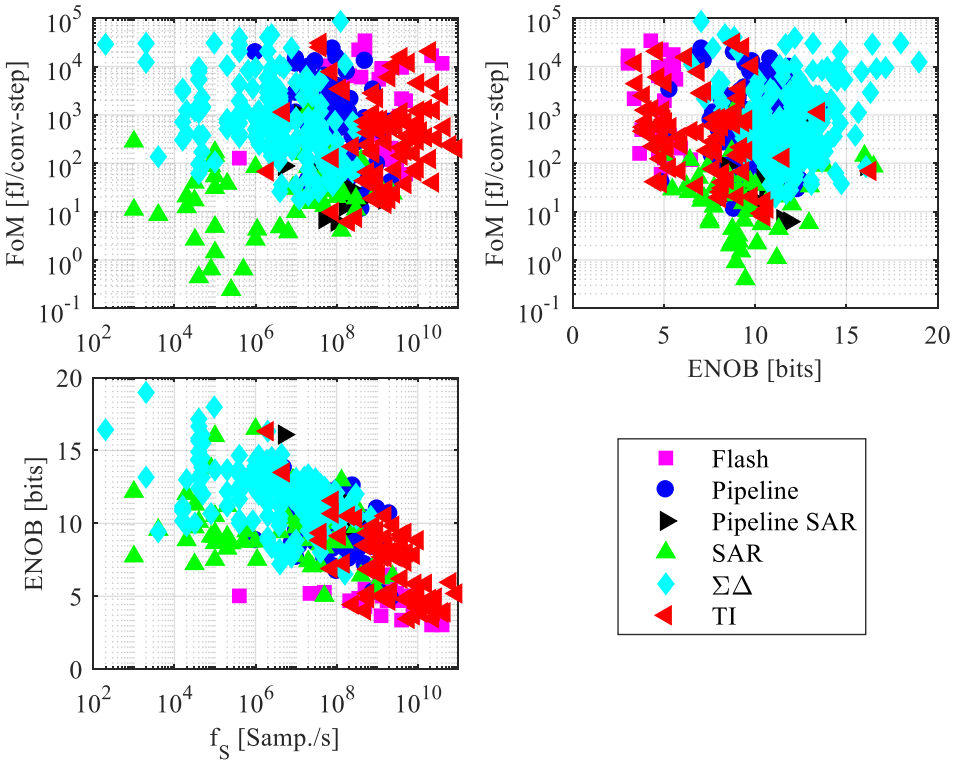


Figure 1-1. ADC performance survey from publications in ISSCC and VLSI 1997-2017 [47]

Figure 1-1 shows performance survey of major ADC architectures published in ISSCC and VLSI conferences from 1997 to 2017, in terms of effective-number-of-bits (ENOB), sampling rate and Weldon figure-of-merit (FoM). It can be seen that Flash architecture is popular for low-resolution, high-speed applications due to its high conversion rate. However, it is hard to survive in high-resolution applications as the power and hardware overhead increases exponentially with ADC resolution. Second, Pipeline ADC makes a balance between conversion speed and resolution. This

multi-step data conversion distributes the conversion task into different stages and time slots to increase the timing and hardware efficiency. Also, inter-stage gain helps suppress the noise/offset impacts from the later stages. However, it becomes harder and harder to design high performance amplifier, which prevents pipeline ADC from migrating to deeply scaled technologies. As we previously pointed out, SAR ADC benefits significantly from the technology scaling because fast logic circuits permit high SAR conversion speed, high lithography means high improved achievable resolution. All these results in improved FoM for SAR ADCs. However, the multi-step conversion manner limits its conversion speed. Another important type of ADC is sigma-delta (Σ-Δ) ADC, which is a type oversampling ADC. Although the resolution of each sample result is low, the quantization results from sample to sample are correlated. The noise shaping characteristic established by integrator(s) and feedback loop pushes the quantization noise to high frequency beyond the signal bandwidth. This renders Σ-Δ ADCs capabilities of achieving high resolution. However, effective signal bandwidth of a Σ-Δ ADC is much smaller than its sampling frequency due to oversampling. Lastly, time-interleaved ADCs have been very popular in recently years for achieving high conversion rates [6] [8], [48], [49]. Ideally, the ADC sampling rate scales proportionally with the number of channels while keeping FoM as the same as channel ADC by means of time-interleaving. However, timing/gain mismatches and offset between channels greatly limited the efficiency and achievable resolutions, and dedicated calibration and optimization are required to alleviate these imperfections, and therefore reduces the power efficiency of TI ADCs.

1.3 Contributions

This dissertation largely has following contributions:

First, we, for the first time, quantitatively analyzed the offset impact on loop-unrolled (LU) SAR ADCs, and proposed a statistical model to predict the expected resolution and yield of an LU SAR ADC design with a given offset standard deviation of its comparator design.

Second, we proposed a LU SAR architecture with offset background calibration to efficiently improve its achievable resolution and power efficiency and implemented an 8-bit prototype to

verify the effectiveness of the calibration.

Third, we, for the first time, quantitatively analyzed the bit-wise impact of comparator noise on SAR ADC resolution, and proposed a strategy for optimizing the power efficiency, noise and speed of high resolution SAR ADCs.

Fourth, an extended SES calibration technique with large calibration range was proposed for calibrating DAC capacitor mismatch for high resolution SAR ADCs.

Lastly, a 12-bit asynchronous SAR ADC was implemented to verify our proposed noise, speed and power efficiency optimization technique and capacitor mismatch calibration technique.

1.4 Dissertation organization

This dissertation consists of 8 chapters. Following this chapter of introduction, Chapter 2 illustrates the operation of SAR architecture and design challenges. Chapter 3 presents our analysis of comparator offset mismatch impacts on the linearity of loop-unrolled (LU) SAR ADCs and our proposed statistical model. In Chapter 4, the dependence of effective resolution of SAR ADCs on comparator noise is derived and presented, and bit-wise examinations of noise impact is studied. Chapter 5 presents our proposed statistical calibration technique for SAR ADCs. Chapter 6 presents our 8-bit LU SAR ADC prototype with comparator offset background calibration, followed by Chapter 6, where a 12-bit asynchronous high-speed SAR ADC prototype with comparator noise optimization and SES capacitor calibration is presented. Finally, in Chapter 8, we summarize this dissertation and present a few potential directions of future work.

Chapter 2 : SAR ADC ARCHITECTURE AND DESIGN CHALLENGES

SAR ADCs are an increasingly attractive architecture in nano-scaled CMOS technologies. Thanks to the fact that SAR ADCs, which comprise comparators, capacitors, and logic circuits, can maintain a large voltage input range without resorting to static circuits such as amplifiers. However, SAR ADCs also face important challenges in the context of applications with more and more demanding bandwidth, power-efficiency and resolution. In this chapter, we review the SAR ADC operation and design challenges in terms of capacitor mismatch, thermal noise and speed. Also, asynchronous SAR architecture, which has been widely used to improve the conversion speed, is also discussed.

2.1 SAR ADC architecture and principle

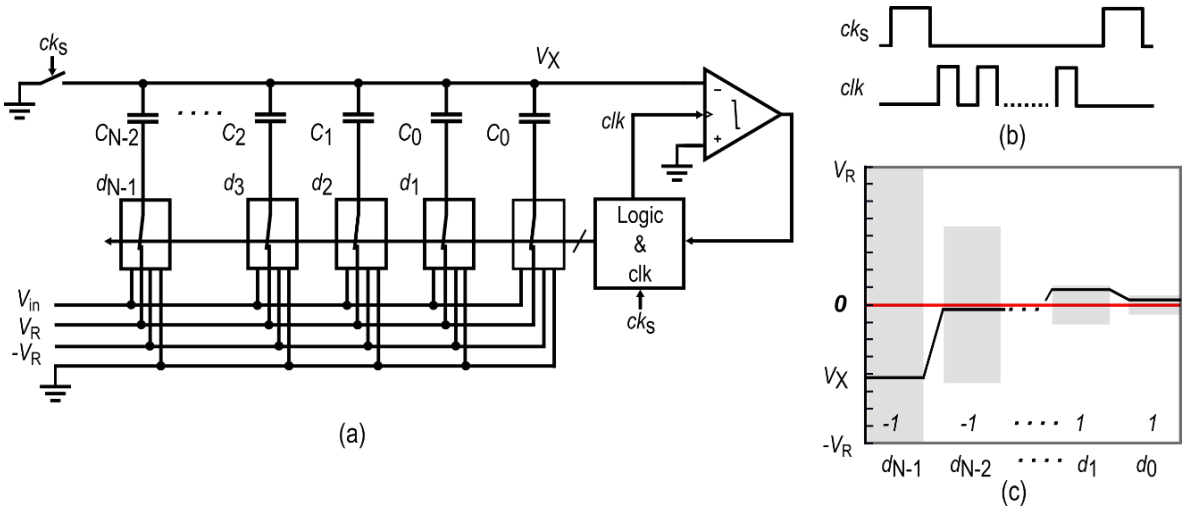


Figure 2-1. Schematic diagram of a conventional N-bit CR SAR ADC

Figure 2-1 shows the diagram of a traditional *N*-bit charge redistribution (CR) SAR ADC, which consists of switches, an *N*-bit capacitive DAC, a comparator and a digital comparator. The conversion of the SAR ADC works in a sequential binary search fashion. During the SAR operation,

the feedback mechanism tries to minimize the voltage seen by the comparator at the summing node, V_X, by approximating the DAC output to the input V_{in} illustrated by

$$V_{X,i} = V_{in} - V_R \sum_{j=N-1}^{i} \frac{d_j C_j}{C_{total}}, \tag{2-1}$$

where index $i = N\text{-}1, N\text{-}2, \ldots, 0$. After all the bits are resolved, the absolute value of the final summing node voltage $V_{X,0}$ should be less than 1/2 LSB of the N-bit DAC if all the blocks are ideal. Then V_{in} can be estimated according to the resulting DAC inputs by

$$\begin{aligned} V_{in} &= V_R \sum_{j=N-1}^{0} \frac{d_j C_j}{C_{total}} + QE \approx V_R \sum_{j=N-1}^{0} \frac{d_j C_j}{C_{total}}, \\ QE &= V_{X,0}, \end{aligned} \tag{2-2}$$

where QE denotes the quantization error of the conversion.

However, in a real implementation, various non-idealities and challenges are involved in the conversion and undermine the accuracy of the conversion. Also, the sequential operation manner of the conventional SAR prevents it moving to high-speed applications.

2.2 Design challenges in high-speed and high-resolution SAR ADCs

2.2.1 Thermal noise

Thermal noise affects the linearity of an SAR ADC largely in two ways. First, during the sampling phase the thermal noise arising from switch resistances cannot be separated after the input signal is sampled, which is the well-known KT/C noise and can be calculated by

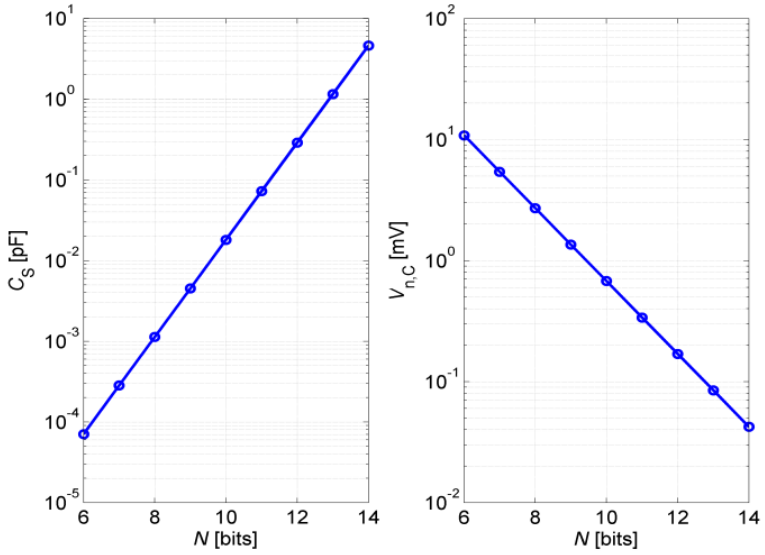
$$V_{n,S}^2 = KT / C_S \tag{1-3}$$

where K is the Boltzmann constant, T the absolute temperature and C_S the total sampling capacitance. One can see that the integrated noise power only depends on sampling capacitance in a given temperature, which means that as the resolution target goes higher, a larger sampling capacitance should be chosen. The other vital noise source is from the thermal noise of the

comparator which might trigger the comparator to a wrong output when the summing node voltage is comparable to the input referred noise level, $V_{n,c}$. The signal-to-noise ratio (SNR) of the SAR ADC considering these two noise sources can be calculated by,

$$\begin{aligned} \mathrm{SNR} &= \frac{V_R^2}{2(KT/C_S + V_{n,C}^2 + QN)}, \\ QN &= \frac{LSB^2}{12} = \frac{1}{12}\left(\frac{2V_R}{2^N}\right)^2, \end{aligned} \tag{2-4}$$

where QN represents the quantization noise, V_R the reference voltage of the DAC. Figure 2-2 (a) and (b) shows the minimum sampling capacitance and maximum comparator noise (rms value) requirements targeting for a 3 dB SNR (0.5 bit) loss with V_R=1.2V, respectively.



(a) (b)

Figure 2-2. (a) Sampling capacitance and (b) comparator noise requirements for < 3 dB SNR loss target

There are two important observations from Figure 2-2. First, the minimum capacitance increases exponentially as the resolution increases. Second, for high resolution ADCs, the noise performance is very challenging. For example, $V_{n,C} \approx 100\mu V$ for $N = 13$ bits. Thus, power budget for comparator needs to be increased and/or comparison speed needs to be slowed down resulting in a smaller bandwidth to reduce the integrated noise .

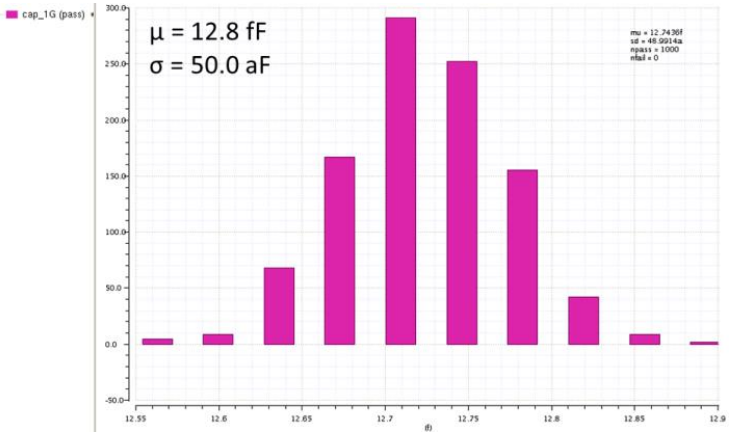


Figure 2-3. Monte-Carlo simulation histogram of a 12.8 fF MOM capacitor in a 65-nm CMOS technology

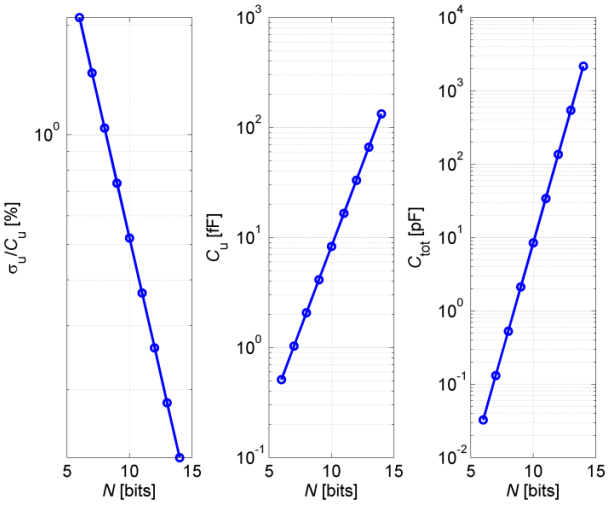


Figure 2-4. Mismatch requirement of capacitance aiming at DNL<1/2 for binary N-bit ADCs

2.2.2 Capacitor mismatch and sub-2-radix SAR ADC

In binary weighted SAR ADC, the capacitance mismatch is a significant problem as it modifies (2-1) to

$$V_{\mathrm{X},i} = V_{\mathrm{in}} - V_{\mathrm{R}} \sum_{j=N-1}^{i} d_j 2^{j-N} - V_{\mathrm{R}} \sum_{j=N-1}^{i} \frac{d_j \Delta C_j}{C_{\mathrm{total}}}, \tag{2-5}$$

where the first two terms in the RHS reflect the ideal behavior while the third term represents the

extra error resulted from capacitance mismatch. The most straightforward way to mitigate the problem is by increasing the dimensions and therefore the capacitance of the unit capacitor. According to Pelgrom scaling rule [33], [68], [69], the relative matching property of a metal capacitor in CMOS technology can be described as

$$\sigma\left(\frac{\Delta C}{C}\right)=\frac{K_{\mathrm{C}}}{\sqrt{C}}, \tag{2-6}$$

where K_{C} is Pelgrom's coefficient for the dependence of σ(ΔC/C) on the capacitance and only depends on the technology and the capacitor structure employed. (2-5) and (2-6) implies that the matching property can be improved by sizing up the unit capacitance in binary SAR ADCs.

The minimum unit capacitance based on matching consideration can be estimated from the perspective of differential non-linearity DNL [31]. The largest DNL generally occurs at the middle code as the number of switched capacitors from code 100…0 to code 011…1 is 2^N-1 and is larger than that between any other consecutive codes, then the standard deviation of DNL at the middle code can be estimated as

$$\sigma\left(\mathrm{DNL}_{\mathrm{mid}}\right)=\sigma\left(\frac{\Delta C_{N-1}-\sum_{i=N-2}^{0}\Delta C_i}{C_{\mathrm{total}}}\frac{V_{\mathrm{R}}}{\mathrm{LSB}}\right)=2^N\sigma\left(\frac{\Delta C_{N-1}-\sum_{i=N-2}^{0}\Delta C_i}{C_{\mathrm{total}}}\right). \tag{2-7}$$

If we assume the unit capacitances are independent and identically distributed (i.i.d.) normal variables, one can easily have

$$\sigma\left(\mathrm{DNL}_{\mathrm{mid}}\right)\approx 2^N\sigma\left(\frac{\sum_{i=N-1}^{0}\Delta C_i}{2^N C_{\mathrm{u}}}\right)=\sqrt{2^N-1}\sigma\left(\frac{\Delta C_{\mathrm{u}}}{C_{\mathrm{u}}}\right), \tag{2-8}$$

where C_{u} is the unit capacitance of the DAC. If we aim at DNL < 0.5 within 3-sigma control limit, the relative mismatch of unit capacitance can be calculated by

$$\sigma\left(\frac{\Delta C_{\mathrm{u}}}{C_{\mathrm{u}}}\right)<\frac{1}{3\sqrt{2^N-1}}. \tag{2-9}$$

Based on (2-6) and (2-9) the minimum unit capacitance and the total capacitance of the N-bit DAC can be determined. Figure 2-4 presents the required minimum relative mismatch, unit capacitance and total capacitance of an ADC with resolutions from 6 to 14 bits, respectively. The parameter K_c in (2-6) is extracted with $\sigma(\Delta C/C) = 1.5\%$ and $C = 1$ fF, which is inferred from our simulations of a metal-oxide-metal (MOM) capacitor from a 65 nm technology, shown in Figure 2-3, and the results provided in [31] [68], [69].

It can be seen from Figure 2-4 that it is extremely expensive and even infeasible ($C_{\text{total}} > 1$ nF for $N > 10$ bits) to achieve high resolution by solely relying in Pelgrom rule. Therefore, various analog or digital calibration techniques have been proposed to break this constraint. In [70], the authors proposed to correct the capacitor mismatch by adding an additional *small* DAC with adjustable reference voltage, which, similar to (2-1), can be modeled as,

$$\begin{aligned} V_{\text{X},i} &= V_{\text{in}} - \sum_{j=N-1}^{i} d_j \frac{V_{\text{R}}(1+\alpha_{\text{R},j})(C_j + \Delta C_j)}{C_{\text{total}}}, \\ \alpha_{\text{R},i} &= \frac{1}{1+\Delta C_j / C_j} - 1, \end{aligned} \tag{2-10}$$

where $\alpha_{\text{R},j}$ is the reference correction coefficient. The essence of this technique is to use adjustable reference to compensate the error resulted from its associated capacitance. This means that multiple reference sources or complicated generation circuits are needed. Alternatively, in many works such as [65], [71], the MSB capacitors are corrected in post manufacturing trimming which requires redundant small capacitor arrays insert during the design phase. However, this technique sometimes suffers from large step-size or large variations due to small dimensions of the compensation capacitors.

Another major calibration technique category for SAR ADCs is digital calibration such as [1], [2] and [63], where the conversion error induced by capacitor mismatch can be corrected in code domain without pursuit of absolute matching of capacitors. In presence of capacitance mismatch, (2-1) can be written as

$$V_{\mathrm{X},i} = V_{\mathrm{in}} - V_{\mathrm{R}} \sum_{j=N-1}^{i} \frac{d_j (C_{j,0} + \Delta C_j)}{C_{\mathrm{total}}} = V_{\mathrm{in}} - V_{\mathrm{R}} \sum_{j=N-1}^{i} d_j w_j,$$
$$w_j = \frac{C_{j,0} + \Delta C_j}{C_{\mathrm{total}}}. \tag{2-11}$$

The mismatched DAC can be modelled as a non-binary one considering capacitance variance. Instead of treating the mismatch of capacitors physically, if we somehow figure out the weight of individual capacitances the conversion output of the SAR ADC can be calibrated in code domain by

$$V_{\mathrm{in}} = V_{\mathrm{R}} \sum_{j=N-1}^{0} \frac{d_j C_j}{C_{\mathrm{total}}} + QE \approx V_{\mathrm{R}} \sum_{j=N-1}^{0} d_j w_j. \tag{2-12}$$

Nonetheless, the effectiveness of this approach is conditional. The authors of [72] have proved that the result is recoverable in digital domain as long as the non-binary DAC capacitors are scaled in sub-radix-2 manner, which means

$$C_i < \sum_{j=i-1}^{0} C_j. \tag{2-13}$$

Figure 2-5 compares the definition of sub-radix-2 against radix-2 (binary) and super-radix-2, respectively.

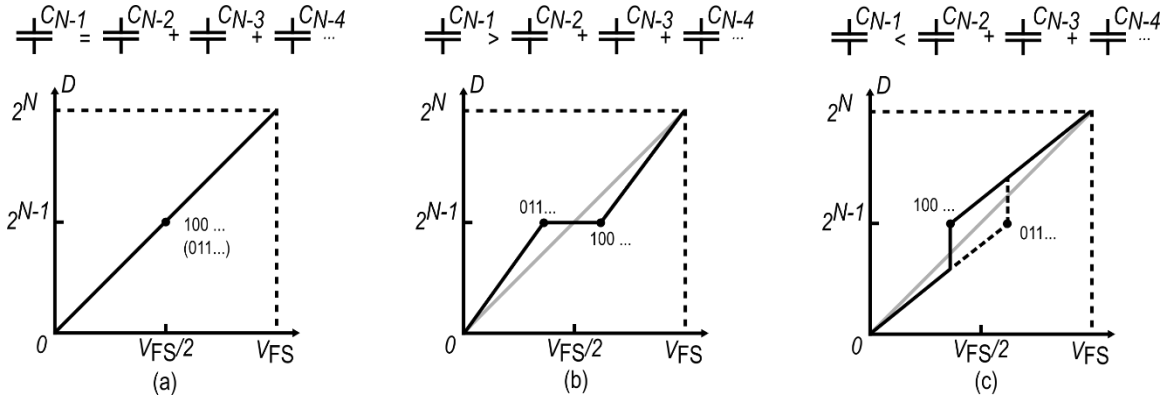


Figure 2-5. Transfer curves with (a) radix-2, (b) super-radix-2 and (c) sub-radix-2 in MSB

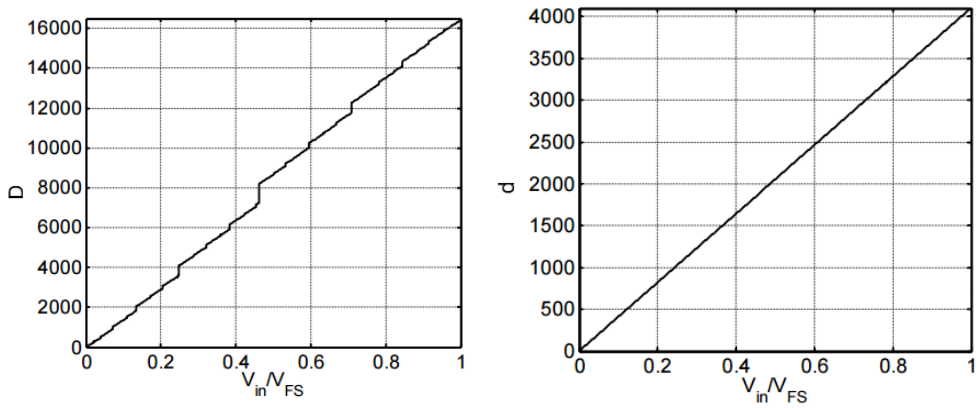


Figure 2-6. Transfers curve of a 12-bit sub-radix-2 SAR ADC before and after calibration

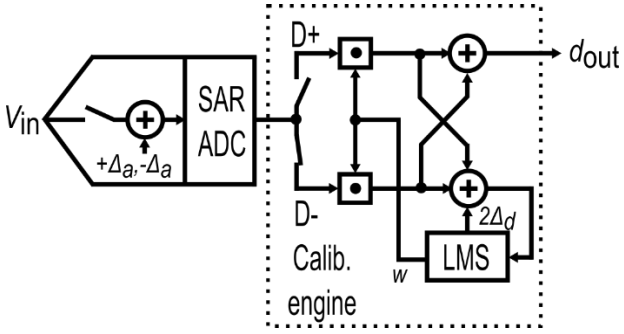


Figure 2-7. Diagram of the offset double conversion (ODC) calibration [1] for sub-radix-2 SAR ADCs

However, due to the sub-radix-2 scaling, the effective resolution of an N-bit SAR ADC should be smaller than N and can be calculated by

$$ENOB \le \log_2\left(\frac{1-r^N}{1-r}+1\right), \tag{2-14}$$

where r is the radix or the scaling factor of the DAC capacitors. Figure 2-6 shows transfer curves of a 12-bit ADC (14 raw bits) before and after calibration.

For such weight-based digital calibration methods, another important step is to figure out the value of bit weights. Figure 2-7 presents the diagram of the offset-double-conversion (ODC) algorithm [1]. This algorithm requires the analog part of the ADC to quantize each input sample twice with opposite injections, $+\Delta_a$ and $-\Delta_a$, respectively. Then the two different outputs, D_+ and D_-, are compared to learn the weight vector, $W = [w_{N-1}, w_{N-2}, \dots, w_0]$, and Δ_d, the digital representative

of Δ_a, using an LMS based calibration engine. Meanwhile, the output of the ADC can be resolved by summing the weighted outputs (after correction), d_+ and d_-. Alternatively, there are also some other weight learning algorithms such as split-ADC [73] and numerous correlation based algorithms [2], [63]. All these calibration techniques are digital-intensive with minor modifications in analog circuit and, therefore, become very attractive in nano-scaled technologies.

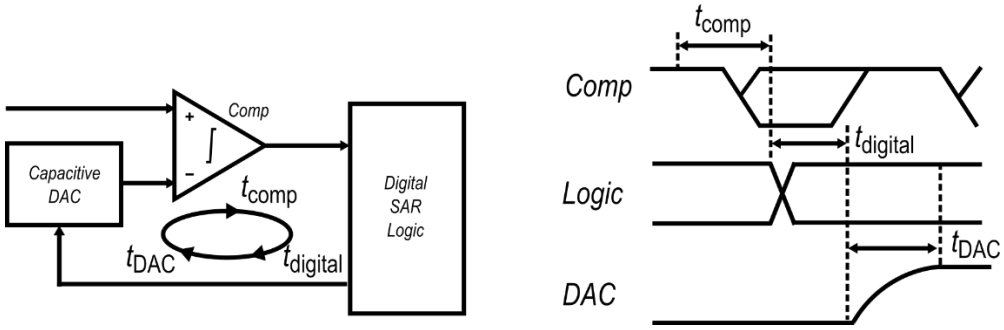


Figure 2-8. Illustration of bit cycle of SAR ADCs

2.2.3 Conversion speed and settling error

The speed of SAR ADC is bounded by its sequential conversion manner. As shown in Figure 2-8, the SAR critical path (for each bit) can be summarized as [11]:

$$T_{\text{critical}} = t_{\text{comp}} + t_{\text{digital}} + t_{\text{DAC}}, \tag{2-15}$$

where t_{comp}, t_{digital} and t_{DAC} represent the comparator resolving time, the digital delay through the SAR feedback path and the DAC settling time, respectively.

The resolving time for comparator is a function of the input signal level as the larger the input signal, the faster the latch output are regenerated to logic level. The digital delay highly depends on the technology and logic circuit design. In high-speed design, dynamic logic and/or full custom design techniques are generally employed to optimize the speed [5]. DAC settling time arises from the fact that after resolving current bit and before moving to the next one, the summing node voltage V_X takes time to settle. A conversion error may occur if the comparator decision is being made before V_X settles to certain precision. In fact, adequate DAC settling sets the minimal time required

for a single conversion step, which also sets a limit of the SAR ADC conversion speed. One key factor limiting the DAC settling speed is the finite on-resistance, R_{on}, of the switches which connect the switching plates of capacitors to $\pm V_R$. To achieve an N-bit resolution, the settling error of V_X must be less than half of LSB. Thus, the required settling time for an N-bit SAR ADC is derived by

$$t_{DAC} > R_{on} C_{DAC} \ln\left(2^{N+1}\right). \tag{2-16}$$

One can see that settling requirement becomes more and more critical as resolution goes higher. The two basic approaches to improve the settling error are increasing the size of switches and minimizing the DAC capacitance. Nonetheless, reducing the on-resistance of switches leads to large parasitics and power consumption. The advantages of reducing the DAC capacitance are two-fold. First, it improves the speed according to (2-16), and second, the reduced DAC capacitance means low switching power for the reference sources. However, for high resolution, the matching requirement and thermal noise impose lower boundaries for the choice of DAC capacitance.

2.3 Asynchronous SAR ADC and design challenges

2.3.1 Loop-unrolled SAR ADC

To enhance the sampling rate of SAR ADCs, both the architecture and timing control have been thoroughly explored, aiming to overcome the timing constraint imposed by the sequential conversion. In [9], instead of using an external clock to trigger comparisons, an asynchronous SAR ADC internally generates the clock for the next comparison upon the completion of current comparison, thereby exploiting the dependency of comparator delay on its input level to optimize the bit conversion time budget and simplify the logic control circuits. In [5], a single-channel SAR ADC achieves >1 GS/s by means of alternating two comparators during the SAR conversion and eliminating the comparator reset phase in binary search clock cycles. A traditional single-bit comparator is replaced by a 2-bit flash quantizer in [10] to resolve 6 bits in 3 cycles, doubling the throughput of each cycle at the expense of increased comparator power consumption. In [4], [11], the loop-unrolled (LU) architecture (as shown in Figure 2-9) was proposed, which uses six

comparators instead of one for a 6-bit implementation. Similar to [5], the reset phase of the comparators is not in the SAR cycle. Instead, all the comparators are clocked only once for each sample and are reset together after all the bits are resolved. Another advantage of this architecture is that each latched comparator serves as part of SAR controller that feeds the comparison result directly to its corresponding DAC input buffer without additional delays from the logic circuit. This type of SAR architecture has also been used in SAR-assisted pipeline ADCs [12] and two-stage SAR ADCs [36] to improve the stage speed.

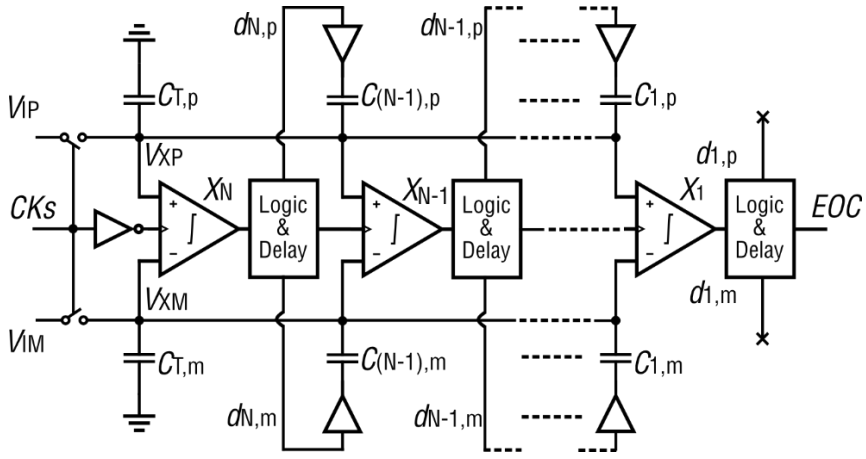


Figure 2-9. A loop-unrolled SAR ADC architecture [4], [11], [12].

In a conventional SAR ADC that uses a single comparator, the offset voltage of the comparator manifests itself as a shift in the ADC transfer curve by the same amount as the offset, without causing any distortion. An LU-SAR ADC, however, is affected by mismatched offsets among comparators similar to other comparator-based topologies such as the flash ADC. This issue becomes more severe as resolution increases, because of the least-significant-bit (LSB) voltage decreases exponentially. A corresponding decrease in comparator offset comes with large costs and compromises the advantages of the SAR architecture. For pipelined LU-SAR ADCs [12], the offset-induced error in the first stage can be recovered by redundancy between stages, while offset-induced errors in the later stages are suppressed by the inter-stage gain. Previously published 6-bit LU-SAR ADCs [4], [35] rely on foreground offset calibration to mitigate the offset mismatch issue.

However, this requires complicated power-on calibration and/or interruption of system operations when recalibration is needed due to process, voltage and temperature (PVT) variations. Also, the foreground calibration precision is limited. Recently in [34], an 8-bit LU-SAR architecture was proposed using hybrid of foreground calibration (on MSB comparators) and background calibration (on LSB comparators). The offset mismatch of the first 4 MSB comparators are coarsely mitigated by foreground calibration, and one redundant bit is, in part, to recover the error caused by offset mismatch. Nevertheless, the last 5 LSB comparators are all calibrated to have the same offset of a dedicated reference comparator, whose offset was coarsely calibrated with the MSB comparators in foreground, in real time and in a rotational manner. While the problem of dynamic comparator offset has been investigated for charge-sharing ADCs [13], the literature lacks an analysis for LU-SAR ADCs.

2.3.2 High-resolution asynchronous SAR ADCs

The design of high-speed, high-resolution analog-to-digital converters (ADCs) in deep-submicron CMOS is very challenging due to reduced voltage headroom and low intrinsic transistor gain imposed by the fabrication processes. The traditional pipeline ADC, which used to be the topology-of-choice for such applications, relies on high-precision amplifications and is therefore not very scalable. While digital calibration techniques have been disclosed [52]- [55]to cope with the nonlinearity caused by limited amplifier gain, they come at the cost of significant hardware complexity and power consumption overheads. On the other hand, SAR ADCs, which are very switching intensive and do not rely on static amplifiers, benefit from technology scaling and have been adopted for very performance-demanding applications. As the specifications of SAR ADCs approach higher resolutions, the comparators start to play a critical role concerning the overall ADC performance, frequently dominating the total power budget. The rationale is threefold: first, advances in lithography allow smaller unit capacitances in the capacitive DAC, reducing the impact of the latter to the total power consumption in ADCs that are not noise-limited; second, reduced ADC quantization noise floors demand proportionally low noise levels from the comparators,

which normally have a huge impact the overall power consumption; third, as the resolution grows, the voltage seen by the least-significant bits (LSBs) comparators decreases, increasing the decision/regeneration time and, therefore, limiting the speed of SAR ADCs.

In order to continue to push forward the performance of high-resolution high-speed ADCs, scientific efforts have taken place on different research fronts. To alleviate SNR degradation due to comparator noise, [56] reported an adaptive-tracking-averaging technique, which relies on averaging out the LSB noise and recovering errors in previous comparisons by adaptively tracking the residue voltage and repeating the LSB comparison multiple times. Similarly, [57] presents a data-driven noise-reduction technique, by carrying multiple comparisons and applying majority voting when a close-to-zero voltage is detected on the DAC. Also, [58] and [59] rely on the code distribution of the repeated LSB comparisons to infer the residue voltage based on the pre-learned noise parameter of the comparator. However, since the relationship between voltage and code distribution is nonlinear, the algorithm is very hardware intensive. Furthermore, all these strategies based on repetition trade off noise for time, and end up slowing down the ADC operation. Alternatively, the pipeline-SAR ADC, which consists of multiple stages of SAR quantizers, became a popular topology for ADCs with effective-number-of- bits (ENOB) >10 bits and speeds from ~10 MHz to ~100 MHz [60]- [63]. While the residue amplifier inserted between the SAR stages contributes with its own noise, its gain improves the input-referred SNR of the subsequent quantizer stages. On the other hand, since a small feedback factor is required when employing SAR stages with relatively high inter-stage gain, the design of the residue amplifier is very challenging as it requires high loop gain and bandwidth. Although pipeline SAR ADCs with open loop dynamic amplification have been reported [63]- [64] [63], these generally require dedicated calibration to cope with amplifier nonlinearity and process-voltage-temperature (PVT) variations.

Being a switching-intensive topology, the speed of SAR ADCs has improved significantly in recent years due to faster transistors available in deep submicron technologies and topological innovations. As we mentioned earlier, the loop-unrolled (LU) architecture is very promising for

high speed applications. However, in asynchronous SAR architectures that comprehend multiple comparators, the offset mismatches manifest themselves as signal dependent errors, i.e. distortion on the ADC transfer curve. The works in [34], [45] reported techniques to calibrate the offset mismatch in background in 8-bit ADCs. Nevertheless, the effectiveness of similar techniques was not yet confirmed in higher resolution SAR ADCs. Another limiting factor of high resolution SAR ADCs is the trade-off between the comparator speed, noise and power consumption [66]. To the best of our knowledge, no single channel SAR ADC with > 10 ENOBs and > 100 MS/s was previously reported.

2.4 Summary

This chapter presents the review of SAR ADC operation and its major challenges in deeply scaled technologies. Also, state of art asynchronous SAR ADCs have been briefly reviewed. In particular, loop unrolled SAR architecture, as a promising candidate for high-speed is reviewed along with its shortages. Lastly, state of art high-resolution SAR ADCs have been reviewed.

Chapter 3 : EFFECT OF COMPARATORS OFFSETS IN LU-SAR ADCS

Loop-unrolled SAR (LU-SAR) ADC is a promising architecture for high-speed, power-efficient applications, as it breaks the SAR critical loop dependency at the cost of low hardware-efficiency. However, due to the presence of multiple comparators, the offset mismatch issue arises as it introduce signal dependent conversion error to the transfer curve of the ADC, which means it causes distortion. Therefore, this architecture is hard to migrate to high-resolution applications as the cost to reduce the comparator mismatch are largely expensive. This chapter is to investigate the mismatch source of dynamic comparator, and the mechanism how it affects the linearity of LU-SAR ADCs. Analytic model is derived to establish the relationship between the effective resolution and individual comparator offset. Lastly, statistical analysis is applied based on this analytical model to predict the yield of LU-SAR ADCs given a resolution target and standard deviation of the comparator design.

3.1 Offset in Strong-Arm latch comparator

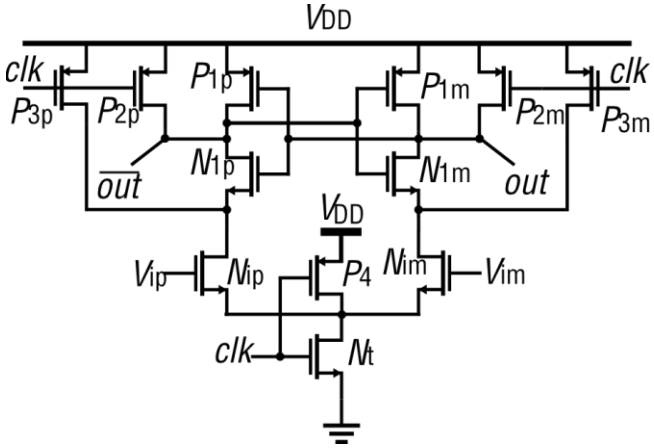


Figure 3-1. A Strong-Arm latch voltage comparator

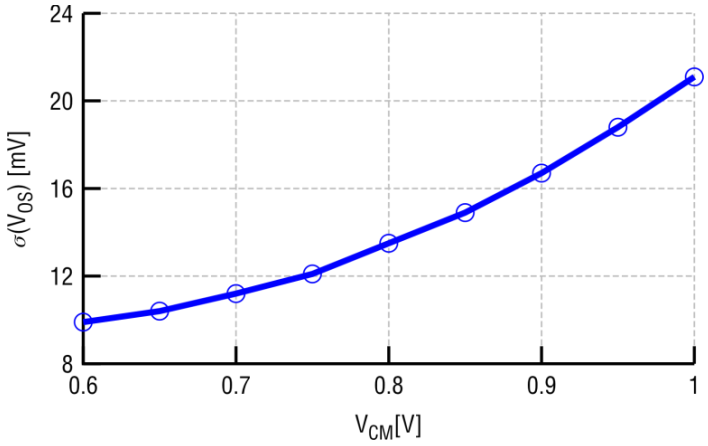


Figure 3-2. Simulated comparator offset dependency on common-mode voltage

The Strong-Arm latch voltage comparator [14], [15], shown in Figure 3-1, finds popular usage in high-speed, low-power ADC designs because of its excellent power efficiency. The offset voltage of this type of comparator can be approximated by [16], [17]

$$V_{OS} = \Delta V_{TH} + \frac{(V_{GS} - V_{TH})_{1,2}}{2}\left(\frac{\Delta\beta_{1,2}}{\beta_{1,2}} + \frac{\Delta R_{1,2}}{R_{1,2}}\right) \tag{3-1}$$

where $\Delta V_{TH1,2}$ represents the threshold voltage mismatch of the input transistors, while $(V_{GS} - V_{TH})_{1,2}$ is the overdrive voltage, and $\Delta\beta_{1,2}$ and $\Delta R_{1,2}$ are the gain and load mismatches of the input pair, respectively. In a 130-nm technology, a minimum sized Strong-Arm comparator exhibits a standard deviation of offset voltage >30 mV according to statistical simulations, which is close to the LSB voltage of a 6-bit ADC with 1.2 V of supply voltage. As we will see in Section III, comparators with such a random offset level would drastically reduce the effective resolution of an LU-SAR ADC. The typical solution to mitigate comparator offset is to balance the discharging speed of the two branches of the comparator by adding extra digitally controlled current sources [11] to output nodes of the input pair diverting some current to compensate the offset, or by adding capacitors [12] to the latch output slowing down the faster side and matching with the slower one. Also, the statistical element selection (SES) technique [18], [19] has proven being able to achieve high precision in comparator offset calibration. Nevertheless, the digital control words are quite long considering that multiple comparators are being used. Also, these calibration techniques

generally take place in foreground, and do not compensate process, voltage and temperature (PVT) variations.

Furthermore, as offset impacts the comparator result only when the input level is relatively small, the second term in (1) reveals the dependency of offset on the input common-mode level. Simulation results of a design example in a 130-nm technology show that the offset standard deviation doubles when common-mode voltage varies from 0.6 V to 1.0 V, as shown in Figure 3-2.

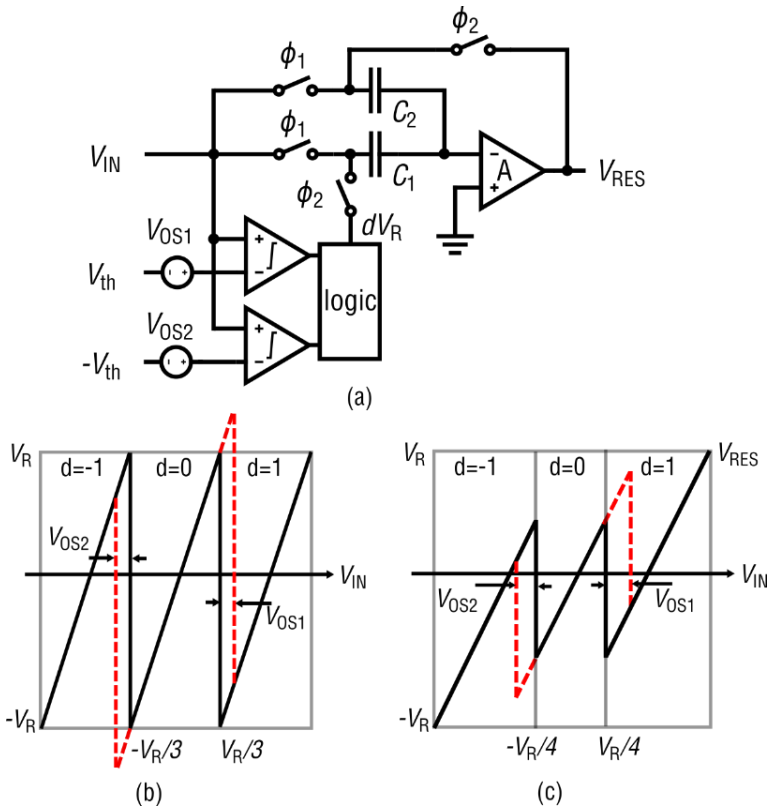


Figure 3-3. Impact of comparator offset mismatch on multi-step ADC

The issue of comparator offset mismatch in multi-step ADC has been extensively studied for pipeline ADCs. Figure 3-3 shows a 1.5-bit pipeline ADC stage, consisting of two comparators and a switched capacitor amplifier. In the presence of comparator offset, the residue transfer curve is drifted from its ideal (solid line) to a shifted one (dashed line) in Figure 3-3 (b). We may see that if the input falls into the offset sensitive window, the output residue would saturate the following stage, and therefore cause non-linearity. One solution to this issue is to provide redundancy for the

inter-stage gain with respect to the stage resolution [20]. As shown in Figure 3-3 (c), reducing the gain to 2 and setting the comparator thresholds to $\pm V_R/4$ lends some headroom for accommodating the errors from comparator offset, and the offset errors introduced by the last stage translates into small input referred errors thanks to the cascaded gain between stages.

The LU-SAR operation is similar to its pipeline counterpart but without residue amplification. Figure 3-4 (a) and (b) illustrate the SAR operations without and with the presence of offset mismatch. Since an ideal binary DAC residue range follows binary scaling, the error from comparator offset, therefore, saturates the following conversion. Employing redundancy has been used in SAR ADCs [1], [2] to avoid missing levels in the calibration of capacitor weights, and has been employed to solve DAC settling error [21], both at the cost of more conversion steps than the achieved resolution due to sub-radix-2 scaling. However, since there is no residue amplification between bit conversions, the offset introduced errors in later bits are not scaling down. On the contrary, as we will see in Section III, the errors by the later comparator offsets dominate the SNDR degradation for the SAR ADC.

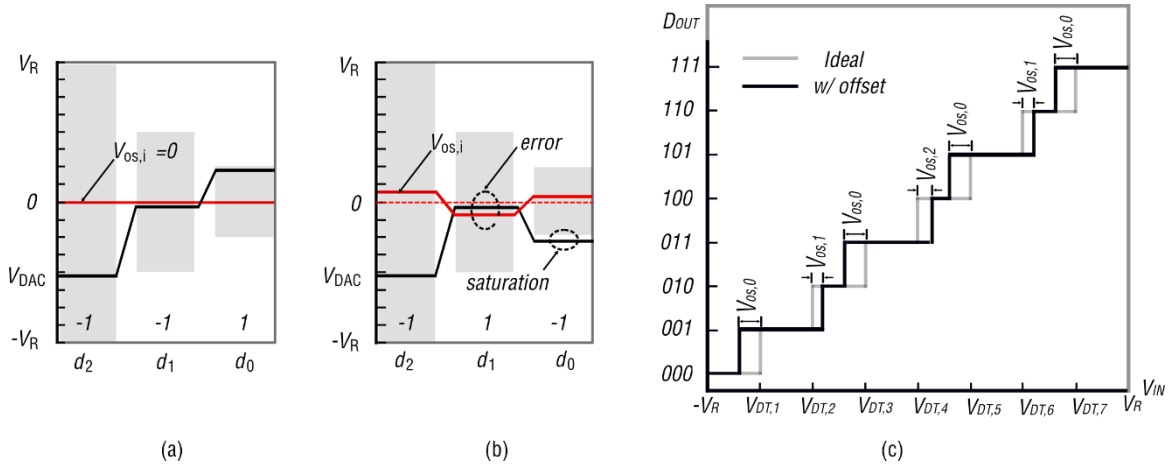


Figure 3-4. 3-bit SAR ADC operation example without (a), with (b) offset mismatch, and the transfer curve comparison of ideal comparators (grey line) and comparators with offset mismatch (dark line) (c)

Figure 3-4 (a) shows the ideal conversion procedure of the LU-SAR ADC using a 3-bit DAC example, where the differential residue voltage $V_{\mathrm{DAC},i}$ at the inputs of the comparator at the i-th

cycle of the binary search algorithm ($i = 0$ is the LSB decision) is given by

$$V_{\mathrm{DAC},i} = V_{\mathrm{in}} - V_{\mathrm{R}} \sum_{j=B-1}^{i+1} \frac{k_j C_j}{C_{\mathrm{total}}}, \tag{3-2}$$

where B is the resolution of the ADC, V_{in} the differential input sampled voltage, V_{R} the reference voltage, C_{B-1}, C_{B-2}, …,C_0 are the DAC capacitances and $k_j \in \{-1, 1\}$ represents the comparison result. Note that for $i = B - 1$, the summation in (3-2) is empty and returns zero.

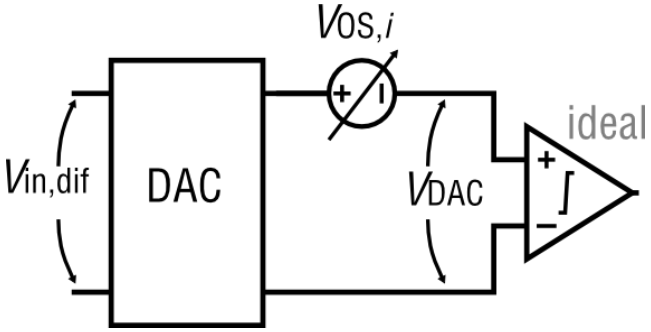


Figure 3-5. Modeling mismatched comparator offset voltages in LU-SAR ADC as a dynamic offset voltage

The impact of the comparator offsets on the LU-SAR ADC can be modeled using the circuit shown in Figure 3-5, where all the comparators are substituted by an offset-free comparator, and the offsets are modeled by the variable voltage source $V_{\mathrm{OS},i}$. This voltage assumes the value of the offset voltage of the comparator used at the actual conversion. The residue voltage becomes

$$V_{\mathrm{DAC},i} = V_{\mathrm{in}} - V_{\mathrm{R}} \sum_{j=B-1}^{i+1} \frac{k_j C_j}{C_{\mathrm{total}}} + V_{\mathrm{OS},i}, \tag{3-3}$$

from which one can see that the essence of the ADC operation is to compare and approximate the input to the thresholds generated by the DAC and comparator offsets. The thresholds of the transitions for different binary output codes K with $\{k_{B-1}, k_{B-2}, \ldots, k_0\}$, are given in different cycles i. For example, the mid-scale transition point from {-1,1,…,1} to {1,-1,…,-1} occurs at the MSB cycle ($i = B - 1$), while the transitions from {-1,-1,1,…,1} to {-1,1,-1,…,-1} and from {1,-1,1...1} to {1,1,-1,...,-1} happen when $i = B - 2$. As shown in Figure 3-4 (b), the comparator offset causes

error only when the DAC voltage is close to 0. This means the offsets shift the transition thresholds by different amounts for different codes, and the thresholds of transitions for a given code K can be written as

$$V_{\mathrm{T}}[K] = \underbrace{V_{\mathrm{R}} \sum_{j=B-1}^{i(K)+1} \frac{k_{B-j} C_{B-j}}{C_{\mathrm{total}}}}_{V_{\mathrm{DT},K}} - V_{\mathrm{OS},i(K)} \quad (3\text{-}4)$$

where $i(K)$ denotes the i-th cycle that the DAC is equal to 0 for an analog input $V_{\mathrm{T}}[K]$, and $V_{\mathrm{DT},K}$ represents the nominal threshold generated by DAC. Also, $V_{\mathrm{OS},i(K)}$ is dictated by i, and is determined by B unique distinct values. By sweeping over the whole input range, the vector of transition threshold shifts, $\mathbf{\Delta} \boldsymbol{V}_{\mathrm{T}}$, caused by comparator offsets, can be obtained. As shown in Figure 3-4 (c), a 3-bit ADC example, the drift vector is

$$\mathbf{\Delta} V_{\mathbf{T}} = \begin{pmatrix} V_{\mathrm{OS},0} & V_{\mathrm{OS},1} & V_{\mathrm{OS},0} & V_{\mathrm{OS},2} & V_{\mathrm{OS},0} & V_{\mathrm{OS},1} & V_{\mathrm{OS},0} \end{pmatrix}^{T} . \quad (3\text{-}5)$$

3.3 Comparator offset mismatch analysis in LU-SAR ADCs

3.3.1 Static characteristics

To derive the static properties of the LU-SAR ADC in the presence of mismatched comparator offsets, we initially assume that the ADC contains no missing codes. The differential non-linearity (DNL) for a given code K, $\delta[K]$, in an ADC with differential input is defined as

$$\delta[K] = \frac{V_{\mathrm{T}}[K] - V_{\mathrm{T}}[K-1]}{V_{\mathrm{LSB}}} - 1 . \quad (3\text{-}6)$$

Since $V_{\mathrm{DT},K}$ in (3-4) describes the behavior of an ideal ADC, the DNL is given exclusively by the values of the comparator offset voltages. Thus, a vector representation, $\boldsymbol{\delta}$, of the DNL, for a 3-bit example, is given by

$$\boldsymbol{\delta} = \begin{pmatrix} -V_{\mathrm{OS},0} + V_{\mathrm{OS},1} \\ V_{\mathrm{OS},0} - V_{\mathrm{OS},1} \\ -V_{\mathrm{OS},0} + V_{\mathrm{OS},2} \\ V_{\mathrm{OS},0} - V_{\mathrm{OS},2} \\ -V_{\mathrm{OS},0} + V_{\mathrm{OS},1} \\ V_{\mathrm{OS},0} - V_{\mathrm{OS},1} \end{pmatrix} \cdot \frac{1}{V_{\mathrm{LSB}}}. \tag{3-7}$$

It should be noted that we neglect the DNL for the first and last code for eliminating the ADC offset and full scale error, which is a common practice for lab ADC characterization. The integral non-linearity (INL) at code K, $\phi[K]$, is given by

$$\phi[K] = \sum_{j=1}^{K} \delta[j]. \tag{3-8}$$

The INL vector $\boldsymbol{\phi}$ can be obtained by applying the values in (3-7) into (3-8). For the 3-bit example,

$$\phi = \begin{pmatrix} 0 & \frac{V_{\mathrm{OS},1} - V_{\mathrm{OS},0}}{V_{\mathrm{LSB}}} & 0 & \frac{V_{\mathrm{OS},2} - V_{\mathrm{OS},0}}{V_{\mathrm{LSB}}} & 0 & \frac{V_{\mathrm{OS},1} - V_{\mathrm{OS},0}}{V_{\mathrm{LSB}}} & 0 \end{pmatrix}^{T}. \tag{3-9}$$

This result can be extended to any resolution B without loss of generality.

3.3.2 Effective resolution

To relate the static characteristics and ENOB of a LU-SAR ADC in the presence of mismatched comparator offsets, we use the result in [23] (see Appendix A),

$$\Psi = B - \log_4\left(1 + 12\overline{\phi^2}\right), \tag{3-10}$$

where Ψ represents the ENOB, $\overline{\phi^2}$ is the average of squared INL values:

$$\overline{\phi^2} = \frac{1}{2^B - 1} \sum_{j=1}^{2^B - 1} \phi[j]^2. \tag{3-11}$$

Exploiting the symmetry of (3-9), $\overline{\phi^2}$, for any resolution B, can be simplified as

$$\begin{aligned}\overline{\phi^2} &= \sum_{j=1}^{B-1} \frac{2^{-j-1}}{V_{\mathrm{LSB}}^2}\left(V_{\mathrm{OS},j} - V_{\mathrm{OS},0}\right)^2 \\ &= \frac{1}{2}\left(\frac{V_{\mathrm{OS},1} - V_{\mathrm{OS},0}}{V_{\mathrm{LSB}}}\right)^2 + \frac{1}{4}\left(\frac{V_{\mathrm{OS},2} - V_{\mathrm{OS},0}}{V_{\mathrm{LSB}}}\right)^2 + \frac{1}{8}\left(\frac{V_{\mathrm{OS},3} - V_{\mathrm{OS},0}}{V_{\mathrm{LSB}}}\right)^2 + \ldots\end{aligned} \tag{3-12}$$

This equation reveals that $\overline{\phi^2}$ is a weighted summation of individual offset mismatches among the comparators with coefficient scaling exponentially from MSB to LSB. The ENOB ψ as function of the individual offset voltages $V_{\mathrm{OS},j}$ is found by combining (3-10) and (3-11). We can draw an important conclusion based on (3-11): *the value of $\overline{\phi^2}$ (and consequently the ENOB) of a LU-SAR ADC is more sensitive to the offset of the comparators responsible for deciding the LSBs than the comparators used for the MSBs, as a result of the weight 2^{-j-1} inside the summation*. This observation is contrary to pipeline ADCs where the impacts of noise and offset of MSB comparators are more critical than that of LSB ones due to the inter-stage gain and/or redundancy.

3.3.3 Statistical analysis

Equations (3-10) and (3-11) represent ENOB as a function of the individual comparator offsets which can be represented as random variables. Therefore, we study the statistical properties of ENOB in order to obtain insights on the yield. Assume that the offsets of the comparators are independent and identically distributed (i.i.d.). This is a reasonable assumption in practice, if all the comparators use the same design. Also, assume that the comparator offset follows a normal distribution, with zero mean and variance σ_{OS}^2,

$$V_{\mathrm{OS},j} \sim \mathcal{N}(0, \sigma_{\mathrm{OS}}^2), \qquad j = 0,1 \ldots B-1. \tag{3-13}$$

If the difference of two random offsets in (12) is defined as a new random variable

$$X_j = V_{\mathrm{OS},j} - V_{\mathrm{OS},0}, \qquad j = 1,2 \ldots B-1, \tag{3-14}$$

then (11) can be conveniently represented by a summation of single variables. Since both $V_{\mathrm{OS},j}$ and X_j are normally distributed, we may let the vector $\mathbf{X} \in \Re^{B-1}$

$$\mathbf{X} = \begin{pmatrix} X_1 & X_2 & \dots & X_{B-1} \end{pmatrix}^T, \tag{3-15}$$

represent a multivariate normal distribution with a mean vector $\boldsymbol{\mu}_{\mathbf{X}} \in \Re^{B-1}$ and a $(B - 1)\times(B - 1)$ positive definite symmetric covariance matrix $\boldsymbol{\Sigma}$.

$$\mathbf{X} \sim \mathcal{N}_{B-1}(\boldsymbol{\mu}_{\mathbf{X}}, \Sigma), \tag{3-16}$$

where the elements of $\boldsymbol{\mu}_{\mathbf{X}}$ can be calculated by

$$\mathrm{E}[X_j] = \mathrm{E}[V_{\mathrm{OS},j} - V_{\mathrm{OS},0}] = 0,\ j = 1, 2, \dots, B-1, \tag{3-17}$$

and the element $\Sigma_{m,n}$ in the covariance matrix is calculated by

$$\Sigma_{m,n} = \mathrm{Cov}[X_m, X_n], \tag{3-18}$$

where the operators $\mathrm{E}[\cdot]$ and $\mathrm{Cov}[\cdot]$ represent the expected value and the covariance, respectively. Thus, $\boldsymbol{\mu}_{\mathbf{X}}$ is a zero vector and $\boldsymbol{\Sigma}$ is a symmetric matrix and

$$\boldsymbol{\Sigma} = \begin{pmatrix} 2 & 1 & 1 & & 1 \\ 1 & 2 & 1 & \cdots & 1 \\ 1 & 1 & 2 & & 1 \\ & \vdots & & \ddots & \\ 1 & 1 & 1 & & 2 \end{pmatrix} \cdot \sigma_{\mathrm{OS}}^2. \tag{3-19}$$

Note that the non-zero covariances outside the matrix diagonal reveal correlation between the elements of $\mathbf{X}$, as a result of $V_{\mathrm{OS},0}$ being common to all the elements. Finally, we can rewrite (3-11) as a quadratic form in random variables [24, pp. 28], such that

$$\overline{\phi^2} = \mathbf{X}^T \mathbf{A} \mathbf{X}, \tag{3-20}$$

by letting

$$\mathbf{A} = \begin{pmatrix} 2^{-2} & 0 & 0 & & 0 \\ 0 & 2^{-3} & 0 & \cdots & 0 \\ 0 & 0 & 2^{-4} & & 0 \\ & \vdots & & \ddots & \\ 0 & 0 & 0 & & 2^{-B} \end{pmatrix} \cdot \frac{1}{V_{\mathrm{LSB}}^2}. \tag{3-21}$$

Since elements of $\mathbf{X}$ in (3-20) are correlated, it is hard to gain insight into the properties of $\overline{\phi^2}$.

Therefore, $\overline{\phi^2}$ will be expressed in terms of the principal components of $\mathbf{X}$, which can be found as follows. We first define a new random variable vector $\mathbf{Z} = \mathbf{\Lambda_\Sigma^{-1/2} V_\Sigma^T X}$, where $\mathbf{\Lambda_\Sigma}$ and $\mathbf{V_\Sigma}$ are the eigenvalue matrix and orthogonal eigenvector matrix of covariance matrix $\mathbf{\Sigma}$, respectively. One can easily verify that $\mathbf{E[ZZ^T] = \boldsymbol{I}}$, which means elements in $\mathbf{Z}$ are *independent* standard normal variables. Then, we rewrite (3-20) as a function $\mathbf{Z}$,

$$\overline{\phi^2} = \mathbf{X}^T\mathbf{A}\mathbf{X} = \mathbf{Z}^\mathbf{T}\underbrace{\left(\mathbf{\Lambda_\Sigma^{1/2}}\right)^\mathbf{T}\mathbf{V_\Sigma^T A V_\Sigma \Lambda_\Sigma^{1/2}}}_{\mathbf{B}}\mathbf{Z}, \tag{3-22}$$

$$\overline{\phi^2} = \left(\mathbf{V_B^T Z}\right)^T \mathbf{\Lambda_B V_B^T Z} = \mathbf{U}^T\mathbf{\Lambda_B U}, \tag{3-23}$$

where $\mathbf{\Lambda_B}$ and $\mathbf{V_B}$ are the eigenvalue matrix and orthogonal eigenvector matrix of $\mathbf{B}$, respectively, and $\mathbf{U = V_B^T Z}$. Similarly, since $\mathrm{E}[\mathbf{UU^T}] = \boldsymbol{I}$, elements in $\mathbf{U}$ are *independent* standard normal variables. This result is very useful, as it represents $\overline{\phi^2}$ as a function of *independent* standard normal random variables U_j with $j = 1, 2, \dots, B-1$. Expanding (3-22) leads to

$$\overline{\phi^2} = \sum_{j=1}^{B-1} \lambda_j U_j^2. \tag{3-24}$$

where λ_j represents the diagonal elements in $\mathbf{\Lambda_B}$. To illustrate, $\mathbf{\Lambda_B}$ of an 8-bit ADC is given below, where diag[·] indicates diagonal matrix

$$\mathbf{\Lambda_B} = \mathrm{diag}(0.68 \quad 0.17 \quad 0.08 \quad 0.037 \quad 0.018 \quad 0.009 \quad 0.004). \tag{3-25}$$

While (3-23) represents the exact statistics of $\overline{\phi^2}$, given our initial assumptions, its form still leads to cumbersome calculations due to the presence of $\boldsymbol{B}$ - 1 random variables. Various approaches to find a tractable approximation of a linear combination of independent Chi-squared random variables can be found in literature. Perhaps the most straightforward [24], [25], frequently referred to as Patnaik's approximation, consists in finding a distribution $c\chi^2(v)$ that has the same first two moments, i.e. expected value and variance, of $\sum_{j=1}^{N} \lambda\chi_j^2(1)$, where $\chi^2(v)$ denotes a random variable with a Chi-squared PDF and v degrees of freedom. Thus,

$$\sum_{j=1}^{B-1} \lambda_j \mathcal{X}^2(1) \approx c\mathcal{X}^2(v), \tag{3-26}$$

where c and v can be derived as

$$c = \frac{\sum_{j=1}^{k} \lambda_j^2}{\sum_{j=1}^{k} \lambda_j}, \qquad v = \frac{\left(\sum_{j=1}^{k} \lambda_j\right)^2}{\sum_{j=1}^{k} \lambda_j^2}. \tag{3-27}$$

In (3-23), λ_j for j = 1, 2, …, B-1 can be substituted into (3-26) to first find c and v and then to represent $\overline{\phi^2}$ as a single Chi-squared random variable. However, the complexity of computing the eigenvalues of a (B-1)×(B-1) matrix symbolically, i.e. as a function of B, is large for practical values of B and prevents the construction of a broad model. One way to circumvent this limitation is to compute $\mathbf{\Lambda}$ and use it to find c and v numerically, which incurs little overhead[1]. Alternatively, we could use numerical optimization to find the values of c and v that best represent (3-23) by minimizing the mean-squared error between the two sides of (3-25). Aiming for a good accuracy while maintaining the insights of an analytic approach, a mixed methodology is chosen in our analysis. First, we go back a few steps, and assume that the correlations between terms of $\mathbf{X}$ has little impact on the final PDF of $\overline{\phi^2}$ so that they can be disregarded, and the introduced error can be corrected with a simple linear factor on c. In this case, the covariance matrix in (3-19) can be approximated by $\mathbf{\Sigma} = 2\sigma_{\mathrm{OS}}^2 \boldsymbol{I}$. By doing the same decomposition in (3-22), it can be shown that the eigenvalue matrix, is calculated by

$$\mathbf{\Lambda}_{\mathrm{B}} = 2\left(\frac{\sigma_{\mathrm{OS}}}{V_{\mathrm{LSB}}}\right)^2 \mathbf{A}. \tag{3-28}$$

[1]While this approach seems to work well for the upper tail of the PDF, it incurs in significant error on the lower tail, which may make the model unusable for yield calculations. The same observation holds if the Pearson's approximation [26], which uses three moments instead of two, is used.

By feeding the values of $\mathbf{\Lambda}_B$ from (3-27) into (3-26), we find the values of v and c as function of the resolution B.

$$c = \frac{1}{3}\left(1+\frac{1}{2^{B-1}}\right), \qquad v = 3-\frac{6}{2^{B-1}+1} \tag{3-29}$$

Finally, we include a correction factor α in c, to accommodate for errors brought by our approximation, leading to

$$c_\alpha = \alpha\frac{1}{3}\left(1+\frac{1}{2^{B-1}}\right), \quad v = 3-\frac{6}{2^{B-1}+1} \tag{3-30}$$

while $\overline{\phi^2}$ is approximated by

$$\overline{\phi^2} \approx c_\alpha\left(\frac{\sigma_{\mathrm{OS}}}{V_{\mathrm{LSB}}}\right)^2 Y, \tag{3-31}$$

where

$$Y \sim \mathcal{X}_v^2, \tag{3-32}$$

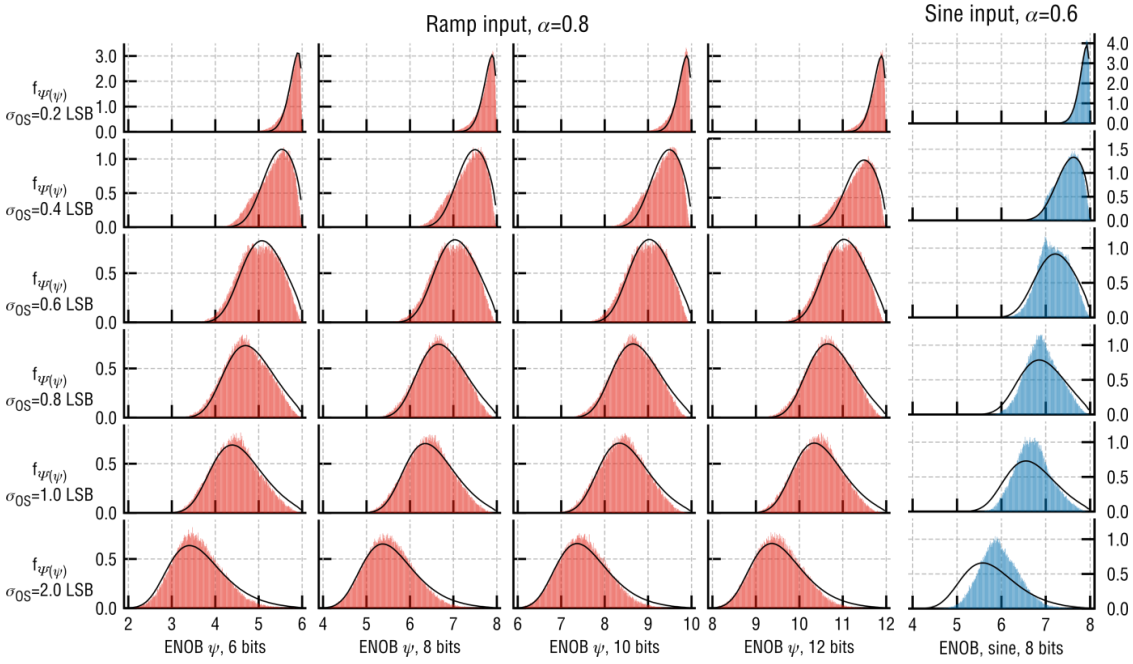


Figure 3-6. Comparison between the simulated (100K-points) and analytic ENOB PDFs with different standard deviations with ramp input (left) and sinusoid input (right)

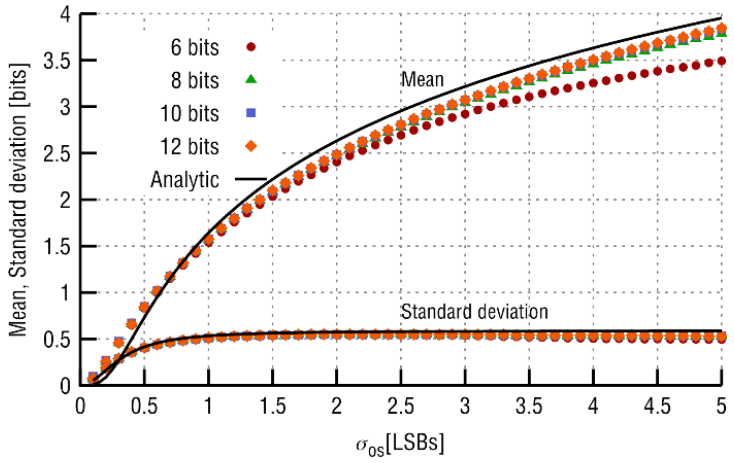


Figure 3-7. Comparison between the simulated (100K-points, α = 0.8) and analytic mean value and standard deviation of ENOB loss with different offset standard deviation

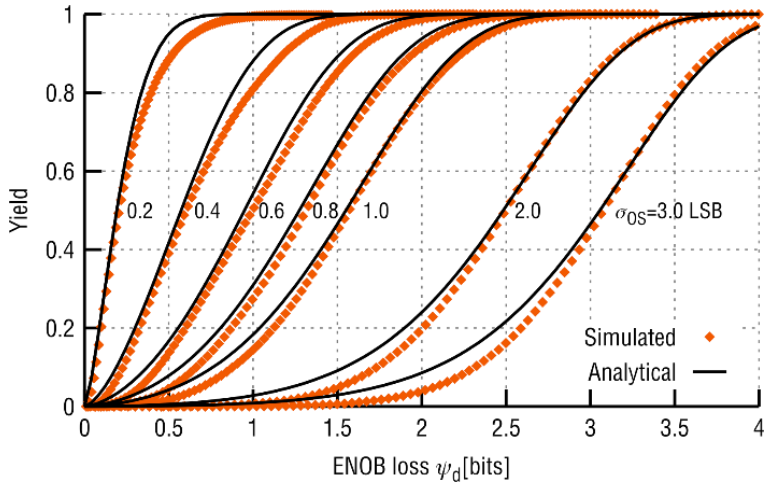


Figure 3-8. Comparison between the simulated (100K-points, α = 0.8) and analytic CDF of ENOB loss of 8-bit ADCs with different offset standard deviation

and $\chi^2(v)$ is a random variable that follows a Chi-squared distribution with v degrees of freedom. Interestingly, (3-31) works very well in approximating $\overline{\phi^2}$ when contrasted to behavioral simulations, even disregarding the correction factor (by choosing $c_\alpha = 1$). However, the best approximation occurs when $c_\alpha \sim 0.8$, and works well over the full range of the simulated combinations of B and σ_{OS}. The comparison results are presented with comments at the end of this section.

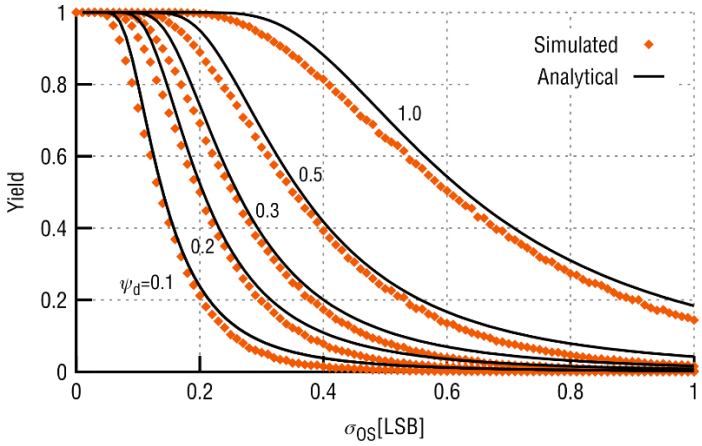


Figure 3-9. Comparison between the simulated (100K-points, α = 0.8) and analytic ENOB yields of 8-bit ADCs with different offset standard deviation

Finally, in order to extract intuitive and meaningful information from our model, the statistics of Ψ should be formulated as a function of $\overline{\phi^2}$. Thus, we rewrite (3-10) as

$$\Psi \approx B - \log_4\left(1+12c_\alpha\left(\frac{\sigma_{\mathrm{OS}}}{V_{\mathrm{LSB}}}\right)^2 Y\right) \tag{3-33}$$

Then, we can derive the PDF of the ENOB Ψ, expressed as a function of the resolution B, offset spread σ_{OS} and V_{LSB}, by applying a change of variables [29, pp. 200]. Finally, the ENOB PDF is described by

$$f_\Psi(\psi) = -\left(\frac{V_{\mathrm{LSB}}}{\sigma_{\mathrm{OS}}}\right)^2 \cdot \frac{2^{2(B-\Psi)}\left(\frac{\sqrt{2}}{2}\right)^\nu}{6c_\alpha\Gamma(\nu/2)} \cdot \left[\left(\frac{V_{\mathrm{LSB}}}{\sigma_{\mathrm{OS}}}\right)^2 \frac{\left(e^{B-\Psi}-1\right)}{12c_\alpha}\right]^{\frac{\nu}{2}-1} \cdot \exp\left(-\left(\frac{V_{\mathrm{LSB}}}{\sigma_{\mathrm{OS}}}\right)^2 \frac{\left(e^{B-\Psi}-1\right)}{24c_\alpha}\right) \ln(2), \tag{3-34}$$

where $\Gamma(\cdot)$ denotes the Gamma function.

In Figure 3-6, we show a comparison between f_Ψ calculated using (3-33) with $\alpha = 0.8$ and through Monte-Carlo simulations on a C++ behavioral model. For each combination of $\boldsymbol{B}$ and σ_{OS}, 100K points are simulated. The ENOB is extracted by applying a linear ramp at the ADC input, measuring the INL and combining these results with (3-10) and (3-11). Notice that this approach considers that the output codes of the ADC are equiprobable, which is a fair assumption if the statistics of the input signal are unknown. However, by far the most common approach to extract

the ENOB of an ADC in practice is by applying a pure tone at the input, and measuring the signal-to-noise-and-distortion ratio (SNDR). The latter case is discussed in the following sub-section.

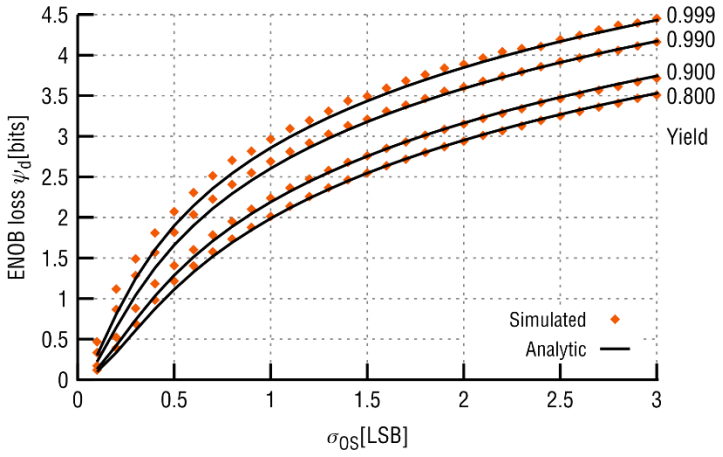


Figure 3-10. Comparison between the simulated (100K-points, α = 0.8) and analytic ENOB loss values of 8-bit ADCs with different offset standard deviation

It is noteworthy that in (3-33) the derivation of the model assumed absence of missing codes on the ADC transfer curve. However, the approximation still provides good accuracy for $\sigma_{OS} \geq 1$ LSB, that virtually guarantees missing codes. This happens mostly because the fitting coefficient alpha is chosen empirically while considering values of V_{os} larger than 1 LSB. Furthermore, we notice that c_α and v do not change much by varying $\boldsymbol{B}$ within a range of practical values. In fact, it can be demonstrated that, as $\boldsymbol{B}$ grows, c and v quickly converge to 1/3 and 3, respectively. Therefore, if we disregard the small error introduced by using fixed c and v in our analysis, the PDF of ENOB can be expressed in terms of the loss of ENOB Ψ_d caused by mismatched comparator offsets, by letting

$$\Psi_d = B - \Psi. \tag{3-35}$$

Finally, we normalize the offset spread to the value of one LSB,

$$\hat{\sigma}_{OS} = \frac{\sigma_{OS}}{V_{LSB}}, \tag{3-36}$$

and a general expression for f_Ψ, which is independent of the ADC resolution can be derived as

$$f_{\Psi_d}(\psi_d) \approx -\frac{2^{2\psi_d}\left(\sqrt{2}/2\right)^{\nu}}{6\hat{\sigma}_{\mathrm{OS}}{}^{2}c_{\alpha}\Gamma(\nu/2)}\cdot\left(\frac{e^{\psi_d}-1}{12\hat{\sigma}_{\mathrm{OS}}^{2}c_{\alpha}}\right)^{\frac{\nu}{2}-1}\cdot e^{-\frac{\left(e^{\psi_d}-1\right)}{24\hat{\sigma}_{\mathrm{OS}}^{2}c_{\alpha}}}\ln(2) \tag{3-37}$$

Our conclusions are in-line with the results presented in Figure 3-6. Note that for a given σ_{OS}, the curves for all ***B*'s** are nearly identical, besides the offset on the X-axis. We can find that $c = \alpha/3$ and $\nu = 3$ provide fairly close approximations, and these values are used for the following analyses.

3.3.4 Analysis using the sine test

The analysis carried out so far assumed equiprobable codes on the ADC output, which is the same as using a ramp input during characterization. While this assumption is reasonable if the statistics of the input signal are unknown, the method commonly employed to extract the ENOB of an ADC uses a sinusoidal input tone. To reconcile the proposed analysis with the sinusoidal test, we can still rely on a scalar fitting coefficient, adjusting the value of α and adopting the same expressions previously found. This approach is verified to provide good estimation of the ENOB statistics for $0 \leq \sigma_{\mathrm{OS}} \leq 0.6$ LSB, if we choose $\alpha = 0.6$. For $\sigma_{\mathrm{OS}} > 0.6$ LSB, the large probability of missing codes on the ADC transfer, together with the non-uniform probability distribution of the input signal, significantly change the shape of the PDF. Therefore, (3-36) is pessimistic in determining the ENOB statistics of an ADC driven by sinusoidal signals for $\sigma_{\mathrm{OS}} > 0.6$ LSB. Fortunately, this is not very problematic in practice, since $\sigma_{\mathrm{OS}} > 0.6$ LSB leads to excessive resolution loss even for low-resolution loop-unrolled SAR ADCs (approximately 1 bit, on average, as will be demonstrated on the next section). In conclusion, all the derivations presented in this paper are valid if employed with the sinusoidal test, by making $\alpha = 0.6$ and limiting the analysis to $\sigma_{\mathrm{OS}} \leq 0.6$ LSB.

3.3.5 Expected value and variance of ENOB

The ENOB loss caused by mismatched comparator offset voltages can be described by

$$\Psi_d \approx \log_4\left(1+12c_{\alpha}\hat{\sigma}_{\mathrm{OS}}^{2}Y\right). \tag{3-38}$$

Due to the presence of a logarithmic term in (3-37), we may estimate the expected value and

variance using a Taylor series expansion [30]. Dropping higher order terms, and using $\mathrm{E}[Y] = v$, and $\mathrm{Var}[Y] = 2v$, we can write

$$\mathrm{E}[\Psi_d] = \log_4(1+12c_\alpha\hat{\sigma}_{\mathrm{OS}}^2 v) - \frac{12c_\alpha\hat{\sigma}_{\mathrm{OS}}^2 v}{\ln 4(1+12c_\alpha\hat{\sigma}_{\mathrm{OS}}^2 v)^2}, \tag{3-39}$$

$$\mathrm{Var}[\Psi_d] = \frac{72c_\alpha^2 v\hat{\sigma}_{\mathrm{OS}}^2}{(\ln 2)^2(1+12c_\alpha\hat{\sigma}_{\mathrm{OS}}^2 v))^2}. \tag{3-40}$$

In Figure 3-7, the calculated mean values and standard deviations of ENOB losses using (3-38) and (3-39) are compared with those of 100-K points Monte Carlo simulations.

3.3.6 Yield

The yield considering offset mismatch can be estimated from the CDF of *Y*, which is given by

$$F_Y(y) = \frac{\gamma(v/2, y/2)}{\Gamma(v/2)} = p(v/2, y/2) \tag{3-41}$$

where $\Gamma(\cdot)$, $\gamma(\cdot)$and $p(\cdot)$ denote the Gamma function, the incomplete lower Gamma function, and the regularized Gamma function, respectively. Since Ψd is monotonic, the probability of an ENOB loss smaller than Ψd,max can be calculated by

$$\mathrm{P}\{\Psi_d \le \Psi_{d,\max}\} = \mathrm{P}\left\{ Y \le \frac{4_{d,\max}^{\Psi} - 1}{12c_\alpha\hat{\sigma}_{\mathrm{OS}}^2} \right\}. \tag{3-42}$$

Also, since $F_Y(y) = P\{Y \le y\}$, we can write

$$\mathrm{P}\{\Psi_d \le \Psi_{d,\max}\} = p\left(v/2, \quad \frac{4^{\Psi_{d,\max}} - 1}{24c_\alpha\hat{\sigma}_{\mathrm{OS}}^2} \right). \tag{3-43}$$

Equation (3-42) can be used to gain several insights. First, using (3-43), the yield of a design with a given comparator offset level and a maximum acceptable ENOB loss can be estimated (see Figure 3-7 and Figure 3-8):

$$\mathrm{Yield}\Big|_{\substack{\hat{\sigma}_{\mathrm{OS}}=a \\ \Psi_{\mathrm{d,max}}=b}} = p\left(v/2, \quad \frac{4^b - 1}{24c_\alpha a^2} \right). \tag{3-44}$$

Second, given a comparator design (with known offset statistics) and a specification on maximum ENOB loss, the yield can be estimated as (see Figure 3-9):

$$\Psi_d \Big|_{\substack{\hat{\sigma}_{\mathrm{OS}}=a \\ Yield=b}} = \log_4\left(p^{-1}(v/2,b)24a^2c_\alpha + 1\right), \tag{3-45}$$

where $p^{-1}(\cdot)$ denotes the inverse regularized Gamma function. Finally, for a target yield and a target ENOB, the standard deviation of the offset can be calculated as (see Figure 3-10):

$$\hat{\sigma}_{\mathrm{OS}} \Big|_{\substack{\Psi_{d,\max}=a \\ Yield=b}} = \frac{\sqrt{6}}{12}\sqrt{\frac{4^a-1}{c_\alpha p^{-1}(v/2,b)}}. \tag{3-46}$$

3.4 Summary

This chapter presents the analysis of the impact of comparator offset mismatch on the linearity of LU-SAR ADCs. The mechanism of the linearity degradation is perceived, and an analytic model is established to quantitatively prove the complication. Based on the model, strategies can be employed for alleviating offset impact are introduced. Furthermore, statistical analyses were carried out. Equations (3-44)-(3-46) provide useful guidance in defining the comparator offset specifications.

Chapter 4 : ANALYSIS OF COMPARATOR NOISE IMPACT ON SAR ADCS

As described in Chapter 2, comparator noise plays a more and more important role in SAR ADC design as resolution increases. This is because on one hand the reduced LSB voltage requires a proportionally small noise level on comparator, which is hard to design and power consuming; on the other hand, it generally requires compromise in speed of the ADC to achieve low noise comparator. This chapter is to investigate mechanism of comparator noise impact on the ADC resolution in binary and non-binary SAR ADCs; Also, analytic models is derived to provide guidance of defining comparator noise specifications. Based on the analysis, strategies to optimize the noise, power efficiency and speed are drawn in high level.

4.1 Comparator noise impact on binary SAR ADCs

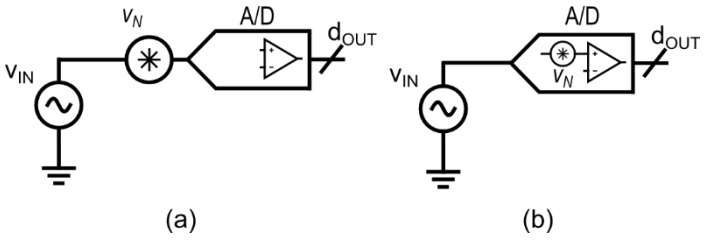


Figure 4-1. Comparator noise analysis model: additive noise model (a) and noisy comparator mode

Conventionally in the initial design phase, the additive noise model, shown in Figure 4-1 (a), is widely used to calculate and/or simulate the comparator noise impact on ADC resolution in high level, and, accordingly, a comparator noise specification can be derived. However, this model is considered to be valid based on the assumption that the ADC is a ideally linear system, which is not exactly true because the quantization is nonlinear process. Figure 4-1 (b), which models the comparator noise as a random voltage sources added to the comparator input, shows a more accurate model. Figure 4-2 shows the simulation result comparison of these two modeling ways.

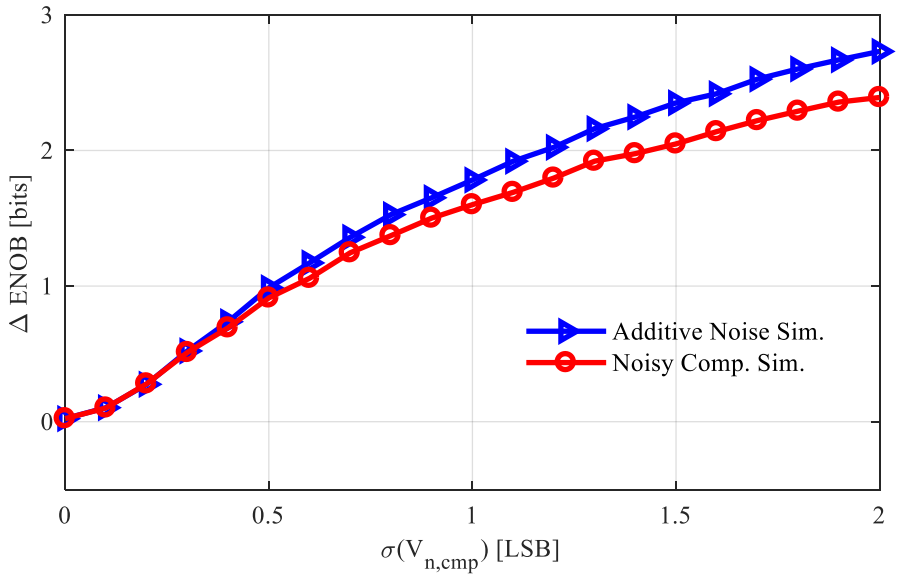


Figure 4-2. ENOB loss comparison between additive model and noisy comparator model

One can see the additive noise is valid when the noise sigma is no more than 0.5 LSB. When the noise level increases, the estimation using additive model becomes more and more pessimistic. However, the shortcoming of the second model is not analytical due to the nonlinear operation of the ADC.

4.1.1 Input referred comparator noise of SAR ADC [37]

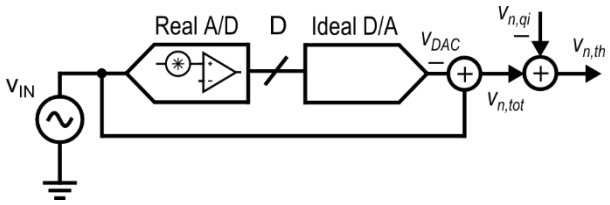


Figure 4-3. Input referred noise calculation model

Since the quantization of the ADC is a nonlinear process, it is not accurate to consider the comparator noise additive to the input of the ADC. Instead, the input referred noise is a signal dependent value. In [37], the authors proposed a generic statistic model for calculating the input referred noise of the ADC. As shown in Figure 4-3, the input referred noise is investigated from

conversion residue perspective. $V_{\mathrm{n,tot}}$ is the conversion error with *a given input level*, V_{in}. It should be noted that this residue may not be limited within ±0.5 LSB, because comparator noise is considered, which can result in excessively large residue. If we remove the ideal quantization error from this residue voltage, it ended up with the input referred quantization error due to thermal noise of the comparator, that is

$$V_{\mathrm{n,th}} = V_{\mathrm{n,tot}} - V_{\mathrm{n,qi}}, \tag{4-1}$$

where $V_{\mathrm{n,qi}}$ denotes the ideal quantization error. Then the problem is to calculate the total noise with presence of comparator noise and the ideal quantization error.

As we pointed out previously, impact of comparator noise depends on the input level of the ADC, which means we need to go through the SAR conversion process to find out the input referred noise. Figure 4-4 shows the explanation of comparator noise complication. The left hand side figure shows that the voltage seen by the noisy comparator in *k*-th comparison is a function of the input and all the previous comparison results, that is

$$V_{\mathrm{X},k} = V_{\mathrm{in}} - \sum_{i=0}^{k} b_i 2^{-i} V_{\mathrm{R}}, \tag{4-2}$$

where V_{R} is the reference voltage of the DAC, b_i's comparator result of *i*-th comparison. Note that for i=0, the summation is empty and returns 0. The right hand side figure explains how the probability of each possible comparator result with a given input and with the presense of noise. If we assume that thermal noise permits a normal distribution with a standard deviation of σ, one can see that

$$\mathrm{P}\left(b = 1 \mid V_{\mathrm{X}}\right) = Q\left(\frac{V_{\mathrm{X}}}{\sigma}\right), \tag{4-3}$$

$$\mathrm{P}\left(b = -1 \mid V_{\mathrm{X}}\right) = Q\left(-\frac{V_{\mathrm{X}}}{\sigma}\right), \tag{4-4}$$

where,

$$Q(x)=\int_0^{+\infty}\frac{1}{\sqrt{2\pi}}e^{\frac{x^2}{2}}dx. \tag{4-5}$$

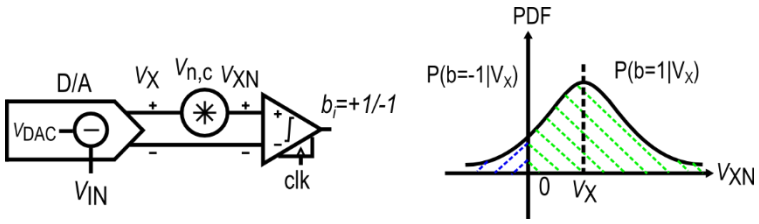


Figure 4-4. Illustration of comparator noise in SAR conversions

In principle, any given input may have 2^N possible conversion results of an N-bit ADC, which correspondent to 2^N possible conversion residue voltages, $V_{\text{n,tot}}$, according to (4-2). The probability of each code can be calculated by

$$\mathrm{P}\left(d_{out}=D\,|\,V_{\text{in}}\right)=\prod_{k=1}^{N}Q\left(b_k\cdot\frac{V_{\text{X,k}}\left(V_{\text{in}}\right)}{\sigma}\right), \tag{4-6}$$

where d_{out} is the binary output of the ADC, D a possible result of ADC conversion, and b_k the k-th comparison results that leads to ADC output of D, namely

$$D=\sum_{k=1}^{N}b_k\cdot 2^{N-k}, \tag{4-7}$$

Then the total noise power can be calculated by the summation of all the possible residue voltages weighted by the correspondent probability, that is

$$V_{\text{n,tot}}\left(V_{\text{in}}\right)=\sum_{k=0}^{2^N-1}P\left(d_{\text{out}}=k\,|\,V_{\text{in}}\right)\cdot V_{\text{X,N}}\left(V_{\text{in}},d_{\text{out}}\right), \tag{4-8}$$

where $V_{\text{X,N}}$ is the final residue and it value can be found by (4-2). With the total noise power available from (4-8), the input referred comparator noise power can be calculated by

$$V_{\text{n,th}}^2\left(V_{\text{in}}\right)=V_{\text{n,th}}^2\left(V_{\text{in}}\right)-V_{\text{n,qi}}^2\left(V_{\text{in}}\right). \tag{4-9}$$

Figure 4-5 and Figure 4-6 show the calculated noise power of a 4-bit ADC example (without loss generality) with two different noise levels, respectively. One can see that the input referred comparator noise is not uniform as V_{in} varies. From Figure 4-5 one may assume that the noise is

"periodical" when sweeping V_{in} with a period of 1 LSB. However, Figure 4-6 reveals that this assumption does not hold for $\sigma \geq 1$ LSB.

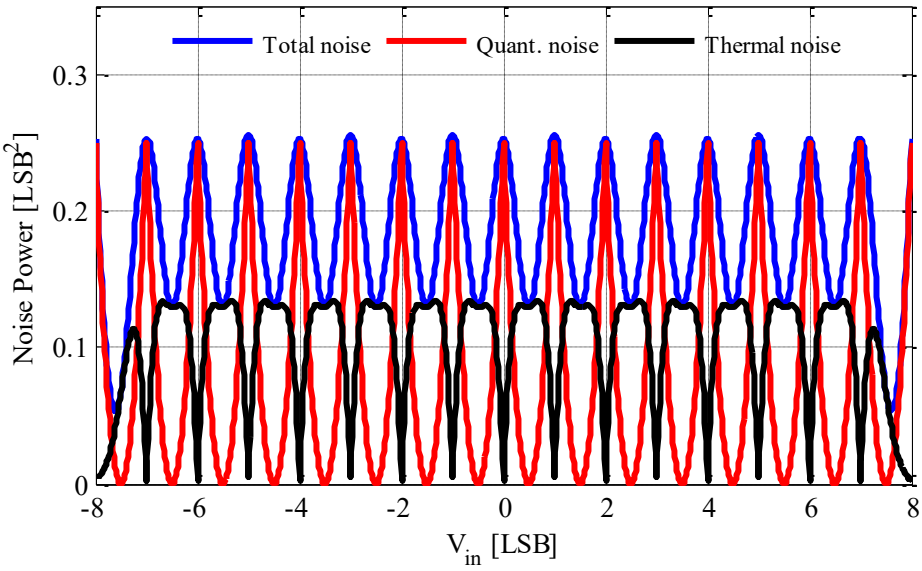


Figure 4-5. Calculated noise power versus Vin, σ=LSB/3

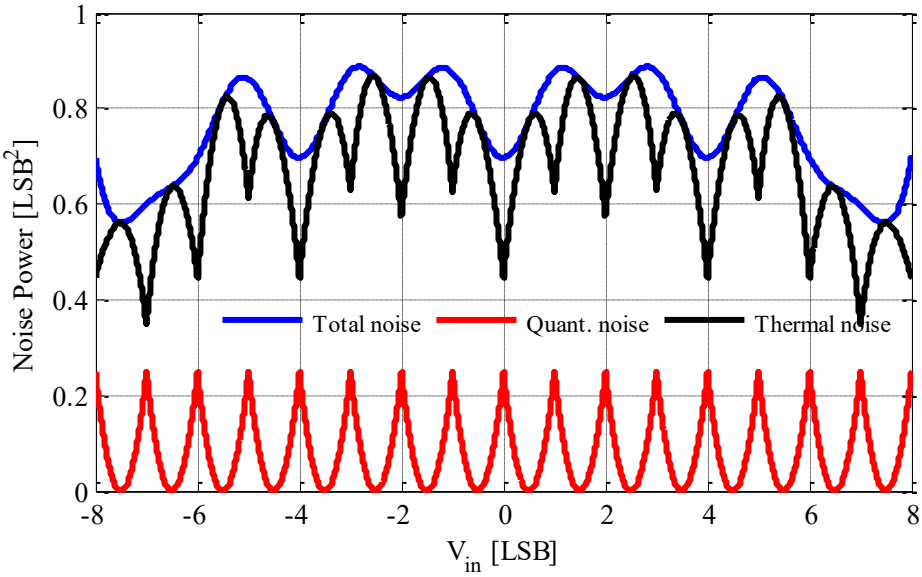


Figure 4-6. Calculated noise power versus Vin, σ=LSB

4.1.2 Analytical calculation of ENOB loss due to comparator noise

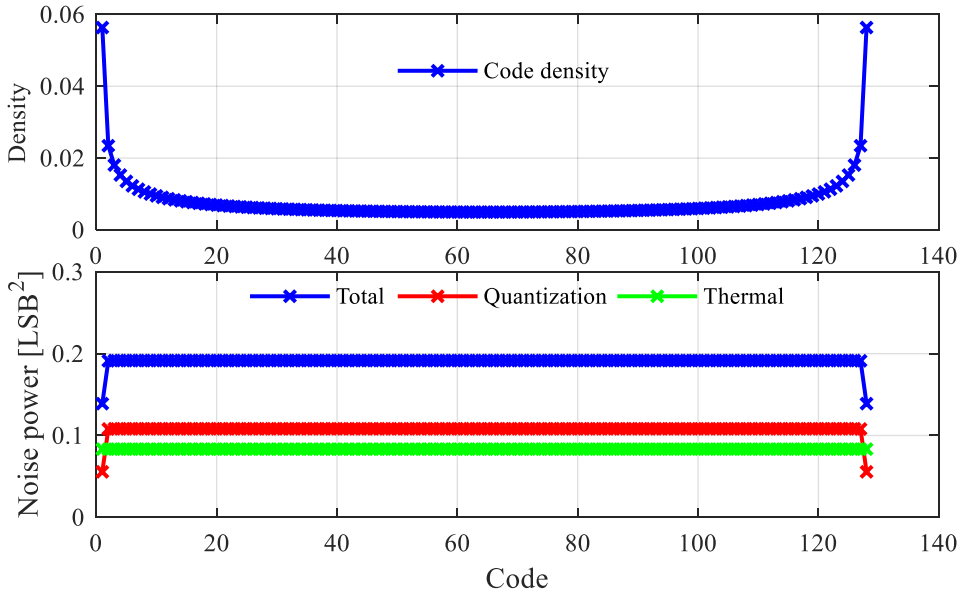


Figure 4-7. A 7-bit SAR ADC code density of a full-scale sinusoid signal and its calculated noise power with σ=LSB/3

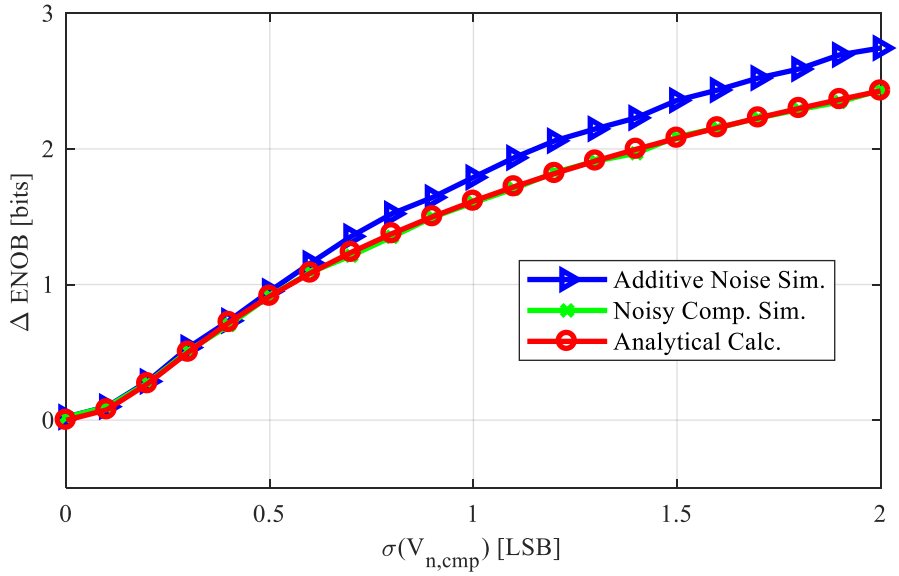


Figure 4-8. ENOB loss comparison between additive model and noisy comparator model

In the beginning of this chapter, we have pointed out that the additive model for comparator

noise is not accurate in estimating the ENOB loss when $\sigma \geq 0.5$ LSB, because the ADC conversion is not a linear process. In previous subsection, we have derived the input referred thermal noise of the ADC as a function input level [37]. If we know the distribution of ADC input signal, then we can calculate the averaged noise power of the ADC over full scale input by

$$\overline{V_{\mathrm{n,fs}}^2} = \int_{-V_{\mathrm{R}}}^{+V_{\mathrm{R}}} V_{\mathrm{n,tot}}^2\left(v_{\mathrm{in}}\right) \cdot \mathrm{P}\left(v_{\mathrm{in}}\right) dv_{\mathrm{in}}, \tag{4-10}$$

where $\mathrm{P}(v_{\mathrm{in}})$ is the probability density of the input signal distribution. To simplify the calculation, we just do the integration in code wise, then the integration of (4-10) becomes

$$\overline{V_{\mathrm{n,fs}}^2} = \sum_{d=0}^{2^N-1} \overline{V_{\mathrm{n,tot}}^2}\left(d\right) \cdot \mathrm{P}\left(d\right), \tag{4-11}$$

where $\mathrm{P}(d)$ is the code density of the input signal. Then the signal-to-noise-ratio (SNR) of the ADC can be calculated by

$$\mathrm{SNR} = \frac{V_{\mathrm{R}}^2}{2\overline{V_{\mathrm{n,fs}}^2}}. \tag{4-12}$$

Figure 4-7 shows the code density of a 7-bit SAR ADC and its calculated noise power with a full-scale sinusoid test signal. According to (4-12), the SNR and, then, the ENOB of the ADC can be calculated. Figure 4-8 shows the calculated ENOB of the 7-bit example ADC (without losing generality). Also, the result is compared with the behavioral simulation results. One can see that analytical calculation meets the noisy comparator behavioral simulation very well.

4.1.3 Bitwise investigation of comparator noise impact

If we want to optimize the noise impact of comparator, it is worthwhile to examine the noise impact in bitwise of SAR ADC. Figure 4-9 shows the calculated input referred noise of a 4-bit SAR ADC example according to (4-8) and (4-9) with only one comparison being noisy and all the rest comparisons being noiseless. As we can see from Figure 4-9, the noise contributions of individual comparisons are not identical. Instead, the LSB comparisons contribute more noise power than the MSB ones, and the contribution scales exponentially with a radix of 2. If we assume the noise of

each comparisons are additive, which is only true when the noise power is relatively small compared with quantization noise power according to our analysis in previous subsection, so the total averaged thermal noise power can be calculated by

$$\overline{V_{\mathrm{n,th}}^2} = \sum_{i=0}^{N-1} 2^{N-i-1} \cdot \overline{V_{\mathrm{n,th0}}^2}, \tag{4-12}$$

where $\overline{V_{\mathrm{n,th0}}^2}$ is the averaged power of each lobe in Figure 4-9 over the full scale range, and can be calculated by integral of thermal noise power upper left figure divided by the full scale range. It should be noted that this equation applies when all the comparisons have the same noise power level, so the shapes of all the thermal noise lobes in Figure 4-9 are identical.

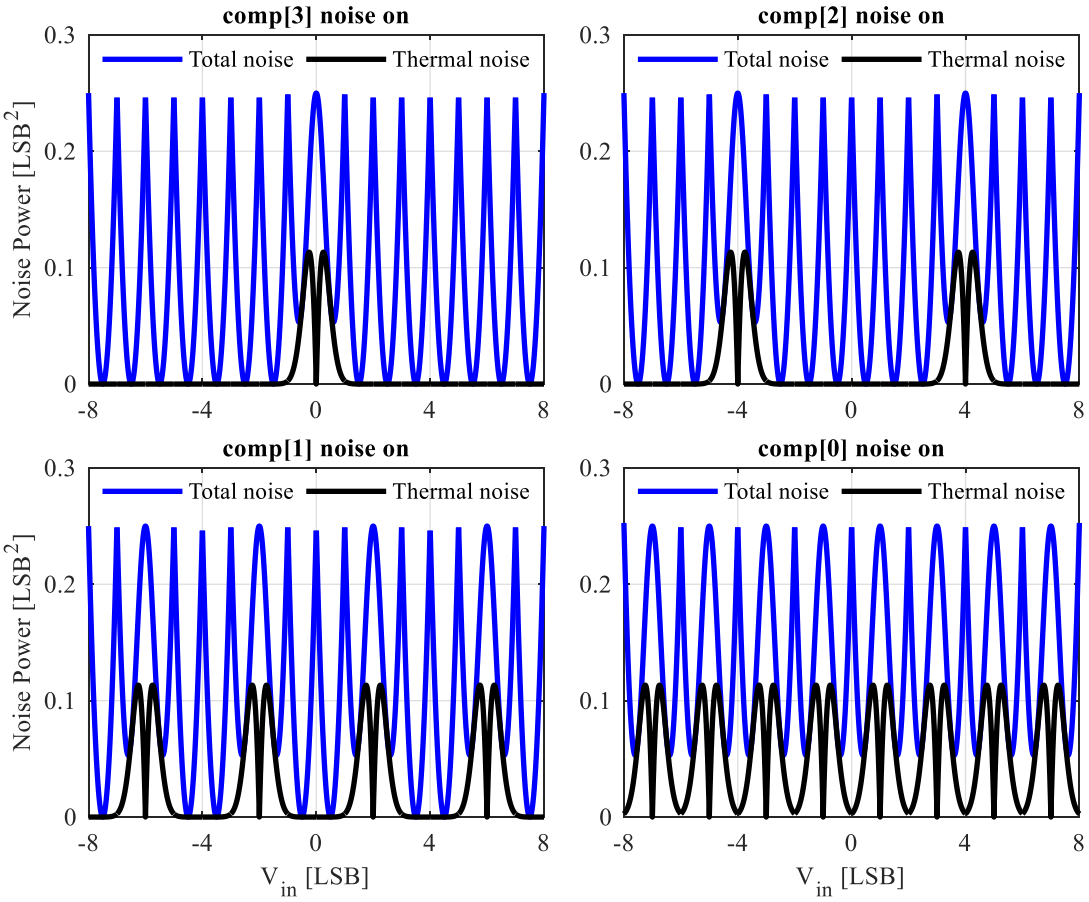


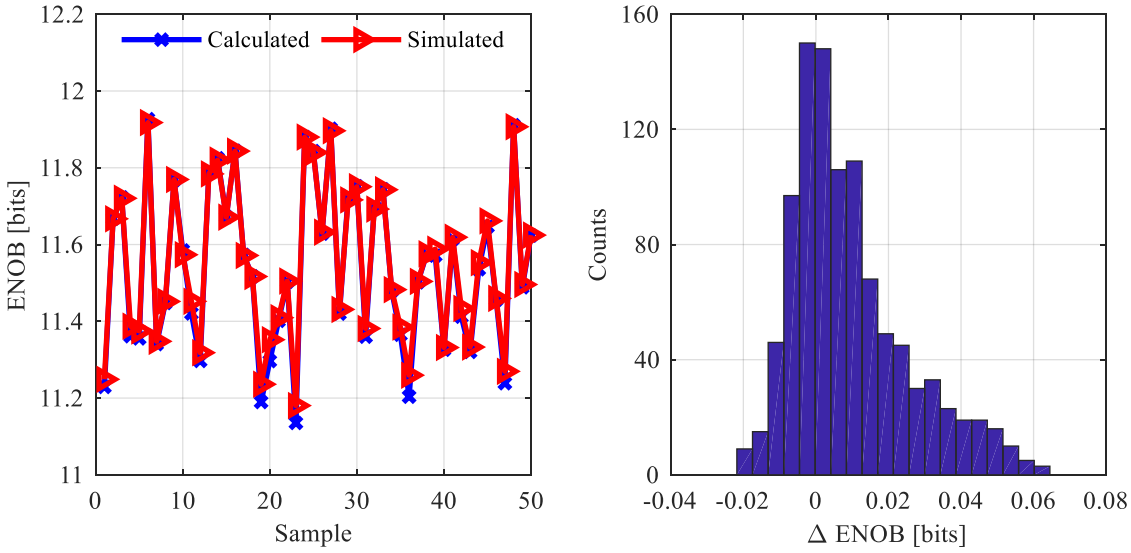
Figure 4-9. Calculated noise power with only one noisy comparisons in a 4-bit SAR ADC, σ=LSB/3

If we consider different noise level for each comparison, then (4-12) can be rewritten as

$$\overline{V_{\mathrm{n,th}}^2} = \sum_{i=0}^{N-1} 2^{N-i-1} \cdot \overline{V_{\mathrm{n,th}i}^2}, \tag{4-12}$$

where $\overline{V_{\mathrm{n,th}i}^2}$ is the averaged power of each lobe in i-th comparison with $i = 0$ denoting the LSB and $i = N$-1 the MSB. Form Figure 4-8, one can see that, with noise sigma less than 0.6 LSB, the comparative noise can be treated as additive noise to the input. That means in such cases $\overline{V_{\mathrm{n,th}i}^2}$ can be approximated by comparator noise power,

$$\overline{V_{\mathrm{n,th}}^2} = \sum_{i=0}^{N-1} 2^{N-i-1} \cdot \overline{V_{\mathrm{n,comp}i}^2}. \tag{4-13}$$



(a) (b)

Figure 4-10. MC Comparison of the calculated and simulated ENOBs of a 12-bit SAR ADC (σ ⩽0.6 LSB) (a) 50-sample MC ENOB comparison and (b) 1000-sample ENOB difference histogram

Figure 4-10 shows the comparisons of the calculated ENOBs using (4-13) and simulated ENOBs in time-domain behavioral of a 12-bit SAR ADC based on Monte-Carlo simulations, where the noise levels of comparisons are different and are randomly chosen while with its standard deviation less than 0.6 LSB. It can be seen from the results that the noise calculated results and the simulated results are highly consistent, which validate the accuracy of the model in (4-13) when the noise

voltage sigma is relatively small. Figure 4-11 shows the sample comparison while with noise standard deviation limit to 1 LSB. One can see that the accuracy of model of (4-13) degrades. This is predictable from Figure 4-8. It should be noted that the prediction using (4-13) is more pessimistic than it really is, which is also revealed by the asymmetry of the histogram in Figure 4-11 (b).

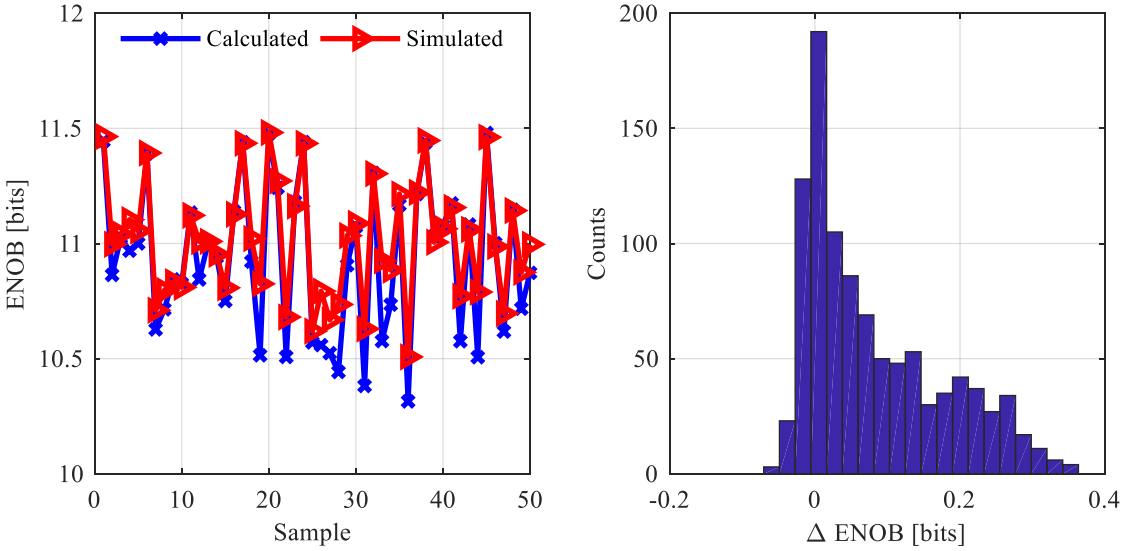


Figure 4-11. MC Comparison of the calculated and simulated ENOBs of a 12-bit SAR ADC ($\sigma \leqslant 1$ LSB) (a) 50-sample MC ENOB comparison and (b) 1000-sample ENOB differrence histogram

4.2 Comparator noise impact in sub-binary SAR ADCs

Sub-binary SAR ADCs have been widely used in digitally calibrated ADCs [1], [2], [40]. The sub-radix-2 scaling in the capacitive DAC avoids excessively large residue in the final stage of the SAR conversion by placing redundancies between the bits, and, therefore, guarantees the residue convergence and conversion precision of the SAR quantization [38]. It has also been demonstrated that the redundancy is able to tolerate the dynamic errors, such as dynamic offset from comparator, incomplete settling and so on, to certain extent depending on the scale of the redundancy [1], [39], [40]. For a sub-binary SAR ADC, shown in Figure 4-12, the capacitance of (k+1)-th capacitor is

less than summation of that of all the lower rank capacitors

$$C_k < \sum_{i=0}^{k-1} C_i. \tag{4-14}$$

The redundancy of a sub-binary SAR ADC can be calculate by [30]

$$R_k = \pm \frac{\sum_{i=0}^{k-1} C_i - C_k}{\sum_{i=0}^{N-1} C_i} V_{\mathrm{R}}, \tag{4-15}$$

where V_{R} is the reference voltage of the DAC. R_k basically measures how much dynamic error, such as dynamic offset, incomplete settling and comparator noise, occurring in k-th comparison the ADC can tolerate. One can see for a binary weighted SAR ADC, the redundancy of all the bits are 0.

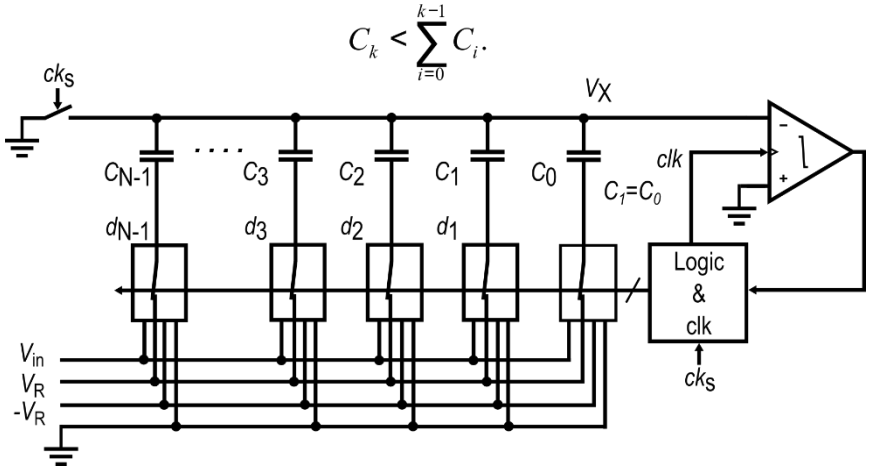


Figure 4-12. Sub-binary SAR ADC diagram of an N-bit (raw) SAR ADC

With redundancy in place, we expect the noise performance of a sub-binary SAR ADC, as shown in Figure 4-14. Table 4-1 shows an exemplary 7-bit SAR ADC with 8-raw-bit and a radix close to 1.9. Figure 4-13 shows the calculated input referred thermal noise power. Compared with Figure 4-7, the noise power 7-bit binary SAR ADC, we can see that input referred noise is not uniform over the full-scale range and the noise impact are attenuated in certain input levels. That is because the errors caused by comparator noise power in MSBs are can be recovered by the later conversions. However, this since the redundancy decreases as SAR conversion proceeds, and the later

comparisons correspondents to more threshold levels in the transfer curve of the ADC, so the noise impact attenuation occurs in certain input levels.

Table 4-1. Weight and redundancy of a 7-bit SAR ADC with 8-raw-bit and ~1.9 radix DAC (V_R=1 V)

k	Weight (W_k)	Redundancy (R_k) (mV)
8	60	77.5
7	32	46.5
6	17	31.0
5	9	23.3
4	5	15.5
3	3	7.8
2	2	0
1	1	0
0	0.5	0

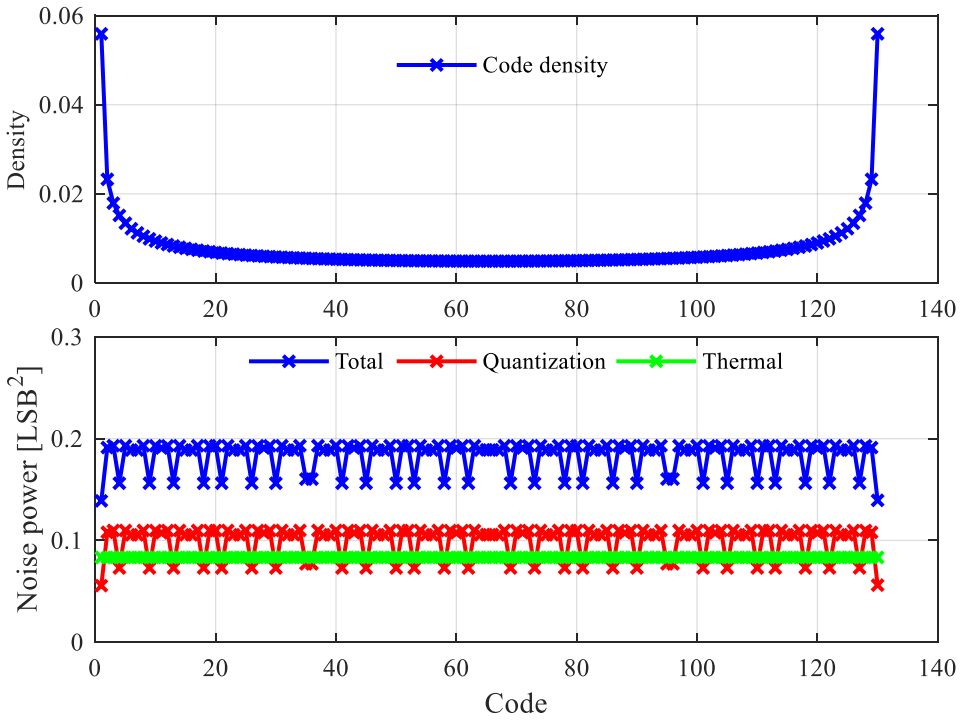


Figure 4-13. A 7-bit sub-binary SAR ADC code density of a full-scale sinusoid signal and its calculated noise power with σ=LSB/3

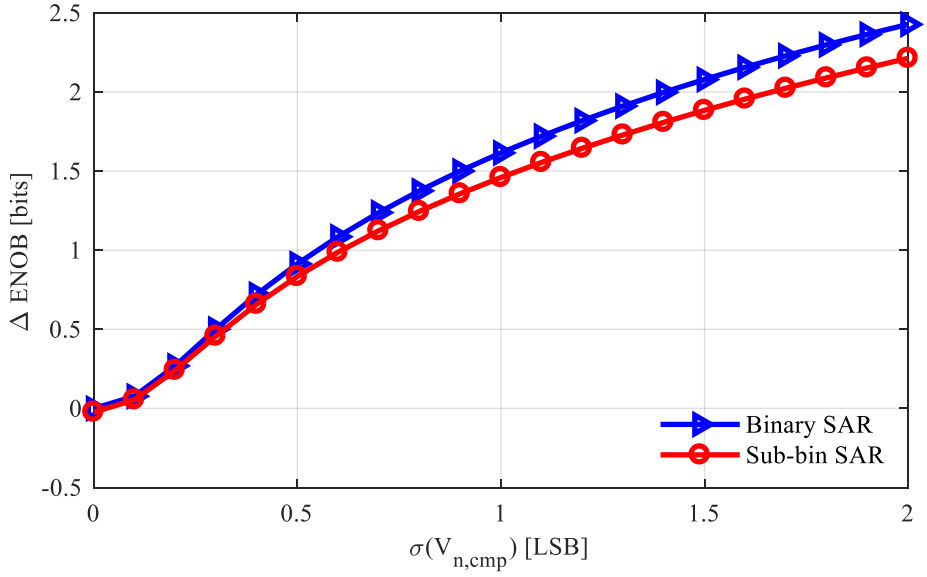


Figure 4-14. ENOB loss comparison between binary and sub-binary SAR ADCs

.3 Comparator noise and power optimization in SAR ADCs

The analysis in previous sections reveals that the noise impacts of different comparisons are not equally important. Therefore, we may consider the design of comparator as an optimization problem. This may be especially important for high-resolution SAR ADC design, where the comparators consume significant portion of the power consumption due to the low noise requirement. Figure 4-15 shows the scaling technique of comparator synthesis, where in order to reduce the input referred noise voltage of an optimized design in (*N*-1)-bit SAR ADC by half to accommodate the requirement of an *N*-bit ADC, it requires a 4× increase in both power consumption and transistor area.

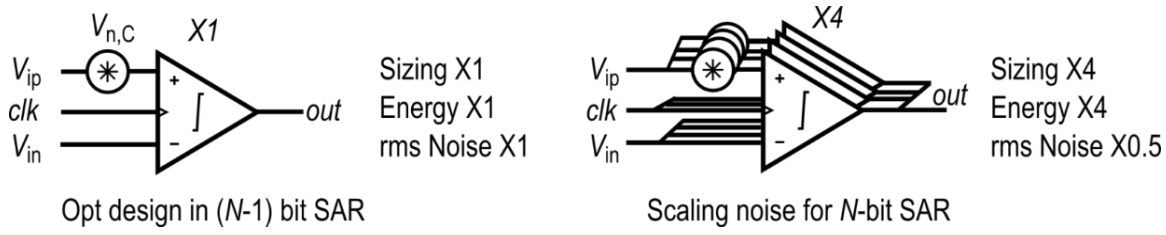


Figure 4-15. Scaling of comparator noise and power

In order to estimate the power consumption of a comparator with any noise power. Here we simplify the relationship between the noise and power of comparator as

$$\overline{V_{\mathrm{n,comp}}^2} = \frac{K_{\mathrm{P0}}}{E}, \tag{4-15}$$

where K_{P0} is a technology and delay related parameter of comparator design, E the energy consumption for one comparison. K_{P0} in a given technology can be extracted from an optimized comparator design with certain noise specification. Then (4-13) can be written as

$$\overline{V_{\mathrm{n,th}}^2} = \sum_{i=0}^{N-1} \frac{2^{N-1} K_{P0}}{2^i E_i}. \tag{4-16}$$

In the design of comparator, the total input referred thermal noise is defined by the system or application requirement. Then the optimization problem becomes

$$\begin{aligned} &\min_{\{E_i\}} \left(E_0 + E_1 + \cdots + E_{N-1} \right) \\ &\text{subject to: } \sum_{i=0}^{N-1} \frac{1}{2^i E_i} = \frac{\overline{V_{\mathrm{n,th}}^2}}{2^{N-1} K_{\mathrm{P0}}}. \end{aligned} \tag{4-17}$$

Solving this optimization problem,

$$E_i = \frac{1 - \left(\sqrt{2}/2 \right)^N}{1 - \sqrt{2}/2} \frac{2^{N-1-i/2} K_{\mathrm{P0}}}{\overline{V_{\mathrm{n,th}}^2}}, \tag{4-18}$$

$$\begin{aligned} E_{\mathrm{total}} &= \left(\frac{1 - \left(\sqrt{2}/2 \right)^N}{1 - \sqrt{2}/2} \right)^2 \frac{2^{N-1} K_{\mathrm{P0}}}{\overline{V_{\mathrm{n,th}}^2}} \\ &\approx \frac{11.6 \cdot 2^{N-1} K_{\mathrm{P0}}}{\overline{V_{\mathrm{n,th}}^2}}. \end{aligned} \tag{4-19}$$

From (4-18), one can see that, the ADC have best energy efficiency if the energy efficiency if the energy scales exponentially with a radix of $\sqrt{2}$ from MSB to LSB. Now let us compare the result with conventional SAR ADCs where all the comparisons have the same energy budget. That is

$$E_0 = E_1 = E_i. \tag{4-20}$$

Plug (4-20) into (4-16), one can have

$$E_i = 2\left(1-\left(1/2\right)^N\right)^2 \frac{2^{N-1}K_{P0}}{\overline{V_{n,th}^2}}, \tag{4-21}$$

$$\begin{aligned} E_{total} &= N \cdot E_i = 2N \cdot \left(1-\left(1/2\right)^N\right) \frac{2^{N-1}K_{P0}}{\overline{V_{n,th}^2}} \\ &\approx \frac{2 \cdot N \cdot 2^{N-1}K_{P0}}{\overline{V_{n,th}^2}}. \end{aligned} \tag{4-22}$$

Compare (4-19) and (4-22), one can see that with scaling technique, the SAR ADC has better power efficiency than that without scaling. Figure 4-16 shows the energy consumption comparison of SAR ADCs with and without energy/noise scaling, where we can see the noise/energy scaling between SAR steps might provide a strategy for power efficiency optimizations, which seems more and more appealing for high resolution SAR ADCs.

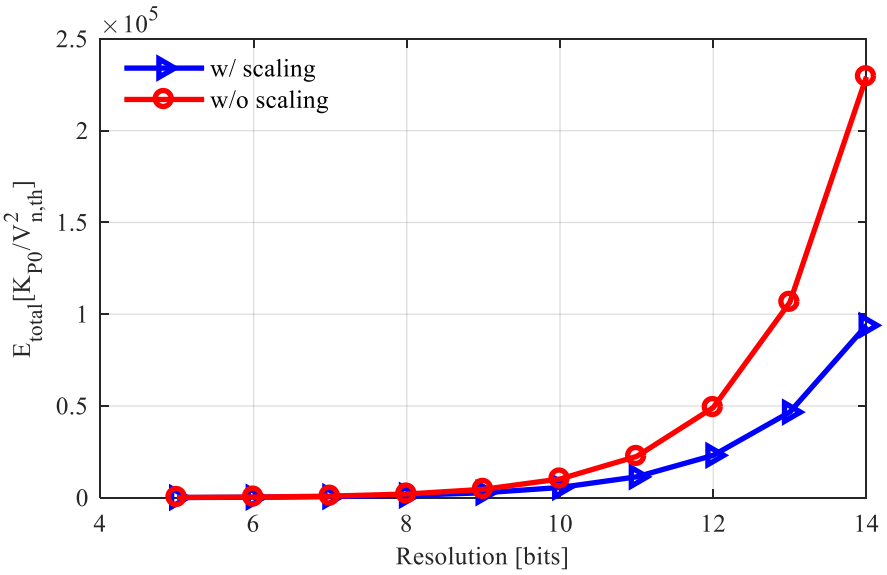


Figure 4-16. Comparison of energy consumption of SAR ADC w/ and w/o energy scaling

4.4 Summary

In this chapter, we investigate the comparator noise impact on the resolution of SAR ADCs. The calculation of input referred noise power of SAR ADC due to comparator noise has been reviewed. The impact of comparator noise is investigated in bit-wise in both binary and sub-binary SAR ADCs, and it has been demonstrated that the comparator noise impact factor scales exponentially along conversion steps. An optimization strategy for power efficiency has been proposed based on our analysis.

Chapter 5 : STATISTICAL ELEMENT SELECTION CALIBRATION FOR CAPACITOR MISMATCH IN SAR ADCS

Devices mismatch is a crucial issue in modern CMOS technology, and is the fundamental factor that limits the performance of various circuits, such as resolution of flash ADCs, distortion of DACs and phase mismatch in RF transceivers and so on. Statistical element selection (SES) calibration has been demonstrated as an effective technique in addressing transistor mismatches in many CMOS integrated circuits. This chapter is to review the principle SES technique and present the extension of this technique for capacitor mismatch calibration for high-resolution SAR ADCs, where large calibration range and fine tuning step-size can be achieved by using our proposed design techniques.

5.1 SES calibration for mismatch calibration

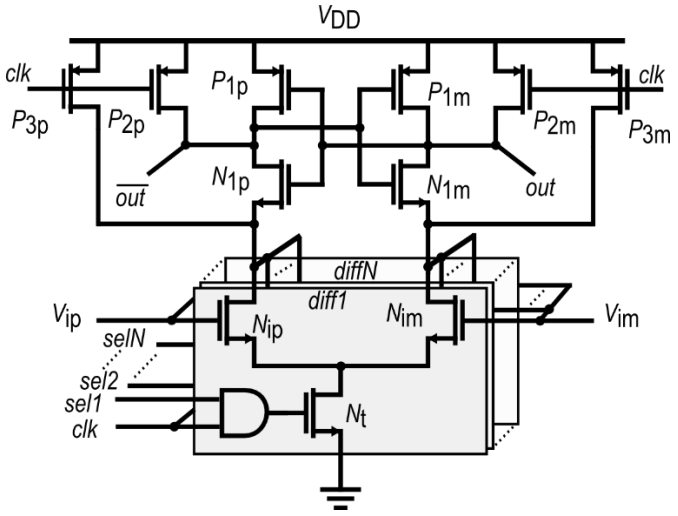


Figure 5-1. Reconfigurable comparator using SES calibration

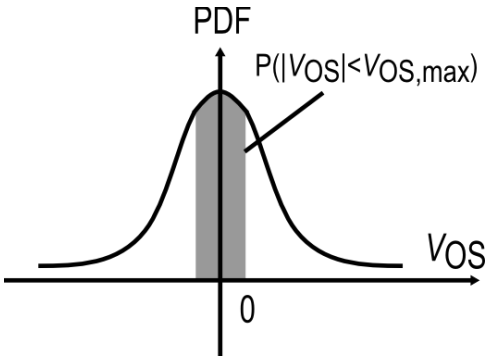


Figure 5-2. Offset distribution of a comparator

Statistical element selection (SES) calibration has been explored in correcting MOS devices mismatch in ADC, DAC and RF frontend circuits [41]-[44]. In [41] and [42], SES calibration techniques are employed to calibrate the offset of dynamic comparators. The principle can be illustrated using the design example shown in Figure 5-1. In order to achieve certain offset specification, the most straightforward way is arbitrarily increasing the dimensions of the input transistor, of which the threshold mismatch is the key offset contributor. This results in excessively large parasitics and power consumption and degrade the performance of the comparator. In SES-based comparator, shown in Figure 5-1, instead of using large input transistors, the input pair and tail transistor are equally split into N subsets, and each of them can be digitally enabled and disabled with very little extra overhead of a few logic gates. Such a reconfigurable structure provides a pool of $(2^N - 1)$ comparator different configurations, which is a tremendously large space to search for one "good" design. With a given number of selected elements, K, if we assume that the offset permits a Gaussian distribution, shown in Figure 5-2, then the probability of failure is

$$P_{\text{fail}} = (1-p)^{C_N^K}, \tag{5-1}$$

where p is the probability of meeting the specification,

$$p = P(|V_{\text{OS}}| < V_{\text{OS,max}}), \tag{5-2}$$

From (5-1), the exponential function drastically brings down the failure probability even if p is much smaller than 1.

The benefit of such a break-recombine design is to break the constraint imposed by the Pelgrom's scaling rule [33], such that by post-manufacturing processing a small offset can be achieved with small active area, which is beneficial for power and speed considerations.

5.2 Proposed SES calibration for capacitance mismatch

As we have explained in Chapter 2, it is desired to keep the capacitance of SAR ADCs small for the considerations of speed and power-efficiency. However, the minimum capacitance is largely bounded by two factors: thermal noise and process variation. Figure 5-3 shows the total DAC capacitance lower boundary (without capacitance calibration) imposed by the matching requirement ($3\sigma_{DNL}< 0.5$ LSB) and *KT/C* noise requirement (ENOB loss < 0.5 bit). It is clear that the mismatch requirement is far more stringent than the thermal noise limit, so it would be desirable to move the blue curve closer to the red one by using capacitance calibration techniques, and the calibration precision in high resolution is very hard to achieve. Also, as the total capacitance increases, the capacitor spans a large area and, therefore, systematic variation may become dominant, which requires the calibration to have large tuning range.

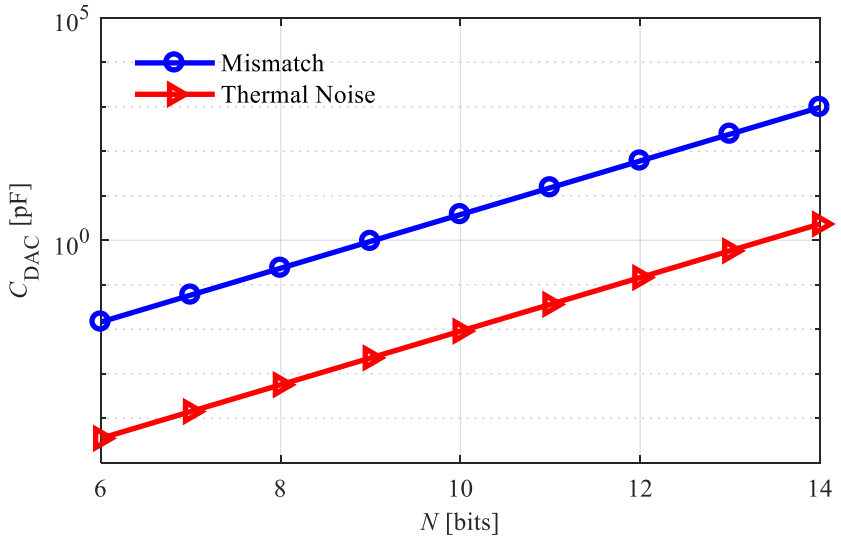


Figure 5-3. DAC capacitance lower boundary by mismatch and thermal noise

5.3 Capacitance calibration based on SES with built-in (BI) variations

5.3.1 Calibration range

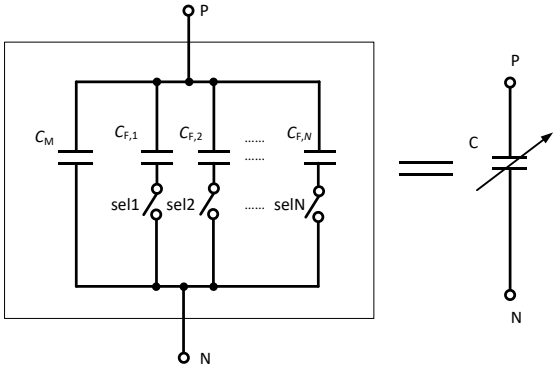


Figure 5-4. Reconfigurable capacitor and its equivalence

Table 5-1. Capacitor parameters of SES calibration

C_M	8.5 fF
N	14
K	7
$C_{F,i}$	1.5 fF / 7
$K_C(=\sqrt{C}\frac{\sigma_C}{C})$	$\sqrt{1.5\text{ fF}}\cdot 1\%$

Consider the capacitor structure in Figure 5-4, where a reconfigurable capacitor consists of two parts, the main part C_M and the fractional part $C_{F,i}$, where the fractional part consists of multiple elements and can be digitally switched on and off. If all the fractional elements are identical, as we know from SES algorithm, selecting K fractional elements from N possible elements enables a huge search space which translates into a very fine tuning in presence of process variations. The tuning precision can actually be improved by increasing N [41]. However, the tuning range is limited. Let us take an example of 10 fF capacitor design, of which the nominal design parameters are listed in Table 4-1. In this example, the total fractional capacitance accounts for 15% of the unit capacitance to ensure a relatively large calibration range. Here we assume process variance is Gaussian and

Pelgrom's area scaling rule applies. This is because its dimension can be relatively small, which has been validated in [68] with silicon results by properly selecting the geometry and metal layers. To simplify the problem, we only study the statistics of the fractional capacitances, because the purpose is virtually using the reconfigurable fractional part to calibrate the main part mismatch.

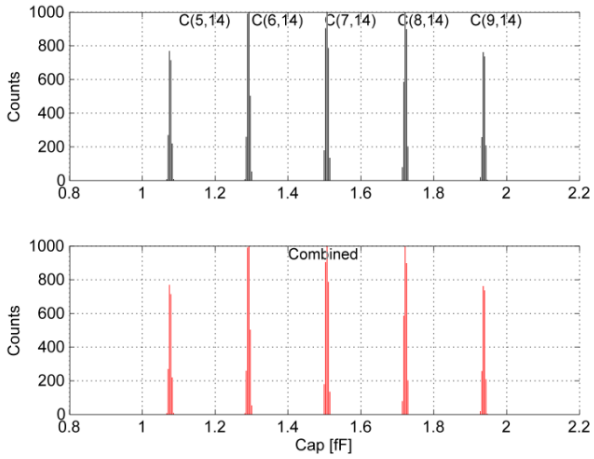


Figure 5-5. Fractional capacitance distribution histogram

Table 5-2 Fractional capacitances for ±25% built-in variations ($K_C = \sqrt{1.5\ \text{fF}} \cdot 1\%$)

i	$C_{F,i}$	$\sigma(\Delta C_{F,i}/C_{F,i})$	i	$C_{F,i}$	$\sigma(\Delta C_{F,i}/C_{F,i})$
1	0.161 fF	1.15%	8	0.218 fF	0.99%
2	0.169 fF	1.13%	9	0.226 fF	0.97%
3	0.177 fF	1.10%	10	0.235 fF	0.96%
4	0.185 fF	1.07%	11	0.243 fF	0.94%
5	0.194 fF	1.05%	12	0.251 fF	0.92%
6	0.202 fF	1.03%	13	0.260 fF	0.91%
7	0.210 fF	1.01%	14	0.268 fF	0.89%

Figure 5-5 shows the histogram of the fractional capacitance distribution with all fractional elements identical, where K = 5, 6, 7, 8 are chosen to try to form a large calibration range. That resulted capacitances highly concentrate around the nominal values, and there are significant gaps

between consecutive selecting numbers. That means this method cannot cover a relatively large tuning range with small steps, and, therefore, is not suitable for our targeted capacitor calibration. Also, the distribution of combined capacitance is concentrated around the nominal values, meaning there is excessively large redundancy for calibration nearby these values. According to (5-1), this does not help improve the yield significantly.

In order to enlarge the tuning range, we propose to introduce "built-in variations" among the fractional elements in Figure 5-4. As shown in Table 5-2, we design the fractional elements with different nominal values with ± 25% (of 1.5 fF) built-in variations. The relative mismatch can be estimated by [33], [68]

$$\sigma\left(\frac{\Delta C_{\mathrm{F},i}}{C_{\mathrm{F},i}}\right)=\frac{K_{\mathrm{C}}}{\sqrt{C_{\mathrm{F},i}}}. \tag{4-3}$$

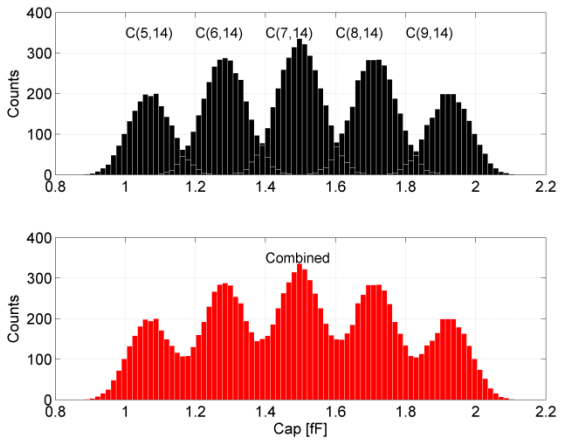


Figure 5-6. Fractional capacitance distribution with BI variations

Figure 5-6 shows capacitance distribution with nominally linear built-in variations. Thanks to the built-in variations, the distribution of each *K*, becomes more spread and bridges the gap between the consecutive *K*'s. Therefore, it provides "continuous" tuning range from 1fF to 2fF, which is ± 5% of the 10 fF unit capacitance.

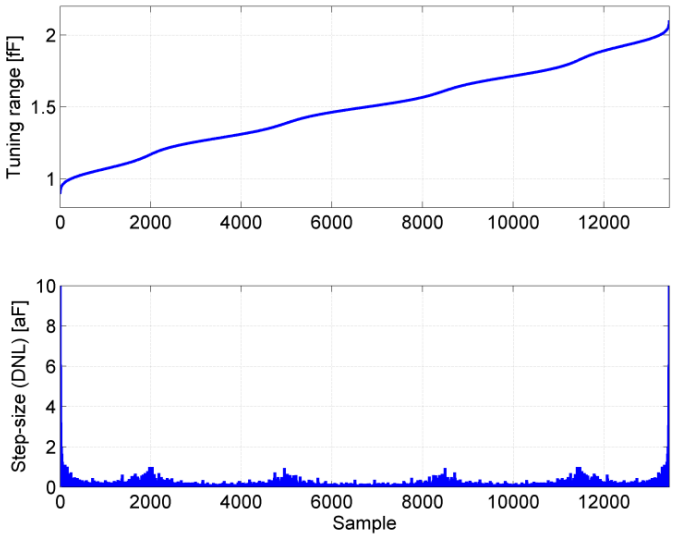


Figure 5-7. Tuning range and step-size of the SES with BI variations

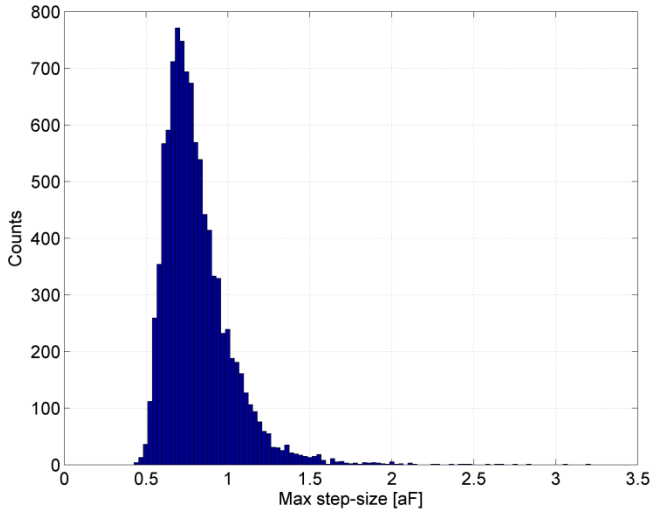


Figure 5-8. Maximum step-size histogram in 1fF~2 fF based on10,000-run MC simulation

5.3.2 Calibration precision

Now let us check the tuning step-size by sorting all the combined capacitance in Figure 5-6, as shown in Figure 5-7. One can see that the tuning range covers well the 1fF ~ 2 fF range. The step-size is obtained by calculating the "DNL" of tuning range curve. One can see in the range of interest,

the step-sizes are well below 2 aF, which translates into 0.02% of the 10 fF unit capacitance. Figure 5-8 shows the 10,000-run statistical simulation of the maximum step-size histogram, which reveals that in most of the runs the maximum step-sizes are below 2 aF.

In the example above, we arbitrarily choose $K_C/\sqrt{1.5\ \text{fF}} = 1\%$, which is inferred from our simulations on a commercial design kit and some published data in [68]. However, this parameter might vary significantly with foundry, technology node, and even the capacitor structure. Especially if we need to do custom design of capacitors, there is no reference to extract this parameter precisely. Thus, it is important to verify the robustness of this SES-based calibration over K_C. Figure 5-9 presents the maximum step-size simulation versus capacitance mismatch parameter K_C, where the max step-size is the maximum value among the smaller 99% samples extracted from 1000-run MC simulations. It is interesting to find that for $K_C/\sqrt{1.5\ \text{fF}} < 1\%$, a smaller relative mismatch means a larger maximum step-size, while for $K_C/\sqrt{1.5\ \text{fF}} > 1\%$, the maximum step-size almost keep constant.

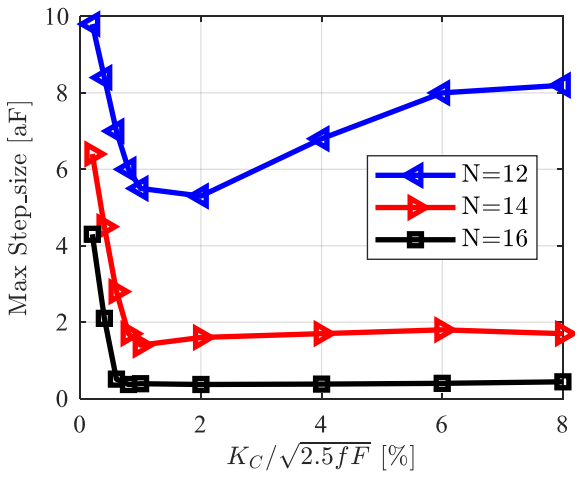


Figure 5-9. Maximum step-size of versus capacitance mismatch parameter K_C

To sum up, by embedding built-in variations, the unit capacitor structure in Figure 5-10, can achieve >±5% tuning range, and a tuning step-size as small as 0.02%. The modelling is based on assumption that the fractional capacitance permits Pelgrom's area scaling rule. From Figure 5-9 the step-size of the calibration is relatively stable over a large range of mismatch parameter K_C. Also,

the step-size can be decreased by increasing the number of fractional elements while with the cost of longer control word and calibration time. As for implementation, the built-in variations can be introduced by adjusting the finger length parameter of the structure in Figure 5-10.

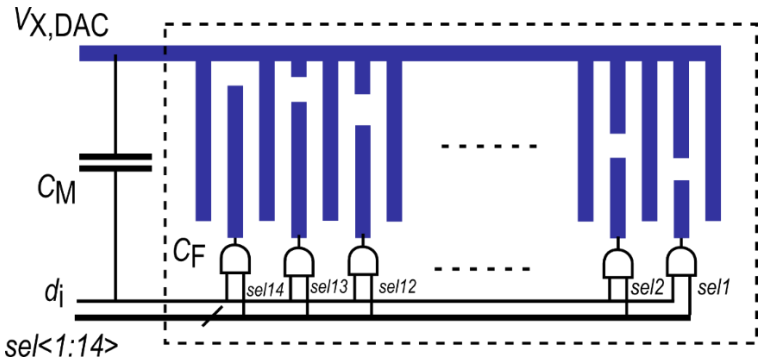


Figure 5-10. Possible implementation of embedding built-in variation

5.4 Summary

This chapter reviews the SES calibration techniques. And an extended calibration technique for capacitor mismatch in SAR ADC has been proposed. By inserting built-in variations between capacitor elements, the SES capacitor has relatively extended calibration range and less sensitive to the mismatch parameters of technologies. The fine tuning calibration step-size arises from the random mismatch of the ADC.

Chapter 6 : 8-BIT 150 MS/S LU-SAR ADC WITH BACKGROUND OFFSET CALIBRATION

In section II, the impact of offset mismatch on the linearity of LU-SAR ADC was analyzed. Equations (3-44) – (3-46) provide useful guidance in defining the comparator offset specification. Consider an 8-bit LU-SAR ADC as an example. In order to design for a 0.5-bit ENOB loss target and a yield target of 99%, according to Figure 8, the comparator offset should be as low as 0.15 LSB. This is a very stringent requirement considering typical mismatch levels in modern CMOS technology. Assuming that the threshold mismatch of the input pair is the dominant contributor [15], the comparator offset can be estimated as [33]

$$V_{OS} \approx \sqrt{2}\frac{A_{VT}}{\sqrt{WL}}, \tag{6-1}$$

where A_{VT} is Pelgrom's coefficient, and is about 4-5 mV·μm in the 130 nm technology under consideration. The factor of $\sqrt{2}$ arises from the differential input transistors. If we relied on scaling up the transistor size to meet the offset mismatch requirement, the resulting transistor area would be greater than 87 μm^2 assuming LSB = 4 mV, which is infeasible due to large parasitic capacitance.

In order to mitigate the effects of offset mismatch in LU-SAR ADCs efficiently, this work therefore takes the approach of auto-zeroing all the comparator offset in real-time. In this section, we present our proposed LU-SAR ADC architecture with offset mismatch calibration and the implementation of a fabricated 8-bit ADC.

6.1 Proposed ADC topology

Error! Reference source not found. 6-1 shows the proposed 8-bit asynchronous SAR ADC a rchitecture and its timing diagram. The ADC consists of a pair of bootstrapped switches, 8 identically designed, offset self-calibrated comparators, a 7-bit capacitive DAC, and supporting

logic circuits. During the conversion phase, the ADC works asynchronously similarly to [4], [11], [12] in a way that the following comparison is triggered by the completion of its previous comparator after some delay, which is optimized to achieve sufficient DAC settling accuracy[4].

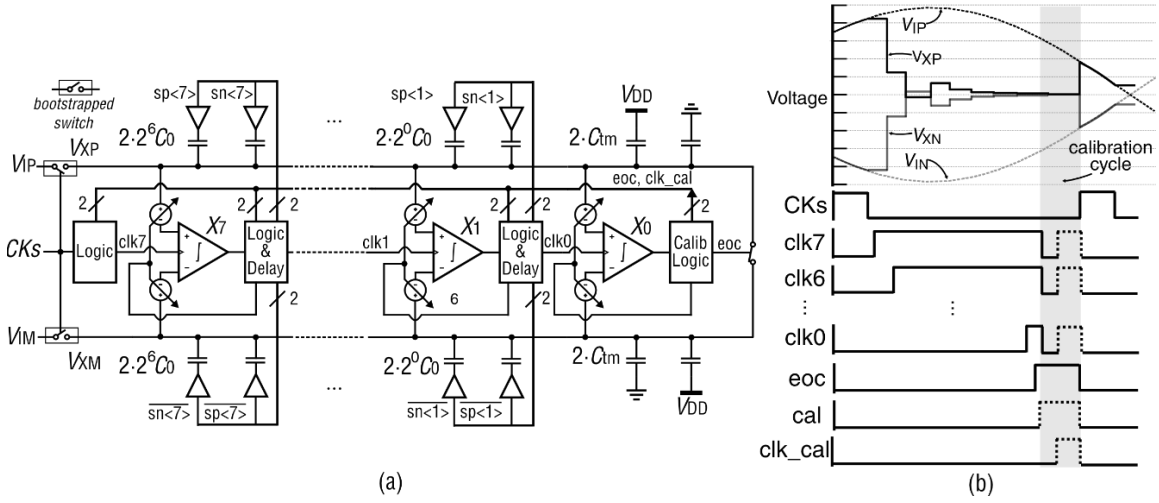


Figure 6-1. Proposed 8-bit asynchronous SAR ADC (a) and its timing diagram (b).

As pointed out in [16],[17], the comparator input common-mode fluctuation brings about additional dynamic offset. Therefore, a split-capacitor DAC [5], instead of a monotonic switching DAC that is conventionally used in sub-10 bit SAR ADCs [2], [4], [16], is chosen to maintain the DAC output common-mode at a constant level. Figure 10 shows a comparison of capacitor switching procedures using MSB capacitor as examples and the corresponding DAC voltage curves. The monotonic DAC switches the capacitor in only one side of the differential DAC after each comparison, resulting in a monotonic common-mode change during the binary search procedure; the split-capacitor DAC, however, maintains a constant common-mode by switching half the capacitor from each side of the differential DAC symmetrically, and thus avoid the dynamic offset from bit to bit.

To calibrate the random offset mismatch and increase the achievable resolution, a calibration phase is inserted following the conversion phase, as shown in Figure 6-1 (b). The end-of-conversion signal, *eoc*, which is triggered by the completion of the LSB comparator, marks the beginning of this phase (denoted by waveform *cal*). By shorting the differential DAC output, the outputs of both

two sides of the DAC are reset to common-mode voltage. It is noteworthy that differential outputs after normal SAR conversion are both close to the common-mode with a difference less than 1 LSB of the DAC, which guarantees fast settling. All the self-calibrated comparators are then clocked once to auto-zero their individual offsets. The auto-zeroing process of the comparator will be described in detail in the next subsection. Considering the high convergence speed of such a deterministic calibration technique, a pseudo-random number (PRN) generator is used to control the calibration randomly occurring in roughly once every 8 cycles [32].

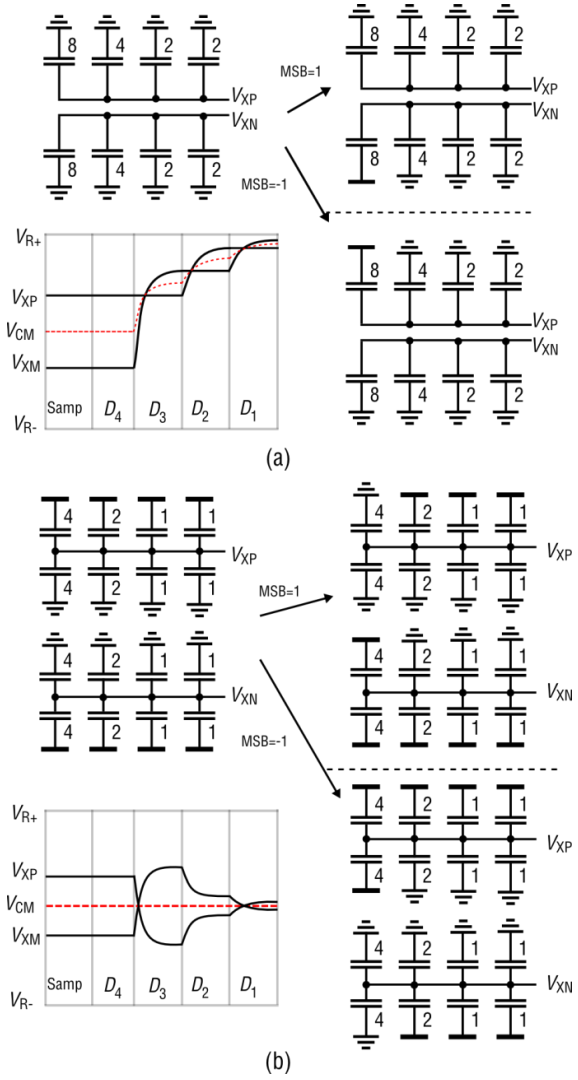


Figure 6-2. 3-bit DAC switching and common-mode comparison for monotonic switching (a) and split-cap switching (b).

Although our proposed calibration shares some similarities with [34] including the idea of calibrating the LU-SAR comparators in background and adjusting comparator offset using charge pump and auxiliary differential pair, the following differences and/or advantages of our LU-SAR architecture are highlighted. First, instead of using different designs for MSB, LSB and reference comparators as in [34], all the comparators in our ADC are designed to be identical, which saves design effort while with some power penalty. Also, since they are calibrated in background, the foreground calibration steps in [34] for MSB comparators are not needed. Second, since offset mismatch in [34] can only be detected when the reference comparator and comparator under evaluation give different outputs, this calibration potentially suffers from losing tracking when a DC or very low frequency signal is fed to the ADC. This is not an issue in our calibration scheme because all the comparators are independently calibrated to zero offset. Third, although the technique in [34] does not need an explicit calibration cycle compared to our calibration, a redundant bit may be necessary to accommodate the offset variations of MSB comparators.

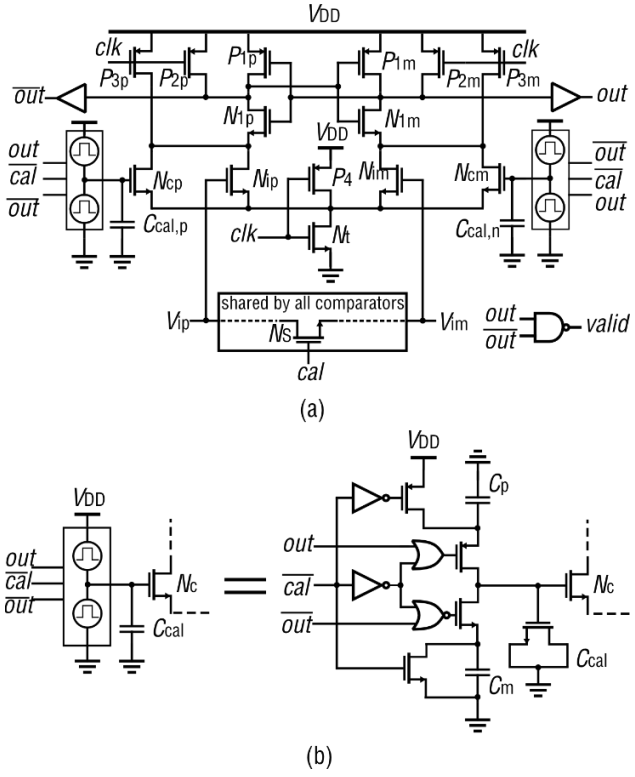


Figure 6-3. Detailed circuit schematic of self-calibrated comparator

6.2 Circuit implementation

6.2.1 Offset self-calibrated comparator

The offset self-calibrated comparator is a critical block for implementing the proposed technique. The comparator circuit, shown in Figure 6-3 comprises a Strong-Arm latch dynamic comparator combined with differential offset calibration circuits. The reset transistors P_2, P_3 and P_4 guarantee that every comparison is subject to the same initial conditions, thus avoiding memory effects. Also, transistors N_{cp} and N_{cm} divert a portion of the differential current from the input pair and introduce offset to counter the random offset of the comparator. The value of the built-in offset is controlled by the differential voltage between $C_{\text{cal,p}}$ and $C_{\text{cal,m}}$, which are adaptively adjusted according to the comparator offset. Before the calibration phase, two small capacitors C_{p} and C_{m} are pre-charged to V_{DD} and *GND*, respectively; During the calibration phase the inputs of comparator are shorted, and the comparator is clocked to identify the polarity of its offset, then the result is used as a feedback to determine whether calibration capacitor, C_{cal}, absorbs charge from C_{p} or pushes charge into to C_{m}, driving the stored voltage into the direction of minimizing overall offset. A single calibration cycle (including resetting comparator and DAC, firing the comparator and refreshing the calibration voltages) takes typically less than 600 ps in the designed ADC. The calibration range is determined by the size ratio of calibration pair transistors to input pair transistors. When convergence is achieved, the offset dithers around zero, behaving as calibration noise. The calibration speed is a function of capacitance ratio of C_{p} and C_{m} to C_{cal}. A larger ratio leads to a larger step-size thus faster calibration rate but, however, a larger calibration noise after convergence. The comparator employed in this design presents an input referred offset voltage before calibration of approximately 2 LSBs (~10mV). Therefore, in this work, the calibration range is designed to be larger than ±40mV with a step size of ~80 μV. The step-size is achieved by sizing C_{p} and C_{m} as 1 fF, which are implemented by interconnect parasitics, and C_{cal} as 1.5 pF. Note that since the calibration operates in a closed loop, C_{p}, C_{m} and C_{cal} are not required to be accurate, and the

variation of capacitance affect only the calibration noise, which is far below the comparator noise in our design. Since the calibration voltage is relatively stable after convergence and the calibration works in real-time, MOS capacitor is used for C_{cal} to save area due to its higher capacitance density than metal capacitors.

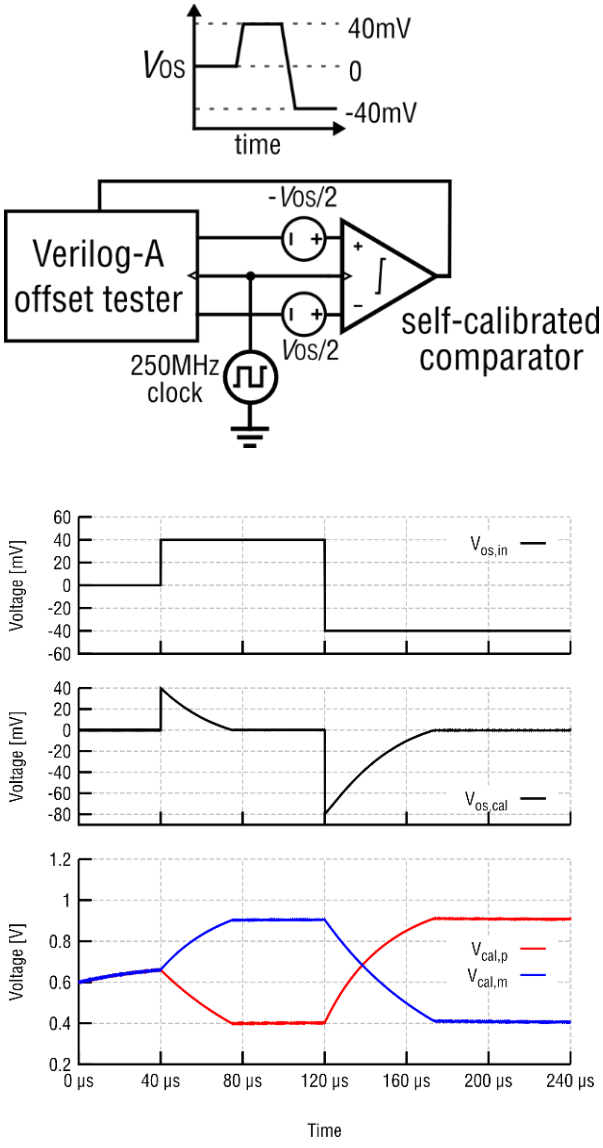


Figure 6-4. Test-bench for comparator calibration range simulation and waveform of calibration process

Figure 6-4 shows the simulation test-bench used to characterize the calibration range and step-size of the comparator, where a Verilog-A offset tester dictates the calibration-and-measurement process, and the two voltage sources are used to mimic the comparator offset. As shown in the

calibration waveform in Figure 6-4, the comparator is assigned a zero initial offset, so $C_{cal,p}$ and $C_{cal,m}$ have no differential voltage, but adjust the common-mode from the initial state; When the input offset changes to 40 mV, the calibration voltages diverge adaptively to bring the offset back to zero; After the offset input switches to -40 mV at 120 μs, the offset of the comparator are observed to gradually converge to zero from -80 mV with the calibration voltages change accordingly. The comparator gets calibrated in 60 μs. The measurement of the offset takes 15 clock cycles followed by an extra clock cycle for calibration. The calibration noise is 50 μV_{rms} according to the simulation. Thanks to the offset calibration, the comparator can be down-sized with a relaxed offset requirement. This is important in this architecture because in the later comparisons all the previous comparators are not reset, the nonlinear capacitance introduced by the comparator input transistors participates in the charge redistribution. Therefore, it is necessary to minimize the input transistor size. In this comparator, the input transistor is sized down to thermal noise constraint, thanks to the large calibration range of the self-calibration.

It is noteworthy that comparing a zero input during the calibration renders the comparator a larger chance of meta-stability than normal. However, the calibration technique is able to tolerate the occurrence of meta-stability. As depicted in Figure 6-3 (b), if the comparator has not made a solid decision by the end of the calibration cycle, out and $\overline{out}$ block the operation of charging/discharging and the calibration is skipped for the current sample. On the other hand, the appearance of meta-stability is a good indication of close-to-zero offset, so skipping the calibration in such cases would not cause any problem.

By employing background offset calibration, of which calibration precision is limited by thermal noise, the offset mismatches among comparators are greatly reduced. In this design, the input referred noise voltage is designed to be 0.4 mV_{rms} (~0.1 LSB). The offsets calibrated to this variation level, as revealed by Figure 8, are sufficient to achieve 0.5-bit ENOB loss target and a yield target of 99%.

6.2.2 DAC capacitors and buffers

The 7-bit capacitive DAC is shown in Figure 6-1, together with the ADC architecture. The custom design technique for metal-oxide-metal (MOM) capacitor proposed in [31] is employed to improve the matching of capacitors while using small unit capacitance, about 1 fF in this design, for the sake of saving switching power and settling time for the DAC. As mentioned before, the comparator input pair introduces non-linear parasitics to the DAC. Therefore, in order to suppress the impact, the termination capacitances C_{tm} are sized to $128C_u$, reducing the input range of the ADC by half. All the DAC buffers are sized proportionally to the corresponding DAC capacitors to achieve a balanced settling time from bit to bit.

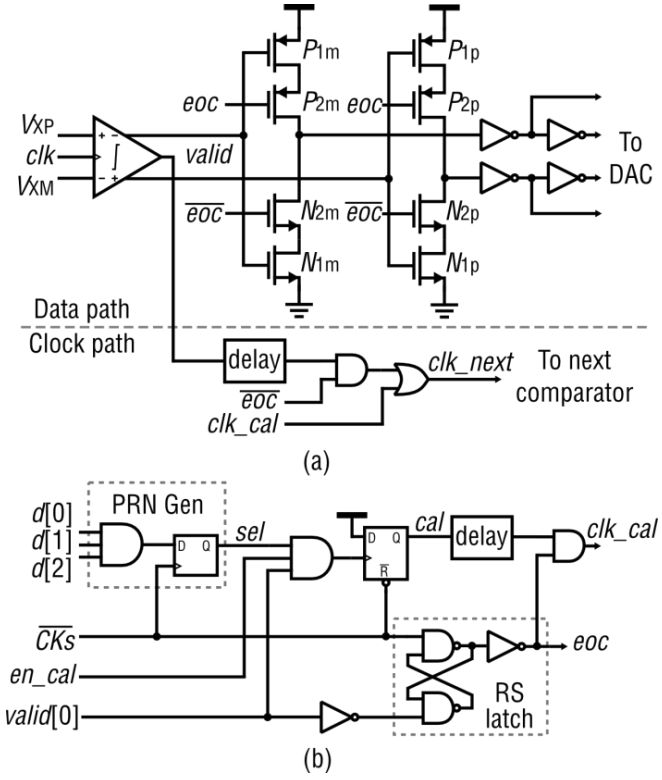


Figure 6-5. Logic circuits in comparator stage (a) and calibration controller (b)

6.2.3 Logic controller

As mentioned before, one of the advantages of the multi-comparator SAR architecture is to save timing budget by splitting the path of generating the asynchronous SAR clock and that of feeding

the data to DAC for binary search. Most of the logic circuits are distributed to the vicinity of the individual comparators with reduced routing parasitics in the path. Figure 6-5 (a) shows the output logic circuits of all the comparators except the LSB comparator. In the data path, the comparator outputs are fed to the DAC passing only a few buffer gates, however, transistors P_2 and N_2 are inserted to an inverter and controlled by eoc to block the DAC switching during the calibration phase while relying on node parasitic capacitance to preserve the DAC inputs from conversion phase. In the clock path, a dedicated delay is added to compensate the settling time of the DAC before clocking the next comparator. During the calibration phase, the asynchronous clock path is by-passed, and all the comparators are triggered by a global calibration clock *clk_cal*. The LSB comparator is followed by the calibration control logic, as shown in Figure 6-5 (b). An RS-latch is used to generate the eoc signal, which marks the end of conversion phase and beginning of the reserved calibration phase. A simple PRN generator by using 3 LSB outputs of the ADC from the previous sample enables a 1/8 opportunistic calibration.

6.3 Measurement results

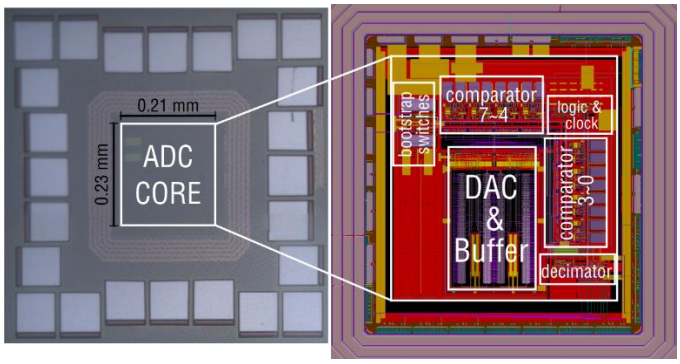


Figure 6-6. Chip die photograph and ADC core circuit layout

The prototype 8-bit ADC proposed in Section IV has been fabricated in a 130-nm technology. Figure 6-6 shows the die photograph and ADC core active circuit layout, which occupies an area of 0.048 mm^2. The total sampling capacitance is about 512 fF in each side of the differential DAC, half of which is from the termination capacitor. The differential input range of the ADC is 1.2 V_{pp}

with a 1.2-V supply voltage. In order to adapt to the input-output (IO) circuits speed, the ADC outputs are down-sampled by $8\times$ by an internal decimating circuit for testing purpose. The prototype ADC features a control bit en_cal, shown in Figure 6-5 (b), for observing the difference with and without the calibration enabled. The measured results are summarized in Table 6-1.

Table 6-1. Summary of measured performance

Technology	130nm CMOS
Resolution	8 bits
Input capacitance	512 fF
Supply voltage	1.2 V
Sampling rate	150 MS/s
Input range	1.2 V_{pp}
DNL (LSB)	-0.10/0.80
INL(LSB)	-0.80/0.81
SFDR	51.7 dB
Nqst. SNDR	42.9 dB
Peak SNDR	45.4 dB
Power	640 μW
FoM	37.5 fJ/conv-step
Active area	0.048 mm^2

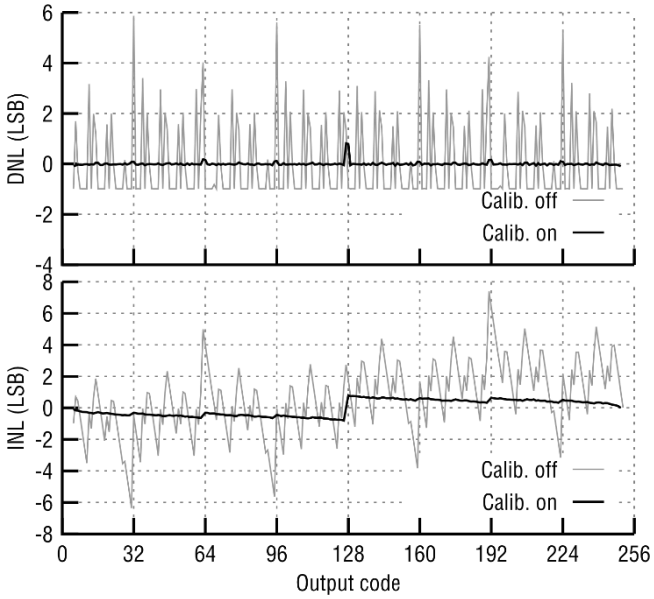


Figure 6-7. Measured DNL and INL with calibration on and off

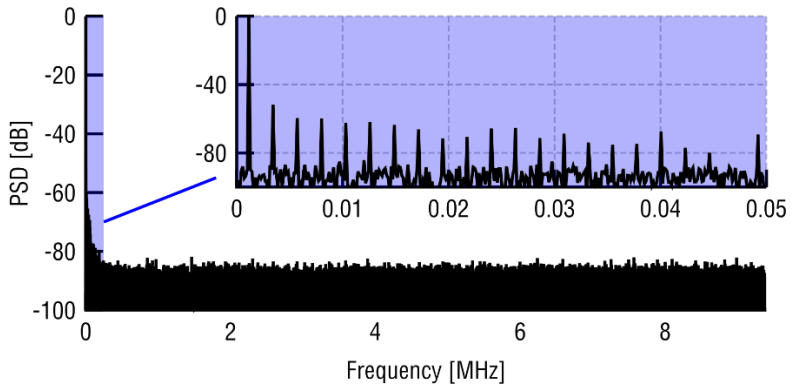


Figure 6-8. FFT plot with 74.99 MHz input frequency at 150MS/s (decimated by 8×)

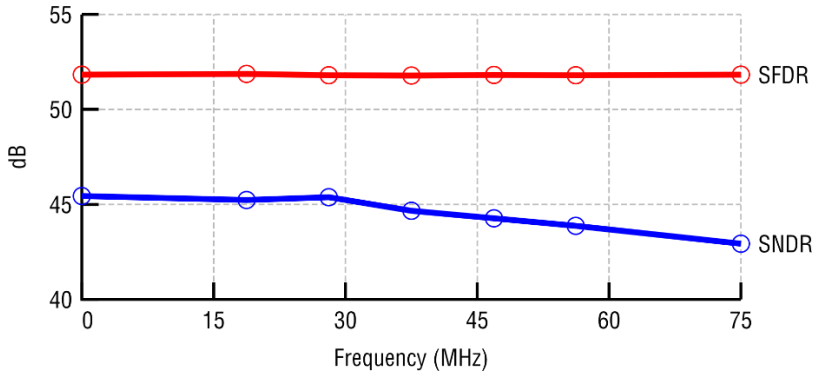


Figure 6-9. Measured dynamic performance versus input frequency at 150 MS/s

Figure 6-7 shows the measured DNL and INL before and after calibration. We can see that before calibration missing code is observed from DNL with -1 LSB in some codes and the INL is -6.35/7.40 LSB. After calibration, DNL and INL are drastically reduced to -0.10/0.80 LSB and -0.80/0.81 LSB, respectively. Large INL/DNL values are observed in major switching codes largely due to random and/or systematic capacitor mismatch. Figure 6-8 shows the FFT plot of the ADC with 74.99 MHz input frequency at 150 MS/s. It is noteworthy that the bins of signal and harmonics are folded back to low frequency bins in the plot due to the decimation by 8×. Fi.g. 6-9 shows the measured SNDR and SFDR versus input frequency up to about 75 MHz at 150 MS/s. The peak SNDR that measured at low input frequencies is 45.4 dB translating to an ENOB of 7.25 bits; The SNDR at Nyquist frequency is 42.9 dB and an ENOB 6.83 bits. The ADC consumes 640 µW power from a 1.2-V supply. The resultant Walden Figure-of-Merit (FoM) is 37.5 fJ/conv-step according

to

$$\text{FoM}=\frac{\text{Power}}{2^{\text{ENOB}} f_S}. \tag{6-2}$$

6.4 Summary

This Chapter presents an offset calibration for LU SAR ADCs, and an 8-bit prototype is fabricated and measured to verify the effectiveness of the calibration technique. The background calibration extensively reduces DNL from -1.0/5.86 LSB to -0.10/0.80 LSB, and INL from -6.35/7.40 LSB to -0.80/0.81 LSB. The ADC achieves an FoM of 37.5~fJ/conv-step at 150 MS/s. The proposed ADC architecture is expected to achieve better speed and power efficiency in a more advanced technology thanks to faster comparators and logic circuits, and reduced parasitics.

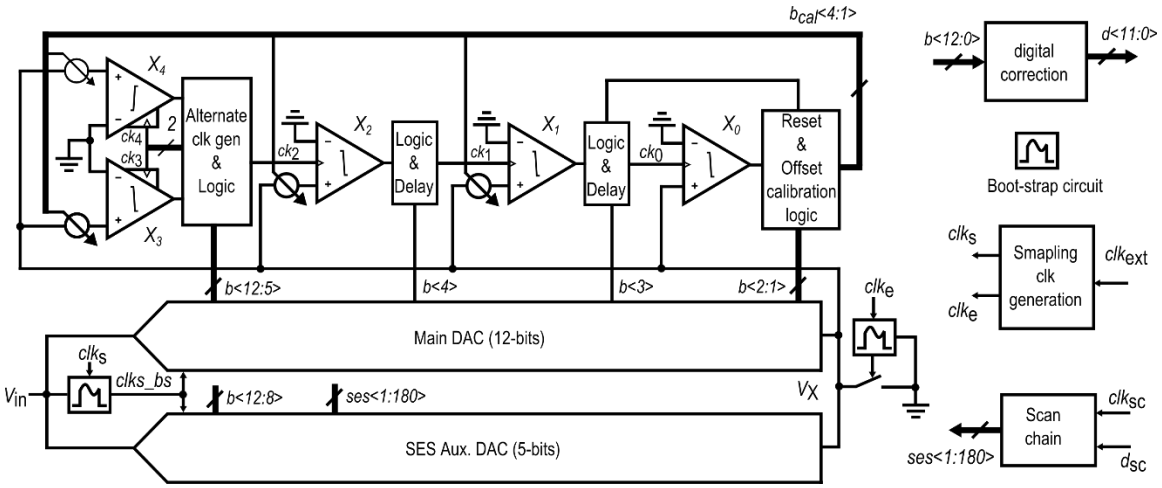
Chapter 7 : 12-BIT 125MS/S ASYNCHRONOUS SAR ADC DESIGN

Based on our noise analysis in Chapter 4, we know that employing noise/power scaling along SAR conversion steps is a direction for optimizing speed and power-efficiency for high-resolution, high-speed SAR ADCs. This noise/power scaling technique can be implemented by using multiple comparators with different noise/power specifications. This chapter presents a power-efficient, 12-bit asynchronous SAR ADC design that uses 5 comparators with different performance in terms of noise and speed, such that the ADC has more degrees of freedom to optimize noise and speed. Also, the ADC has 13 bit raw outputs with 1 bit redundancy to recover the error caused by dynamic non-idealities. In addition, a statistical element selection (SES) technique has been employed to calibrate the capacitor mismatch of capacitive DAC. Implemented in a 1P9M 65nm CMOS technology, a 12-bit prototype fits into an active area of 500 μm × 200 μm. At 125 MS/s, the ADC achieves a signal-to-noise-and-distortion ratio (SNDR) of 64.4 dB and a spurious-free-dynamic-range (SFDR) of 75.1 dB at the Nyquist input frequency while consuming 1.7 mW from a 1.2 V supply. The resultant figure-of-merit (FoM) is 10.3 fJ/conv-step.

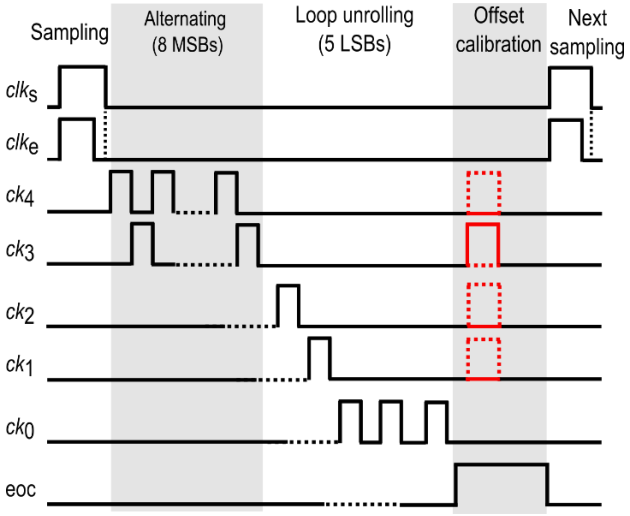
7.1 Proposed asynchronous SAR ADC topology

Figure 7-1 shows the architecture of our proposed 12-bit SAR ADC and its timing diagram. The ADC employs sub-binary radix DAC with redundancy and has 13 raw output bits to recover the dynamic errors occurred in MSB conversions, which largely consists of the dynamic settling errors and thermal noise and offset from the MSB conversions. Unlike in traditional SAR ADCs, where all the bits share a single comparator, this ADC utilizes 5 different comparators. The first 8 MSB bits are resolved by two comparators, X_4 and X_3, that work alternately removing the reset time from the SAR loop. The rest 5 bits are resolved the rest 3 comparators in a loop-unroll manner. However,

the LSB comparator, X_0, is responsible for resolving the last 3 LSBs. All the comparators work asynchronously to maximize conversion speed and simplify the logic control. As stated previously, the comparators are with different noise and power specifications, which are listed in Table 7-1, for implementing high-speed and power-efficient design.



(a)



(b)

Figure 7-1. Propose SAR architecture (a) and its timing diagram (b)

Table 7-1. Specification of comparators

Comparator	$\sigma(V_{n,comp})$ (mV)	Energy (fJ/comp.) (@0.1 mV input)	Delay (ns) (@0.1 mV input)
X_4	0.35	100	0.1
X_3	0.35	100	0.1
X_2	0.2	180	0.2
X_1	0.15	300	0.28
X_0	0.09	800	0.35

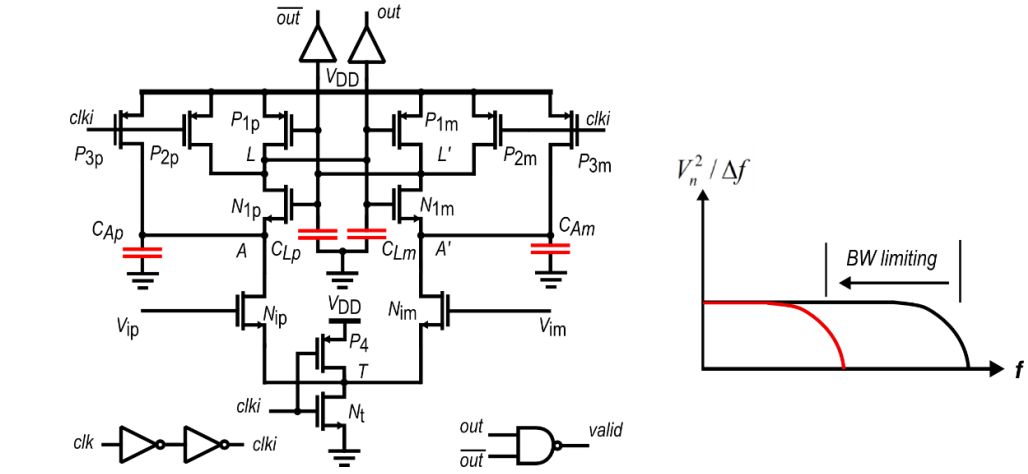
Since more than one comparators are used, the comparator offset mismatch between these comparators arises as a problem in this architecture like in [34], [45]. This is more problematic in high resolution ADCs. So in this ADC, a background calibration technique similar to our calibration technique in [34] is employed with important modifications to improve calibration precision. The LSB comparator, X_0, is chosen as the offset calibration reference, and the rest comparators are all calibrated to have the same offset as X_0. As shown in Figure 7-1 (b), an offset calibration phase, which is marked by the end-of-conversion (*eoc*) signal, is reserved with a budget of 1-bit conversion time. Each comparator is calibrated once every 4 clock cycles, and all the comparators are calibrated in a rotational fashion. The calibration procedure is as follows. First, after the normal SAR conversion, DAC voltage has converged to a value that is close to the offset voltage of the LSB comparator with a difference less than 1 LSB. Then the comparator under calibration is clocked once to compare the same DAC residue voltage, and the output is then compared with the LSB, b_0. Finally, if the two outputs are different, the offset voltage is adjusted in the direction that potentially makes its output to be the same as that of the reference comparator.

In order to further improve the power-efficiency, the total DAC capacitance are sized down to close to thermal noise limit, which is about 820 fF. Our proposed SES calibration technique in Chapter 5 is utilized for calibration of the capacitance mismatch by adding a 5-bit auxiliary DAC, as shown in figure 7-1 (a), to compensate the capacitance mismatch in the first 5 MSB capacitors of the main DAC. Also, 1-bit redundancy has been distributed among the last 8 LSBs to recover the dynamic errors, and, therefore, a digital correction block is necessary to convert the 13-bit raw

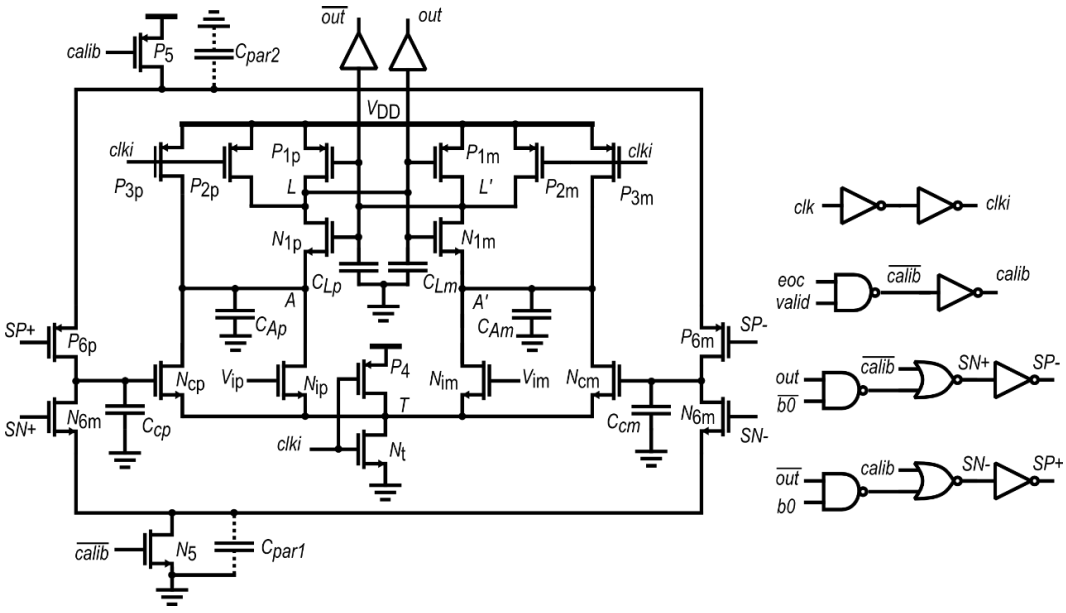
output to its 12-bit binary counterpart. The detailed circuit designs will be given in the following sub-sections.

7.2 Circuit implementation

In this section, the circuit implementation of the 12-bit SAR ADC is presented, including comparators, capacitive DAC and SES calibration, clock generation and logic and controller circuit.



(a)



(b)

Figure 7-2. Comparator schematics (a) LSB comparator and (b) offset self-calibration comparator

7.2.1 Comparator design and calibration

Figure 7-2(a) shows the schematic of the LSB comparator, which resolves the last 3 LSBs and also serves as the offset calibration reference comparator. As we pointed out before, the LSB comparator has the most stringent noise requirement, and, therefore, is most power consuming. The most straightforward method to attenuate the comparator noise is to increase the power budget and proportionally increase the transistor sizes. However, this is not efficient as each 2× increase of transistor sizes can only result in 1.4× increase in input referred noise voltage.

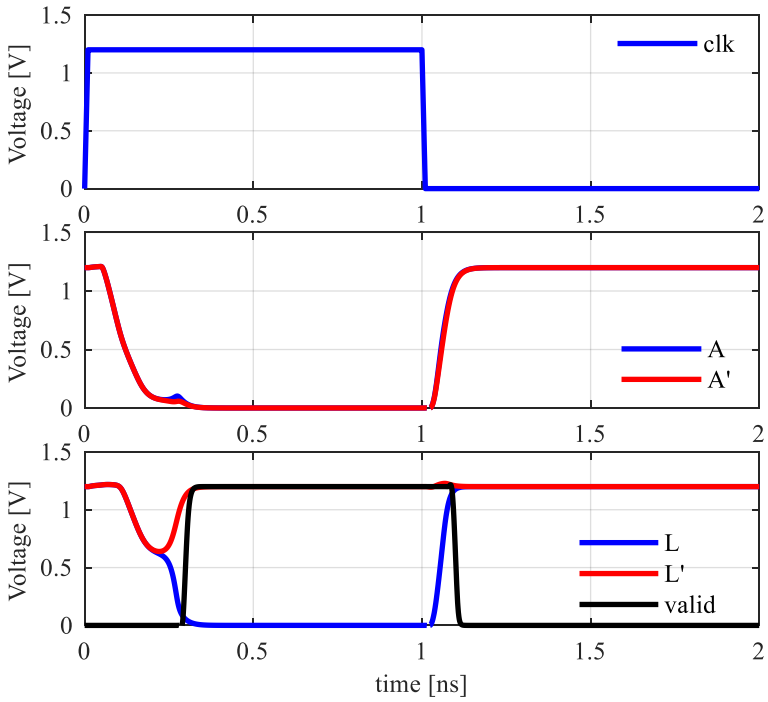


Figure 7-3. Waveforms of a comparator internal nodes

Figure 7-3 shows the waveform of the internal nodes of a comparator. In [47], the authors divide the comparator operation into four phases: resetting, sampling, regeneration and decision phases. In resetting phase, the latch and all the principle internal nodes are reset to *VDD*. When it comes to sampling phase, the *clk* signal turns off all the resetting transistors and turns on the tail transistor to activate the comparison. The internal nodes, *A* and *A'*, are then discharged with different speeds depending on the input voltage difference until one of the NMOS latch transistors is turned on. This

process can be viewed as an integration, of which the length depends on the capacitance seen at this node. After one of NMOS latch transistors, *N1p* and *N1m*, is turned on, the comparator enters regeneration phase, where the positive feedback of the latch starting from a small voltage difference established in sampling phase. Lastly, the comparator is in decision phase after the latch output voltage exceeds certain amount and cannot be reversed.

The noise impairment of the comparator matters mostly in sampling phase and regeneration phase. In sampling phase, the noise impact can be suppressed by using larger sizes for the input transistors. However, this gives large parasitical capacitance to the DAC. One the other hand, with a given input transistor size, the noise impact can be improved by increasing the time of integration process, which can be done by adding explicit capacitance to nodes *A* and *A'*, as it helps average out the noise voltage on nodes *A* and *A'*. From the frequency perspective, by adding the capacitors the bandwidth of the internal nodes decreases, so the integrated of the noise power decreases accordingly. Similarly, the same strategy can be used to the latch output nodes to suppress the noise impact in regeneration phase. Figure 7-4 shows the simulated curves of noise, energy and delay of a comparator with different bandwidth limiting capacitance values. Similar to our comparator in

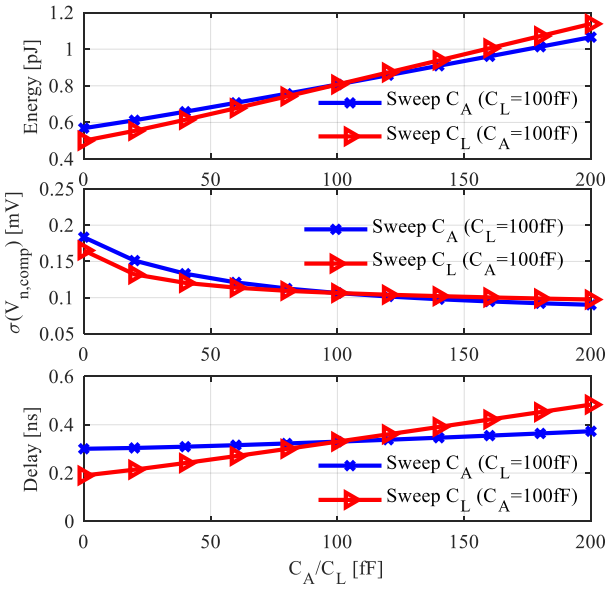


Figure 7-4. Simulated noise, energy and delay of a comparator with bandwidth limiting capacitors

For all the other comparators, X_1-X_4, they use the same architecture as shown Figure 7-2 (b). Other than different noise/speed specifications, listed in Table 7-1, another important difference compared to LSB comparator is that they must be adjustable in their offsets voltage. The core part of the comparator is still a strong-arm comparator. In order to calibrated the offset voltage, similar to our comparator in [45], another pair of transistors are added in parallel with the input transistor, and this auxiliary differential transistors are biased by voltages store on two calibration capacitors, C_{cp} and C_{cm}. If the bias voltages are set properly, its overall offset voltage can be adjusted to be the same as the LSB comparators. The voltage adjustment is carried out by two dedicated charge pumps composed by transistors including *N5*, *N6*, *P5* and *P6* and capacitors C_{par1} and C_{par2}. The calibration works as follows. First, during the normal SAR conversion, C_{par1} and C_{par2} are pre-charged to *GND* and *VDD*, respectively, and all the switches, *N5*, *N6*, *P5* and *P6* are turned off; After the LSB bit, b_0, is resolved by comparator X_0, the comparator under calibration compares the same residue voltage on the DAC. The result, b_{cal}, is then compared with *b0* to determine if the bias voltages on C_{cp} and C_{cm} need to be updated. If the outputs are the same, we assume that the offset of the comparator under calibration is reasonably close to that of X_0, and, therefore, the charge pump operations are skipped. On the other hand, if the outputs are different, the charge pump will drive the bias voltage in a differential manner such that the offset of the comparator under calibration approaches that of the reference comparator, X_0. For example, if b_{cal}=1 and b_0 =0, it means the comparator offset should decrease, and, therefore, *SN*+ and *SP*- will be on to subtract some charge from C_{cp} by C_{par1} and add some charge to C_{cm} from C_{par2}; To the contrary, if b_{cal}=0 and b_0 =1, which means the comparator offset should increase, then all the operations should be done in the opposite way.

The testbench setup for characterizing the comparator calibration is shown in Figure 7-5. The calibration process is controlled by a Verilog-A block, which generates the input waveform for the comparator under calibration, X_{cal}, for measuring the offset voltage using binary search, and generates a small random input for X_{cal} and X_0, to identify the offset difference between them.

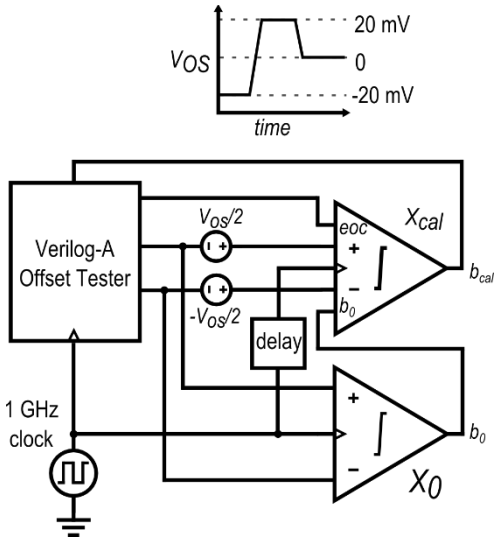


Figure 7-5. Simulation setup for characterizing comparator offset calibration

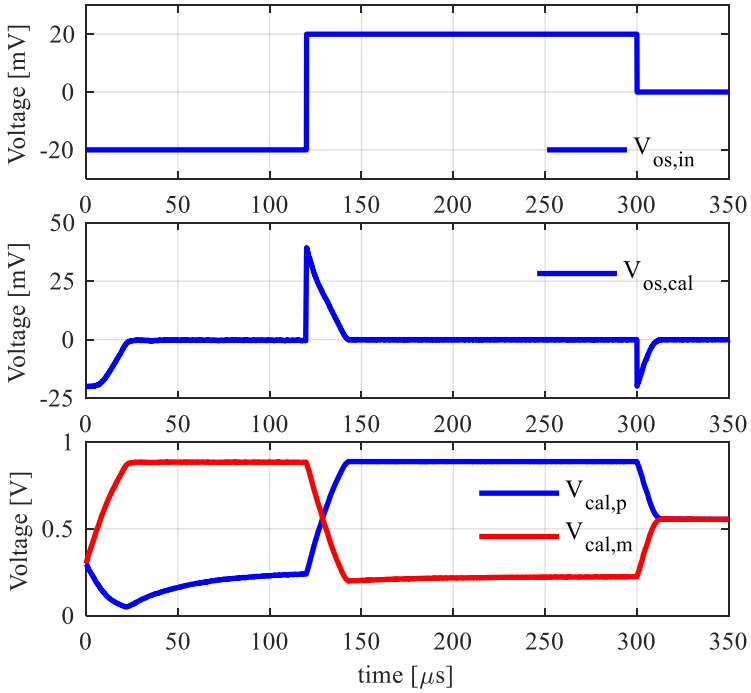


Figure 7-6. Calibration range and step-size simulation, and waveform of calibration process for comparator X_3

Table 7-2. Calibration parameters of comparators

Comparator	$\sigma(V_{os,comp})$ (mV) (before calibration)	Calibration range	Calibration step-size
X_4	10	>40 mV	< 40 μV/step
X_3	10	>40 mV	< 40 μV/step
X_2	6.8	>30 mV	<20 μV/step
X_1	3.2	> 20 mV	< 20 μV/step
X_0	2.2	-	-

Figure 7-6 shows the simulated waveforms of calibration of the second LSB comparator, X_3. The comparator under calibration is assigned an offset of -20 mV, on can see that the calibration responds by establishing a differential voltage on the auxiliary differential pair, and eventually reduces the voltage to close to zero. The offset voltage of X_3 is then changed to 20 mV at 120 μs, one can see that calibration responds to this change accordingly and brings the overall offset voltage back to zero again. It should be noted that the calibration range is determined by the transistor size ratio of N_c to N_i; and the step-size of the calibration by capacitance ratio C_{par}/C_{cal}. In order to minimize the calibration noise in steady state, the charge pump capacitor, C_{par}, is implemented by parasitics, and the calibration capacitor, C_{cal}, by NMOS capacitor (2.5V varactor) due to its high capacitance density. The simulated calibration parameters are listed in Table 7-2, where the values of calibration range are chosen to cover the $3(\sigma(V_{os,Xcal})+ \sigma(V_{os,X0}))$.

7.2.2 Capacitive DAC design and SES calibration

The capacitive DAC of the SAR ADC is shown in Figure 7-7, which consists of a 12-bit main DAC and a 5-bit auxiliary DAC for calibrating the first 5 MSB capacitor mismatches of the main DAC. The DAC is sub-binary with redundancy to accommodate the incomplete settling and comparator noise and offset mismatch. The incomplete settling basically is most severe in MSB, while the comparator noise and mismatch are more of importance for LSB bits according to our analyses in Chapter 4 and Chapter 5. The DAC capacitance values are listed in Table 7-3 with the resultant redundancy calculated redundancy according to (4-15). The total DAC capacitance is

about 820 fF which is close to the thrmal noise limit for a 12-bit ADC, The first 5 MSB capacitors are binarily scaled for calibration convenience.

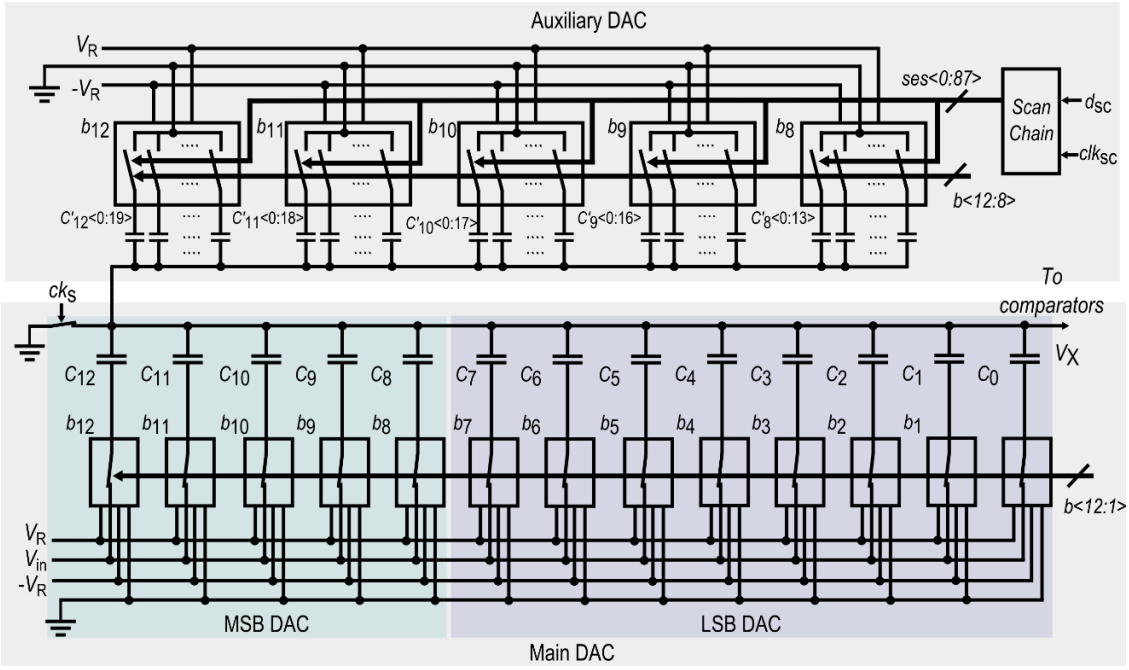


Figure 7-7. Capacitive DAC with SES calibration

Table 7-3 DAC parameters and redundancy (C_u = 0.4fF, V_R = 1.2V)

	Capacitance (C_k+C'_k) (C_u)	Weight(W_k)	Redundancy (R_k) (mV)
C_{12}	992+32	1024	±7.6
C_{11}	496+16	512	±7.6
C_{10}	244+12	256	±7.6
C_9	120+8	128	±7.6
C_8	58+6	64	±7.6
C_7	36	36	±2.9
C_6	18	18	±2.9
C_5	10	10	±1.7
C_4	6	6	±0.6
C_3	3	3	±0.6
C_2	2	2	0
C_1	1	1	0
C_0	1	0.5	0

7.2.3 Clock generation

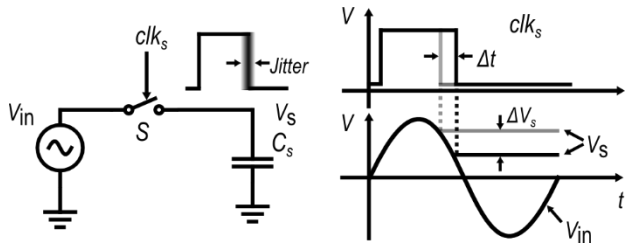


Figure 7-8. Clock jitter impairment in sample-and-hold circuit

Sampling clock jitter is very critical for high-speed and high-resolution ADCs. As shown in Figure 7-8, the random uncertainty of the sampling edge of the clock signal results in random deviation of the sampled signal from its ideal value with a dynamic input signal. Consider a sinusoid input signal *Asin(ωt),* where *A* is the signal amplitude, and *ω* the angular frequency. Then for the *n*-th sample, the voltage error caused by a sampling edge difference, Δ*t*, can be calculated by

$$\begin{aligned}\Delta V_S\left(nT_S\right) &= A\left(\sin\left(\omega\left(nT_S+\Delta t\left(n\right)\right)\right)-\sin\left(\omega nT_S\right)\right)\\ &\approx A\omega\Delta t\left(n\right)\cos\left(n\omega T_S\right)\end{aligned}, \tag{7-1}$$

where T_S is the clock period. Assuming σ_j^2 denotes the variance of the sampling edge timing error, then the resultant noise power in the sampled signal is calculated by

$$\sigma_{err}^2 = \frac{\left(A\omega\sigma_j\right)^2}{2}. \tag{7-2}$$

Finally, since the input signal power is $A^2/2$, the SNR limit considering sampling clock jitter can be calculated by

$$SNR = -20\log_{10}\left(2\pi f\sigma_j\right). \tag{7-3}$$

It can be seen that the SNR degradation depends on the frequency of the *input signal* and the jitter of the clock, regardless the signal amplitude or the clock frequency. Figure 7-9 presents the calculated SNR boundary due to clock jitter.

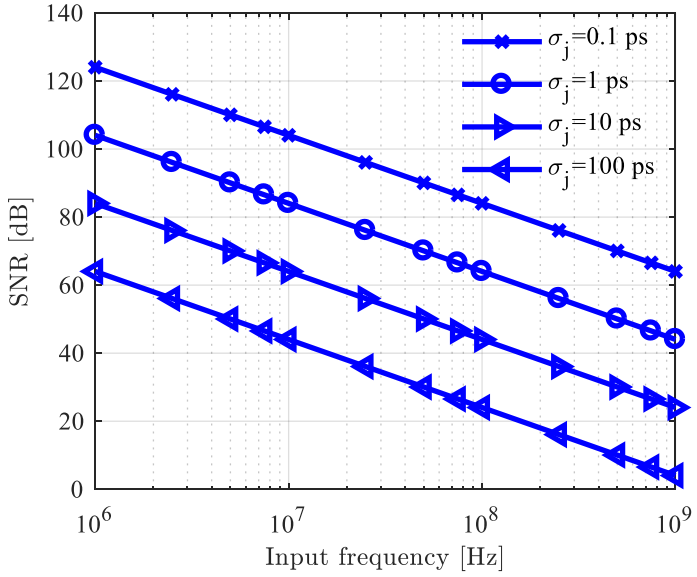


Figure 7-9. SNR boundary due to clock jitter versus input frequency

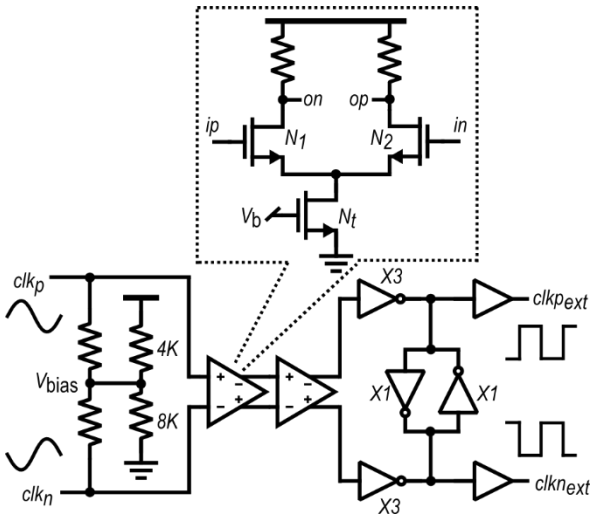


Figure 7-10. Clock recovery circuit

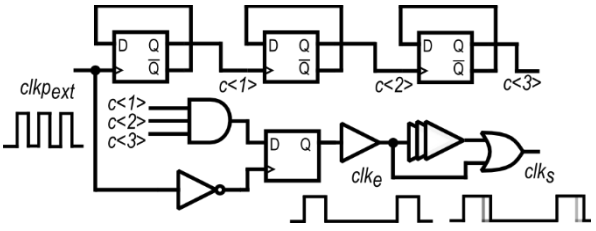


Figure 7-11. SAR clock generation circuit

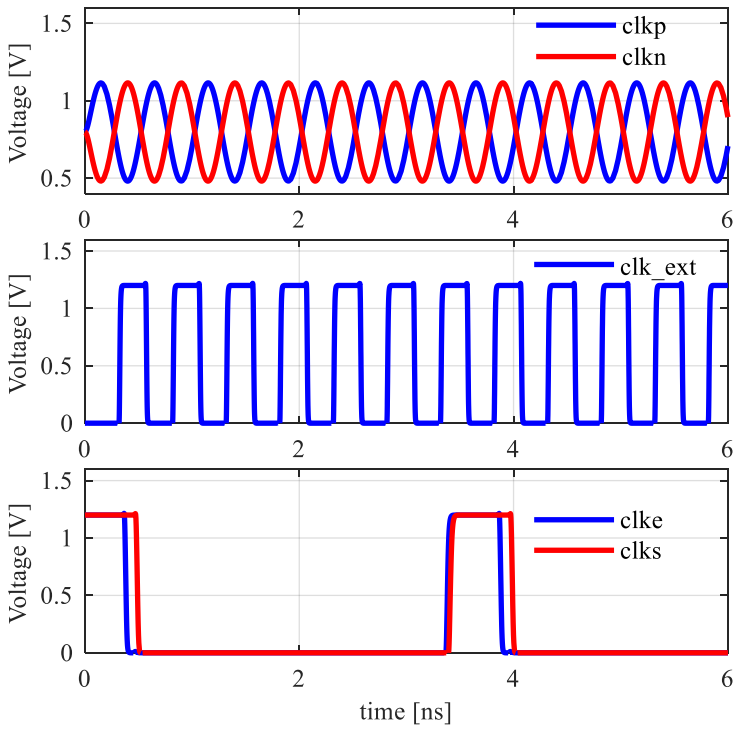


Figure 7-12. Clock generation waveform

For SAR ADCs, the clock signal generally has a duty cycle much less than 50%, because the quantization phase takes larger portion of the clock period than the sampling phase due to its multi-step quantization manner. This demands a system clock whose frequency is much higher than the SAR sampling clock. For instance, if a 250-MHz SAR clock with 12.5% duty cycle is needed, a 2-GHz system clock should be available to generate the SAR clock. Figure 7-10 shows the clock recovery circuit of this ADC, which converts a differential input sinusoid signal to an on chip logic clock. The input signal is firstly amplified by two cascaded amplifiers before being converted to logic levels by a cross-coupled latch. Figure 7-11 presents the SAR clock generation circuit, where a 3-bit counter is utilized to facilitate the 12.5% duty cycle for *clke*. The delayed sampling clock, *clks*, is then generated by a delay-line and an *OR* gate. It should be noted that the jitter-critical clock is *clke*, so we should try to keep its generation path as short as possible. Figure 12 shows the simulated waveform of clock recovery and generation circuit. The simulated jitter (phase noise) performance of the sampling edge of *clke* is presented in Figure 13. It reveals that the integrated

jitter is about 100 fs, which is translates to a > 80 dB SNR for a 100-MHz input signal according to the calculations shown in Figure 7-9 assuming that the jitter contributed by the signal source is negligible.

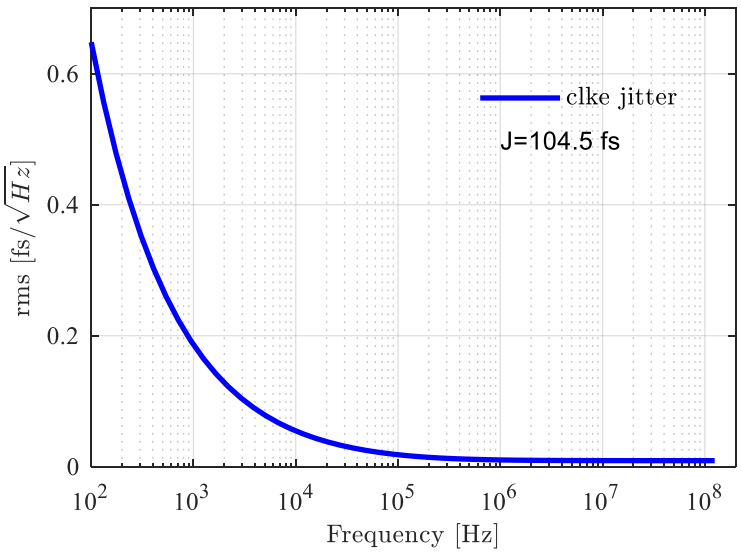


Figure 7-13. Simulated jitter of sampling clock falling edge

7.2.4 Logic and control circuits

A. Alternate comparator controller

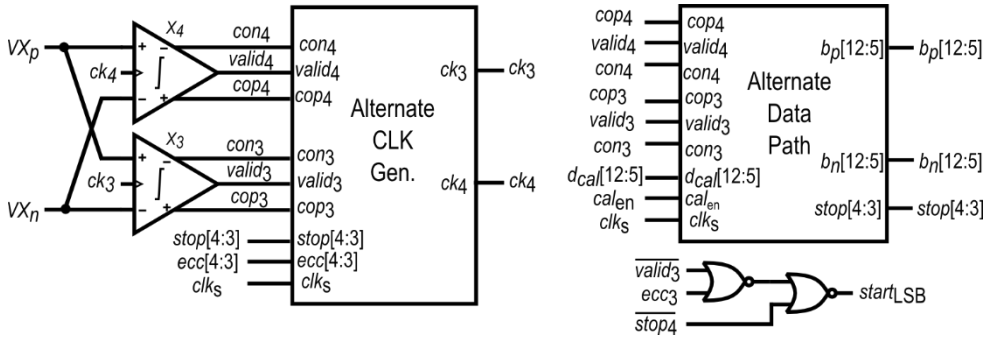


Figure 7-14. Logic diagram of the alternate comparators

Figure 7-14 shows the logic diagram of the alternate comparators, which are responsible for resolving the first 8 bits of the ADC. The block consists of two parts, clock generation and data saving part. The asynchronous clock generation, by using the completion signals of comparators,

valid4 and *valid3*, greatly simplifies the logic complexity and maximize the speed. Figure 7-15 and Figure 7-16 show the clock generation circuit and the waveform, respectively. After the sampling of the ADC, the falling edge of the sampling signal triggers comparator, X_4, to start the quantization, and the valid signal of X_4 then triggers X_3. After X_3 finishes the second bit comparison, the completion signal, $valid_3$, will in turn trigger X_4 to resolve the next bit. After all the first 8 bits are resolved, which is marked by stop4 and stop3, the alternate comparators stops working and trigger the LSB comparators by giving an rising edge to *startLSB*.

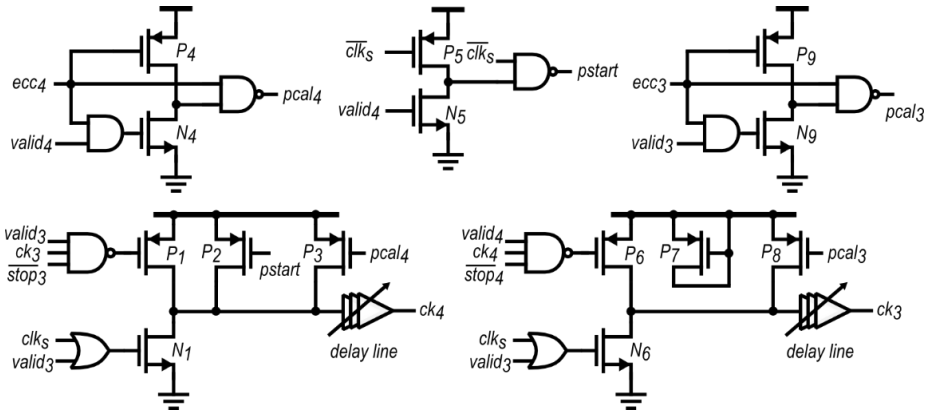


Figure 7-15. Alternate clock generation circuit for MSB comparators X_3 and X_4

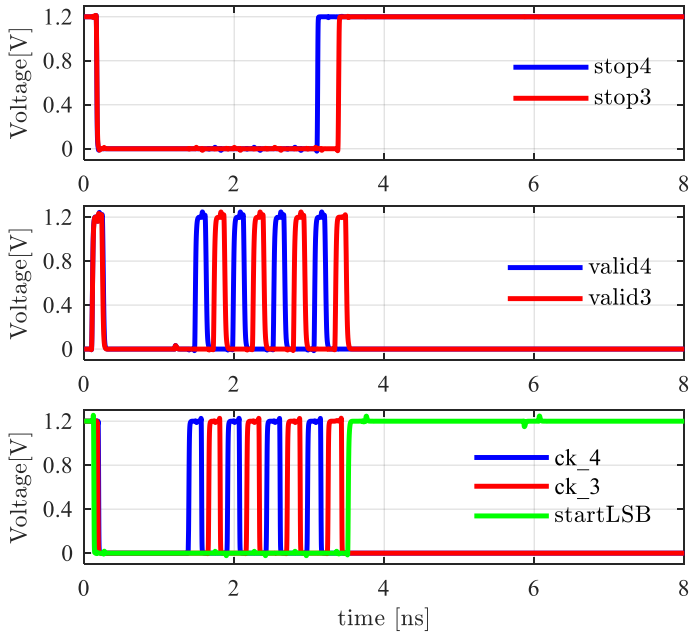


Figure 7-16. Waveform of alternate clock generation

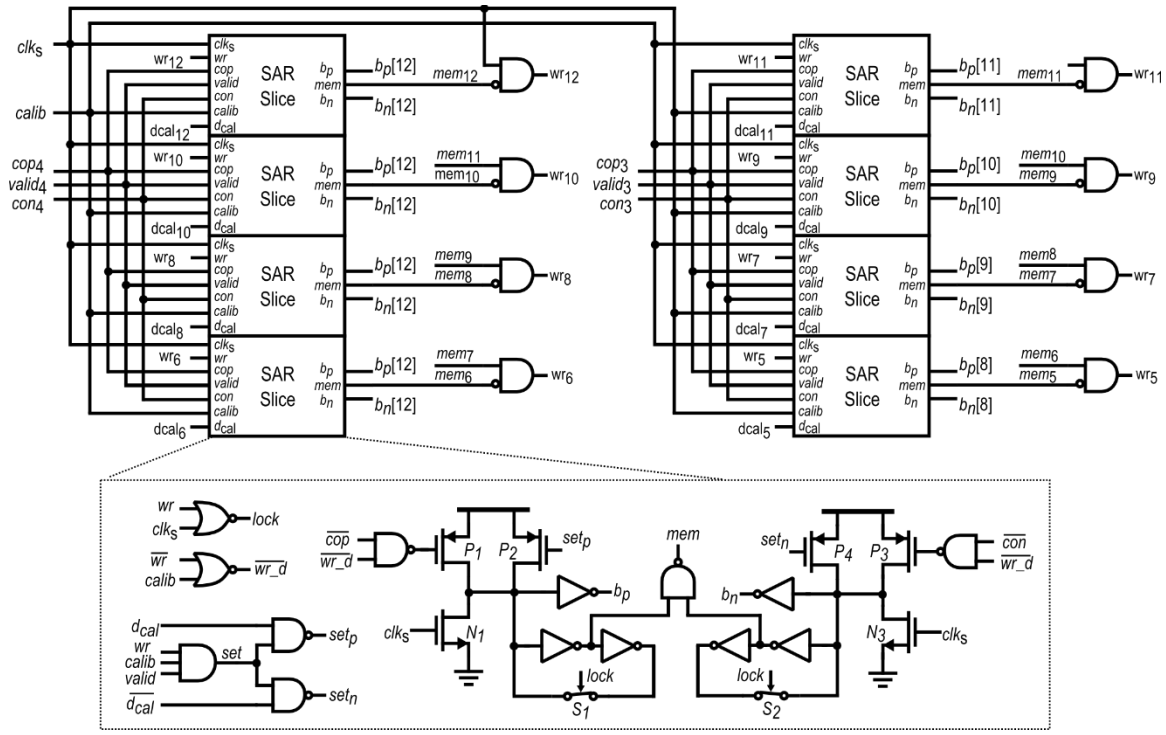


Figure 7-17. Data path for alternate comparators X_3 and X_4

Figure 7-17 shows the diagram for the alternate comparators. It consists of 8 identical SAR slices. The SAR slices is to store the output of the comparator after the comparison result is available, and control the DAC switching and free the comparator for next comparison.

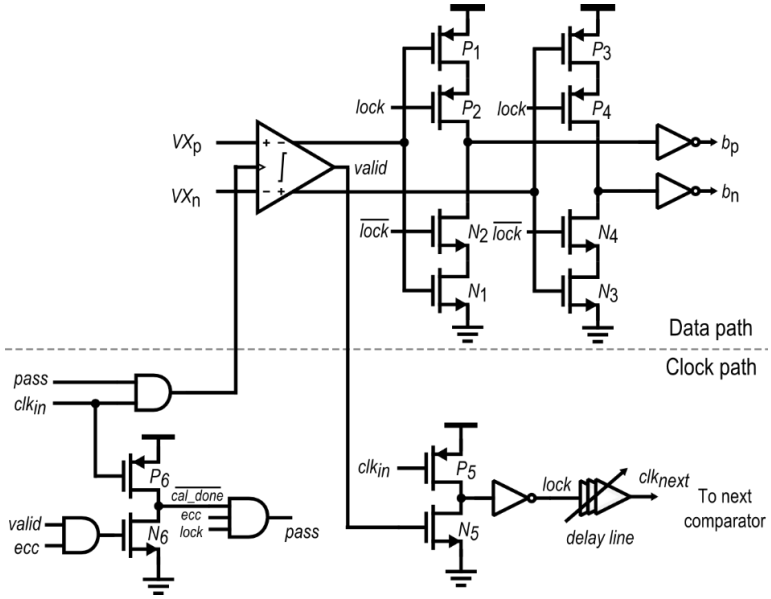


Figure 7-18. Data and clock logic for LU comparators X_1 and X_2

B. Loop-unrolled comparator controller

Figure 7-18 shows the schematic for the LU comparators, X_2 and X_1, which is similar to our design in [45]. By using dynamic circuit in the data path, the delay of the comparator to DAC switching is minimized. The delay line in the clock path is digitally programmable to guaranttee enough time for DAC settling.

C. LSB comparator controller

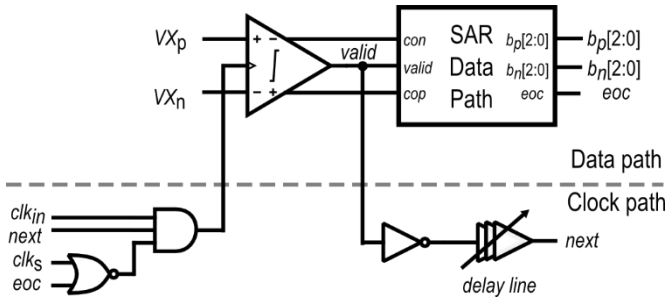


Figure 7-19. Data and clock logic for LSB comparator X_0

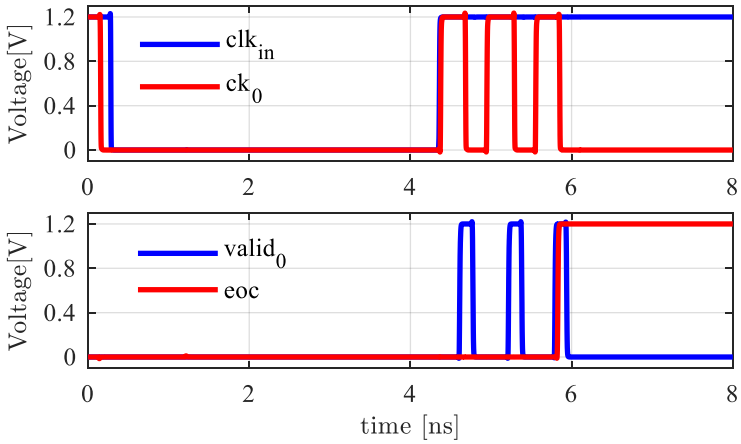


Figure 7-20. Clock generation waveform for the LSB comparator

Figure 7-19 and Figure 7-20 show the schematic and waveform for the LSB clock generation. After the completion of all the previous bits, marked by the rising edge of clk_{in}. The LSB comparator is triggered to resolve the last 3 LSBs. At the end of the LSB conversion, end of conversion, *eoc*, marks the availability of the ADC results for current sample.

7.3 Measurement results

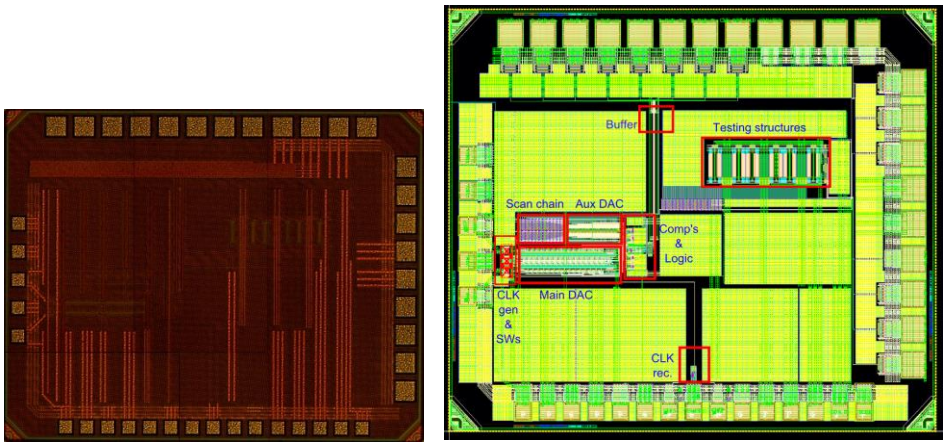


Figure 7-21. Chip photograph and layout

The prototype 12-bit ADC proposed has been fabricated in 65-nm technology. Figure 7-23 shows the die photograph and ADC core active circuit layout, which occupies an area of 0.1 mm^2. The total sampling capacitance is about 830 fF in each side of the differential DAC. The differential input range of the ADC is 2.4 V_{pp} with a 1.2-V supply voltage. In order to adapt to the input-output (IO) circuits speed, the ADC outputs are down-sampled by 4× by an internal decimating circuit for testing purpose.

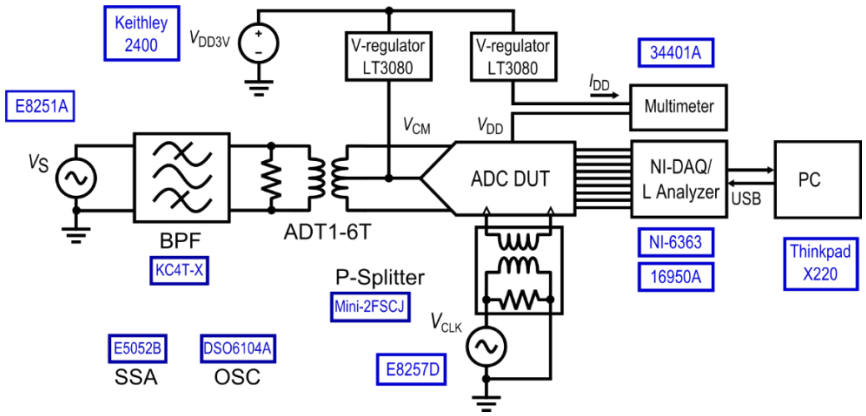


Figure 7-22. Measurement setup of the SAR ADC

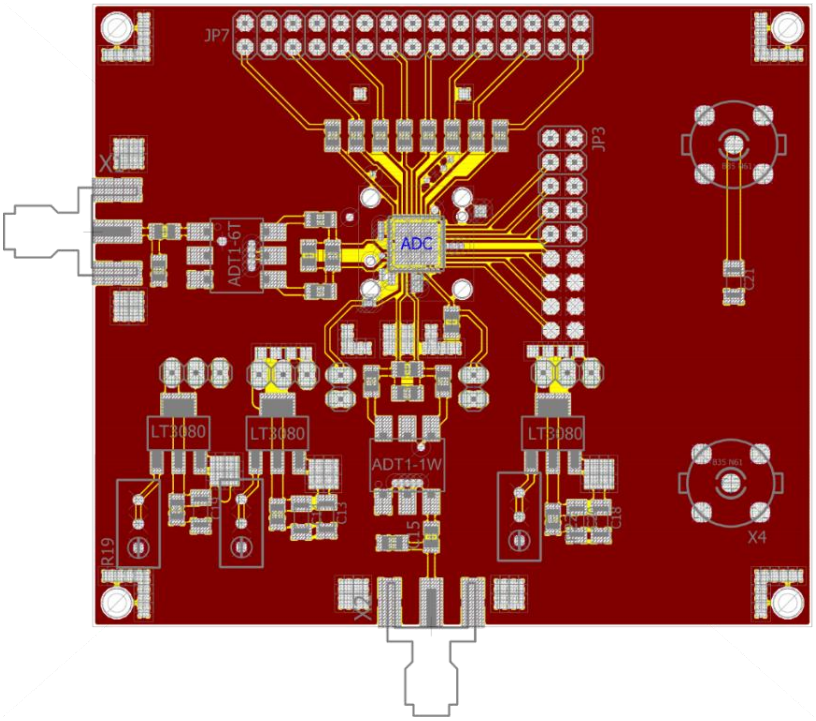


Figure 7-23. PCB design of 12-bit ADC evaluation board

Table 7-4. Summary of measured performance

Technology	65nm CMOS
Resolution	12 bits
Input capacitance	830 fF
Supply voltage	1.2 V
Sampling rate	125 MS/s
Input range	2.4 V_{pp}
DNL (LSB)	-0.7/1.1
INL(LSB)	-1.5/0.75
Nqst. SFDR	75.1 dB
Peak SFDR	80.7 dB
Nqst. SNDR	64.4 dB
Peak SNDR	65.8 dB
Power	1.5 mW
FoM	10.3 fJ/conv-step
Active area	0.1 mm^2

The measurement setup of the 12-bit SAR ADC is shown in Figure 7-22. The differential input signal is obtain on PCB, as shown in Figure 7-23, by using a transformer. The differential clock is generated in a similar way. In order to lower the supply noise impact, all the ADC supply is generated by low noise regulators on the PCB. The measured results are summarized in Table 7-4.

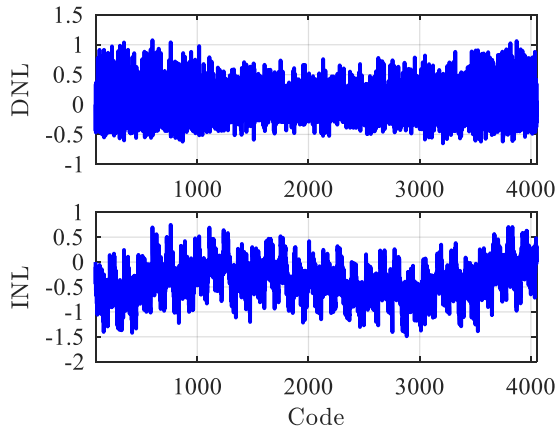


Figure 7-24. Measured INL and DNL

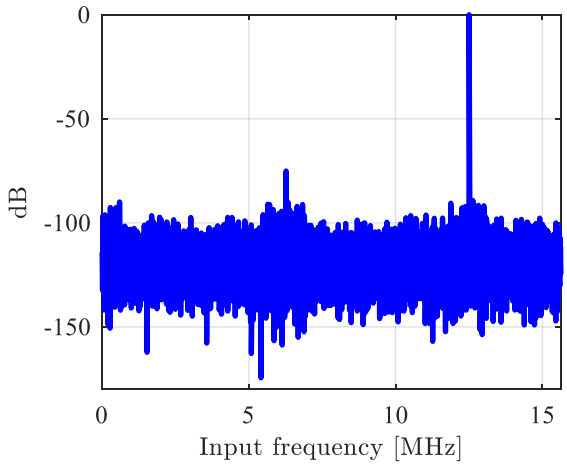


Figure 7-25. FFT plot of with ~75MHz input frequency (down-sampled by 4×)

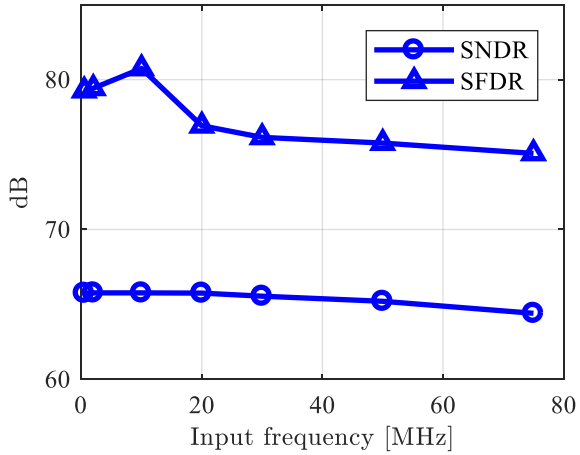


Figure 7-26. Measured dynamic performances versus input frequency

Figure 7-24 shows the measured INL/DNL plots extracted with 500 KHz input frequency. It shows that the ADC achieves a DNL of -0.7/1.1 LSBs and an INL -1.5/0.75 LSBs. Figure 7-24 shows the FFT plot of the ADC with ~75 MHz input frequency at 125 MS/s. It is noteworthy that the bins of signal and harmonics are folded back to low frequency bins in the plot due to the decimation by 8×. Figure 7-26 shows the measured SNDR and SFDR versus input frequency up to about 75 MHz at 125 MS/s. The peak SNDR that measured at low input frequencies is 65.8 dB translating to an ENOB of 10.63 bits; The SNDR at Nyquist frequency is 64.4 dB and an ENOB of 10.4 bits. The ADC consumes 1.7 mW power from a 1.2-V supply. The resultant Walden Figure-of-Merit (FoM) is 10.3 fJ/conv-step according to

$$\text{FoM}=\frac{\text{Power}}{2^{\text{ENOB}} f_S}. \tag{7-1}$$

7.4 Summary

This Chapter presents an asynchronous multi-comparator SAR ADC architecture with power and speed optimization, and a 12-bit prototype is fabricated and measured to verify the effectiveness of our proposed design techniques. Implemented in a 1P9M 65nm CMOS technology, a 12-bit prototype fits into an active area of 500 μm × 200 μm. At 125 MS/s, the ADC achieves a signal-to-noise-and-distortion ratio (SNDR) of 64.4 dB and a spurious-free-dynamic-range (SFDR) of 75.1 dB at the Nyquist input frequency while consuming 1.7 mW from a 1.2 V supply. The resultant figure-of-merit (FoM) is 10.3 fJ/conv-step.

Chapter 8 : CONCLUSION AND FUTURE WORK

8.1 Final remarks

In order to improve the LU-SAR ADC resolution and power efficiency, this work investigates the impact of the offset mismatch of comparator on the ADC linearity. Quantitative analyses and conclusions have been drawn to provide guidance for design of SAR ADC of this kind. Moreover, statistical model have been proposed to establish a relationship between comparator offset standard deviation, expected effective resolution, and yield. This model can be used for calculating one of these three parameters with the others available in the design phase, i.e. predicting the yield of a design with a given mismatch specification of comparator and a given resolution target. In order to address the comparator offset issue, a LU-SAR ADC topology has been proposed and an 8-bit ADC prototype was fabricated in a 130nm CMOS technology and measured to showcase the effectiveness of the calibration algorithm.

If we further increase the resolution target of the ADC, comparator noise plays a vital role in the performance of the ADC. That is because a large resolution target demands tremendous power consumption to increase the SNR and tends to limit the speed of the ADC. In order to break the trade-offs in speed, power and noise, a multi-comparator, asynchronous SAR ADC architecture is proposed. The comparators have different noise and speed specifications according to their importance in determining the noise performance of the ADC, such that more degrees of freedoms are available to optimize the overall performance of the high-resolution ADC. Also, in order to address the capacitor mismatch issue in high resolution ADC, a statistical calibration technique with enlarged calibration range and very fine tuning step is proposed, which allows the total capacitance to be downsized to close to noise limit. A 12-bit prototype of this ADC architecture was fabricated in a 65nm CMOS technology and measured to demonstrate the effectiveness of this optimization methodology and the capacitor calibration for high-speed and high-resolution ADCs.

8.2 Future work

As the speed and efficiency of ADC becomes more demanding, there are several future directions can be carried out based on the work presented in this thesis.

A. High-speed applications ADCs can be implemented by time-interleaving (TI) both ADC architectures. The LU-SAR ADC architecture proposed in Chapter 4 is inherently convenient for timing-interleaving, because the channel ADC are all with zero offset after calibration. Therefore, there is no need to calibrate the offset mismatch among channels. For high resolution SAR ADCs, TI appears to be a reasonable architecture because the speed is intrinsically limited by the multi-step conversion fashion of the SAR architecture. The proposed SES-based calibration algorithm can be extended for timing skew calibration in TI ADCs thanks to its enlarged calibration range and fine tuning step.

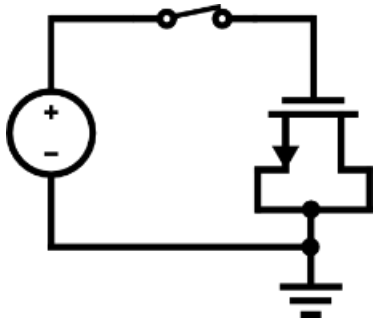


Figure 8-1. Characterization of NMOS for CS SAR ADC

B. The proposed techniques including LU-SAR with offset calibration, noise optimization strategy, and capacitor mismatch calibration can be applied for another power-efficient type of SAR ADCs – charge sharing (CS) SAR ADCs. Particularly, the authors in [13] proposed to use MOS transistor as capacitor in the capacitive DAC, which makes the ADC very efficient in both power and area. However, the capacitor mismatch is also an important problem preventing it from migrating to high resolutions. As shown in Figure 8-1 and (8-1), the dimensional mismatch and/or threshold mismatch can lead to charge mismatch between unit capacitors. Given the fact that the threshold mismatch is random

and the dominant factor, shown in Figure 8-2 and Figure 8-3, we can use our SES algorithm to calibrate the capacitor mismatch in CS SAR ADCs with very cheap overheads.

$$Q_{gg} \approx Q_{ch} = C_{ox} WL(V_{GS} - V_{TH}) \tag{8-1}$$

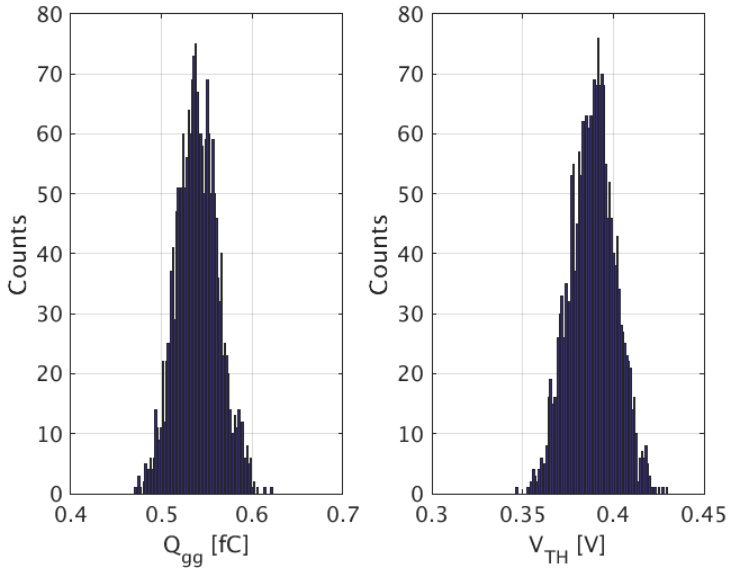


Figure 8-2. MC simulated a transistor gate charge and threshold voltage distribution highly correlated

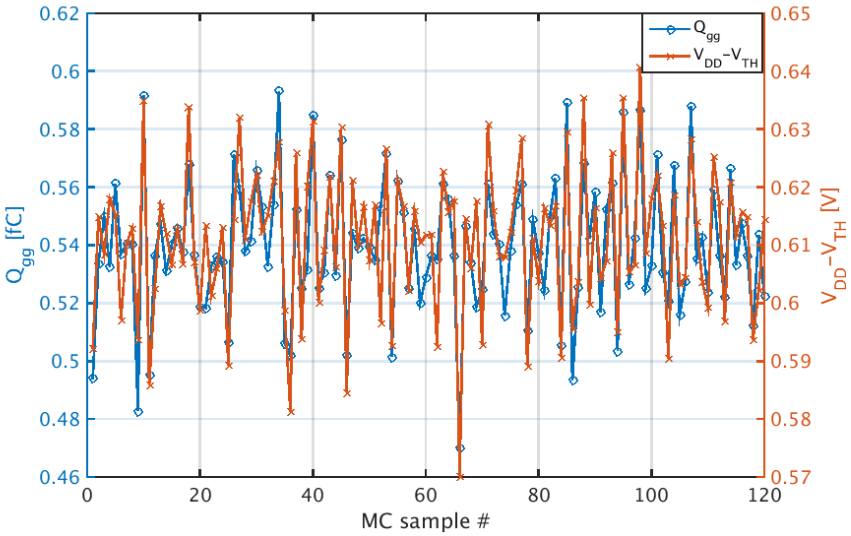


Figure 8-3. MC simulation samples of a transistor gate charge and its threshold voltage high correlated

C. The existing foreground SES-based calibration techniques have been criticized for its

lacking capability of tracking temperature variations despite its very fine tuning precision. In order to address this issue, neat and efficient on-chip temperature sensors, like [50], [51], can be integrated as part of our calibration circuit. With the availability of the chip temperature, extensive calibrations can be carried out to learn the calibrated performance of the circuits and store the best calibration codes for different temperature intervals.

APPENDIX A

This appendix is to derive the relationship between the static characteristics and the resulting quantization noise of an ADC. The quantization noise of an ideal ADC is defined as in (A-1).

$$V_{\text{noise}}^2 = \frac{1}{\left(2^B - 1\right)V_{\text{LSB}}} \sum_{j=1}^{2^B-1} \int_{-V_{\text{LSB}}/2}^{V_{\text{LSB}}/2} u^2 \mathrm{d}u = \frac{V_{\text{LSB}}^2}{12}. \tag{A-1}$$

The quantization noise of a non-ideal ADC can be described as a function of the INL by changing the integration limits, as (A-2)

$$V_{\text{noise}}^2 = \frac{1}{\left(2^B - 1\right)V_{\text{LSB}}} \sum_{j=1}^{2^B-1} \int_{\phi[j]-\frac{1}{2})V_{\text{LSB}}}^{(\phi[j+1]+\frac{1}{2})V_{\text{LSB}}} u^2 \mathrm{d}u. \tag{A-2}$$

Solving (A-1) yields (A-2),

$$V_{\text{noise}}^2 = \frac{1}{\left(2^B - 1\right)V_{\text{LSB}}} \sum_{j=1}^{2^B-1} \frac{u^3}{3} \Big|_{(\phi[j]-\frac{1}{2})V_{\text{LSB}}}^{(\phi[j+1]+\frac{1}{2})V_{\text{LSB}}}. \tag{A-3}$$

Finally, expanding (A-3) leads to

$$\begin{aligned} V_{\text{noise}}^2 = \frac{1}{\left(2^B - 1\right)} \frac{V_{\text{LSB}}^2}{12} \sum_{j=1}^{2^B-1} & (-4\phi[j]^3 + 4\phi[j+1]^3 + 6\phi[j]^2 \\ & + 6\phi[j+1]^2 - 3\phi[j] + 3\phi[j+1] + 1) \end{aligned} \tag{A-4}$$

Note that most of the terms are canceled when we compute the summation, because they appear twice with opposite signs. Also, the INL of the first and the last code transitions $\phi[1]$ and $\phi[2^{\mathrm{B}} - 1]$), by definition, are zero. Therefore, (A-4) can be simplified as

$$V_{\text{noise}}^2 = \frac{1}{\left(2^B - 1\right)} \sum_{j=1}^{2^B-1} \left[\frac{V_{\text{LSB}}^2}{12} + V_{\text{LSB}}^2 \phi[j]^2 \right]. \tag{A-5}$$

Finally, solving the summation leads to

$$V_{\text{noise}}^2 = \frac{V_{\text{LSB}}^2}{12} + \frac{V_{\text{LSB}}^2}{2^B - 1} \sum_{j=1}^{2^B-1} \phi[j]^2. \tag{A-6}$$

Defining $\overline{\phi^2}$ as the mean value of ϕ^2, (A-6) can be rewritten as a more intuitive form as

$$V_{\text{noise}}^2 = V_{\text{LSB}}^2\left(\frac{1}{12}+\overline{\phi^2}\right). \tag{A-7}$$

We can relate V_{noise} and ENOB assuming a full-range input signal as (A-7) [30].

$$V_{\text{noise}}^2 = \frac{V_{\text{LSB}}^2}{12}\left(\frac{2^B}{2^\Psi}\right)^2. \tag{A-8}$$

Combining (A-7) and (A-8), the ENOB can be represented by

$$\Psi = B - \log_4\left(1+12\overline{\phi^2}\right). \tag{A-9}$$

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