Self-healing Narrowband MEMS Filter Design for RF Receivers

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Abstract

As the radio frequency (RF) spectrum is becoming increasingly occupied, receivers are designed to resist out-of-band interferers. Due to lack of on-chip high quality factor (high-Q) filters, conventional receivers pursue frequency translation using mixers and VCOs, which inevitably increases power consumption and area and degrades noise and linearity. The piezoelectric AlN contour mode resonator filter, with its high-Q, low insertion loss and compatibiliy with CMOS integration, has emerged as a viable option for a high performance channel selection filter as the first stage of a direct sampling receiver. However, maintaining frequency precision for any high Q filter is challenging in the presence of both random and systematic process variations. To address this, the extended statistical element selection (ESES) method is applied to compensate for the frequency variations using a combinatorial redundancy scheme.

This research explores the feasibility, advantages, implementation, and testing of a heterogeneously integrated switchable AlN filter system that can minimize parasitics and "self-heal" to increase yield and to realize uniform loading. In addition, several design techniques are proposed to implement the self-healing filter to a 1 GHz receiver frontend, including breaking LNAs into sub-LNAs to select sub-filters and using current summing to uniformly combine signal outputs. To control parasitics, 3-D integration is used to limit the interconnection lengths between the CMOS switches and the AlN resonators.

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1 Introduction

1.1 Motivation

Emerging MEMS resonators are exciting candidates for high quality filtering elements [1]. Among all MEMS resonator materials, Aluminum Nitride (AlN) contour mode resonators (CMR) have demonstrated the potential for high quality factor (Q) filters with varying frequencies on a single chip [2]. This motivates the implementation of such devices in software-defined radio (SDR) [3,4,5], where frequency selection can be achieved via an array of switchable filters. Despite the promising features of AlN resonator filters, challenges of process variation and of parasitic capacitance and inductance exist as barriers to realizing the full potential in integrated receiver applications. To address these challenges, the goal of this research is:

Designing and testing a heterogeneously integrated switchable AlN filter system that can minimize parasitics and "self heal" to increase yield and realize uniform loading.

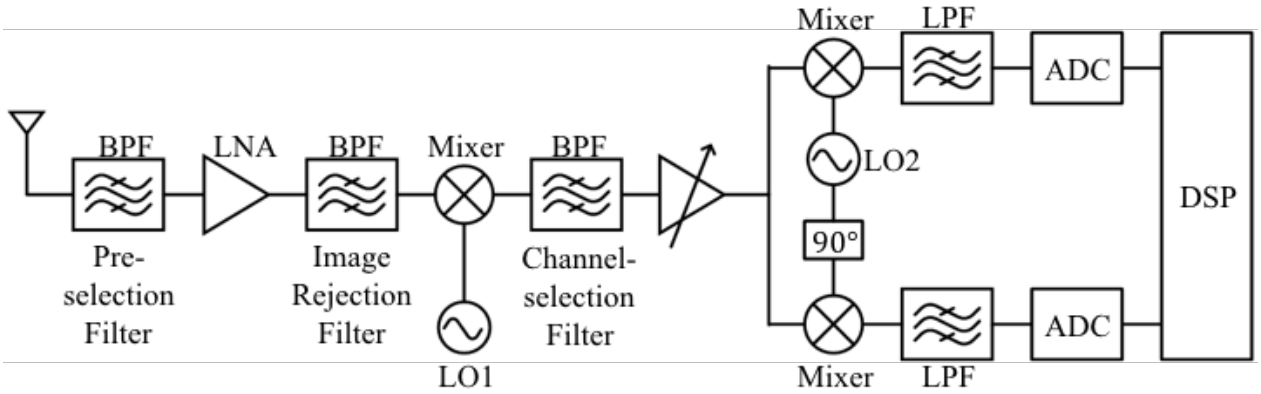
For such a system to *self heal*, the filter will reconfigure its circuit structure by digital control to calibrate its center frequency (f_0), bandwidth (BW), insertion loss (IL) and out-of-band rejection (OBR) to meet the system specifications. The calibration range is designed to cover process and environmental variations so that one design can adjust to various conditions and all of the designs in aggregate can achieve yield improvements.

1.2 Background

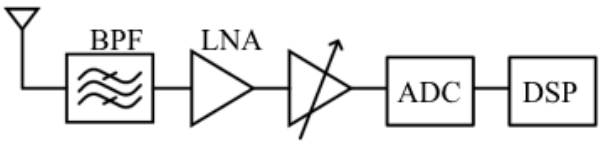
1.2.1 RF receiver design challenges

With the rapidly growing wireless communication technology, modern electronic devices: smart phones, fitness monitors and sensor networks are required to be compatible with multiple communication standards. This puts pressure on the RF components (e.g. receivers) to be able to function under strong interferences. Due to non-linearity in the transistor based components, interferers in other frequency channel can fold into the desired signal channel. When the interference power is strong, the folded components can exceed the receiver dynamic range, causing gain degradation during the signal amplification. Furthermore, if the interferer is a modulated signal, modulation can transfer from the interferer to the desired signal.

To avoid signal corruption from interference, conventional receiver architectures incorporate multiple filtering stages. The most widely used configuration in RF receivers is the super-heterodyne architecture [25]. Shown in Figure 1-1a, the received signal is first filtered by a pre-selection filter, amplified by the LNA and then passes through an image-rejection filter before translated from RF to IF. Following this stage, the signal is again filtered and demodulated to baseband. The second mixing stage can be I/Q modulation [25] to retrieve better signal information. Super-heterodyne architecture relies on multiple filtering and frequency translation components, making the receiver bulky and challenging for integration.



(a)



(b)

Figure 1-1 (a) Super-heterodyne receiver architecture. (b) Direct sampling receiver architecture.

A more simplified architecture uses direct sampling, as shown in Figure 1-1. After going through a channel selection filter, the signal of a desired channel is selected. Following amplification by the LNA, the signal is directly sampled by a sub-sampling ADC. The sub-sampling operation has a frequency translation effect, bringing the signal to base band while being digitized. This architecture relies on the first channel selection filter to suppress strong interferers. Since an interferer may fall only one or two channels away from the desired signal, the filter must provide a very high selectivity (i.e., a high *Q*). Moreover, during the sub-sampling stage, the aliasing effect will fold noise from bands at all integer multiplications of sampling frequency to the base-band, which will desensitize the digitization stage. This requires the filter to further suppress out-of-band noises to limit the overall folded noise level.

Another challenge with the channel selection filter is due to the fact that a different carrier frequency may be allocated to the user at different times, since such a filter would need a variable, yet precise, center frequency [26]. The variability can be fulfilled by adding switchable multi-frequency branches. The precision requirement is a property hard to reach, especially for high Q filters. For mechanical filters, center frequency is determined by device parameters including effective density and effective Young's modulus, which are easily affected by process induced variations. Change of thickness as trivial as 2 nm can cause center frequency shift by a few MHz, which is the channel bandwidth for some applications.

Based on the discussion above, to simplify the receiver architecture without sacrificing system performance, a channel selection filter that is highly selective, easily integrated and robust in terms of center frequency against process variations is needed.

1.2.2 AlN MEMS resonators and filters

The AlN CMR resonator is part of a class of piezoelectric resonant devices that are able to span a broad range of frequencies from a few MHz up to GHz on the same silicon chip [6]. These resonators can achieve quality factors above 1,000 in air over the entire frequency spectrum [7]. Figure 1-2a is an SEM image of a two-port AlN CMR resonator. An AlN film is sandwiched between top electrodes (input and output) and bottom plate (ground). When applying an electric field across the film, the AlN structure expands laterally. The film can be excited in contour-mode resonant vibrations via the piezoelectric coefficient d_{31} as long as the signal frequency coincides the device natural frequency f_o, which is set by the pitch of the electrode, P.

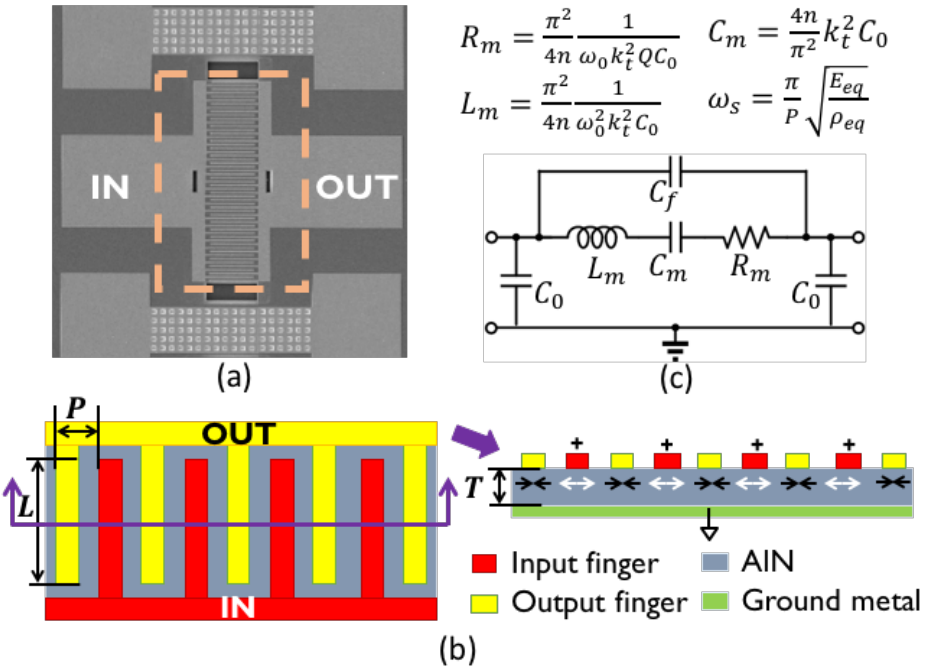


Figure 1-2 AlN contour-mode resonator (a) SEM picture of the resonator. (b) Diagram of the resonator. (c) Lumped circuit model of the resonator.

The signal in the mechanical domain is transmitted in the AlN film through energy exchange between elastic energy (stress) and kinetic energy (mass motion), which can be modeled by a mechanical second-order system determined by mass density ρ, Young's modulus E, quality factor Q, and device geometry. Due to the similarity between the mechanical system to an RLC second-order circuit, the AlN resonator is modeled using the Butterworth-Van Dyke model [8]. The lumped circuit components are derived from

the material parameters and the device dimensions (Figure 1-2c). The electrode length L, electrode number n and the AlN film thickness T set the resonator motional resistance R_m, intrinsic capacitance C_0 and the resonant tank L_m, C_m. The electrical and mechanical coupling is represented by coupling coefficient k_t^2 and is determined by the ratio of C_m and C_0. The transfer function of the RLC tank takes the form of a resonator with capacitive feedthrough (as illustrated in Figure 1-3).

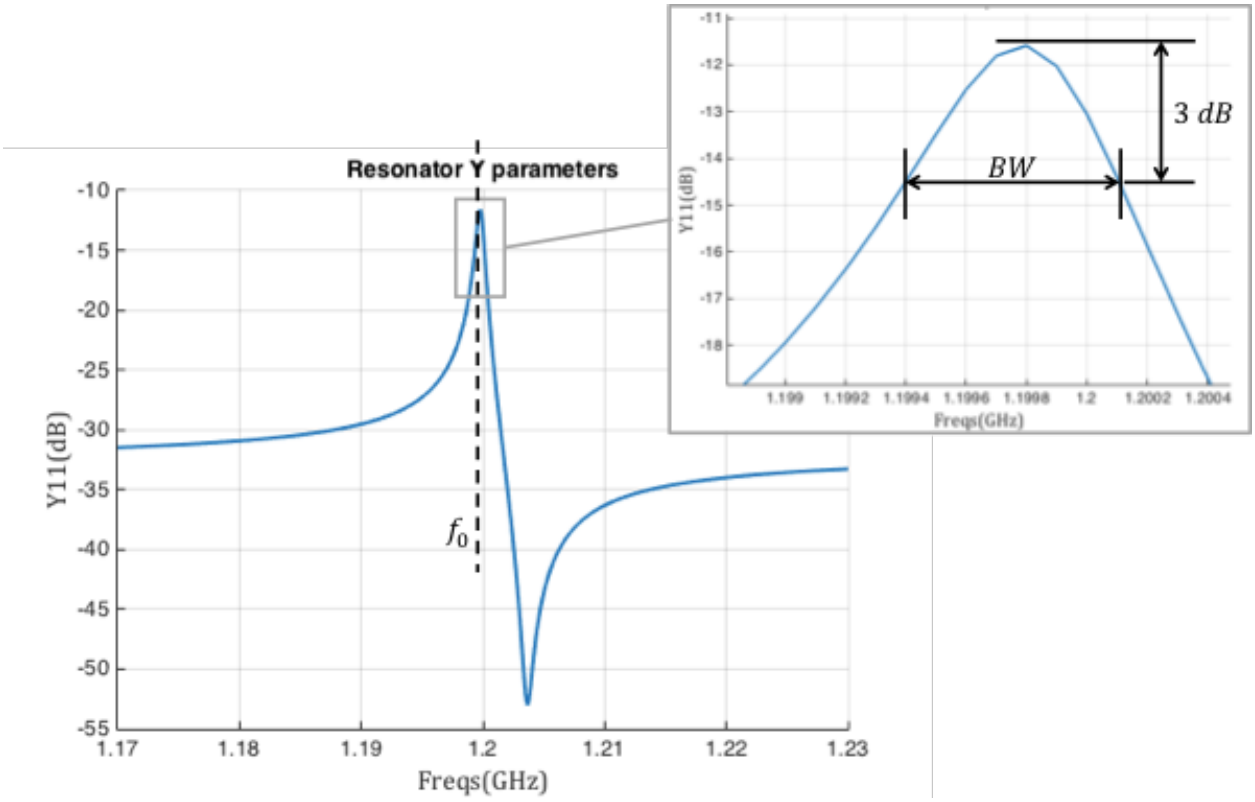


Figure 1-3 Input admittance, Y11, of an AlN two-port resonator with the output port short-circuited.

To build a robust channel selection filter and to achieve the desired filter performance specifications requires proper interconnection of multiple AlN two-port resonators. A switchable array of smaller "sub-filters" provides the capability to select the best combination of parallel-connected sub-filters in order to implement self healing. This section describes the design considerations involved in the self-healing filter array.

AlN contour mode resonator-based filters must meet specific design goals for the application of channel selection. First, fractional bandwidth (FBW, the ratio between the filter 3 dB BW and the center

frequency f_0) needs to be small enough to achieve channel selection at RF frequencies. Second, the out-of–band rejection (OBR) needs to be larger than 20 dB to reject out-of-channel interferers. Third, as the first stage of a receiver, low insertion loss is critical to ensure system SNR is adequate. Finally, since it serves as a connection between antenna and transceivers, the channel selection filter is required to be impedance matched to the characteristic impedance of the antenna feed, which is usually 50 Ω for low-noise systems.

In this work, a coupled resonator filter topology with three series-connected AlN contour-mode two-port resonators is implemented to meet the specifications for a channel-selection filter [9]. The three identical resonators are connected in series, resulting in three resonant modes from the interaction between the RLC branches (Figure 1-4). Without considering process variations, this filter topology has been reported to offer center frequency above 1 GHz, insertion loss below 3 dB, FBW around 0.3% of center frequency, out-of-band rejection above 20 dB [4]. The insertion loss can meet the 9 dB noise figure (NF) spec for the Long-Term Evolution (LTE) wireless communication protocol [10] with a moderate receiver frontend NF spec of 3 dB. The 20 dB OBR can alleviate the linearity specification of the third-order interception point (IP3) by 30 dB.

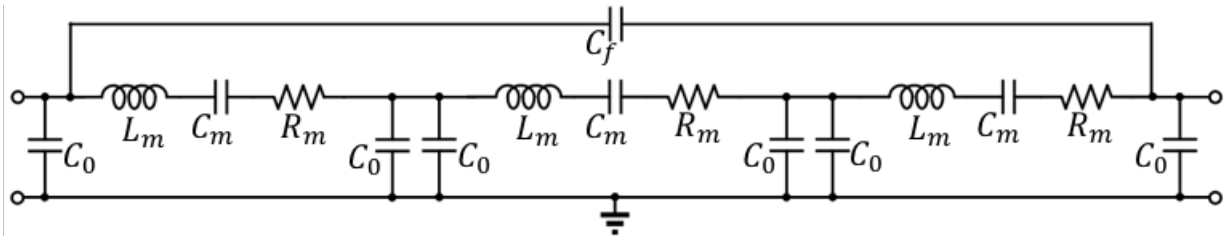


Figure 1-4 AlN resonator filter schematic model.

To maximize power transmission from the input to the output port, the filter needs to be terminated by a proper resistance $R_0 = \left|\frac{1}{j\omega_0 C_0}\right|$. For a channel selection filter operating at 1 GHz, to match to a 50 Ω antenna, the intrinsic capacitance would be greater than 3 pF. To achieve an intrinsic capacitance of 3 pF, the resonator AlN film size is around 350 μm by 350 μm (a larger resonator aspect ratio is desired to accommodate the flip-chip pad separation rule with 3D integration – see Section 5.4.1). A larger resonator

not only requires longer release time, but is also at higher risk of fracture during fabrication due to large trapped residual stresses in the AlN. Therefore, a larger filter area can be formed by coupling many smaller sub-filters electrically. Each *RLC* resonant circuit comprises an array of k smaller resonator filters (sub-filters) coupled electrically in parallel, so that the termination resistance is k times lower than a single sub-filter. In previous experiments, a sub-filter size that is matched to 350 Ω and $k = 4{\sim}7$ is a proper selection to achieve overall 50 Ω impedance. To implement SES on the AlN resonator filters, the total area of the selected sub-filters should be the same for all k selections out of a total N sub-filters in the array. To improve the effective filter yield while keeping the load matched, the number of M possible combinations of k out of N sub-filters can be large and so it can take a long time to calibrate to find the best combination (or even an adequate combination that meets the specifications).

1.2.3 Process variations in AlN MEMS resonator filters

From the lumped circuit model of the AlN resonators, given the center frequency f_o, the quality factor Q determines the resonator bandwidth (BW) as well as the insertion loss at resonance. Intrinsic capacitance C_0 contributes to the out-of-band transimpedance. The coupling coefficient k_t^2 sets the separation of the peak and dip frequency (parallel frequency). These four parameters (f_0, Q, C_0, and k_t^2) determine the resonator's electrical performance. In the literature [11], AlN two-port contour mode resonators at room temperature (300 K) achieved a center frequency of 1 GHz, with unloaded quality factor around 2000 and k_t^2 of 1.35%. The high Q and low insertion loss make AlN resonators good candidates for channel selection filters.

The corresponding deviations in the parameters (Q-value, f_0, C_0 and k_t^2) due to process variations induce deviations in the resonator electrical characteristics. For example, a 1 GHz center frequency corresponds to interdigitated electrode half pitch $W = 2$ μm. A pitch change of 12 nm would cause a frequency shift of 6 MHz, which is the bandwidth of the resonator when it is loaded with a 50 Ω impedance. To study the statistical characterization of resonators, 10 identical two-port resonators were

laid out in a row with a total length of 0.5 mm. Four chips that are on the same wafer fabricated by the Institute for MicroElectronics, A-Star Singapore (IME), were measured to obtain the center frequency for the 40 filters (Figure 1-5). Δf_0 is the difference between the center frequency of each filter and the mean value of the 10 filters on the same chip. The important observation is that the distribution of the center frequency of the devices exhibits a linear relationship with the device position. Therefore, systematic error is dominating the AlN resonator center frequency variations, as expected . Previous works have reported the statistical characteristics of the AlN two-port resonator filter performance [4], shown in Table 1-1. Among the four parameters, center frequency shows a biggest difference between inter-chip and intra-chip standard deviation (σ). The inter-chip deviation reaches 5.3 MHz, which is the bandwidth of some communication channels [10]. This can cause problems when we design a channel selection filter for a specific communication band. The self-healing method can be used to improve this filter performance.

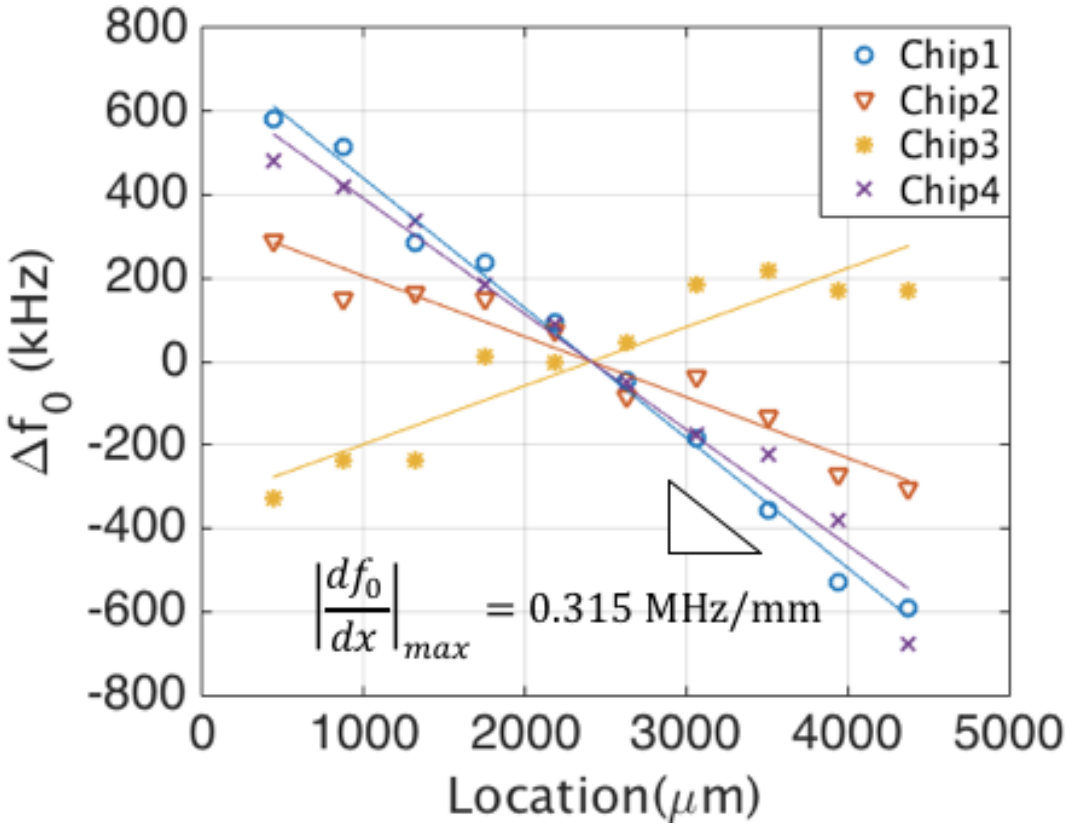


Figure 1-5 Resonator center frequency data collected from 40 resonators on 4 chips.

Table 1-1 Statistical study of AlN resonator filters.

	f_0 (GHz)	IL (dB)	BW (MHz)	OBR (dB)
Pooled mean value	1.15	4.44	3.83	24.81
Pooled STD	0.0053	0.65	0.23	1.91
Intra-chip STD	0.0002	0.62	0.059	0.53

1.2.4 Conventional tuning and trimming methods in MEMS resonator filters

AlN MEMS resonator filters, due to their high Q characteristic, have been used as stable frequency references. In such applications, the main performance metrics are its center frequency (f_0), Q value, insertion loss (IL), out-of-band rejection (OBR) and in-band ripple. In transition from research laboratories to commercial products, these metrics require precise control. According to the process variation measured, f_0 variations dominate all other metrics, therefore, f_0 control is crucial. Research investigation in f_0 control techniques can be categorized into tuning and trimming. The former provides f_0 tuning by changing the device effective stiffness, and the latter provides f_0 trimming by changing the device effective density.

Mechanisms commonly employed to alter the effective stiffness involve electrostatic and thermal tuning. In electrostatic tuning devices, an electrical spring with stiffness tunable via a DC voltage is added to provide f_0 tuning. The small stiffness of the electrical spring, due to low-efficiency electrostatic transduction, limits the technique to low-frequency low-stiffness flexural-mode resonators [12]. A relatively high frequency (20 MHz) IBAR oscillator with temperature compensation is designed in [13]. The tuning range is achieved through high DC control voltage (>10 V), making it inappropriate for portable electronic device applications. In thermal tuning devices, a tunable heater element is added, resulting in changing resonator temperature and tuning frequency due to large TCF. Wide tuning range (3000 ppm) can be achieved [14] at a cost of additional bulky heating elements.

Trimming methods permanently shift device parameters by selectively adding or removing material, usually after fabrication. Examples of this class of technique include laser or ion beam trimming through a transparent package [15] and localized oxide growth using thermal actuation [16]. *In situ* trimming corrects process variations and packaging uncertainties at the same time, which makes it attractive. However, the tuning accuracy is limited by the laser or ion beam diameter. Also fine tuning each device is generally too time-consuming for mass production.

1.2.5 Statistical Element Selection (SES) method in MEMS resonator filters

SES is a self-healing methodology that can be used to alleviate the variation challenges when using AlN resonators. SES is a post manufacturing calibration technique that accommodates large-scale process variations to improve the matching of transistors [17].

According to Pelgrom's transistor mismatch model [23], standard deviations of the current factor and threshold voltage are proportional to $1/\sqrt{WL}$. Thus, it is a traditional approach to improve transistor matching by increasing the sizing. An alternative approach is redundancy, where a large number (N) of devices are built and the best one is chosen, which consumes N times the area. In contrast, SES exploits combinational redundancy by selecting k devices out of N devices, resulting in an exponential increase in the number of available combinations C_N^k. SES has been demonstrated to lower CMOS offset by multiple orders of magnitude at a relatively low circuit overhead [18,19,20,21]. A similar technique can be used to fine tune MEMS resonators, since the variations in the device performance are affected by random variations. However, from the statistical study of the resonators in the experimental fabrication process, systematic variations dominate the on-wafer center frequency variation. In a production environment, although the equipment would be better controlled and trim techniques would be put in place to reduce the systematic process variation, to precisely control each individual device is time consuming. The original SES approach needs to be extended to solve the problem.

For the original SES methodology, the distribution of the combined k elements is created by the random variation of the equally sized N elements. A large number of combinations aggregated around the nominal design value with a deviation close to the random variation. This allows extremely high calibration resolution to be realized. However, since only the values from the random variations are present in the N sub-devices, the combined device parameter will not exceed the range of random variation. This would self-heal when the wafer-level variation is in the same range as the chip-level. However, in the presence of systematic variation, the calibration target window will deviate from the mean value on the chip. With no sub-device in the calibration window range, the calibration success rate drops rapidly.

1.3 Proposed system and contributions

Commonly used trimming techniques are effective for coarse f_0 calibration, but they are costly to calibrate for each individual device. An SES based reconfigurable filter design can provide a fine calibration resolution, but the calibration range is limited. Based on these methods, this work assumes die to die variation is eliminated by coarse trimming and adopts extended the SES method to maintain fine resolution while enabling f_0 reconfiguration over a relatively broad tuning range.

To realize the statistical selection for MEMS filters, a heterogeneously integrated receiver frontend system in Figure 1-6 is proposed. Figure 1-6 shows a receiver structure with a channel selection filter and a gain stage as the front-end of a direct sampling receiver. Without self-healing, the filter center frequency is prone to process variations. To implement self-healing, the filter is separated into an array of sub-filters. In the calibration phase, a sub-set of the sub-filters that meet the filter specifications are selected to function as a single filter. This implementation follows the self-healing method of Statistical Element Selection (SES) [17]. Adding selectability to a filter array, however, requires complex selection control circuitry. The switching control circuit needs to ensure uniform loading and minimized parasitic overhead. Therefore, the low noise amplifier (LNA) is separated in the receiver front-end into sub-LNAs, with each of the sub-LNAs serving as the switching components. A summing stage follows the array to sum signals from selected branches. After going through a variable gain amplifier, the signal is ready to be sampled through a band-pass sampling analog-to-digital converter (ADC). Parasitic capacitances and inductances from packaging are present at the interface between the sub-filters on the MEMS chip and the sub-LNAs on the CMOS chip. Since the performance of both the LNA and the filters is sensitive to these parasitics, flip-chip bonding for interconnection is used to reduce wiring parasitics.

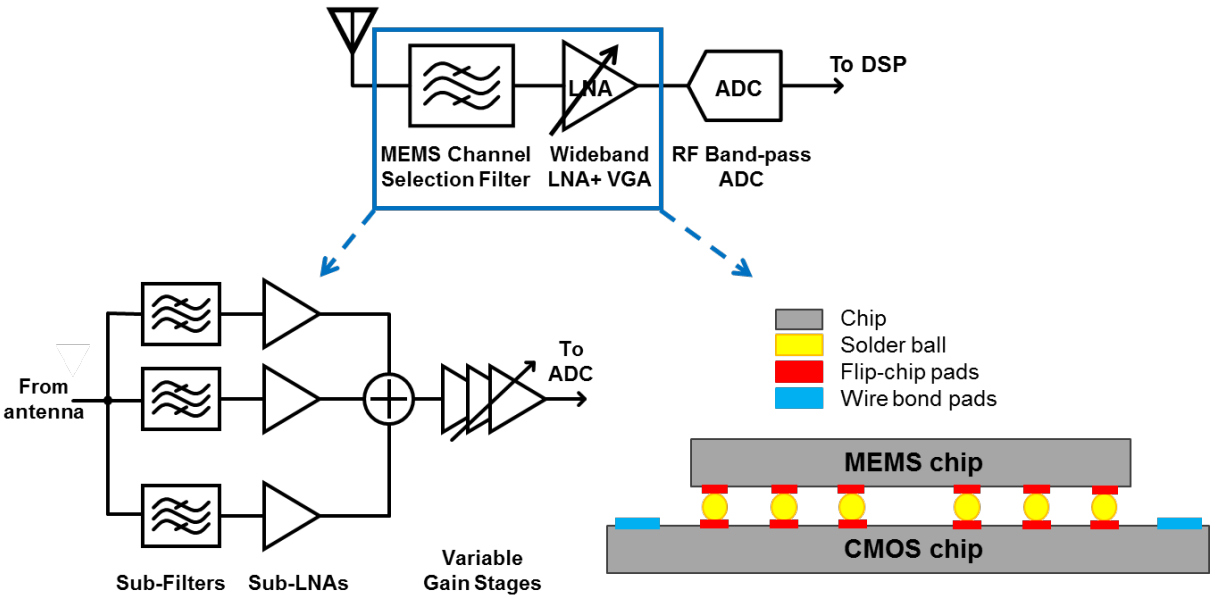


Figure 1-6 Proposed receiver frontend.

Since the (E)SES method is suitable for most devices where the performance deviation is affected by random variation, this method has a wide application space in the future emerging technologies, especially with device scaling. This work presents high-yield AlN resonator filters as a specific and unique application of ESES. Process variation is an intrinsic challenge that inhibits the use of many types of MEMS high-*Q* filters in front-end subsystem in commercialized receivers. Improving the filter yield can unleash the power of these devices to improve real-world RF systems.

To achieve this goal, the following specific design and methodology contributions are needed to make these self-healing resonator arrays a reality:

1) ESES calibration design method for MEMS filters

GHz-level AlN MEMS resonator filters are the target of study to apply and demonstrate the extended Statistical Element Selection algorithm. The generalized design method optimizes yield for center frequency accuracy with minimum area overhead to overcome both systematic and random process errors. Since the ESES corrects center frequency errors resulting from location on the die, it is widely applicable to most MEMS filters whose center frequencies are sensitive to process variations including feature size lithography error, inhomogeneous metal deposition or

etching inaccuracies. This method works well with conventional trimming methods and improves fine frequency tuning efficiency for industrial mass production.

2) Ground switch for on/off function with uniform loading

Most applications of RF MEMS in SDR involve switching to alter the operating bands. Due to the relatively high resistance in CMOS transistors, any switch appearing on the signal path will contribute to insertion loss. An on/off ground switch is introduced as a new mechanism that avoids deterioration in the device power transfer arising from series switch control. By disconnecting the RF ground from the bottom electrode of the resonator, the two-port device cannot generate substantial internal electric fields for piezoelectric drive or sense, effectively turning off the resonator. The self-healing filter array employs this ground switching mechanism. S-parameter measurement for the on and off states provide characterization of isolation and validation of the overall effect on the array performance.

3) Multi-input single-output LNA to handle output coupling

To further limit deleterious impact of switching on insertion loss, this work will be the first to integrate circuit components that are already present in the common receiver architectures to perform switching on MEMS devices. The LNA serves both as an amplifier and a switch, which together with a summing circuit stage that follows it, aggregates signals from each of the selected bands. Summing electrically at the output stage of the LNA avoids electromechanical coupling at the output ports of the MEMS sub-filters. The co-design of the LNA and the filter interface takes both circuit components and the MEMS components into consideration so that the overall system achieves improved performance.

4) Instantiation in a CMOS-MEMS flip-chip process

IME will flip-chip bond the MEMS and CMOS chips, resulting in a minimal impact of capacitive and inductive parasitics by lowering the routing distances. A redistribution layer (RDL) is built in the IME process flow to further alleviate CMOS routing parasitics. This work is the

first time that this process is used for integrating MEMS devices with CMOS circuits. This approach allows for a MEMS chip that is larger than the CMOS chip.

2 Wide range calibration approach

2.1 ESES method

To increase the tuning range and to accommodate other dominant variation sources, the N sub-elements in SES can be sized non-uniformly. For this *extended* SES (ESES) method [22], the overall size of k elements already spans a range for the nominal case, and this range can be controlled by making the nominal sizes of the elements to be a design parameter. With random variation "designed in," the distribution of the overall size of k elements creates a wider calibration tuning range.

In applying the ESES method to AlN MEMS resonator filters to calibrate wafer level process variation, a tradeoff exists between tuning range and tuning resolution. According to the statistical measurement data, resonator center frequencies vary up to 10 MHz across the IME-fabricated wafers over mm-scale distances. To form a filter with smooth passband, the frequency interval between successive sub-filters needs to be less than 250 kHz. Covering a 10 MHz range with 250 kHz intervals would require 40 sub-filters. More sub-filters would be required considering the redundancy for higher yield. This brute-force approach significantly increases area overhead and the limitation motivates ESES as a good complementary technique to combine with wafer-scale trimming – i.e., coarsely trim to reduce wafer-level variation and use ESES for fine frequency calibration. Since the cost for trimming scales with accuracy, the implementation of ESES after trimming is proposed as a balanced solution for mass production.

To implement ESES, parameters for the "pseudo-variation" sequence in design of center frequencies in the array need to be determined. First, the sequence parameters (number of sub-filters N, frequency range F_{ps} and frequency values f_{0i} of sub-filters $i = 1..N$) of the pseudo-variation affects the calibration range and resolution. For a given value of N, a small interval ensures high calibration resolution and better success rate, but the total calibration range would be sacrificed. Optimization on these parameters is needed to maximize calibration yield in limited area overhead. Secondly, since the sub-filter center

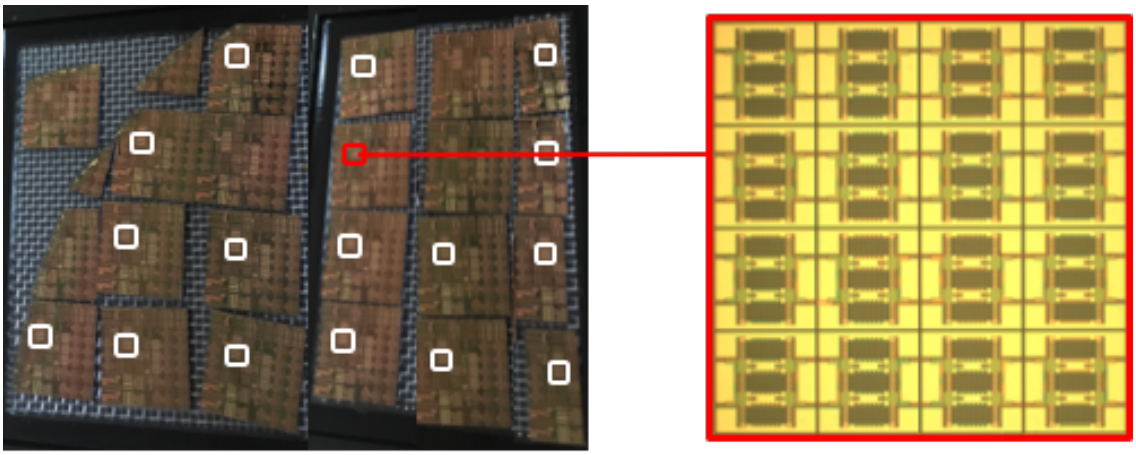
frequency will be affected by the filter location, the effectiveness of ESES will be influenced by the layout placement of the sub-filter pseudo frequency shifts. In one scenario, the filter pseudo frequency shift is opposite the geometrical process variation in frequency, which shrinks the calibration range. Conversely, if the filter pseudo frequency shift aligns with the geometrical process variation in frequency, the interval will be doubled, reducing the calibration resolution. Therefore, for a given pseudo-variation sequence, the placement of each pseudo frequency shift within the layout needs to be optimized.

2.2 ESES design optimization

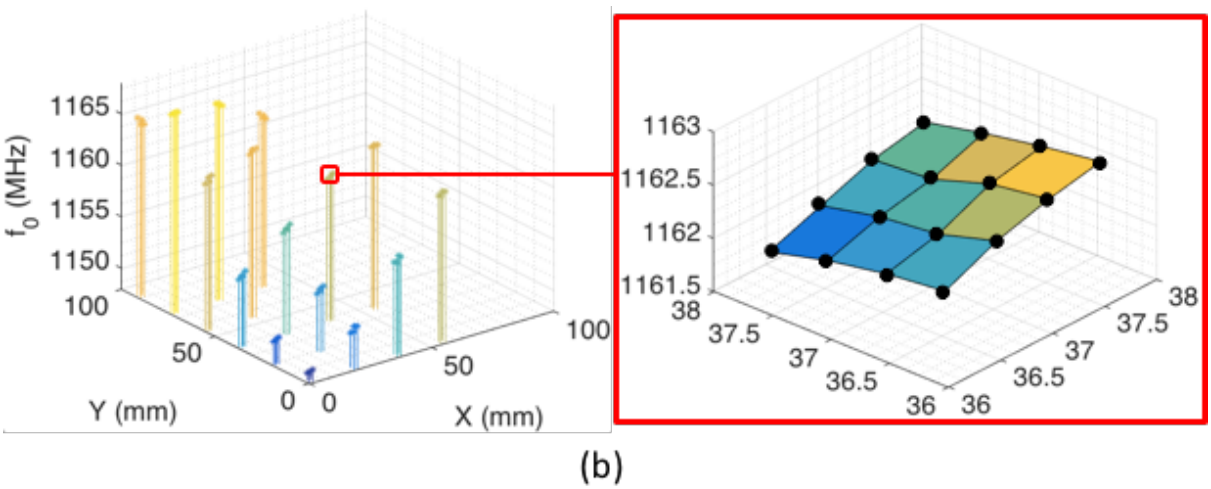
2.2.1 Filter and resonator statistical data collection

The center frequency (f_0) variation is systematically dependent on the filter location, and so the distribution of f_0 has a geometrical dependence. The assumption of a normal distribution for f_0 where all dies to have the same mean value across the wafer [4] does not properly represent the wafer-level statistical distribution.

The testing structures to capture the wafer-level distribution are shown in Figure 2-1a. 16 identical two-port resonator filters were laid out in a 4×4 matrix on 2×2 mm^2 chips on a same wafer fabricated by A*STAR Institute of Microelectronics (IME). The wafer-level f_0 distribution with respect to location is shown in Figure 2-1b.



(a)



(b)

Figure 2-1 Wafer-level center frequency profile measurement.

The gradient of center frequency gradually changes across the wafer, with smooth curvature. For a 2×2 mm single chip, the area is sufficiently small for the f_0 gradient profile to be modeled as a plane (*i.e.,* linear variation). For any "random" chip on a wafer, the plane center frequency shift from the wafer mean (Δf_{0c}) and the normal vector direction angles (α and β) are random variables (Figure 2-2).

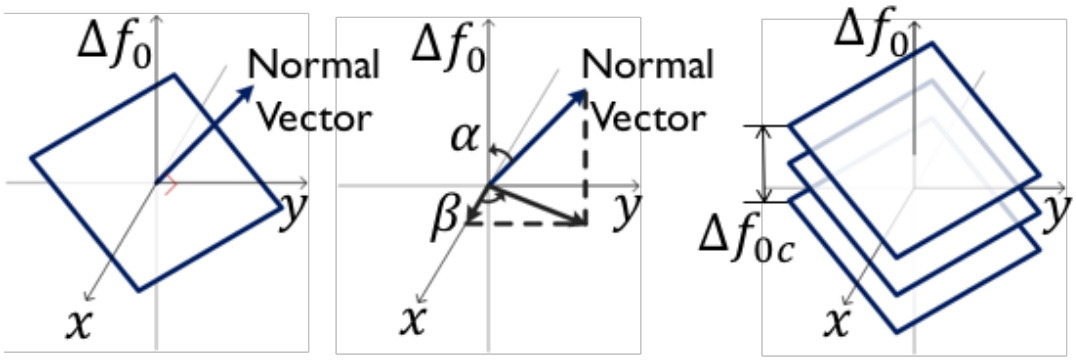


Figure 2-2 Plane model for cell-level center frequency distribution.

For all the 71 chips on the single wafer tested, these variables are extracted. A histogram of each measured variable are summarized in Figure 2-3.

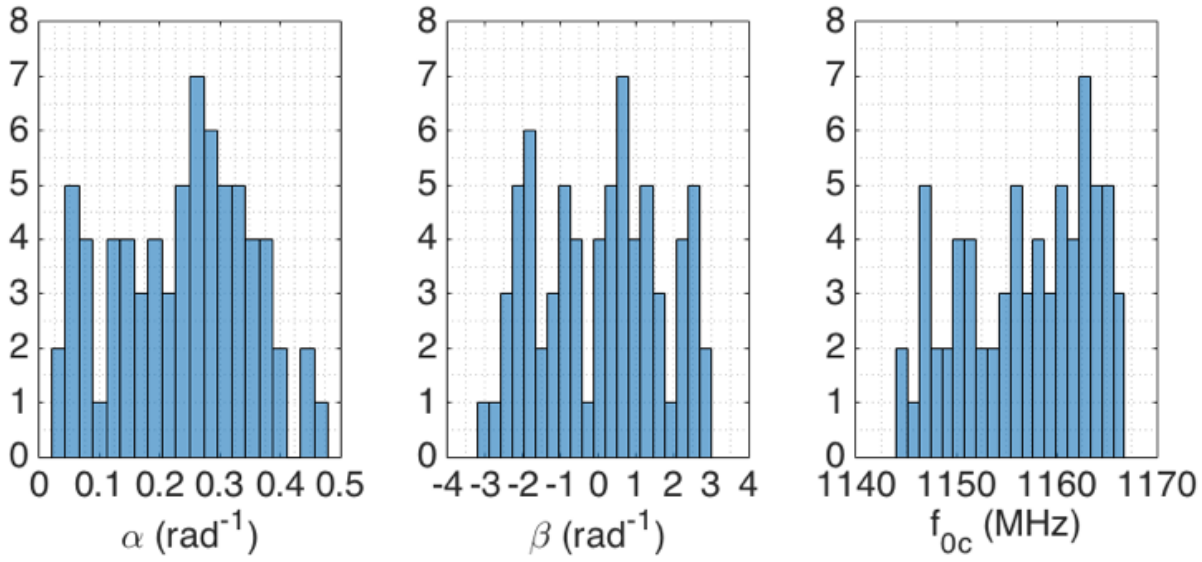


Figure 2-3 Histogram of f_0 plane parameters, taken from measurements.

The histograms indicate that α, β and Δf_{0c} may be modeled with a uniform distribution. Table 2-1 summarizes the distribution parameters, which is raw data taken from an un-trimmed wafer. In a production environment, the actual range of Δf_{0c} would be dependent on the accuracy of trimming.

Table 2-1 Performance statistics of standalone MEMS filters for 1136 samples measured across 71 dies.

	f_0 (MHz)	BW (MHz)	IL (dB)	OBR (dB)
Mean	1158	2.75	2.91	20.1
Standard Deviation	6.95	0.102	0.187	3.02
	α (rad^{-1})	β (rad^{-1})	Δf_{0c}* (kHz)	–
Min	0	$-\pi$	−450	–
Max	0.4	π	450	–
* Assumed Δf_{0c} distribution after trimming				

In order to simulation the statistical behavior of AlN resonator filters, the two-port network parameters of the filters need to be generated from lumped resonator circuit components R_m, L_m, C_m and C_0, which are variables following the statistical distribution determined by the statistical distribution of the resonator parameters f_0, Q, k_t^2 and C_0. To get the statistics of these parameters, 19 4x4 resonator

arrays on the same wafer were measured. The histograms of these parameters are shown in Figure 2-4. The statistics are shown in Table 2-2. From the histogram, the parameters Q, k_t^2 and C_0 follow normal distribution. The center frequency is dominated by systematic variations, but is also affected by random variations. To extract the random variation distribution, the center frequency data is extracted by subtracting the estimated geometric variation from the measured parameter. The residue would be the result of the random variation.

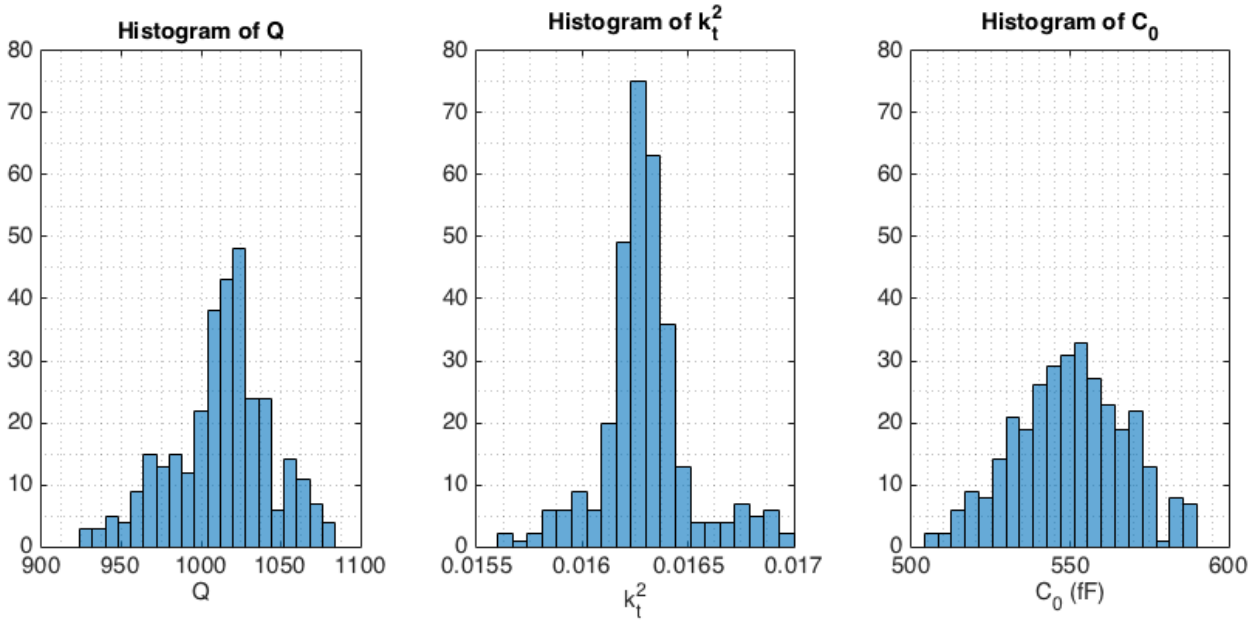


Figure 2-4 Histogram of resonator parameters, taken from measurements.

Table 2-2 Performance statistics of standalone MEMS resonator for 304 samples measured across 19 dies.

	f_0 (MHz)	Q	k_t^2	C_0 (fF)
Pooled mean value	1147	1013	1.63%	550.2
Pooled standard deviation	0.087*	31	0.021%	1.75
* The standard deviation after linear regression				

Using the statistical model, the systematic and random variations of the resonator parameters are characterized. The total result would be the sum of both effects. Equations (2.1-(2.7 show the calculation for these parameters.

$$\alpha = \text{Uniform}(0,\ 0.4\ \text{rad}^{-1}) \tag{2.1}$$

$$\beta = Uniform(0,\ 2\pi) \tag{2.2}$$

$$df_0(x,y) = \frac{x + y\,tan\,\beta}{cot\,\alpha\sqrt{1 + tan^2\,\beta}} \tag{2.3}$$

$$Q = Norm\left(\mu_Q, \sigma_Q\right) \tag{2.4}$$

$$k_t^2 = Norm\left(\mu_{k_t^2}, \sigma_{k_t^2}\right) \tag{2.5}$$

$$C_0 = Norm\left(\mu_{C_0}, \sigma_{C_0}\right) \tag{2.6}$$

$$f_0 = Norm\left(\mu_{f_0}, \sigma_{f_0}\right) + df_0(x,y) \tag{2.7}$$

2.2.2 Basic layout pattern

Since the normal vector angles α and β follow a uniform distribution, the chances for either side of a chip to have higher f_0 than the other is equal. To prevent the pseudo variation sequence from being offset by geometrical variation, it is preferable to duplicate all pseudo frequencies in the four sides of a chip. This leads to a centro-symmetric placement of the sub-filters. The filters are designed in a squared shape, so the most symmetrical placement for the N sub-filters would be when N is a square of an integer, and the N sub-filters are placed in an $\sqrt{N}\times\sqrt{N}$ array. For the number of distinct frequencies, $N/4$ would ensure duplicating all pseudo-frequencies on the four sides. The smallest number meeting these requirements is $N = 16$. Figure 2-5 shows a pseudo-frequency placement for this configuration. With the resonator core and necessary peripheral pads and routing, each filter takes a 500×500 μm square, and the total chip area becomes 2×2 mm. The four filters in the center would not differ significantly even with

geometrical variation. Therefore, a fifth frequency is assigned in the center. The effectiveness of this layout placement is evaluated by sweeping the frequency values, as discussed in the next section.

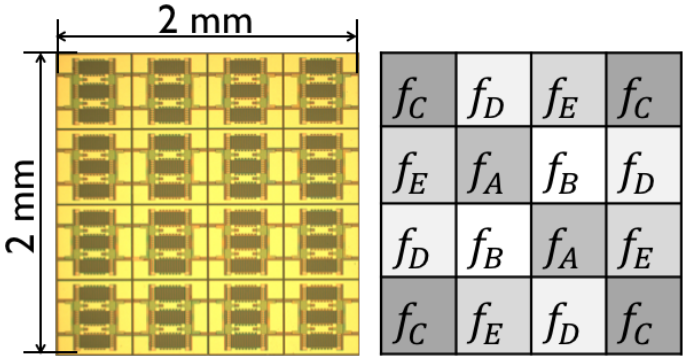


Figure 2-5 Basic layout for ESES filter array.

2.2.3 Layout placement rotations for a pseudo-variation sequence

To optimize the layout placement for pseudo-variation, the success rate needs to be compared among different pseudo-variation sequences. To simplify the following, the pseudo frequencies are sorted in the sequence of their values: $f_{-2} < f_1 < f_0 < f_1 < f_2$. The pseudo range being the range of the values in the pseudo-variation sequence, can be expressed as $F_{ps} = f_2 - f_{-2}$. In the discussion, the frequency sequence is designed to center around the target frequency: $f_{tar} = \frac{f_2 + f_{-2}}{2}$. The selection of f_{-1}, f_0 and f_1 can be any value within the range of $[f_{-2}, f_2]$. Enlisting all combinations would be impossible, but discretizing the interval and a search through all combinations leads to the optimized sequence. In this discussion, the range $[f_{-2}, f_2]$ is evenly divided into 8 intervals. If we define the difference between each pseudo frequency and the target as: $\Delta f_i = f_i - f_{tar}, i = -2, \ldots 2$, the interval can be represented as in Figure 2-6 and all 35 combinations are listed in Table 2-3.

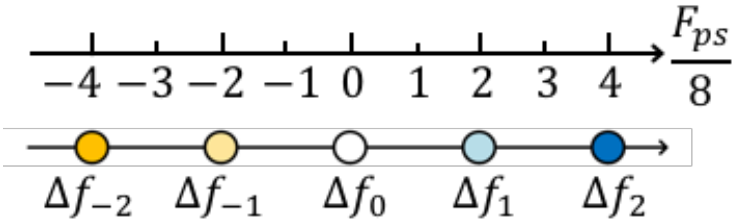


Figure 2-6 Frequency interval for the pseudo frequency in ESES filter array.

Table 2-3 Combinations of frequency interval for the pseudo frequency in ESES filter array.

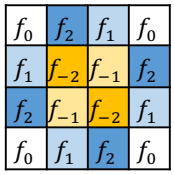
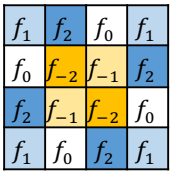
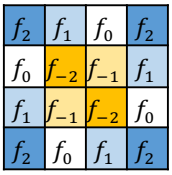
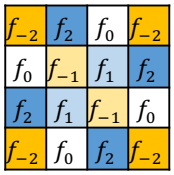
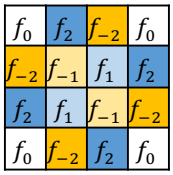
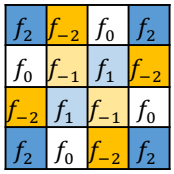
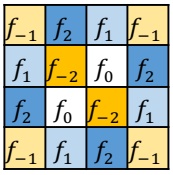
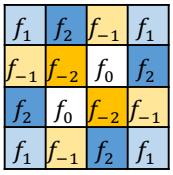
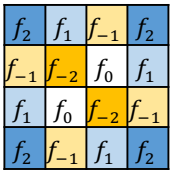
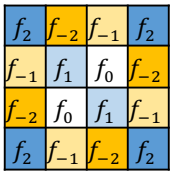
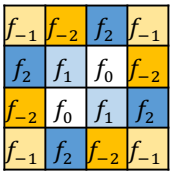
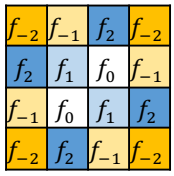
Unit: $\boldsymbol{F_{ps}/8}$								
$\Delta \boldsymbol{f_{-1}}$	$\Delta \boldsymbol{f_0}$	$\Delta \boldsymbol{f_1}$	$\Delta \boldsymbol{f_{-1}}$	$\Delta \boldsymbol{f_0}$	$\Delta \boldsymbol{f_1}$	$\Delta \boldsymbol{f_{-1}}$	$\Delta \boldsymbol{f_0}$	$\Delta \boldsymbol{f_1}$
-3	-2	-1	-3	1	2	-2	2	3
-3	-2	0	-3	1	3	-1	0	1
-3	-2	1	-3	2	3	-1	0	2
-3	-2	2	-2	-1	0	-1	0	3
-3	-2	3	-2	-1	1	-1	1	2
-3	-1	0	-2	-1	2	-1	1	3
-3	-1	1	-2	-1	3	-1	2	3
-3	-1	2	-2	0	1	0	1	2
-3	-1	3	-2	0	2	0	1	3
-3	0	1	-2	0	3	0	2	3
-3	0	2	-2	1	2	1	2	3
-3	0	3	-2	1	3			

Considering the centro-symmetry property, there are 36 distinct rotations for such a configuration. The symmetrical passband of the filter allows further reduction of the number of independent rotations to 30 (Figure 2-7, Table 2-3).

Table 2-4 Combinations of frequency rotation for the pseudo frequency in the ESES filter array.

Rotation	$\boldsymbol{f_A}$	$\boldsymbol{f_B}$	$\boldsymbol{f_C}$	Rotation	$\boldsymbol{f_A}$	$\boldsymbol{f_B}$	$\boldsymbol{f_C}$
11	f_{-2}	f_{-1}	f_0	61	f_{-1}	f_1	f_{-2}

12	f_{-2}	f_{-1}	f_1	62	f_{-1}	f_1	f_0
13	f_{-2}	f_{-1}	f_2	63	f_{-1}	f_1	f_2
21	f_{-2}	f_0	f_{-1}	71	f_1	f_0	f_2
22	f_{-2}	f_0	f_1	72	f_1	f_0	f_{-1}
23	f_{-2}	f_0	f_2	73	f_1	f_0	f_{-2}
31	f_{-2}	f_1	f_{-1}	81	f_2	f_{-1}	f_1
32	f_{-2}	f_1	f_0	82	f_2	f_{-1}	f_0
33	f_{-2}	f_1	f_2	83	f_2	f_{-1}	f_{-2}
41	f_{-2}	f_2	f_{-1}	91	f_2	f_0	f_1
42	f_{-2}	f_2	f_0	92	f_2	f_0	f_{-1}
43	f_{-2}	f_2	f_1	93	f_2	f_0	f_{-2}
51	f_{-1}	f_0	f_{-2}	101	f_2	f_1	f_0
52	f_{-1}	f_0	f_1	102	f_2	f_1	f_{-1}
53	f_{-1}	f_0	f_2	103	f_2	f_1	f_{-2}

11	12	13	61	62	63
					
21	22	23	71	72	73
					

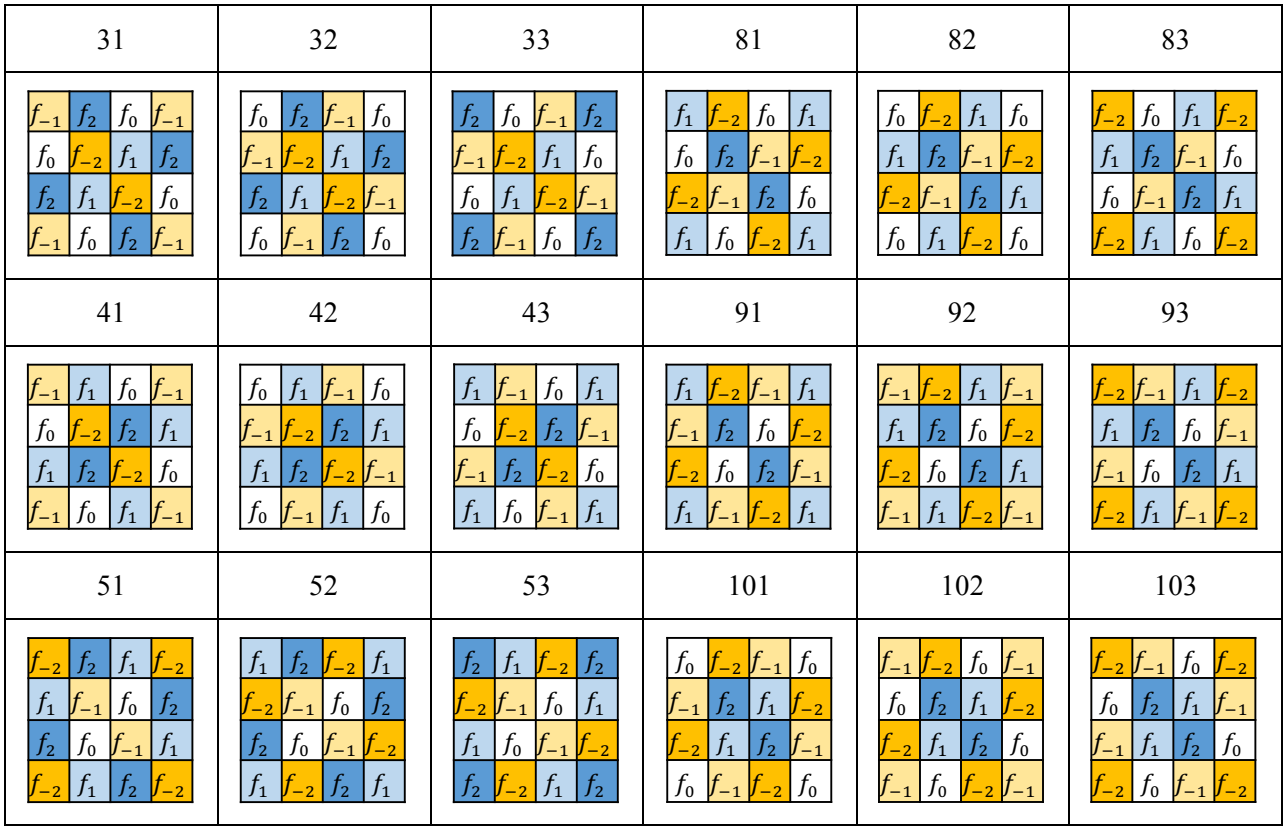


Figure 2-7 Frequency rotation for the pseudo frequency in the ESES filter array.

2.2.4 Monte Carlo simulation for success rate evaluation

For each rotation and interval combination, the success rate is evaluated through Monte Carlo simulation. For each run, the resonator parameters f_0, Q, k_t^2 and C_0 are generated from the statistical model. The lumped circuit components R_m, L_m and C_m are then calculated from the resonator parameters. Using the circuit components, the two-port network parameters of a resonator are calculated. In this thesis, the two-port network matrix is denoted with a bolded initial letter: **S** for S-parameters, **Y** for Y-parameters and **T** for transmission matrix (2.8). The subscript denotes the circuit component associated with the parameter: $\mathbf{S}_{\text{Filter}}$ denotes the S-parameters of the filter.

$$\mathbf{S} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}, \mathbf{Y} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}, \mathbf{T} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{2.8}$$

According to two-port network theorems [26], cascading the transmission matrices of the three series-connected resonators provides the Y parameters of the sub-filter (2.9) and (2.10). After the Y parameters of N subfilters are established, all C_N^k combinations are simulated. For each combination, Y parameters of the selected k sub-filters are added to form the Y parameters of the combined filter. Transformation of Y parameters to S parameters give the simulated filter parameters f_0, BW, IL, OBR and in-band ripple values.

$$\mathbf{T}_{\text{SubFilter}} = \mathbf{T}_{\text{Resonator},1} \times \mathbf{T}_{\text{Resonator},2} \times \mathbf{T}_{\text{Resonator},3} \tag{2.9}$$

$$\mathbf{Y}_{\text{Filter}} = \sum_{i=1}^{k} \mathbf{Y}_{\text{SubFilter},i} \tag{2.10}$$

The success rate (i.e., performance yield) is evaluated with passing criteria. Under the assumption that the wafer has been trimmed so that the wafer variation matches chip variation, the largest f_0 variation slope 0.48 MHz/mm measured in Figure 2-8 represents the worst-case scenario on the wafer. For a 2 mm by 2 mm chip, the largest variation occurs when the slope is in the diagonal of the square (Figure 2-8). The largest f_0 variation on a single chip is around 900 kHz. Thus the maximum value for the frequency center shift Δf_{0c} is ± 450 kHz. All filters on the same elevation will have same geometrical variation. With the 7 level elevations in the 4×4 filter array, the largest f_0 interval will be 140 kHz. This variation is large compared to the deviation of the other filter parameters (BW, IL, OBR). Therefore, the target for ESES calibration is healing the f_0 deviation.

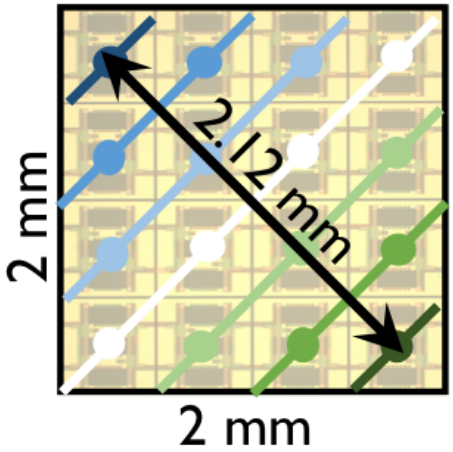


Figure 2-8 A 4×4 sub-filter array on a 2 mm by 2 mm die with center frequency pseudo-variation.

As shown in Table 2-5, the tolerance of the center frequency is set to be ± 20 kHz, which is 3.5 times less than the f_0 interval of 140 kHz and 22.5 times less than the center shift Δf_{0c}. In the center frequency target, the center shift is reflected in the range of targets. In order to cover the wafer level variation, the center frequency for the chip should be able to meet a tuning range equal to the variation.

Table 2-5 Targets for success rate in Monte Carlo simulation.

	f_0 (MHz)	BW (MHz)	IL (dB)	OBR (dB)
Target	$1158 + (-0.45{:}\,0.02{:}\,0.45)$	2.75	< 2.91 dB	> 20 dB
Tolerance	± 0.020	± 0.1	–	–

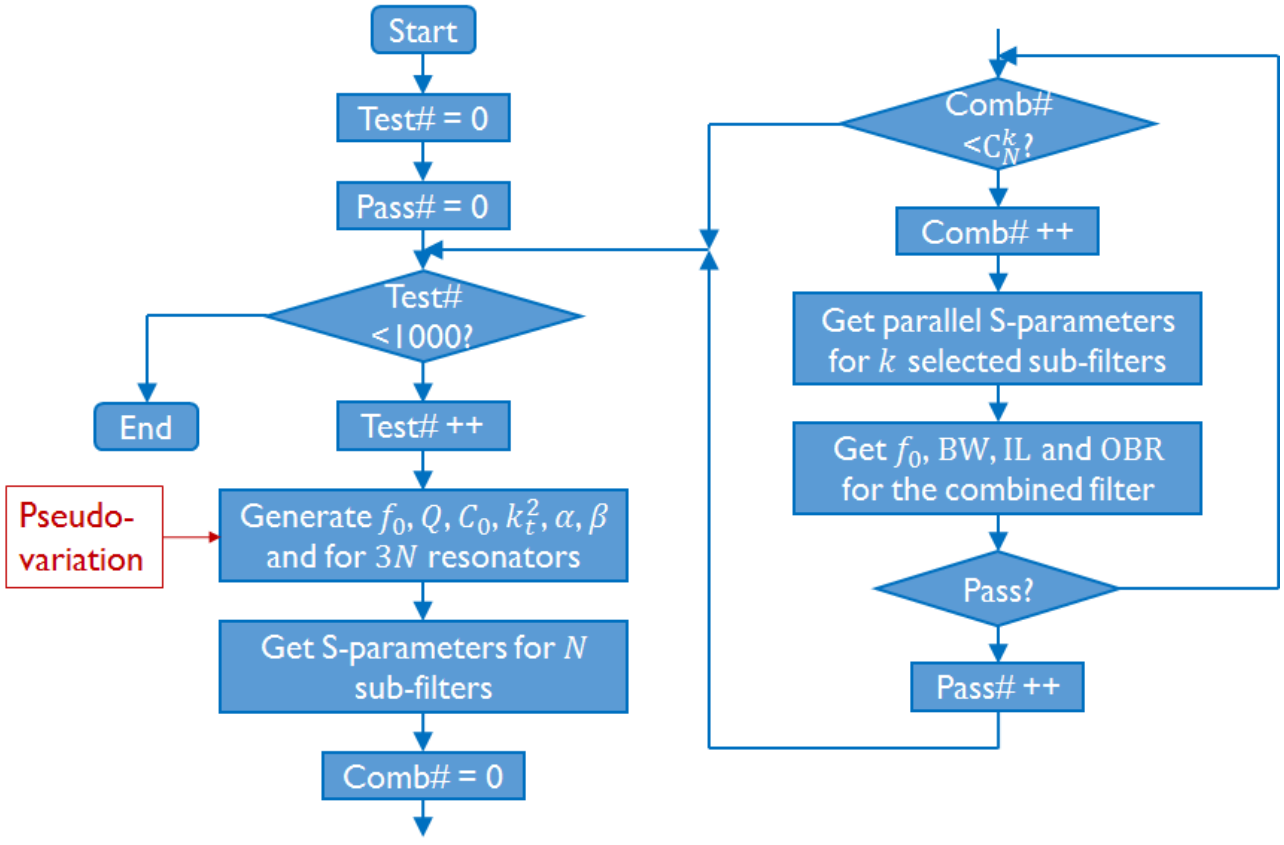
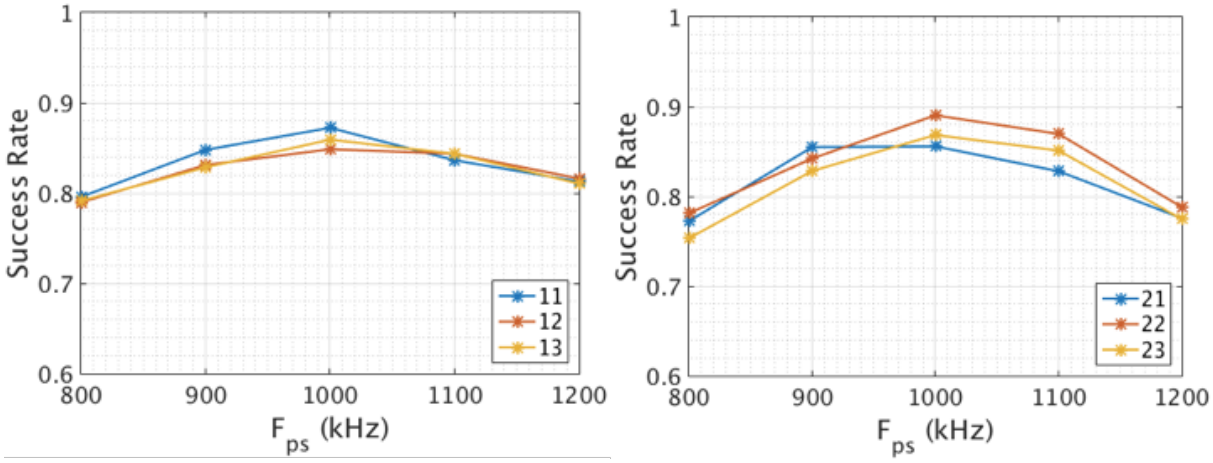


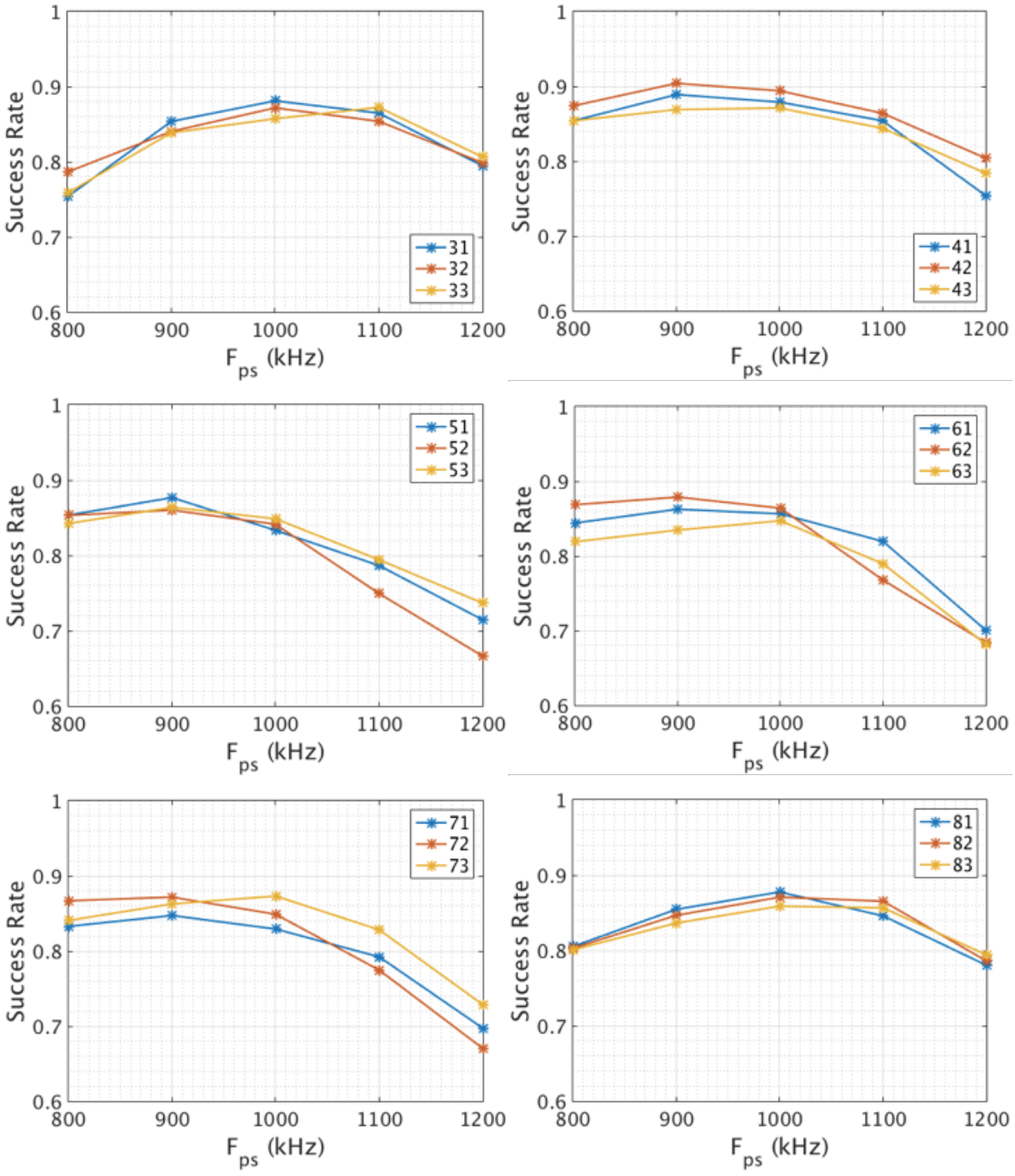
Figure 2-9 Flow chart for Monte Carlo Simulation

Figure 2-9 shows the flow chart for Monte Carlo simulation. First, the resonator parameters are generated from the statistical model. After calculating the lumped circuit model parameters, the resonator s parameters are reached. Cascading three resonator transmission matrices results in a filter transmission matrix. With all N sub-filters calculated, all C_N^k combinations of filter parameters are achieved through adding up the k Y parameters. For each combination, the four filter parameters are evaluated using the passing criteria until one combination passes or all combinations have been tried out. After running 100 tests, the success rate for the filters can be calculated by dividing the successful number of tests by 1000. Since for each set of tests, a different pseudo-variation array is inserted, the success rate can be used to evaluate the pseudo-variation effect in improving success rate. By selecting the pseudo-variation with the highest success rate, the pseudo-variation array is optimized.

2.2.5 Optimization of pseudo-variation sequence

From the discussion in the previous section, the success rate of a pseudo-variation layout depends on the pseudo-range F_{ps}, the f_0 interval, and the rotation. The multi-parameter optimization problem is solved in this work by sweeping the 6 pseudo-ranges F_{ps}, the 30 rotations and the 35 interval combinations to find the best parameter set. Figure 2-10 shows the success rate at each rotation with F_{ps} from 900 to 1300 kHz. Each point is the best success rate among all interval combinations.




Success Rate
F ps (kHz)
31
32
33
41
42
43
51
52
53
61
62
63
71
72
73
81
82
83

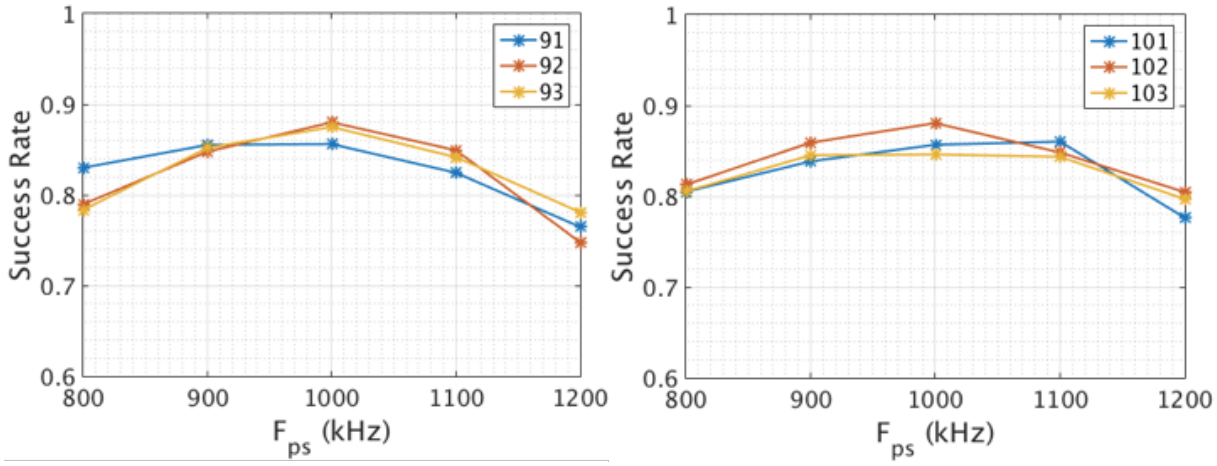
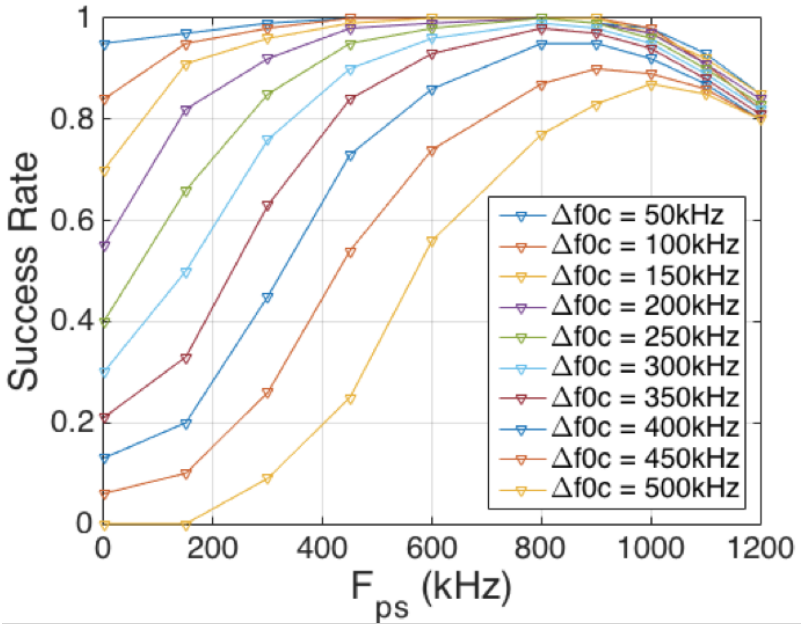


Figure 2-10 Success rate at each rotation with F_{ps} from 800 to 1200 kHz. Table 2-3 and figure 2-6 define the rotations specified in the legends.

The highest success rate peaks at a pseudo-range of 900 kHz with rotation 42 (Figure 2-11b) and an even interval (Figure 2-11c). The best success rate for each rotation vs. F_{ps} peaks most often in even interval cases. Figure 2-11a shows the yield rate performance for this layout configuration at different F_{ps} and different Δf_{0c}. As the centershift increases, the center frequency target is more difficult to meet. As F_{ps} increases, the success rate first increases. This is because the range of combined center frequency increases. As F_{ps} further goes up, the success rate drops due to more filter failures in bandwidth and passing band ripples.



(a)

f_0	f_1	f_{-1}	f_0
f_{-1}	f_{-2}	f_2	f_1
f_1	f_2	f_{-2}	f_{-1}
f_0	f_{-1}	f_1	f_0

(b)

Δf_{-2}	Δf_{-1}	Δf_0	Δf_1	Δf_2
$-\frac{F_{ps}}{2}$	$-\frac{F_{ps}}{4}$	0	$\frac{F_{ps}}{4}$	$\frac{F_{ps}}{2}$

(c)

Figure 2-11 (a) Success rate at different Δf_{0c} for ESES sub-filter array with (b) layout rotation 42 and (c) even interval.

3 ESES Filter Array Implementation and Measurement

3.1 Finger width modulation of resonator center frequency

The center frequency of a resonator is determined by the mass density ρ, Young's modulus E and finger width W. This is valid if the mass loading effect of metal electrodes are not taken into consideration. In the device of study, the finger eleectrodes are made of a molybdenum thin film. The density of molybdenum is larger than AlN, increasing the effective density of the device.

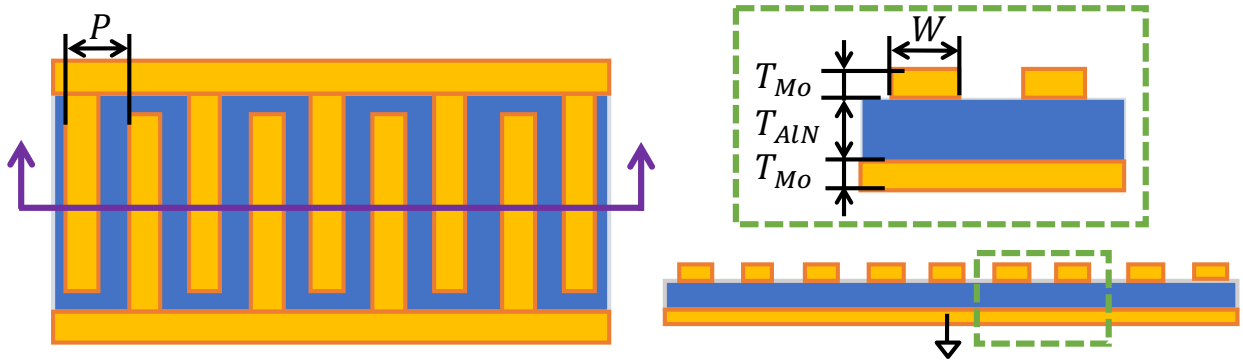


Figure 3-1 Loading effect of metal fingers on AlN resonator.

For the device illustrated in Figure 3-1, the effective density and effective Young's modulus are:

$$\rho_{eff} = \frac{T_{AlN}\rho_{AlN} + T_{Mo}\rho_{Mo} + \frac{W}{P}T_{Mo}\rho_{Mo}}{T_{AlN} + T_{Mo} + \frac{W}{P}T_{Mo}} \tag{3.1}$$

$$E_{eff} = \frac{T_{AlN}E_{AlN} + T_{Mo}E_{Mo} + \frac{W}{P}T_{Mo}E_{Mo}}{T_{AlN} + T_{Mo} + \frac{W}{P}T_{Mo}} \tag{3.2}$$

The effective center frequency is determined by ρ_{eff} and E_{eff}.

$$f_{0eff} = \frac{1}{2P}\sqrt{\frac{E_{eff}}{\rho_{eff}}} \tag{3.3}$$

Therefore, the effective center frequency f_{0eff} should decrease as finger width increases if mass loading is the only factor affecting center frequency. Since the effective density model is only a simplified model of the device, it omits geometrical effects. And since the increased finger width is placed at

different phases of the wavelength, its incremental effect on f_0 is not uniform. Also, increasing W simultaneously adds more electric field stimulus, resulting in higher propagation velocity and tends to increase f_0.

In order to get the relation between finger width (W) and resonator center frequency f_0, resonator responses with different widths were simulated using 2D finite-element analysis to get each f_0 (Figure 3-2). From the simulation result in Figure 3-2c, when filter finger width is less than half finger pitch P, the effect of stimuli dominates the center frequency shift. As finger width gets larger than half finger width, the effect of mass loading dominates the center frequency shift.

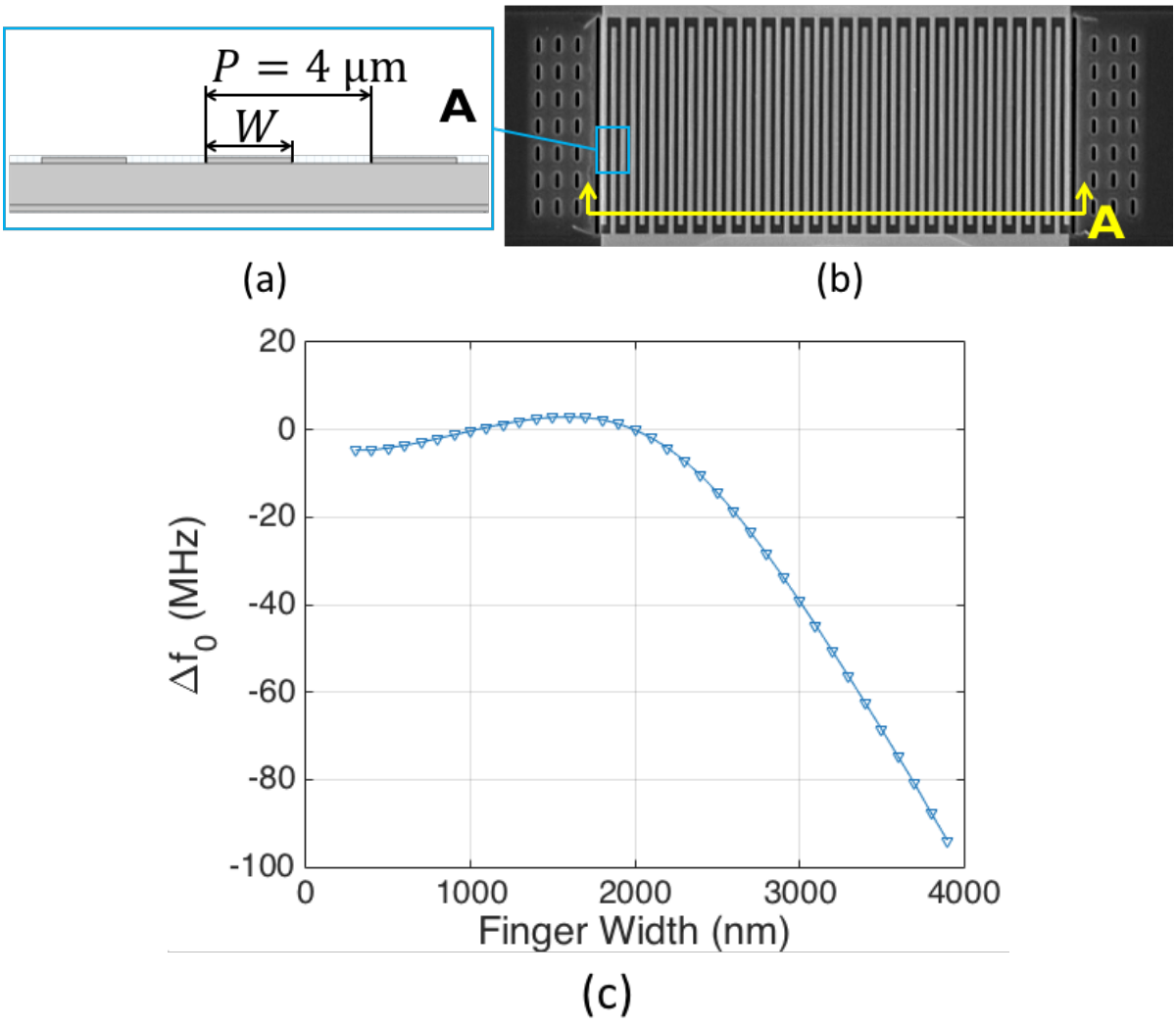
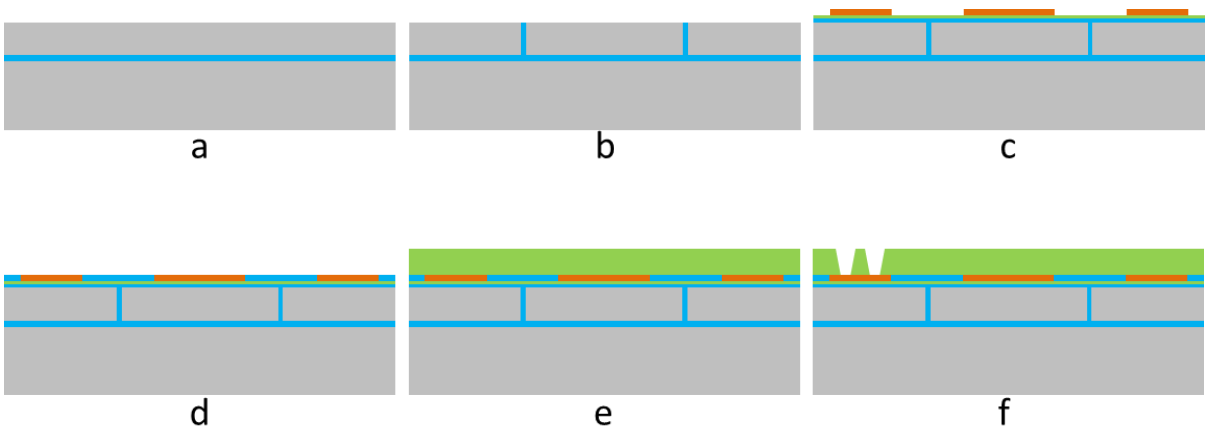


Figure 3-2 (a) 2D finite-element model of AlN resonator. (b) SEM of AlN resonator fingers. (c) Simulated frequency shift vs. layout finger width.

3.2 Fine frequency tuning filter fabrication and measurement

3.2.1 MEMS only fabrication process flow

In the MEMS only process, resonators and filters were fabricated as shown in Figure 3-3. Starting from a stack of 5 µm of Si (device layer of Si) on 1 µm of SiO_2, the process is initiated by defining the isolation trench, which will confine the released areas when the device layer of Si is etched later in the process. Next, 300 nm of SiO_2 is deposited, followed by 50 nm of AlN and then 150 nm of molybdenum, which is patterned to form the bottom electrode of the device. The surface then undergoes planarization, which is very useful for ensuring that devices do not break upon release. Next, 1 µm of AlN is deposited, and vias are etched through the AlN. Next, 150 nm of molybdenum is deposited and patterned to form the top electrodes, connecting to the bottom electrodes through the vias. The surface is then covered with a 500 nm passivation layer of SiO_2. Release holes are then etched down to the device layer of silicon. Lastly, the devices are released from the silicon using a XeF_2 etch followed by a vapor hydrofluoric acid etch to remove residual oxide. The layout of resonators to be fabricated in the MEMS-only process at IME has been automated with a custom script written for use with Cadence at CMU.



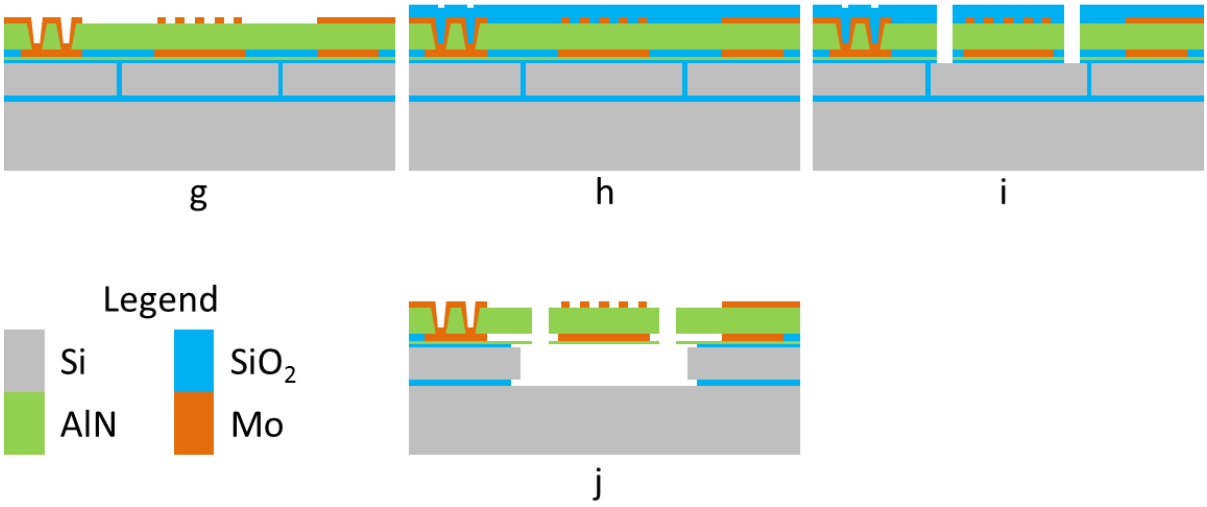
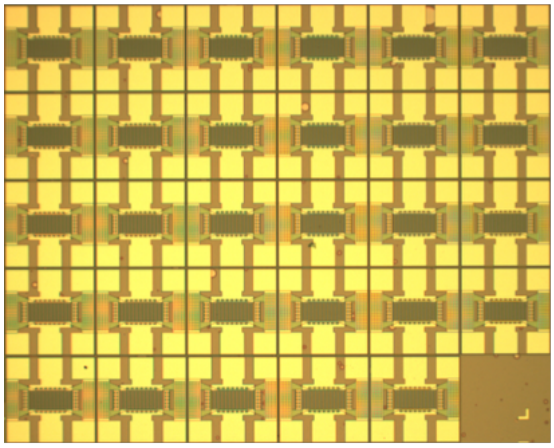


Figure 3-3 MEMS only process flow: (a) Initial wafer. (b) Formation of isolation trench. (c) Deposition and patterning of bottom molybdenum. (d) Planarization. (e) Deposition of aluminum nitride. (f) Etching of vias. (g) Deposition and patterning of top molybdenum. (h) Deposition of silicon dioxide passivation. (i) Etching of release holes. (j) Xenon difluoride release and vapor hydrofluoric acid etch.

3.2.2 Fine finger width modulation test design and measurement

To test the effectiveness of center frequency f_0 tuning using finger width modulation, resonators with arithmetically increasing finger widths are designed for testing. Since frequency shift exists intrinsically between filters at different locations due to systematic errors, it is necessary to compensate for the process-variation-induced frequency profile for each test chip. Figure 3-4 shows the layout for the test chip, where each cell represents a filter with the labeled finger width. Three resonators with the same finger width are placed at corners of the chip to get the f_0 profile plane, where each point on the plane represents the intrinsic f_0 shift at that location. To compensate for linear process variation, the f_0 shift is subtracted from the measured center frequency.

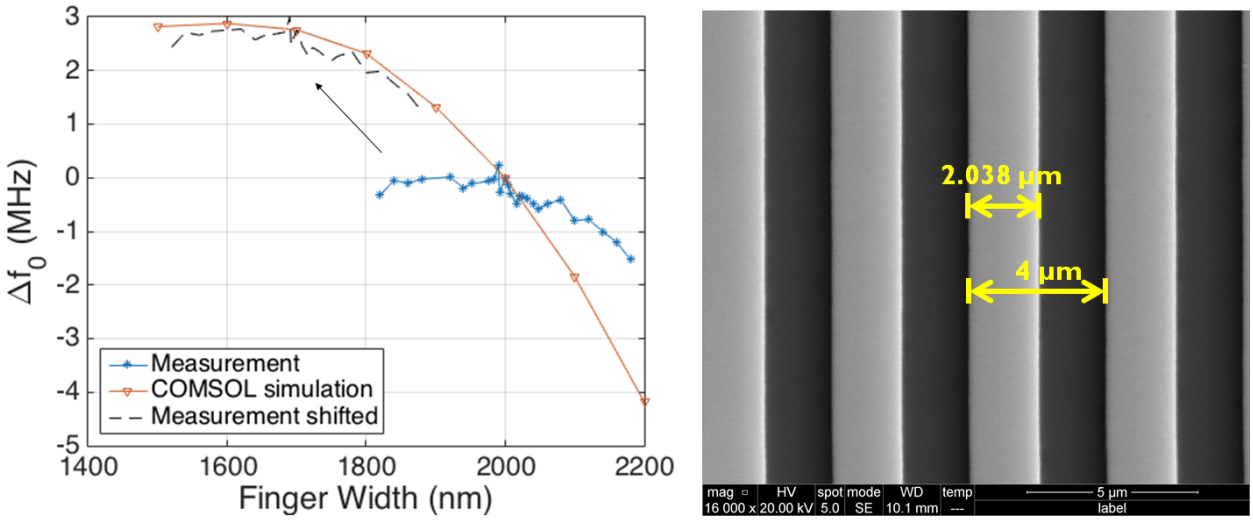


2000	1820	1840	1860	1880	2000
1900	1920	1940	1952	1976	1984
1992	2004	2000	2032	2016	2020
2024	2040	2048	2060	2080	2100
2000	2120	2140	2160	2180	

(a) (b)

Figure 3-4 Test chip for fine frequency shift using finger width modulation

The measured and simulated frequency shifts Δf_0 are shown in Figure 3-5a. The measured Δf_0 shows less sensitivity to finger width than in the simulation. Due to the nonlinearity in Δf_0, the intended tuning range is affected adversely. From the trend of the frequency shift, it matches the simulated frequency shift at a smaller finger width. In real fabrication, the actual finger width may be shifted to a smaller value from the designed width. Shown in Figure 3-5b is a typical SEM image taken from the top of the filter fingers designed to be 2 µm wide with a 4 µm pitch. The finger pitch is designed to be 4 µm. Since pitch in fabrication is determined by mask grid, it is a controlled value. Therefore, by comparing the finger width with the pitch, the actual finger width and be measured. From the image, the actual finger width is larger than the gap, which means the actual finger width is larger than 2 µm. This adverse to the assumption inferred from the finger width modulation trend in Figure 3-5a. To get a better understanding of the finger width relation with center frequency shift, it is desirable to have test structures with larger finger width change range. Also, in choosing the finger width for the fine frequency adjustment applications, to avoid this problem, finger width in future layouts should center at the more sensitive region in the actual fabrication. In this device of interest, all layout finger widths should be larger than 2 µm.



(a) (b)

Figure 3-5 (a) Center frequency shift vs. finger width adjustment (b) SEM image of resonator fingers designed to be 2 µm with a 4 µm pitch

3.2.3 ESES reconfigurable filter design and measurement

Three ESES filter arrays have been designed and fabricated in the same process. Each sub-filter is measured separately. Summing the Y parameters of selected sub-filters combines their filter responses. Under the assumption that trimming is implemented, the largest f_0 variation across wafer is the center-shift $\pm\Delta f_{0c}$. Therefore each filter cell needs to cover a frequency range up to $\pm\Delta f_{0c}$. The filter cell needs to pass all frequency specifications within the range $[f_{0\text{mean}} - \Delta f_{0c}, f_{0\text{mean}} + \Delta f_{0c}]$, together with all the performance specifications in Table 2-5. Due to the nonlinearity in the f_0 shift, the measured F_{ps} is only 500 kHz rather than the designed 900 kHz. Figure 3-6 compares the success rate between measurement and the simulation with the actual F_{ps}. Design 3, with the largest F_{ps} shows the highest success rate. The simulation matches measurement far better than 10% at most points, so as to validate the f_0 plane model and the ESES reconfigurable filter design.

Table 3-1 Design 1-3 finger widths and actual F_{ps}.

Design	1	2	3
Rotation	–	42	42
W_{-2}(nm)	2000	1976	1952
W_{-1}(nm)	2000	1992	1984
W_0(nm)	2000	2000	2000
W_1(nm)	2000	2008	1984
W_2(nm)	2000	2024	2048
F_{ps}(kHz)	0	140	500

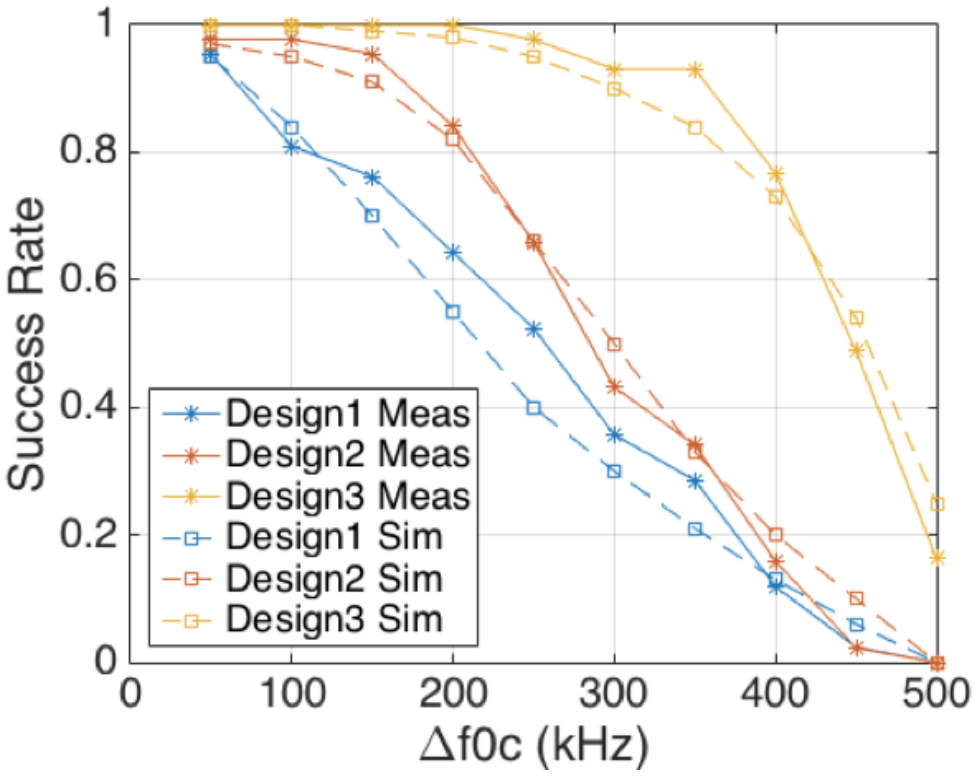


Figure 3-6 Measured and simulated filter success rate.

4 Reconfigurable receiver frontend design

4.1 Systematic specifications

4.1.1 Communication standards

For a receiver to function in a crowded communication spectrum, specific specs need to be met to ensure signal quality. Since the filter in this thesis functions at around 1 GHz, the Long-Term Evolution Evolved Universal Terrestrial Radio Access (LTE E-UTRA) band 8 (a.k.a. E-GSM) with a center frequency at 900 MHz with a channel bandwidth of 3 MHz is used as an example (Table 4-1).

Table 4-1 LTE E-UTRA specifications

Center Frequency	900 MHz
Channel Bandwidth	3 MHz
Modulation	QPSK 1/3
REFSENS	−102.5 dBm
SINR	−1 dB
Implementation margin IM	2.5 dB
Own signal power above REFSENS	6 dB
Power of Interferer	−46 dBm (in-band), −31 dBm (out-of-band)
Bandwidth of Interferer	3 MHz

LTE defines an NF requirement of 9 dB for the User Equipment (UE), the same as the 3G Universal Mobile Telecommunication System (UMTS). This is somewhat higher than the NF of a state-of-the-art receiver, which would be in the region of 5–6 dB, with typically about 2.5 dB antenna filter insertion loss and an NF for the receiver integrated circuit of 3 dB or less. Thus, a practical 3–4 dB margin is allowed. The eNodeB requirement is for an NF of 5 dB.

As for the linearity requirement, the third-order intermodulation requirement is the hardest linearity specification to achieve. Signal requirements dictate the in-band and out-of-band intermodulation specifications. The SNR requirement plus implementation margin is assumed to be 1.5 dB. The wanted signal is 6 dB above REFSENS (i.e., at −96.5 dBm). So the IM3 noise plus the thermal noise combines to up to 6 dB margin. Therefore, the IM3 products must be 1.26 dB below the maximum tolerable noise floor. Thus, $P_{IMD3,in} = -96.5 - 1.5 - 1.26 = -99.26$ dBm and $\text{IIP3} = [3\times(-46) + 99.26]/2 = -19.37$ dBm. Similar methods can be implemented to calculate the out-of-band blocking requirements and $\text{IIP3}_{\text{OOB}} = [3\times(-31) + 99.26]/2 = -1.63$ dBm.

The interference and noise standards from communication links set the specifications for the receiver frontend. High accuracy is needed for the center frequency of the channel filter. With a bandwidth of 3 MHz, the center frequency accuracy within less than 1% of the bandwidth is desired in order not to incorporate out-of-channel interferers. The SES method introduced in chapter 2 can achieve this accuracy. In order to implement ESES, switching is needed to select the wanted sub-filters and shut down the unwanted ones. A low-loss switch mechanism is required to minimize loss on the signal path.

4.1.2 Switching method

Proper design of the switching scheme selects the sub-filters with the desired center frequency and keeps the undesired sub-filters isolated. In previous literature, a switch matrix incorporating CMOS switch transistors at the input and output port of the two-port resonator filter was reported [4]. In this design, there is a tradeoff between the on impedance of the switches and the parasitic shunt capacitance. Series parasitic resistance on the signal path and shunt parasitic capacitance at the two ports contribute to loading mismatches. For a CMOS transistor gate, increasing area lowers the on resistance R_{on}, but also increases the shunt capacitance C_{gs}. This is problematic for the AlN two-port resonators. For example, for a resonator with motional resistance $R_m = 3\ \Omega$, the intrinsic capacitance is $C_0 \approx 450$ fF. In the 28 nm Samsung technology, to reach an R_{on} equal to the motional impedance would result in a gate capacitance

of 150 fF, which is close to the value of C_0, causing significant mismatch of the loading impedance. Moreover, each switch requires a bumping pad to connect the MEMS to CMOS structure, which introduces more shunt capacitor parasitics. In [4], an IL around 8 dB is observed, where the relatively poor value is due to parasitics. Since the IL in the first stage of the receiver adds directly to the NF of the system, it is desired to minimize the number of switches on signal path.

To avoid using switches on the signal paths, this work explores use of active circuit components that are already in a conventional receiver to turn the filter on and off. In an RF receiver frontend, after channel selection through the filter, the input signal is amplified using an LNA to improve the receiver NF performance. As an active component, the LNA can be turned on or off by controlling the bias current. The LNA input impedance can be designed to be the necessary sub-filter termination impedance for its on-state, while the off-state impedance is equivalent to an open circuit. This impedance characteristic is equivalent to a switch. In this proposed work, the LNA is separated into several sub-LNAs, forming a sub-branch together with the sub-filter, shown in Figure 4-1, where each sub-LNA functions as an amplifier and a switch.

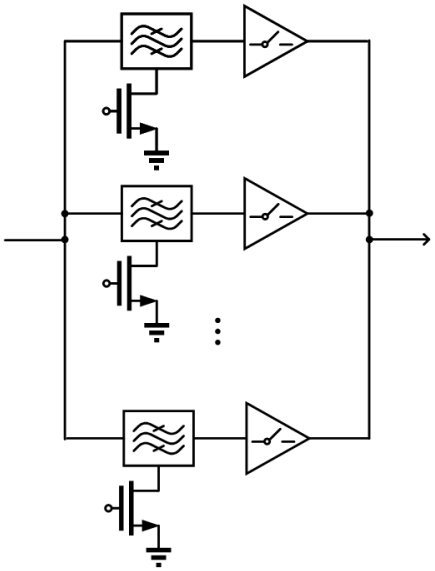


Figure 4-1 Switching scheme using sub-LNAs and ground switches

Due to the existence of the intrinsic capacitance of the sub-filters between their top and bottom electrodes, the ability to disconnect the bottom electrode from the RF ground by adding a CMOS transistor "ground switch" will improve isolation when the sub-filter is in its off state. The second design goal of the ground switch is to ensure that the parallel array with k on-state branches and $N-k$ off-state branches is comparable to k stand-alone on-state branches. During the design, the proper transistor size of the ground switch enables the S11 to be well below −10 dB and the S21 to be flat across the pass-band. Cadence simulation of the sub-filter system with two parallel sub-filter branches, and only one on-state branch provides preliminary verification of the concept by comparing the performance of the sub-filter array with the on/off states of one single sub-filter branch. The S-parameters at the center frequency are shown in Table 4-2. A 30 fF parasitic capacitance to represent the pad is added in simulation. In the three states, the input and output ports are set to have an impedance of 50 Ω. The simulation results show a 6400 dB isolation between on and off state. The hybrid branch presents similar performance to the single on state.

Table 4-2 Simulated S-parameter of ground switching

	On-state	Off-state	On/Off-state parallel
$S11\ (dB)\ @\ f_0$	−13.9	−0.1	−13.5
$S21\ (dB)\ @\ f_0$	−2.06	−6400	−2.09

4.1.3 Proposed system

Conventional communication channel design assumes the 50 Ω impedance matching criteria. The input impedance of the frontend needs to be the same for all combinations selected in the SES array. Also, with the noise figure requirement, the input LNA needs to trade-off between matching and low noise criteria. The gain and noise of the LNA are usually related. With a larger gain, the input referred noise figure of the following stages will have less contribution to the overall noise figure. Since the minimum

input signal is small compared to the resolution of the ADC, the frontend needs to provide a large gain to pump up from low signal power levels. However, the frontend would easily get saturated in the presence of a large signal or a larger interference. Therefore, a solution is to enlarge the dynamic range of the frontend through a variable gain amplifier. The linearity is usually another design factor that needs optimization together with gain and noise figure. In the case of AlN resonator filters, the out-of-band rejection of the filter transfer function can suppress the interferer power, and therefore loosen the requirement for linearity. The receiver frontend architecture proposed in Figure 1-6 considers all of these requirements.

In most RF frontend design, the trade-off among matching, noise figure, voltage, power and linearity constraints the optimization of circuit performance. The significance of each boundary varies with different applications. In the design in this thesis, the frontend follows a high-Q RF channel selection filter. The high out-of-channel rejection suppresses any in-band and out-of-band interferers before entering the LNA, the first frontend active stage. Therefore, this approach relieves the conventional IIP3 requirement.

Taking the AlN two-port resonator filter as an example, the power rejection at the adjacent channel to the desired signal channel has a nominal value of 20 dB, meaning that the two intermodulation interferers are suppressed by 20 dB each. The resultant third-order intermodulation component P_{IM3} in the desired signal channel is 60 dB less, $P'_{IM3} = P_{IM3} - 20\,\mathrm{dB}$. Therefore the IIP3 of the receiver front end is relieved by 30 dB, $\mathrm{IIP3} = [3P_{int} - P'_{IM3}]/2$. With the relieved linearity requirement, the other performance targets are better optimized with less constraints, as reflected in the LNA topology and parameter selection, discussed next.

4.2 LNA design

4.2.1 LNA topology

Since the 50 Ω antenna resistance is set, each selected parallel sub-LNA has a loading impedance of $k\times50\ \Omega$ on the input side. Due to the symmetry characteristic of the filter, the output node should be terminated with the same impedance, which is the input impedance of LNA. As the sub-LNAs directly follow the filter, each sub-LNA needs to provide an input resistance of $R_0 \approx k\times50\ \Omega$. For most narrowband applications, the matching network incorporates inductors. The value of the input resistance is proportional to the matching inductor. In the design in this thesis, for each sub-LNA the input impedance is k times 50 Ω, and we have a total of N sub-LNAs on chip. Therefore, an inductor for each LNA would be area consuming leading to consideration of inductor-less wideband LNA topologies.

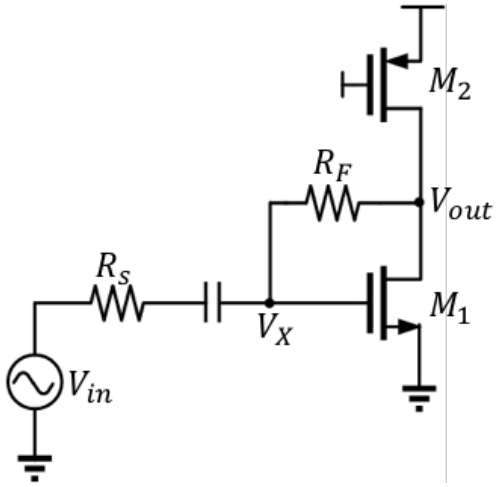


Figure 4-2 Resistive feedback common source stage

The classical approach to satisfy the required impedance matching at the input of an amplifier is to employ negative feedback (Figure 4-2). Because RF is simply in series with a current source and M1 appears as a diode connected device, the input resistance is simplified as

$$R_{in} = \frac{1}{g_{m1}} \tag{4.1}$$

Changing the transconductance of the input transistor adjusts the LNA input impedance. The small-signal drain current of M1, $g_{m1}V_X$, entirely flows through R_F, generating a voltage drop of $g_{m1}V_X R_F$. Hence the voltage gain is

$$A_v = \frac{V_{out}}{V_{in}} = \frac{1}{2}\left(1 - \frac{R_F}{R_s}\right) \tag{4.2}$$

To achieve high gain, it can be chosen that $R_F \gg R_s$, and the voltage gain is approximately $A_v = -\frac{R_F}{2R_s}$. The problem with this topology is that, under the matching condition, the noise figure of this topology will exceed 3 dB. The input transistor M1, with an output impedance of $\frac{1}{2}(R_F + R_s)$, has output-referred noise of

$$V_{nM1,out}^2 = 4kT\gamma g_{m1}\frac{(R_F+R_S)^2}{4}. \tag{4.3}$$

The noise figure due to M1 under matching condition is then

$$F_{M1} = 1 + \frac{V_{nM1,out}^2}{A_v^2 \cdot 4kTR_S} \approx 1 + \gamma. \tag{4.4}$$

This number already exceeds 3 dB. Increasing transconduction g_{m1} can lower NF, but then the matching condition is not met.

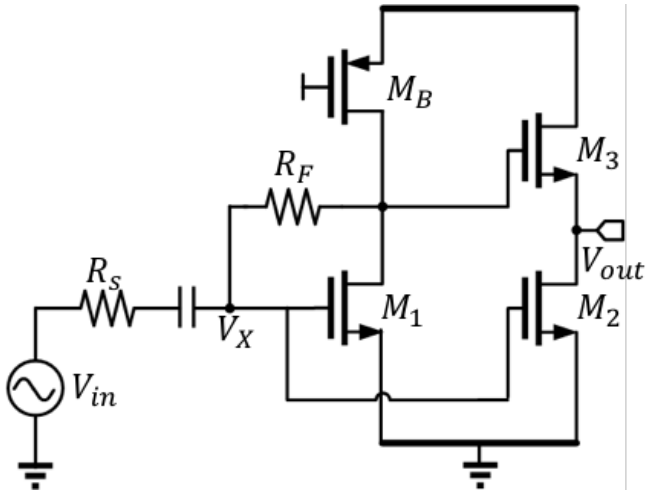


Figure 4-3 Resistive feedback noise canceling LNA

A noise cancellation method will decouple the optimal noise condition from the matching condition and lower the noise figure [23]. The main principle is to eliminate the noise contributed by the input transistor, without degrading the signal (Figure 4-3). The first stage is the resistive feedback common source transistor to meet the impedance matching criteria. The second stage provides signal amplification and noise cancellation. As shown in Figure 4-3, the signal passes through two inverting gain paths, resulting in signals of same phase at the output, which are summed to be the output signal. The noise source of the transistor generates a current through the source resistor and the feedback resistor. The noise at nodes X and Y are then of the same phase. After the second gain stage, the noise phase is shifted by 180°. Designing the gain of the second stage so that the noise amplitudes of the two paths are the same at Y, cancels the noise at the output. That criterion sets the voltage gain of the second stage,

$$A_{v2} = \frac{1}{2}\frac{V_{out}}{V_X} = -\frac{1}{2}\left(1 + \frac{R_F}{R_s}\right). \tag{4.5}$$

Thus, the overall gain for the two stages is

$$A_v = A_{v1} + A_{v2} = -\frac{R_F}{R_s}. \tag{4.6}$$

Under the noise cancellation condition, the main noise contributors are R_F and the second gain stage. The resulting noise figure is

$$F = 1 + \frac{R_S}{R_F} + \frac{\gamma}{(g_{m2}+g_{m3})R_s}\left(1 + \frac{R_s}{R_F}\right)^2. \tag{4.7}$$

To lower the noise contribution from the feedback resistance, one could increase R_F. However, increasing R_F invalidates the assumption that the input stage is a diode and increases the effective input resistance. This constraint limits the minimum noise figure and maximum gain achievable for this topology.

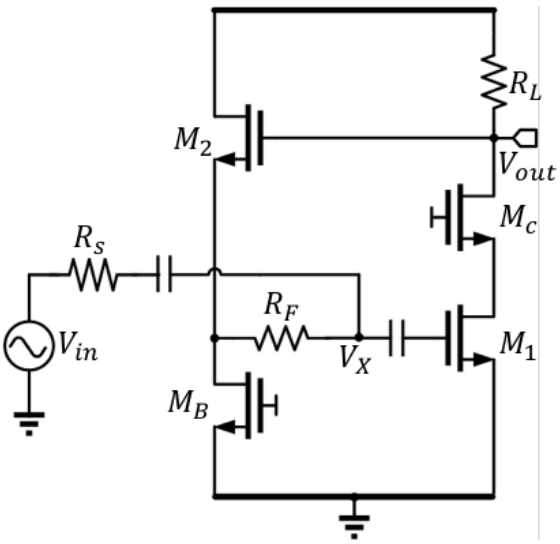


Figure 4-4 Active feedback LNA

In further work in the literature, negative feedback is implemented using the common-drain stage in Figure 4-4 [23]. In this topology, M2 serves as the input matching stage. The second stage of M1 is the main amplifier stage, providing a gain of $A_V = -g_{m1}R_L$. The second stage also provides gain boosting for the common drain transistor that boosts the effective input transconductance. Since the input impedance is determined by both g_{m1} and g_{m2}, there are two degrees of freedom to control the input impedance and the noise figure. This topology effectively decouples the matching and the noise figure. The drawback for this topology is an increase in power consumption due to the added stage. Therefore, the design requires optimization among the gain, NF and power consumption.

4.2.2 Input impedance matching

In the topology in Figure 4-4, input matching occurs when

$$g_{m2} = \frac{1}{R_s(1+|A_V|)-R_F}. \tag{4.8}$$

In this formula, R_s is the source impedance and the voltage gain is $|A_V| = g_{m1}R_L$. Here the input matching stage is constructed with an active g_{m2} in series with R_F. The value of R_F is constrained by

$R_s(1 + |A_V|)$ so that the g_{m2} stays positive. Obviously, a larger R_f requires a larger g_{m2}, and thus leads to a higher power consumption.

4.2.3 Noise figure

The noise factor of the LNA is given by a sum of contributions. From simple small signal analysis, the noise figure is found as:

$$F = F_{R_S} + F_{M1} + F_{M2} + F_{MBias} + F_{R_L} + F_{R_F}$$

$$= 1 + \frac{\gamma_1}{g_{m1}R_s}\left(1 + \frac{g_{m2}R_s}{1 + g_{m2}R_F}\right)^2 + \frac{\gamma_2 g_{m2}R_s}{(1 + g_{m2}R_F)^2} +$$

$$\frac{\gamma_{Bias}g_{mBias}R_s}{(1 + g_{m2}R_F)^2} + \frac{[1 + g_{m2}(R_S + R_F)]^2}{(1 + g_{m2}R_F)^2 g_{m1}^2 R_L R_s} + \frac{g_{m2}^2 R_s R_F}{(1 + g_{m2}R_F)^2}$$

(4.9)

A more interpretable expression can be reached when the matching criterion is imposed:

$$F = F_{R_S} + F_{M1} + F_{M2} + F_{MBias} + F_{R_L} + F_{R_F}$$

$$= 1 + \frac{\gamma_1}{g_{m1}R_s}\left[\frac{2 + |A_V|}{1 + |A_V|}\right]^2 + \frac{\gamma_2}{1 + A_V}\left[1 - \frac{R_F}{R_S(1 + |A_V|)}\right]$$

$$+\gamma_{Bias}g_{mBias}R_S\left[1 - \frac{R_F}{R_S(1 + |A_V|)}\right]^2 + \frac{1}{g_{m1}R_S|A_V|} + \frac{R_F}{R_S(1 + |A_V|)^2}$$

(4.10)

The dominant components in the expression arise from the contribution of input device M1. This noise component can be scaled down by increasing g_{m1}. With a minimum tolerable overdrive voltage, increasing g_{m1} means increasing current, I_1, through M1. The gain factor $|A_V|$ can be kept the same by inversely scaling R_L. Another factor contributing to noise figure is the feedback resistor R_F. When R_F increases, F_{R_F} is increased. However, the negative signs in the expressions for F_{M2} and F_{MBias} lead to the opposite conclusion. That is, when R_F increases, a larger g_{m2} is needed to meet the matching criterion,

and thus introduces more noise. Therefore, increasing R_F will lead to increased power consumption from M2.

4.2.4 Linearity

Since the circuit contains nonlinear feedback, it is prone to linearity issues. The largest signal swing is at the output node, which controls the nonlinearities of the feedback device. The feedback transistor generates second-order distortion at the circuit input, which propagates linearly to the output. This distortion combines with the fundamental tones at the circuit output via M2 to generate third-order distortion, which propagates linearly to the output. This distortion combines with the fundamental tones at the circuit output via to generate third-order distortion. The IIP3 expression has been calculated through Volterra kernals [24]:

$$\mathrm{IIP3} = \frac{\beta}{\sqrt{\left|\left(\frac{1 + A_V + R_F/R_S}{1 + A_V}\right)\left(\frac{K_{2g_{m2}}}{g_{m2}}\right)^2 - \frac{K_{3g_{m2}}}{g_{m2}}\right|}} \tag{4.11}$$

$$\beta = 4\sqrt{\frac{2}{3}\left|\frac{1 + A_V}{(1 + A_V - R_F/R_S)^3}\right|} \tag{4.12}$$

In this formula, $K_{2g_{m2}}$ and $K_{3g_{m2}}$ are the slope and curvature of g_{m2}:

$$K_{2g_{m2}} = \frac{1}{2} \cdot \frac{\partial^2 i_{DS2}}{\partial v_{GS2}^2}, K_{3g_{m2}} = \frac{1}{6} \cdot \frac{\partial^3 i_{DS2}}{\partial v_{GS2}^3}. \tag{4.13}$$

Observing the formula, it can be seen that increasing R_F will improve IIP3. However, increasing R_F will increase noise figure and more power consumption to meet matching criteria. The optimization of the circuit is analyzed in the next section.

4.2.5 Power optimization

From the analysis, increasing g_{m1} can improve the NF at the cost of power consumption. To further lower the power consumption, a current reuse technique reduces the voltage drop across the load resistor

and at the same time improves the gain, noise performance, and power consumption. Shown in Figure 4-5, a PMOS transistor M1p is added at the input to provide more g_m. Since M1p shares current with M1, no additional power is consumed. Also, since there is no additional voltage drop across R_L, the gain can be increased to $(g_{m1} + g_{m1p})R_L$.

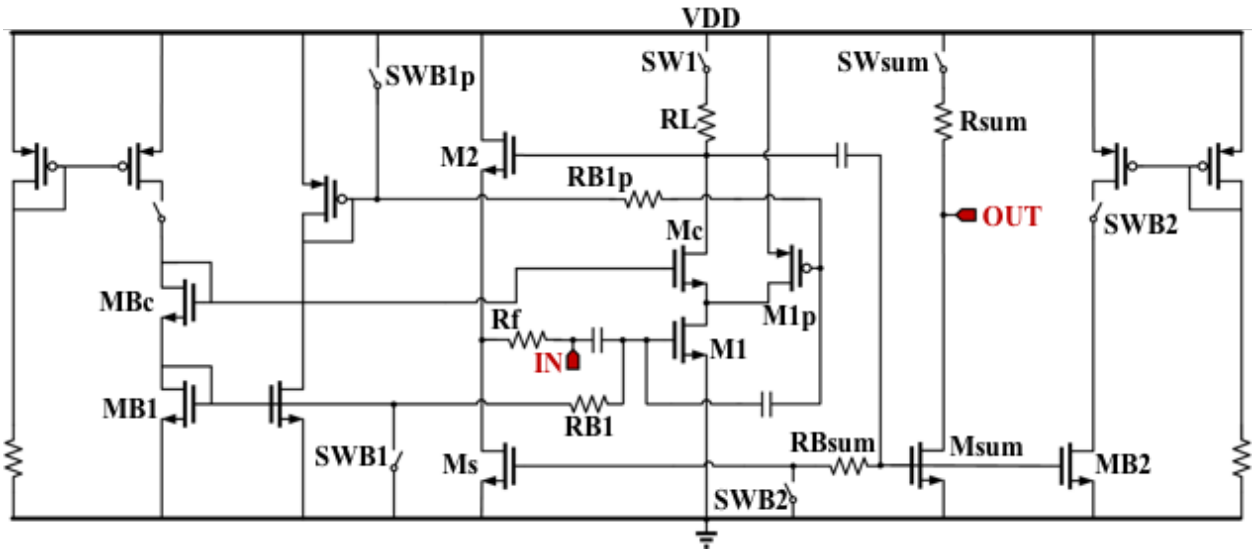


Figure 4-5 Active feedback LNA circuit schematic.

With the current reuse M1p, the g_{m1} terms in the expression of A_V, R_{in} and NF are replaced with $g_{m1} + g_{m1p}$. From the analysis of the noise figure, we can optimize noise and power consumption by sweeping the M1 current I_1 and the feedback resistance R_F while keeping the same overdrive voltage V_{ov} and voltage gain A_V. In this circuit, in order to maximize g_m of M1, M1p and M2, their overdrive voltages were set to 100 mV. No further scaling down is adopted to be conservative on the biasing. Since the bias transistor Mbias contributes more noise with larger g_m, its overdrive voltage is set as 250 mV. A cascade stage Mc is added to avoid oscillation, but is taking up voltage headroom. Therefore, with a 1V voltage supply, the voltage drop across R_L is set as 400 mV. A γ value of 1.2 is used to estimate transistor noise. Using equations (4.8-(4.13), the noise factor, current I_2 and IIP3 values vs. R_F and I_1 are shown in Figure 4-6. The NF is lowered as current I_1 increases, whereas current I_2 and intermodulation intercept

point IIP3 are insensitive to I_1. When R_F increases, the NF and IIP3 are improved, but increased current is drawn through the transistor M2.

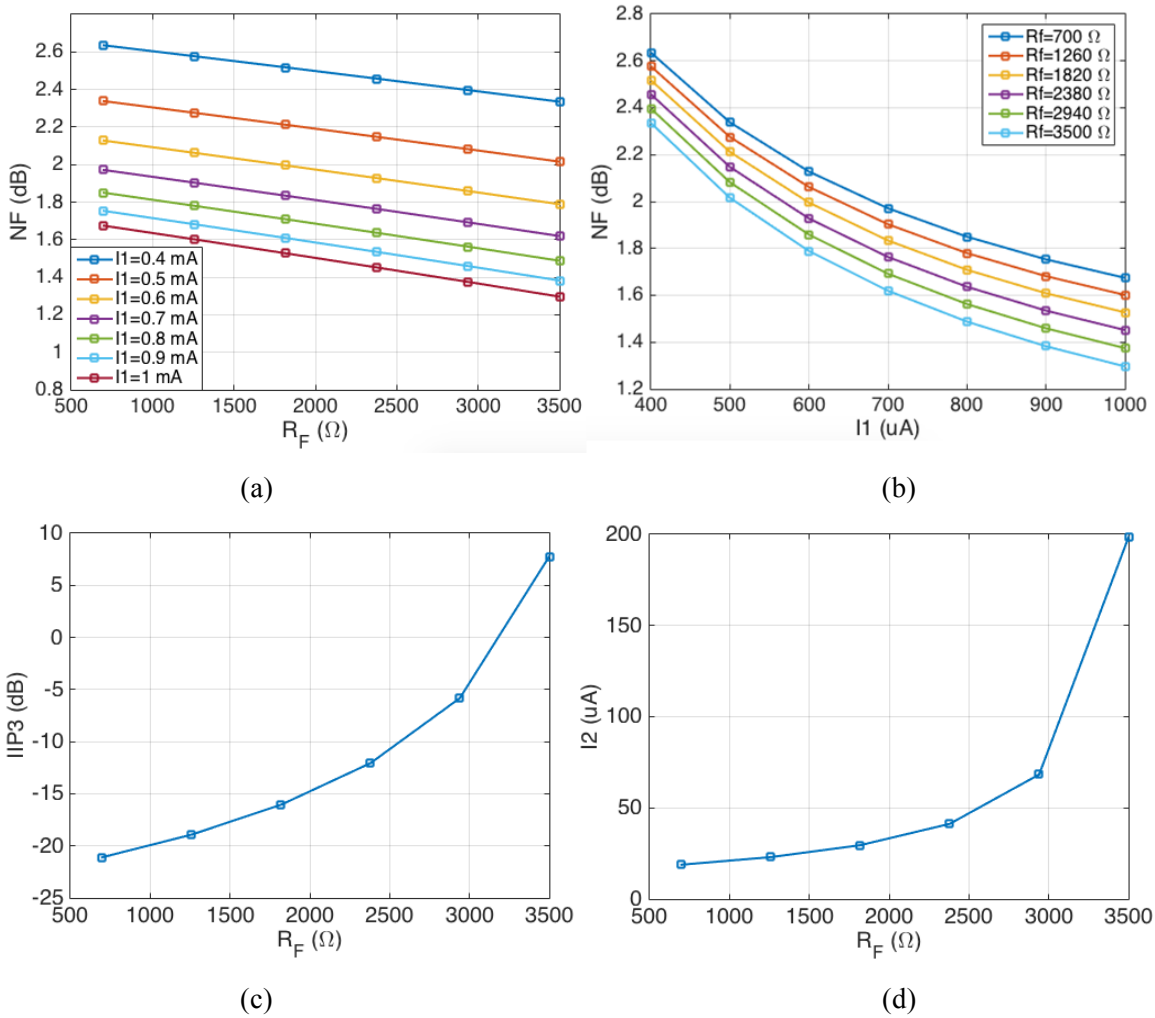


Figure 4-6 LNA design parameter optimization

According to the analysis on the filter's effect on alleviating the system linearity requirement, the IIP3 is a secondary optimization parameter in this circuit. It is then sufficient to optimize based on just NF and total current consumption. Optimization introduces a new parameter $\Delta F/I$ to depict the efficiency of NF improvement by current. Here ΔF is the noise factor subtracted by 2 (i.e. the zero point corresponding to NF = 3 dB). ΔF depicts how much the noise factor is improved from 3 dB. The current I in this formula is the total current summing I_1 and I_2. This parameter shows how much noise factor is improved by consuming additional power. The relation between $\Delta F/I$ and different R_F and I_1 values are shown in

Figure 4-7. The maximum point occurs at $R_F = 420\ \Omega$ and $I_1 = 3.6$ mA, where the NF reaches 1.85 dB. At this point, the IIP3 reaches a value around −2 dBm. Further improving the linearity would require increasing current to have additional power consumption, or require lowering overdrive voltage to affect noise factor. The alleviation of linearity from co-design of the high-Q filter helps the overall circuit design to reach a better optimization point. We therefore use these parameters to build the LNA circuit.

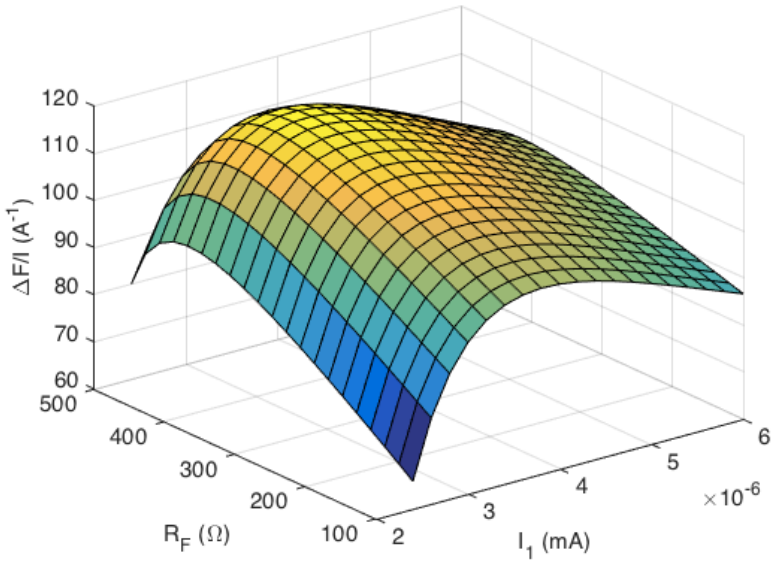


Figure 4-7 LNA design parameter optimization

4.2.6 Switching and summing

A transistor switch in series with the current bias switches the sub-LNA on or off. The impedance at the input and output nodes is taken into special consideration. In its off state, the sub-filter must be loaded by an open circuit (i.e., a high impedance) so that the transimpedance looking into the off-state branch is close to infinity. However, leaving the input node open would result in a floating node and any interference can be amplified and appear at the output node. Therefore, a relatively large resistor R_{B1} (20 kΩ) is inserted between the bias and the input gate. When the current mirror is shut down, the mirror gate is grounded and the input node is grounded at dc through R_{B1}.

The second stage that follows the LNA is a common-source current-summing stage, where the current from all the selected branches flow through the same loading impedance and are summed into an output voltage. With the summing stage, the total output voltage is the linear addition of the output of each branch when performing alone. This summing approach avoids coupling interaction between different branches.

4.2.7 System parasitic optimization

The above analysis is based on the ideal circuit model without necessary routing parasitics from the 3D integration. In the actual implementation, sub-LNAs are spaced apart by around 500 μm from each other. Throughout the chip, to the greatest extent possible, the input and output signal paths are designed to not overlap or interact with DC paths including ground, voltage supply and biasing, since the coupling affects overall performance. There are three main sources of signal degradation from interconnect and device parasitics. First, the parasitics at the input of filters affects the input matching. With a large capacitor to the ground at the input, the effective input impedance would deviate from 50 Ω and result in impedance mismatch, since the antenna impedance is $R_0 = 50\ \Omega$. Assuming perfect matching is reached at the input of the frontend, $R_{in} = 50\ \Omega$ and with a parasitic capacitance of C_{in}, the reflection coefficient at the frontend input is

$$S_{11} = \frac{Z_{in} - R_0}{Z_{in} + R_0}, Z_{in} = R_{in} || \frac{1}{j\omega C_{in}}. \tag{4.14}$$

To reach a S_{11} less than –10 dB at 1.1 GHz, the parasitic capacitance cannot exceed 2 pF.

Second, the capacitances that control the dominant poles of the frontend (e.g., the output of the summing stage of each sub-LNA) will affect the bandwidth of the amplifier, thereby affecting the gain at the desired signal channel. Due to the routing of sub-LNA arrays, the dominant poles are located at the input of the sub-filters, at the input of sub-LNAs and at the output of the summing stages. At the input of the frontend (the input to all sub-filters), the input resistance is set by the matching criteria. Minimal input capacitances limits bandwidth loss, requiring the input signal to be routed on the lower capacitance wiring

of the MEMS chip. Routing from the CMOS chip requires extra bumping pads to connect to the filter inputs, which is a dominant source of parasitic capacitance. Also, routing the signal path on the CMOS chips would inevitably involve overlapping DC paths, which adds more parasitics. Thus, the RF signal is directly fed onto the MEMS filters without routing from CMOS chip. Since the RF input pads are on the MEMS chip, all the other probe pads needs to be on the MEMS chip as well. The power supply and other necessary DC control signal pads are connected from the CMOS chip flipped on top. As for the interconnection between sub-filters and sub-LNAs, no extra routing is needed due to flip-chip bonding, so the parasitic losses due to connection is limited to bumping pad capacitance. The input transistors require ESD protection, and customized input pads minimize the parasitic capacitance due to the pad and the ESD diodes. Regarding the capacitive loss at the output of transistors, the output load of the summing node is scaled in correspondence with routing capacitance. With three dominant poles in the system, in order to keep the 1.1 GHz center frequency within the 3 dB bandwidth, the bandwidth of each pole is designed to be around 2.5 GHz with necessary margin. Therefore, at the input node of the frontend, with a 50 Ω input resistance, the total parasitic capacitance needs to be less than 1.4 pF. At the sub-filter-LNA interconnection, each bump pad should be less than 200 fF for an on-state branch count of $k = 7$.

5 Circuit implementation and measurement

In order to minimize parasitics from packaging and to achieve full integration, the sub-filters and sub-LNAs are fabricated through MEMS and CMOS processes, respectively, and are 3D integrated using flip-chip solder ball bonding. Designs of MEMS devices and CMOS circuits provide characterization for the final system. To protect the MEMS devices during flip-chip bonding, thin-film encapsulation (TFE) is incorporated into the IME process. Furthermore, a redistribution layer (RDL) process realizes routing on the MEMS chip. In the full system prototype, the MEMS structures pass through the entire MEMS+TFE+RDL process at the A-Star Institute of Microelectronics (IME) in Singapore. The corresponding CMOS chips with the frontend circuits are fabricated in the Samsung 28 nm process. Since deeply scaled technologies will dominate next-generation communication products, it is important for RF MEMS devices to adapt to the new technology at an early stage. The solder ball is bumped by Tag and Label Manufacturers Institute (TLMI) and flip-chip bonding is done through IME.

The CMOS chip with full frontend including the 15 sub-LNAs, the S2D, the VGA, the buffer and the digital control system is shown in Figure 5-1a. In this tapeout, commercial RF I/O was not provided. The general purpose I/O has ~ 2 pF capacitance to ground. Therefore, customized RF pads with parasitic capacitance of 180 fF were designed and implemented for the bumping pads. The pad array layout was constrained by the minimum pad pitch for flip-chip bonding design rule. In this tapeout, the solder balls are 50 μm in diameter and the bump pads have a minimum pitch of 100 μm. The 30 solder balls in the center are to be flip-chip connecting the sub-filter outputs to the sub-LNA inputs and the sub-filter ground nodes to the ground switches. Since the input probing pad is designed on the MEMS chip, the output pads and DC signals would need to route on the MEMS chips. The two columns of bumping pads on the chip edge are to bring these signals to the MEMS chip.

The MEMS filter designs are shown in Figure 5-2b. The flip-chip bumping pad array in the middle is compatible with the CMOS pad array. The RF input pads use a GSG configuration. The input routing stays in the peripheral of the chip so that its coupling to other DC paths is limited.

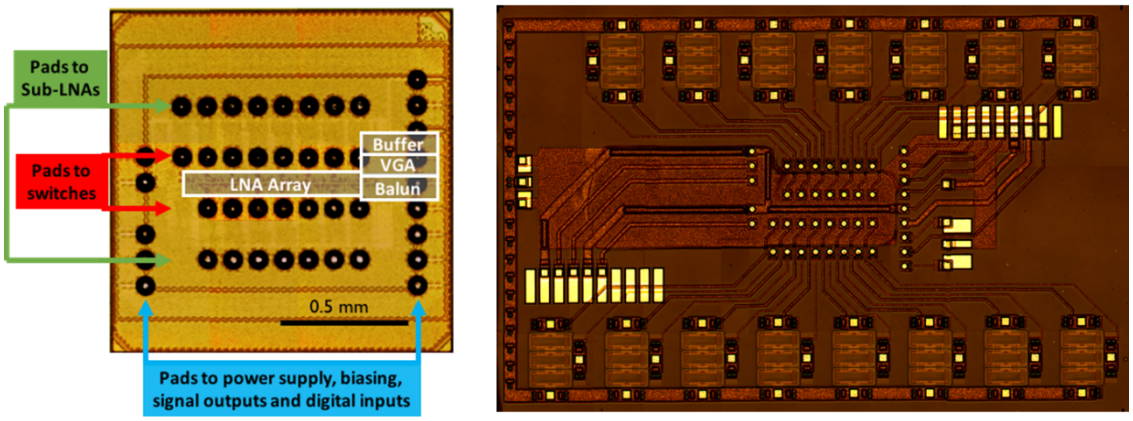


Figure 5-1 Optical image of MEMS and CMOS chips for flip-chip integration.

5.1 Stand-alone frontend components testing

As introduced in chapter 4, the frontend is composed of the sub-LNA array, the balun, the VGA and the output buffer. In order to better understand and characterize the frontend system performance, each component is duplicated in the same tapeout. The characterization chip is packaged using a QFN40 package, and measured using a testbed with an elastomer QFN socket surface mounted on a printed-circuit board (PCB).

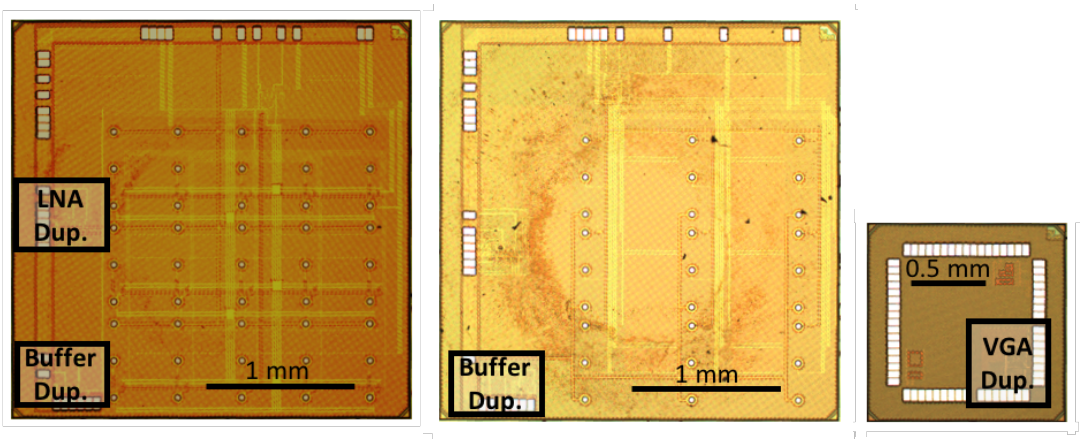


Figure 5-2 Optical image of frontend duplication circuits

5.1.1 Stand-alone LNA design and testing

A duplicated 50 Ω matched LNA array is designed and tested. In the frontend system (Figure 5-3), each sub-LNA is matched to 350 Ω. To achieve 50 Ω total impedance, 7 sub-LNAs are connected to the input node. The output node of each sub-LNA is connected to the summing stage. In order to provide a 50 Ω output load, the buffer stage follows the summing stage and is connected to the output port. Since the PCB and QFN introduces parasitic capacitances at the input of the LNA-array, an 8 nH parallel inductor L_p is placed between the input and the ground to cancel out the parasitics (not present for 3D integration) around 1.1 GHz. A coupling capacitor is placed on the signal path because in the DC domain, the source resistance will load the LNA input, changing the biasing point. In the full frontend, this DC decoupling function is fulfilled by the sub-LNA. In the LNA duplication circuit, general-purpose pads are

used at the input and output, which introduces 2 pF capacitance. This value is similar to the parasitics introduced from the RDL routing at the sub-LNA input (7 bumping pads plus RDL wiring). Since the purpose here is to characterize the LNA performance in the full frontend, it is important to keep the parasitic behavior similar for testing and the real system.

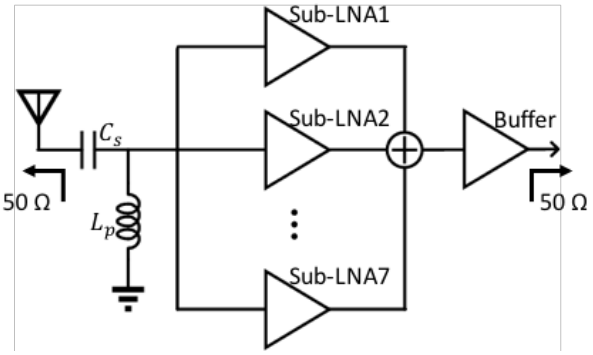


Figure 5-3 Diagram of LNA duplication circuit measurement

Figure 5-4 shows the S-parameter measurement results compared to the simulation. In the presence of an output buffer, the S21 stays around 17 dB until 1.3 GHz. The bandwidth of the LNA is 1.5 GHz, which covers the filter center frequency. The input S11 stays below −10 dB before 950 MHz. This is because the pad and routing capacitances affect the input impedance. The measurement shows NF below 3 dB up to 1.27 GHz, which satisfies the criteria set by the communication protocol.

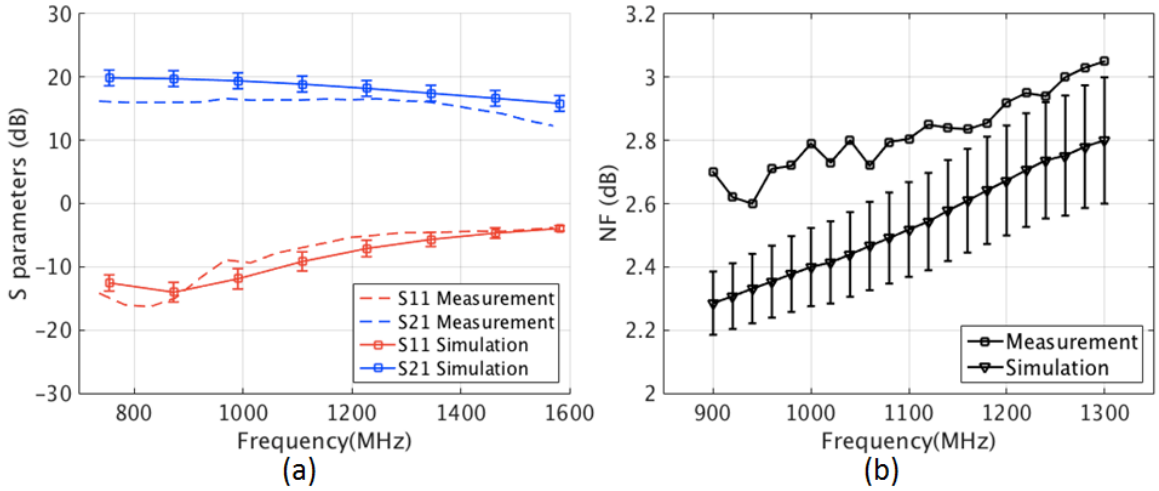


Figure 5-4 Measurement results of LNA duplication (a) S21 and S11 of

5.1.2 Stand-alone Balun, VGA and Buffer stage testing

The other components of the frontend: balun, VGA and buffer were also duplicated in the same fabrication. The measured gain and power consumption of each stage is summarized in Table 5-1 with an estimation of the frontend overall performance. This performance is competitive among the direct sampling receiver architectures in literature [21].

Table 5-1 Testing result of receiver front-end stages

Stage	Gain @ 1 GHz	Power
Filter	−3 dB (est.)	0
LNA	21.1 dB	11.2 mW
Balun	2 dB	8.7 mW
VGA	4.1 ~ -7.4 dB	4.8 mW
Buffer	−5.1 dB	3.2 mW
Frontend	19.1 ~ 7.6 dB	27.9 mW

5.2 MEMS Filter fabrication and testing

Two-port AlN CMR resonators and filters were fabricated at IME. The fabrication can be divided into three main parts: 1) main components in the MEMS-only process which consisted of standalone resonators and filters, 2) a MEMS process with thin-film encapsulation (TFE) process for which the filters were hermetically encapsulated and 3) a redistribution layer (RDL) process that builds three layers of thick copper for routing purposes. The MEMS-only process has been introduced in chapter 2. The RDL process will be shown in section 5.3.1.

5.2.1 MEMS with Thin Film Encapsulation Fabrication Process Flow

The MEMS with the thin-film encapsulation (TFE) process provides hermetic encapsulation of the filters. Filters encapsulation is necessary to protect the device to ensure high yield in the bump bonding process. Figure 5-5 shows the MEMS with TFE process flow. The first steps of the process are identical to those of the MEMS only process up to step (h) (passivation layer SiO_2 deposition). After deposition of the passivation layer, the passivation SiO_2 is etched down to the AlN to form the anchor of the TFE, as shown in (b). This is followed by etching down to the device layer of Si to form the release holes for the resonator, shown in (c). Next the sacrificial layer of Si is deposited and patterned. A 1 μm thick layer of AlN is then deposited to form the capping layer. This layer completely covers the sacrificial Si and anchors, except for small holes above the AlN etch holes that are used to facilitate release of the device. With the cap layer in place, the device is then released with XeF_2 etch followed by vapor HF etch. The device is then sealed hermetically with 3.5 μm of SiO_2. The SiO_2 sealing layer is patterned to reveal the Mo pads. Lastly gold under-bump metallization (UBM) was deposited on the pads to facilitate bump bonding.

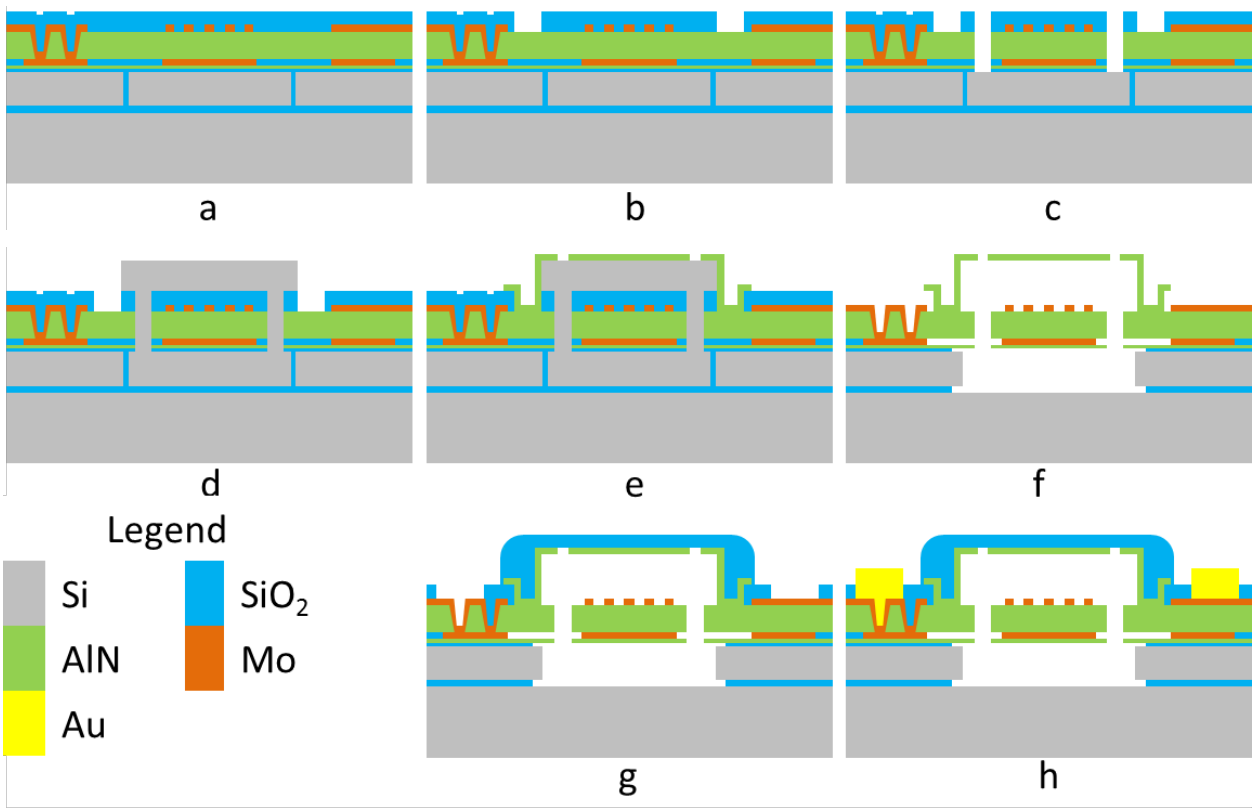


Figure 5-5 MEMS with TFE process flow: (a) Device fabricated through MEMS only process flow up to step h in Figure 3-3(h). (b) Etching of encapsulation anchor. (c) Etching of release holes. (d) Formation of sacrificial silicon. (e) Deposition and patterning of AlN capping layer. (f) Xenon difluoride release and vapor hydrofluoric acid etch. (g) Deposition and patterning of Silicon dioxide sealing layer. (h) Deposition of under bump metallization.

5.2.2 MEMS with Thin Film Encapsulation Device Measurements

In accordance with the CMOS configuration, the MEMS chip is designed with the total number of sub-filters N equaling 15. The finger length of the resonators is 60 μm. The devices are designed so that when k = 7 sub-filters are selected the filter is matched to 50 Ω. A duplication of the filters in the MEMS chip is designed in the same fabrication. Figure 5-6 shows the measured filter S-parameter response with 350 Ω loading.

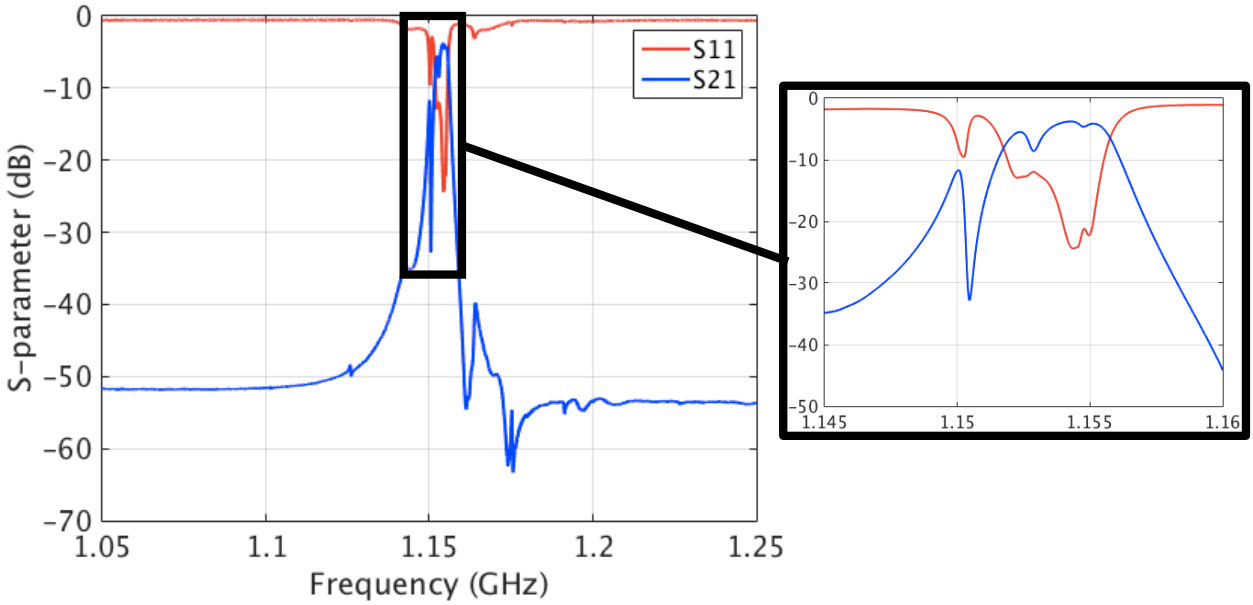


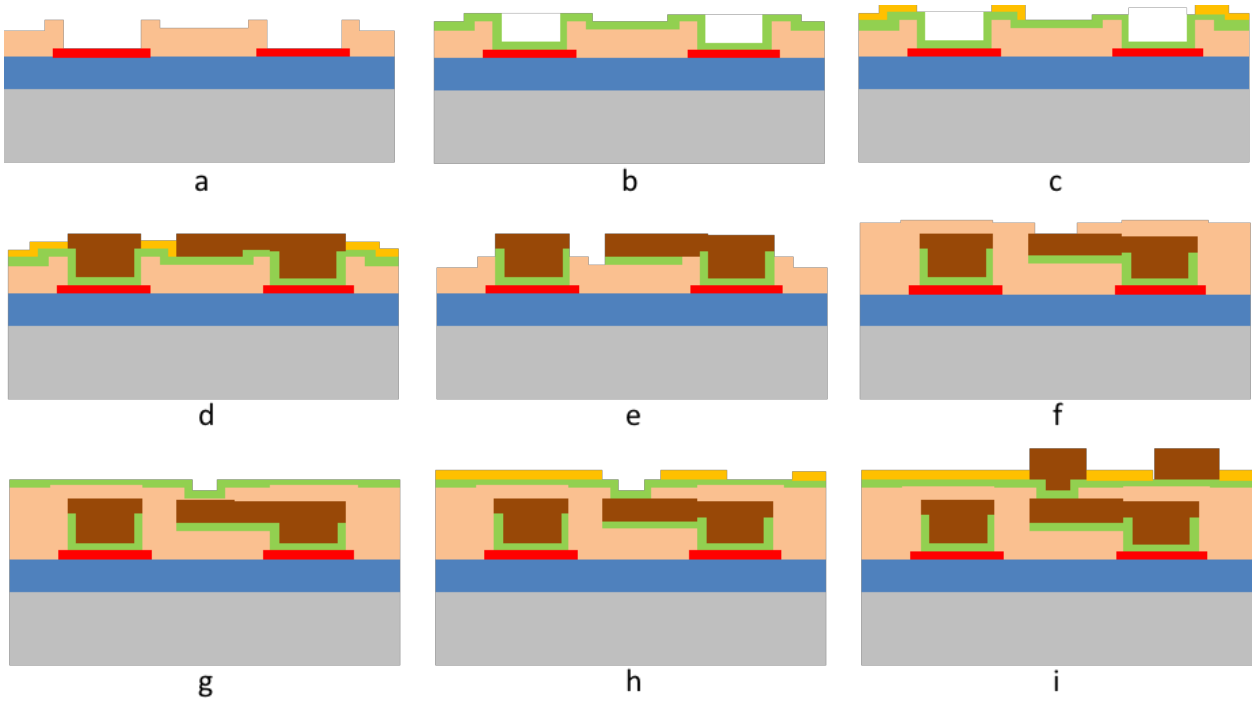
Figure 5-6 S-parameters of 2-port AlN MEMS characterization filter matched to 350 Ω.

The filter response shown in Figure 5-6 is a typical performance of the filter with a center frequency around 1.154 GHz, a bandwidth of 3.82 MHz, an insertion loss (IL) of 3.78 dB and an out-of-band rejection (OBR) of 15 dB. The degradation of IL compared to the MEMS filters reported in chapter 2 is due to the shorter finger length. According to [11], a longer finger length would result in higher Q value for the resonator, and lower IL for the filter. Also, spurious modes exist around the pass band, which increases ripple and lowers the OBR. Since our focus is on compensating the systematic error of center frequency, these degradations will not affect the study of the effectiveness of SES. Also, the interaction between filters and circuit can be shown by comparing the filter performance, the circuit performance and the system performance parameters. The absolute value of these parameters is not the focus of this work.

5.3 RDL Parasitic fabrication and testing

5.3.1 RDL Fabrication Process Flow

The RDL is an essential step in the AlN MEMS fabrication to realize low parasitic routing. Figure 5-7 shows the process flow of RDL fabrication. The first steps of the process are identical to those of the MEMS+TFE process up to step (g) (deposition and patterning of SiO_2 sealing layer). In Figure 5-7, the process only shows from the top molybdenum (Mo) layer. The AlN and bottom layer are hidden for simplicity. After deposition of SiO_2, a first layer of 5 um polyimide is coated and the via between the top Mo and the first layer of RDL (RD1) is etched, shown in (a). Following the polyimide, a 100 nm Cu seed is deposited, shown in (b). After that, photoresist (PR) is used to define the first RDL layer, shown in (c). The RD1 layer is formed by depositing 3 um Cu, shown in (d), followed by lift-off, shown in (e), and seed etch, shown in (f). Before defining the RD2 layer, another polyimide layer is deposited, shown in (g). Then the RD2 and RD3 processes that follow are the same as that for RD1.



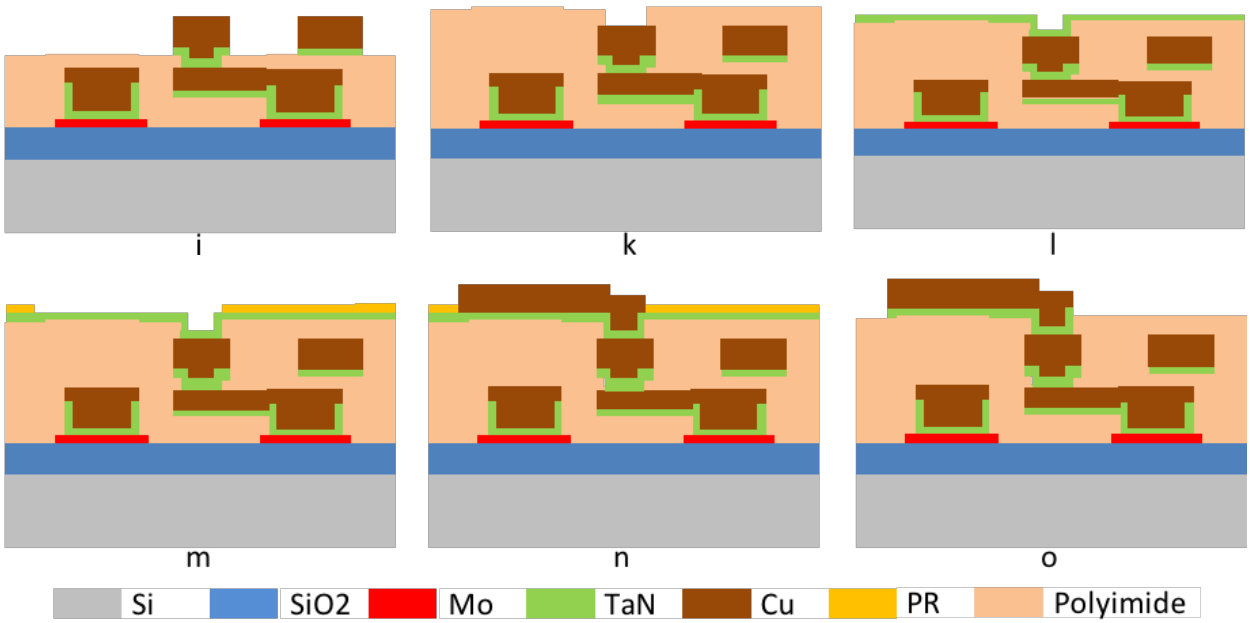
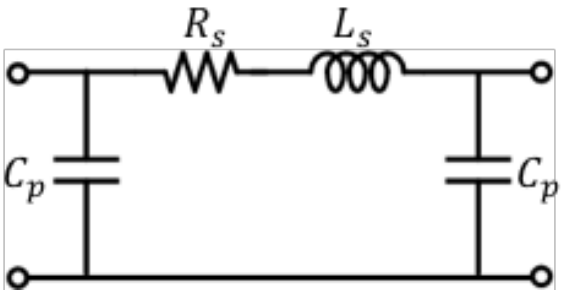


Figure 5-7 Process flow for RDL fabrication

5.3.2 RDL parasitic measurement

Since minimizing parasitics is critical to the frontend performance, the resistive and inductive parasitics on the RDL layer and the capacitive parasitic between two RDL wires need to be characterized. In this design, open, short and thru structures of RDL wires with 1000 µm length were fabricated and tested for determining the S-parameters. A π circuit model (Figure 5-8) is used to model the wiring parasitics. The measured parasitics for two parallel RD1 wires with 10 µm width, 1000 µm length and 90 µm length separation are shown in Figure 5-8. From the table, the inductance for a 1000 µm RD1 wire reaches 1 nH. Analysis in the next section will show that this parasitic inductance affects the filter out-of-band rejection near the center frequency. Since the average length of RDL wirings are around 1400 µm, the average inductance on the ground is 1.4 nH. When seven branches are selected, this value will be reduced by paralleling to 200 pH.



R_s (mΩ/μm)	L_s (pH/μm)	C_p (fF/μm)
0.67	1	0.015

Figure 5-8 Model for RDL routing wire parasitics

5.4 3D stacked frontend bonding and testing

5.4.1 3D Integration through Solder Bump Bonding

With fully functional MEMS chips and CMOS chips with solder balls completed, the process of flip-chip bonding was undertaken at IME. Figure 5-9 shows a cross sectional view of the flip-chip bonding process. Figure 5-9a shows the CMOS chip, and Figure 5-9b shows the MEMS chip. The two chips are bonded together by aligning the solder balls on the CMOS chip with the UBM pads on the MEMS chip. The resulting stack is shown in Figure 5-9c, in which the RF signal and ground pads are now bump bonded to the CMOS chip. As the bonding of the chips requires careful handling and application of force to join the two chips together, the TFE is essential for protecting the resonators from physical damage and ensuring that no devices are broken during the bonding process.

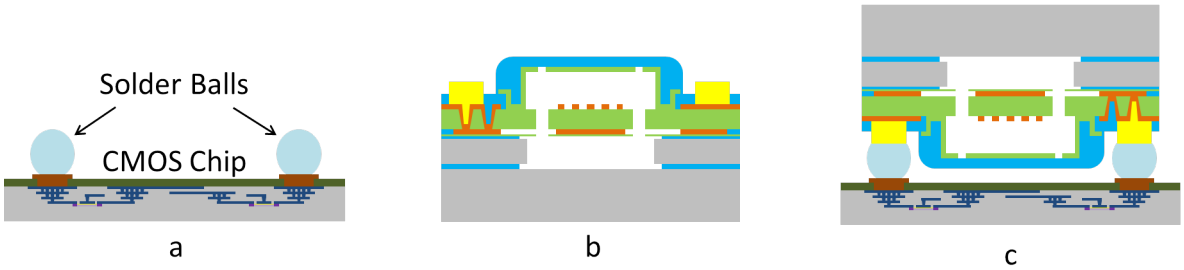


Figure 5-9: Flip chip bump bonding (a) CMOS chip with solder balls. (b) MEMS Chip. (c) MEMS chip flip chip bonded to CMOS chip.

5.4.2 3D stacked frontend measurement setup

At the time of this writing, only one flip-chip sample has been delivered with additional samples expected in the future. This flip-chip stack has a bumping yield issue and only five sub-filters of the 15 in the array function. Figure 5-10 shows the optical image of the 3D stack. The RF input has a GSG configuration and the output is SGS. 150 µm pico probes route the RF inputs to the sample. The DC and logic pads are probed using 100 µm DC wedge probes. The power and ground have been bypass-coupled using 1 µF coupling capacitors. The logic inputs control the scan chain to select different sub-filters. A

National Instruments Digital Acquisition module (NI-DAQ) generates the logic data. A Keysight E5230A network analyzer measures the S-parameters.

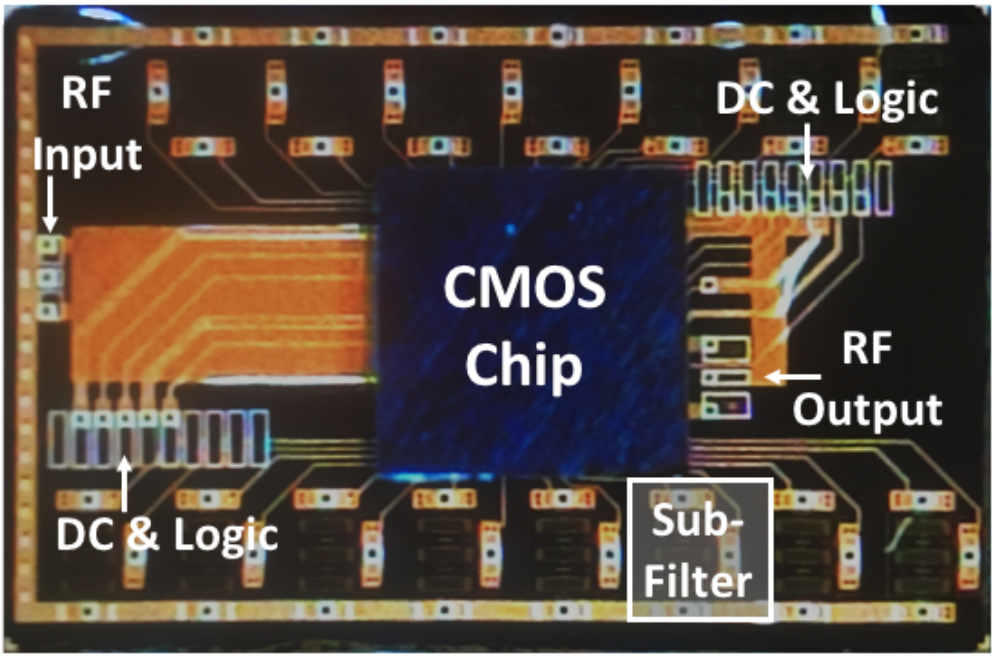
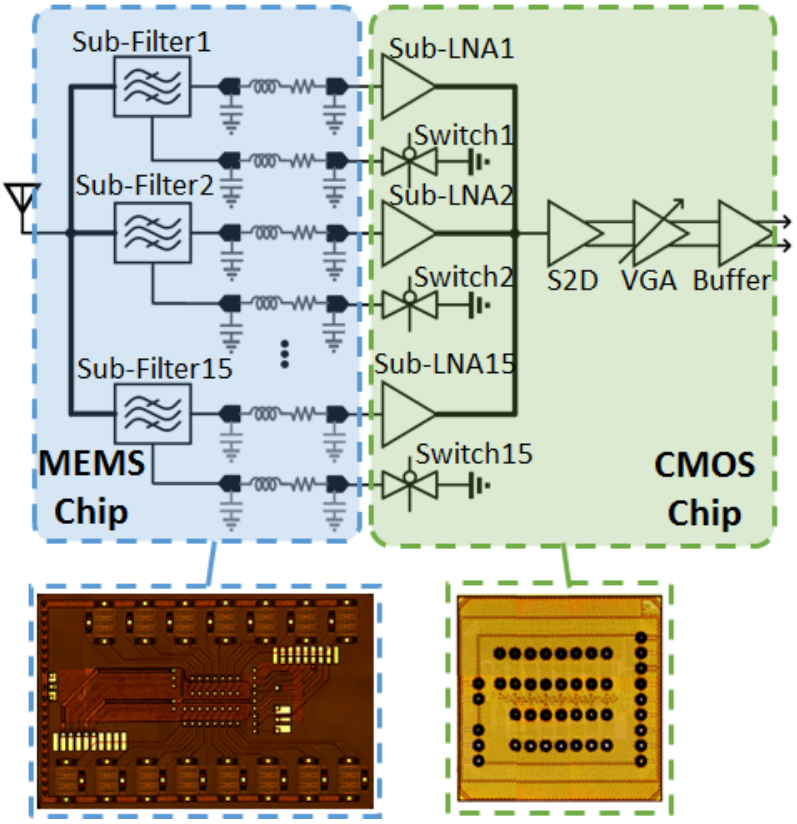
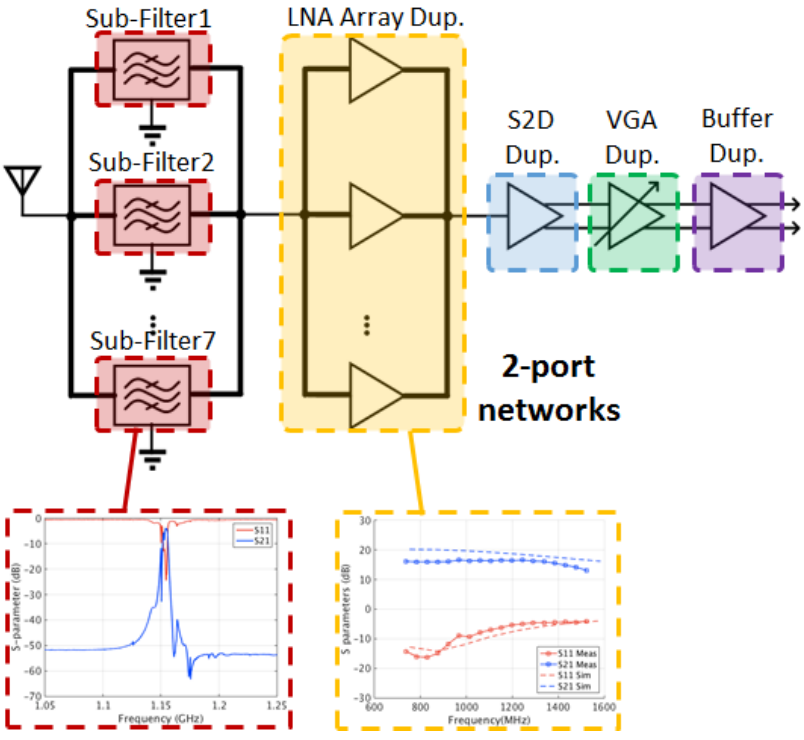


Figure 5-10 Optical image of flip-chip stack

Figure 5-11a shows the schematic diagram of flip-chip measurement. The resonator filters and the routing layers were fabricated on the MEMS chip, while the sub-LNA array, the S2D, the VGA and the output buffer are on the CMOS chip. To evaluate the system performance, the S-parameters of the full frontend is compared to the S-parameters synthesized by cascading measured S-parameters for each individual frontend stage (Figure 5-11b).



(a)



(b)

Figure 5-11 Measurement diagram of (a) flip-chip bonded frontend (b) calculation of cascaded frontend.

Using the same notation in (2.8), the S-parameter of each sub-filter is transformed into Y-parameters. Multiplying each Y-parameter by 7 then leads to the Y-parameter of seven 350 Ω matched sub-filters connected in parallel (5.1). Transforming the calculated Y-parameters of the sub-filter array yields its transmission matrix (T-matrix). Likewise, transforming the measured S-parameters of the sub-LNA array (with 7 sub-LNAs in parallel) yields its T-matrix. Multiplying the two T-matrices results in a two-port network for the cascaded sub-filter array and sub-LNA array (5.2). The following stages, the S2D, VGA and buffer are modeled as gain (S21) rise/drop by their stand-alone gain values.

$$\mathbf{Y}_{\mathrm{Filter}} = \sum_{i=1}^{7} \mathbf{Y}_{\mathrm{SubFilter},i} \tag{5.1}$$

$$\mathbf{T}_{\mathrm{FilterLNA}} = \mathbf{T}_{\mathrm{Filter}} \times \mathbf{T}_{\mathrm{LNA}} \tag{5.2}$$

5.4.3 3D stacked frontend measurement analysis

The S-parameters of these two configurations are shown in Figure 5-12. In the frontend measurement, the five working sub-filters were selected. The VGA is set to work at its maximum gain. An RF input of −30 dBm is injected into the input and the S-parameters were tested through VNA. The performance comparison between the two configurations are shown in Table 5-2. The differences in center frequency and bandwidth (BW) is because the characterization filter is not taken from the same die as the flip chip bonded MEMS chip. The S21 difference between the two configurations is around 1.2 dB. The major difference is the 25 dB drop in the OBR performance. In frequencies far from the center frequency, the cascaded frontend shows a suppression of more than 30 dB, whereas for the flip-chip frontend measurement, the suppression at outer band is only around 10 dB. This means the signal is feeding through the filter in outer bands.

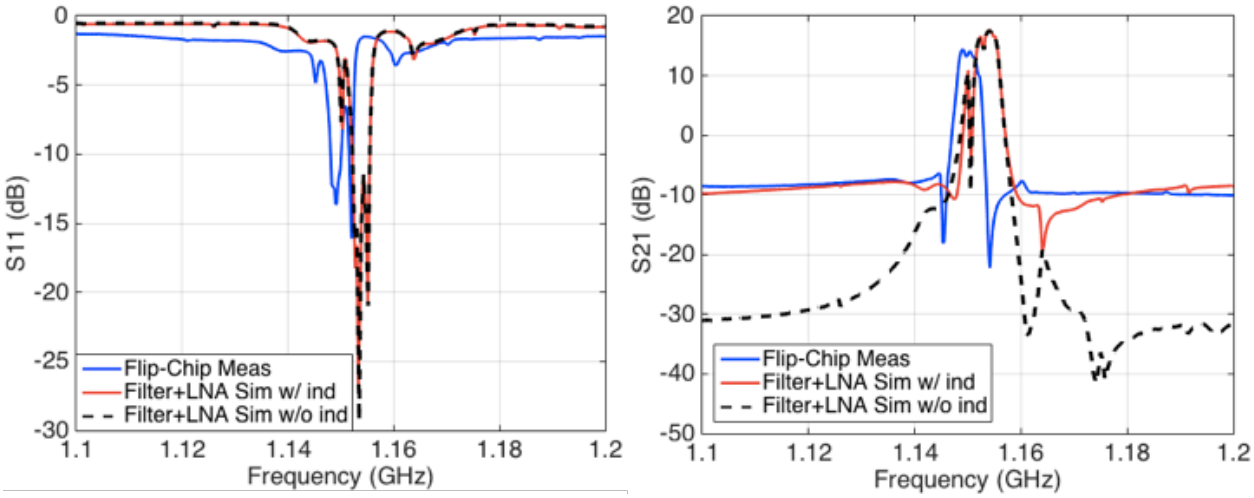


Figure 5-12 S-parameters for the flip-chip bonded frontend and the calculation of cascaded frontend.

Table 5-2 Performance for the flip-chip bonded frontend and the calculation of cascaded frontend.

	f_0 (GHz)	BW (MHz)	S21 (dB)	* OBR (dB)
Flip-chip frontend	1.149	3.50	14.5	23.5
Cascaded frontend w/o L_{GND}	1.154	3.82	17.4	48.4
Cascaded frontend w/ L_{GND}	1.154	3.82	17.4	26.6
* OBR is the difference between the passband IL and the out-of-band suppression				

The signal feedthrough comes from parasitics on the filter ground path. As is discussed in section 5.3.2, an RDL wire with 10 µm width introduces inductance of 0.8 pH/µm. The ground routing on the MEMS chip has an average length of 1.4 mm, which introduces around 1.4 nH parasitic inductance (L_{GND}) on the ground path. With 7 branches selected, the effective ground inductance is 200 pH. At the filter center frequency, this parasitic inductance introduces an inductive impedance of $Z_L = 1.45\ \Omega$. With a loading impedance of $R_0 = 50\ \Omega$, the equivalent circuit when the frequency is at the outer band is shown in Figure 5-13. When the signal frequency is far away from the filter center frequency, the resonant tank is effectively an open circuit. Therefore, the S21 for this circuit represents the feedthrough across the filter

in the frontend. Using the matching criteria, $R_0 = \frac{1}{|j\omega C_0|}$, and the inductance of $L_{GND} = 200$ pH the S21 is calculated to be −33 dB. If the ground inductance is shorted, the S21 becomes −73 dB. This shows that the filter suppression is sensitive to the parasitics on the filter ground, especially the inductive parasitics. In the RDL layout, the inductive parasitic can be reduced by increasing the RDL thickness or the width. Also, the filters should be placed as close to the bumping pads as possible to reduce the routing length

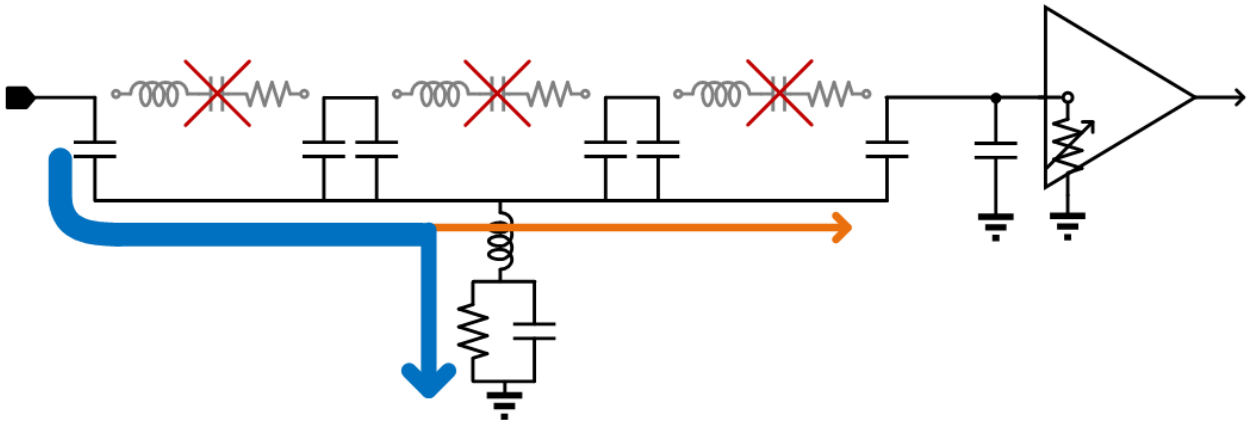


Figure 5-13 Model of feedthrough parasitics.

In order for the filter to function with good passband performance, the sub-LNA needs to provide impedance matching. Figure 5-14 shows the S-parameters in the passing band with 1 to 5 branches selected. The S11 improves as the number of selected branches increase, since the loading of the filter output (and thus the input impedance of the LNA array) gets closer to the antenna impedance of 50 Ω. From the Smith chart (Figure 5-14c), within the passband, as the frequency increases the input impedance converts from inductive region (upper hemisphere) to the capacitive region (lower hemisphere), crossing the pure resistive region (x axis). Due to resistive mismatch, the S11 strays away from the pure resistive region when the number of branches selected is small. As S11 improves, the S21 also gets more flat and obtains less insertion loss (Figure 5-14b). This shows that the LNA is providing impedance matching to improve filter performance.

In order to select different combinations of filter-LNA branches, each combination needs to provide uniform loading. Figure 5-15 shows the S-parameters when only one branch is turned on. With different

single branches selected, the S11 performance stays the same. S21 is mostly the same with some variation believed due to systematic and random errors during fabrication. These test results demonstrate that the selection method is able to achieve uniform loading.

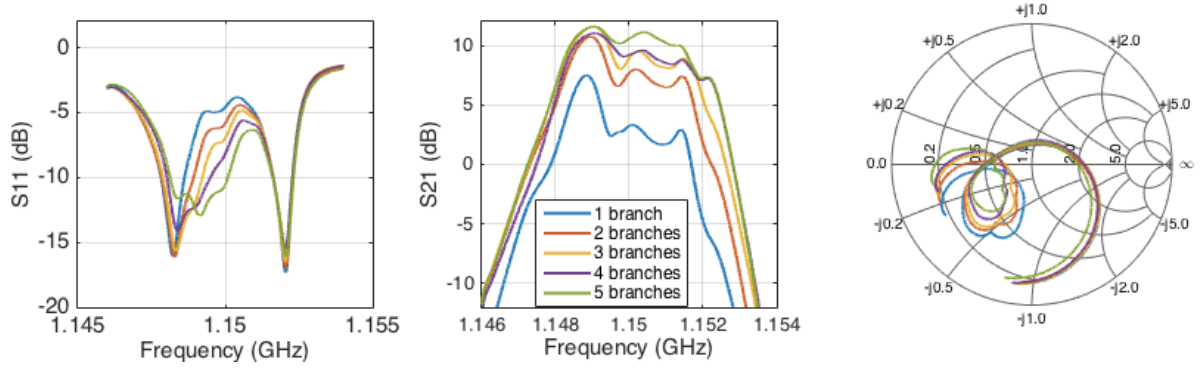


Figure 5-14 S-parameters for the flip-chip bonded frontend with different number of branches selected

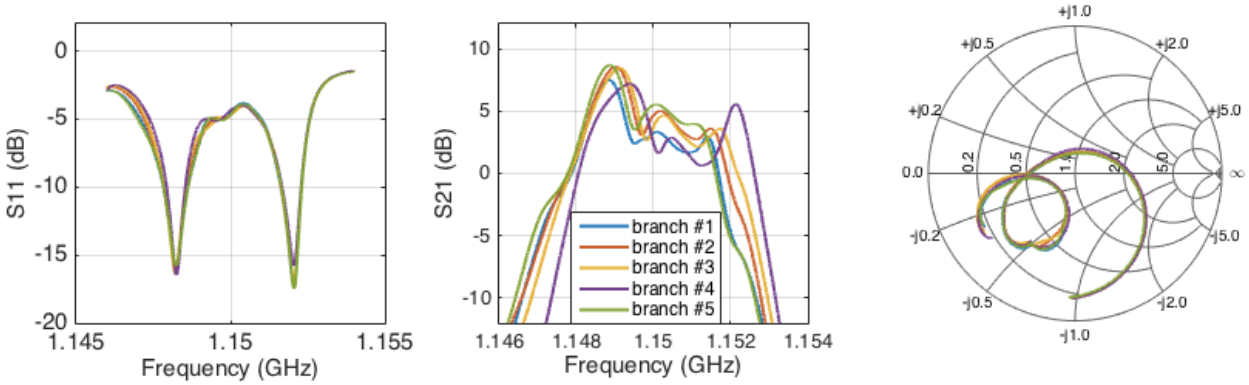


Figure 5-15 S-parameters for the flip-chip bonded frontend with different single branches selected.

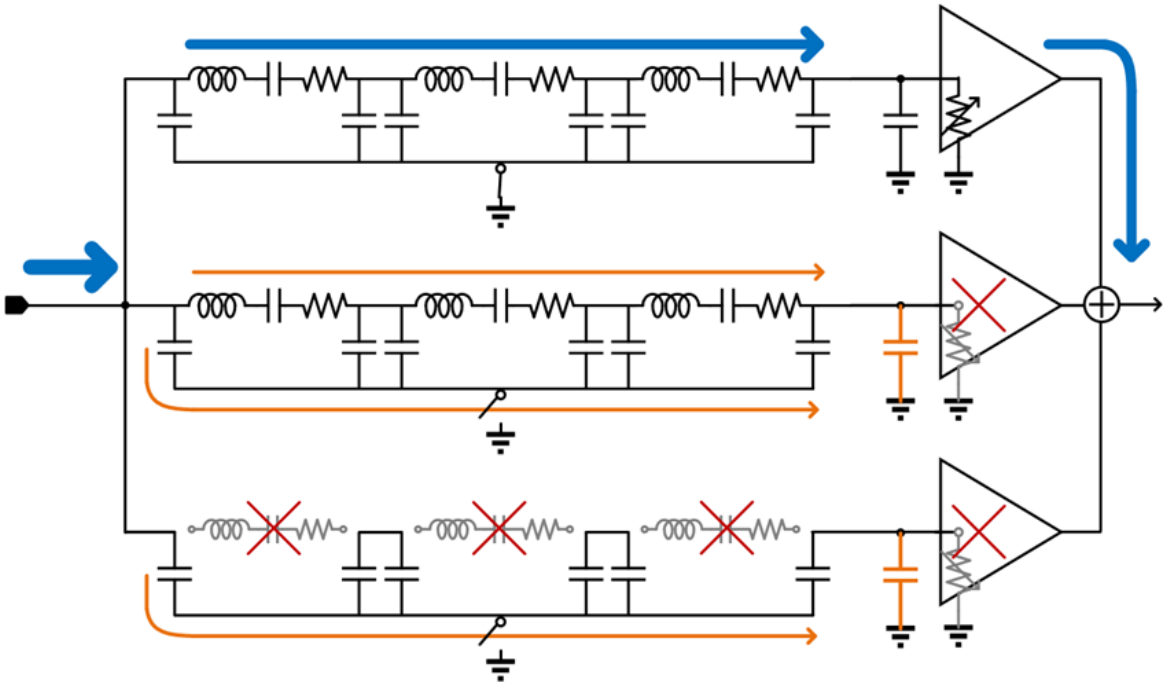


Figure 5-16 Capacitive loading from unselected sub-filter-LNA branches

From the smith chart in Figure 5-14, the input impedance is close to the real axis with five branches turned on. However, the S11 still has capacitive remains. This is contributed by the capacitive parasitics at the receiver input. These capacitors come from the wiring at the input of filter array and the bumping pads between sub-filters and sub-LNAs. Since the input wiring is from the MEMS RDL, the parasitic capacitance is limited according to the extraction in Section 5.3.2. As for the bumping pad capacitances, it is the pads on the unselected branches that load the input, shown in Figure 5-16. There are two types of unselected branch. The first one has a sub-filter with a center frequency close to the selected sub-filters, illustrated in the figure as the middle branch. At the center frequency, this branch is equal to a capacitor shorted by the resonating RLC tank to the input node. The second type is when the unselected sub-filter center frequency is off from the desired center frequency, shown in the figure as the bottom branch. In this case, the bumping capacitor is shorted to the input node through the ground node of the sub-filter. With the ground switch, this path is not fixed to a ground voltage, and therefore the input signal will leak through the ground metal to the bumping pad capacitors. Therefore, all the *N-k* bumping pads on the unselected sub-branches are contributing to the input capacitive load. In the current SES selecting

architecture, these capacitances are not cancelled by on chip inductors. Thus, the increase in the number of sub-branches *N* will scale up the parasitic loss. To overcome the capacitive loss, a cancelling method is called for.

4 Conclusion and future work

4.1 Conclusion

As the communication spectrum is getting more occupied, RF receivers must increasingly avoid signal degradation from large out-of-band interferers. Due to lack of on-chip high-Q RF filters, conventional receivers use complex architectures to transform signal from RF to baseband, which is area and power consuming. The recently emerging AlN contour-mode two-port resonator filter, with its high-Q, low insertion loss and integratibility with CMOS technology, is a promising candidate for the RF channel selection filter. The main implementing challenge is its center frequency inaccuracy due to both random and systematic process variations. To address this issue, this work proposed a 50 Ω self-healing filter design based on Extended Statistical Element Selection (ESES).

A statistical model was established to capture the filter random and systematic variations. 16 filters were laid out in 4×4 array on a 2×2 mm^2 chip. S-parameter measurements were taken on 71 such chips across an 8' wafer. Among the four filter parameters, BW, IL and C_0 are dominated by random variations and reveal Gaussian distribution. Filter center frequency f_0 is dominated by systematic variations and reveal linear dependence on filter location. In the 2×2 mm^2 area, the systematic f_0 shift with respect to its location was modeled using a plane function with angle parameters α, β and center shift Δf_{0c}. Statistical data from the 71 chips shows that the plane model parameters follow a uniform distribution.

ESES pseudo-variation array was implemented on the same 2×2 mm^2 chip with $N = 16$ and $k = 4$. To determine the frequency range and interval in the pseudo-array and the placement in the 4×4 array, the continuous range was discretized and all combinations were tried out in a Monte Carlo simulation. The passing criteria tightens the center frequency tolerance by 22.5 times than the maximum center shift. The best success rate occurs at rotation 42 with an even interval and a pseudo-variation equal to the maximum center shift.

The frequency shift in pseudo variation was implemented through finger width modulation. COMSOL 2D finite element simulation and measurement data were compared to verify the relation between f_0 and finger width W. Nonlinearity in the relation was observed. The sensitive and linear region for this relation occurs when W is larger than half pitch. Three ESES arrays were designed and measured. The success rate matches Monte Carlo simulation result given the actual pseudo frequency range. The success rate improves by 10x compared to non-calibration case.

To further verify the possibility of implementing the ESES in a receiver, a receiver frontend with the self-healing filter array was designed in Samsung 28 nm technology. To reduce loss from signal path switches, a filter selecting scheme using sub-LNAs was proposed. In order to save area, the LNA adopts an inductorless topology with active feedback. To limit parasitics from inter-connection and routing, signal is fed through a redistribution layer wiring fabricated on the MEMS chip. The measurement of the LNA characterization circuit shows a gain of 17 dB and an NF less than 2.8 dB at 1.1 GHz. The frontend measurement shows uniform loading with different subfilter-subLNA branches selected.

4.2 Future work

This work has focused on methods to improve center frequency accuracy in the case of AlN resonator filters. The statistical model is established for a specific fabrication process. In future application of this method to other kinds of MEMS narrowband filters, a characterization run is required to capture the statistics in the fabrication, before taping out the self-healing designs. This would take time and more cost to bring out a product. It will benefit the industry even more if a general layout pattern method that is applicable to other MEMS narrowband filters can be established. This would require mathematical extracting the relation between each layout pattern and the success rate. Also, more fabrication runs for different types of MEMS filters need to be applied to validate these mathematical relations.

Another contribution of this work is in the integration of MEMS filters and CMOS receiver frontends. The aim is to build a frontend that with both stable and low parasitics. In this specific application with intensive SES switching components, the system performance is greatly dependent on the parasitic

control. This work has improved the routing parasitics through RDL fabrication. The parasitics from CMOS and from the integration is still a problem to be solved. In order to cancel out the capacitive parasitics, one could look to building inductors on the CMOS that can cancel out the capacitors at the targeting frequency without adding resistive loss. The inductors can be involved with the sub-LNAs so that by co-designing the MEMS and CMOS, both can benefit. The parasitics can be further reduced when full integration between MEMS devices and CMOS circuits is achieved, when the bumping pad is no longer needed. Also, improvements can be achieved in methods to match the filters to 50 Ω with a smaller area consumption. When the filters get smaller, the routing parasitics will scale as well.

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