Study of the Crystallization Dynamics and Threshold Voltage of Phase Change Materials for Use in Reconfigurable RF Switches and Non-volatile Memories

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Abstract

Chalcogenide phase change (PC) materials can be reversibly transformed between the high resistivity (~ 1 Ω·m) amorphous state (OFF-state) and low resistivity (~ 10^{-6} Ω·m) crystalline state (ON-state) thermally, both are stable at the room temperature. This makes them well suited as reconfigurable RF switches and non-volatile memories. This work will present the understandings of two key characteristics of PC materials, the crystallization dynamics and the threshold voltage (V_{th}), as they determine performance limitations in these applications. Crystallization dynamics describe the correlations of the states, temperature and time; the V_{th} is the trigger of the threshold switching which leads to the "break down" of PC materials from OFF-state to ON-state.

The four-terminal indirectly-heated RF switches with high cut-off frequency (> 5 THz) has advantages over other technologies but its programming power (~ 1.5 W) is yet to be reduced. Measuring the maximum allowed RESET quench time in the crystallization dynamics is critical for designing low power switches. As a major contribution, this work provides a universal methodology for accurate heater thermometry and in-situ crystallization measurements for this study. On the other hand, understanding the V_{th} is essential for high power handling applications as it determines the maximum power that an OFF-state switch can withstand without being spontaneously turned on. This work will discuss new observations and learnings from V_{th} measurements including the geometry dependent V_{th} variations which provide insights into the threshold switching mechanism.

Unlike RF switches, faster crystallization is desired for memories to improve the write speed. The non-Arrhenius crystallization needs to be explored to achieve short crystallization time (< 10 ns) at high temperature (> 700 K). As another major contribution, this work will present a nano-scale (~ 100 nm) high-speed (thermal time constant < 5 ns) PC device for assessing the crystallization time in this regime, and provide a comprehensive learning for the crystallization dynamics from 300 K to 1000 K by developing a unified framework based on the fragility model and growth-dominated crystallization. This can be used to

accurately simulate the crystallization process for any device geometry and estimate the RF switches power and V_{th}.

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Chapter 1: Introduction

1.1 Motivations

For over 40 years, silicon based semiconductor technologies has been the heart of all modern electronics. The key component, the complementary metal-oxide-semiconductor (CMOS) field effect transistor (FET) has been continuously scaled down to smaller size to enable higher computation capability, lower cost, smaller integrated circuit (IC) chip size and lower power consumption [1]. The advancement of this technology has followed the projection of "Moore's Law", which predicted that for every 18 months, the number of transistors on the single chip and the performance of the chip would double [1], [2]. Until recent years, however, this advancement has been observed to slow down due to the fabrication challenges and negative effect of smaller devices as the channel length of a single CMOS transistor approaches sub-10 nm regime [1], [3]–[5].

As Moore's Law will likely come to an end eventually [4], along with innovations in CMOS device architecture, patterning, interconnections and wafer scaling [3], a tremendous amount of "beyond-CMOS" technologies has been proposed and studied as a replacement of CMOS [1], [3], [6]–[8]. Through exploiting new materials with different physical properties, such as III-V materials [7] and carbon based 1-D and 2-D materials [6][8], one can reinvent the way of representing and manipulating information. In this way, new materials and device architecture for digital logic processing will be invented to keep the velocity of technology advancements in computation performance, power and cost. On the other hand, "More than Moore", a complementary strategy, was proposed to focus on innovating the components other than digital logic, such as power management, analog and RF systems, sensors, memories, data storage and their integration with traditional CMOS technology [9][10].

New technologies that combines novel materials and device architecture with "More than Moore" strategy are desired in the future roadmap with the absence of Moore's Law. One example is the radio

frequency (RF) circuits in wireless communication systems, which are the interfaces between binaries and the physical world. Typically, RF circuits are specially designed for various frequency bands for different wireless standards such as 3G, LTE, WiFi, Bluetooth, etc. However, CMOS based RF circuits are difficult to scale since the short channel effects of CMOS FETs and process variations in small nodes can significantly harm the RF circuits performance [11], result in larger area and higher power comparing to digital logic components [12]. A solution to this is to design a single RF system that can accommodate different standards at the same time [13], [14]. Inspired by the idea of field-programmable gate array (FPGA), which allows digital logic reconfigurability, reconfigurable RF has been proposed to allow the circuits to work at various frequency bands reconfigurably and improve the space and power without sacrificing performance [13], [14]. The key components of reconfigurable RF system are the RF switches, which are used to change the topology of the circuits to achieve reconfigurability. Thus, it is critical to select materials and design device architecture appropriately for an RF switch with negligible impact on the performance of existing circuits.

Another example of emerging "More than Moore" technology is non-volatile memory [15], [16]. Memory and storage systems in the traditional computer architecture are hierarchized based on their physical location with respect to the central processing unit (CPU) [17]. Static random access memories (SRAMs) can be integrated within the CPU and have the highest write and read speed. However, SRAM cell is power hangry and large in size [18]–[20]. Besides, the data stored in SRAMs is not persistent without static power being applied. On the second level, dynamic random access memories (DRAM), which provide moderate access speed but much higher density, are made into standalone chip used as the main memory [18]–[20]. Magnetic hard drive can be used on the third level, providing the slowest access speed but also the capability to persist data even during power loss [20], [21]. Flash memory, as an alternative for magnetic hard drive, has higher speed but higher cost [20], [21]. As CPU performance increases, higher speed is required to access main memory or even persisted data. However, the memory performance has been improved in a much smaller rate than the logic performance, causing the problem of "Memory Wall" [22].

Thus, innovations from memory architectures down to memory devices and materials are desired to address this issue. Various non-volatile memory technologies with different physic has been proposed to achieve extremely high SET/RESET speed, low power consumption, good data retention and reliability, high density and 3-D integration capability, with the goal of replacing the existing volatile memories and even unifying the entire memory hierarchy [19], [20], [23]–[27].

In both of the above applications, chalcogenide phase change materials are very promising to be used to build into devices that provide high performance, low power, compatibility with CMOS, and great potential in terms of scaling[13], [14], [22]–[25]. This thesis will focus on the understandings of electrical properties of phase change materials which are critical for using them in both RF switch and non-volatile memory applications.

1.2 Background of Phase Change Materials

1.2.1 Electrical Properties

Chalcogenide phase change (PC) materials, first discovered by Ovshinsky in 1968 [28], were found to have two phases with very different physical properties, such as optical reflectivity and electrical resistivity. Both phases are stable at room temperature (data retention time longer than 10 years) and can be reversibly transformed from one to the other [29]. Amorphous phase PC materials have high resistivity (1 Ω·m to 100 Ω·m) while crystalline phase PC materials have low resistivity (typically < 10^{-4} Ω·m) [29]. The huge difference of resistivity (> 4 orders of magnitude) is due to the different atomic arrangement in two phases. PC materials in the amorphous phase have an atomic structure which is locally ordered but disordered over long range. The atomic arrangement in the crystalline phase is ordered in both short and long range. Amorphous PC materials are regarded as intrinsic semiconductors with localized states caused by the disordered lattice while crystalline PC materials are regarded as degenerate narrow band-gap semiconductor with the Fermi level below valance band [29].

1.2.2 Crystallization and Amorphization

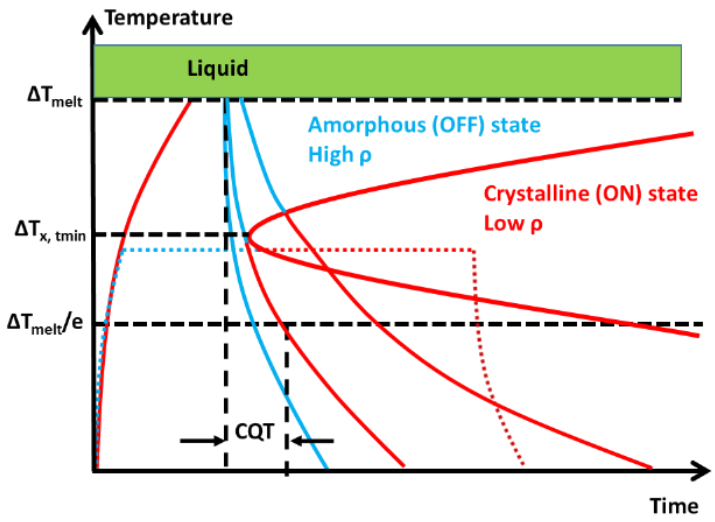

Figure 1.1. Schematic TTT diagram of PC materials and temperature transients for SET (dotted curve), successful RESET, marginal RESET and failed RESET (solid curves) operations. Red represents crystalline (ON) state for PC materials while blue represents amorphous (OFF) state.

In this section, we use relative temperature ΔT with room temperature as the reference point (at room temperature, ΔT = 0 K) so that we can define the thermal time constant and quench time; while in the next sections, we will use the absolute temperature T. A SET operation crystallizes the PC material from the amorphous state by heating it up above its crystallization temperature and holding until the transient falls into the crystalline region in a TTT diagram as shown in Figure 1.1. The closer the ΔT is to $\Delta T_{x,min}$ (the temperature with the minimum crystallization time), the shorter time it takes to SET. A RESET operation amorphizes the PC material from crystalline state by heating it up above ΔT_{melt} and then quenching rapidly. A successful RESET operation requires the ΔT to decrease from ΔT_{melt} to below $\Delta T_{melt}/e$ in time (defined as quench time) less than the critical quench time (CQT). If the quench time is longer than the CQT, even though the PC material underwent melting (due to $\Delta T > \Delta T_{melt}$), the temperature transient may fall into the crystalline region (red boundary in Figure 1.1) and re-crystallize the PC material, keeping the resistivity in the ON-state as in a SET operation. Typically, at low temperatures ($\Delta T < \Delta T_{x,min}$), the crystallization time

is exponentially dependent on $1/T$ and the crystallization is a thermally activated process that follows the Arrhenius behavior. However, when ΔT approaches ΔT_{melt}, the process deviates from the Arrhenius behavior. This phenomenon can be explained by the classic crystallization theory.

1.2.3 Classical Crystallization Theory

According to classical crystallization theory, crystallization of amorphous PC material is a process of two steps: nucleation of crystalline PC clusters followed by growth of crystalline PC material at the crystalline-amorphous interface [30], [31]. The nucleation rate I is proportional to:

$$I \propto D\exp(-\frac{W_0}{k_B T}) \tag{1.1}$$

Where T is the absolute temperature and D is the atomic diffusivity, W_0 is the nucleation barrier which the atoms have to overcome in order to nucleate into a crystalline cluster. For a spherical nucleus, nucleating in the bulk, W_0 is calculated as:

$$W_0 = \frac{16\pi\sigma^3}{3\mu^2} \tag{1.2}$$

Where σ is the surface energy and μ is the free energy difference between amorphous and crystalline PC materials. Specifically, μ can be approximately calculated as [32]:

$$\mu = \Delta H(\frac{7T}{T_{melt} + 6T}\frac{T_{melt} - T}{T_{melt}}) \tag{1.3}$$

Where ΔH is the enthalpy of fusion. Thus, W_0 increases as T increases (μ decreases), since the enthalpy difference between crystalline and amorphous diminishes with increasing temperature.

The diffusivity D can be expressed as [33]:

$$D = D_0\exp(-\frac{E_D}{k_B T}) \tag{1.4}$$

where E_D is the activation energy for atomic diffusion in amorphous PC material, D_0 is the pre-exponential factor for diffusivity. Thus, the nucleation rate I can be approximated as:

$$I = I_0 \exp\left(-\frac{E_D + W_0}{k_B T}\right) \tag{1.5}$$

where I_0 is the pre-exponential factor for nucleation rate that contains information about the attempt frequency and size of amorphous region.

On the other hand, the growth rate, u, of the crystalline grains, after nucleation is also proportional to the diffusivity [33]–[35]:

$$u \propto D\left(1 - \exp\left(-\frac{\mu v_p}{k_B T}\right)\right) \tag{1.6}$$

where v_p is the average volume of the particle attaching to the crystalline grain in the growth process and μ is the free energy difference between amorphous and crystalline phases as metioned above. It can be further approximated as:

$$u = u_0 \exp\left(-\frac{E_D}{k_B T}\right)\left(1 - \exp\left(-\frac{\mu v_p}{k_B T}\right)\right) \tag{1.7}$$

where u_0 is the pre-exponential factor for growth rate.

For T much lower than T_{melt}, the term $\exp(-\mu v_p / k_B T)$ is much smaller than 1. This suggests that driving force for crystallization is big since the free energy of the crystalline phase is much lower than the amorphous phase (by μ). Similarly, as μ is very large at low temperatures, W_0 is negligible; such that the nucleation rate, I, has the same activation energy as the growth. As a result, the nucleation rate and growth rate at low temperatures (T < 800 K) can be approximated respectively as:

$$I = I_0 \exp\left(-\frac{E_D}{k_B T}\right) \tag{1.8}$$

$$u = u_0 \exp(-\frac{E_D}{k_B T}) \tag{1.9}$$

Both mechanisms show Arrhenius behavior where the rates are exponentially dependent on $1/T$. and the crystallization time τ_x is effectively given by:

$$\tau_x = \tau_{x0} \exp(\frac{E_x}{k_B T}) \tag{1.10}$$

where τ_{x0} is a pre-exponential factor and E_x is the crystallization activation energy. Note that in this model E_x is numerically the same as E_D, but we use different notations for the activation energy of crystallization and atomic diffusion.

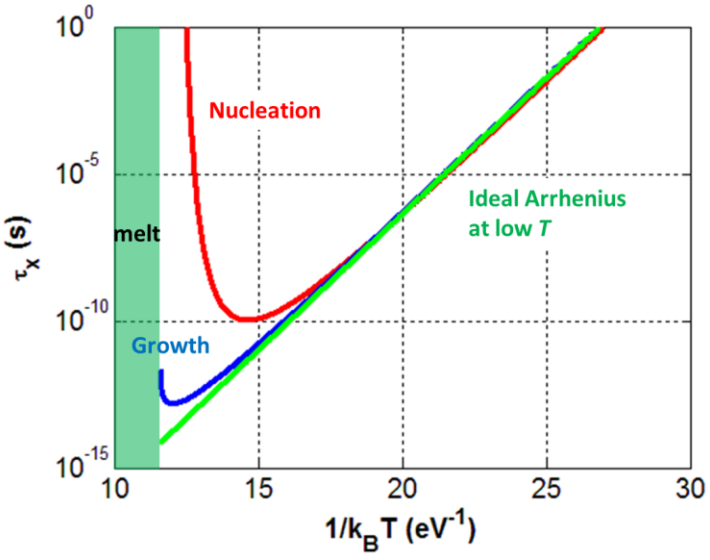

Figure 1.2 The Arrhenius plot schematic for ideal Arrhenius behavior at low T (green), growth-dominated crystallization (blue) and nucleation-dominated crystallization (red)

Typically, only one mechanism dominates during the crystallization process at a particular temperature, making it either a growth dominated process or a nucleation dominated process [31]. Either way, Equation (1.10) describes the temperature-time relation for $T < T_{x,min}$ (the bottom half of TTT curve)

as shown in Figure 1. However, as the temperature goes close to T_{melt} (e.g. in the range of 950 K to 1000 K for GeTe), μ approaches zero and W_0 approaches infinity based on (1.2) and (1.3). As a result, both I and u approach zero and E_x approaches infinity, due to the loss of driving force. This explains the turnover of the TTT diagram that for $T_{x,\min} < T < T_{melt}$ (the top half of TTT curve), τ_x is longer when temperature is higher. Figure 1.2 shows the Arrhenius plot schematic for different mechanisms. The Arrhenius plot is a different way to represent the TTT diagram, by plotting the crystallization time in log-scale versus $1/k_BT$. As explained above, for both nucleation-dominated (red curve) and growth-dominated (blue curve), the turnover of τ_x at high T (> 800 K) is due to the loss of driving force.

1.2.4 Fragility

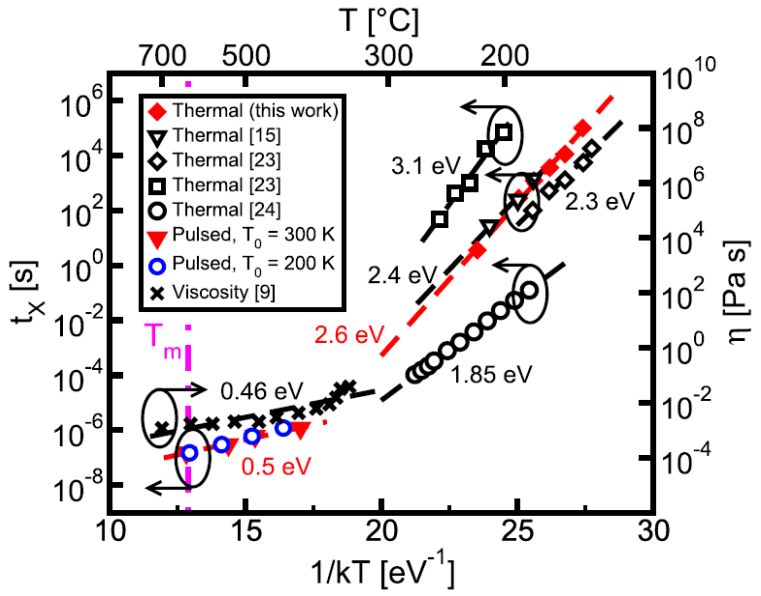

Figure 1.3 Measured crystallization time t_x and viscosity η as a function of $1/k_BT$ using different methods. Adapted from [36].

While the above analysis provides a good starting analytical framework to understand crystallization dynamics as a function of temperature, what is experimentally observed differs somewhat

from the predictions of the above analysis. Figure 1.3 shows the Arrhenius plot of the crystallization time and viscosity, η, in chalcogenides (GST in this case) [36]. The reason for the inclusion of viscosity in the above plot will be evident as we go. It can be seen that at both the crystallization time and η follows two different Arrhenius behaviors with a high E_x (> 2 eV) at low temperatures (T < 600 K) and low E_x (< 0.5 eV) at high temperatures (T > 600 K). The temperature at which this crossover in behavior occurs is much lower than the range in which the loss of driving force occurs. This suggests that this is an effect different from that which causes the "nose" of the TTT diagram above which, rates actually slow down. In Fig 2.1, rates do not actually appear to decrease with increasing temperature. They just increase more slowly above the "kink" point in the curves of crystallization time versus $1/k_BT$.

One possible mechanism for this deviation from a single crystallization process lies in the fragility of the amorphous glass. The amorphous material can behave as a supercooled glass-forming liquid at temperatures above its glass transition temperature [37], [38]. In this concept, the glass transition temperature T_g is defined as the temperature at which the average relaxation time is 100 s or at which the equilibrium liquid has a viscosity η of 10^{12} Pa·s [38], [39]. It is so defined such that the time needed to equilibrate the system becomes of the order of an experimental time scale. Based on a Maxwell equation, η is proportional to the average sheer-stress relaxation time of the glass-forming liquid τ_r, and the high frequency sheer modulus G_∞ [38], [40], [41]:

$$\eta = \tau_r G_\infty \tag{1.11}$$

A simple microscopic picture of free volume in liquid was proposed to give rise to the temperature dependency of τ_r: the liquid is confined as hard sphere cells by surrounding atoms, whose volume V is generally larger than what it should have been for solid V_0 [42], [43]. The free volume is thus defined as:

$$V_F = V - V_0 \tag{1.12}$$

The atom can freely move only if there exists empty cells with volume V_0, the probability of finding which is $\exp(-V_0 / V_F)$. The relaxation time is proportional to the probability of the atom moving:

$$\tau_r \propto \exp(-V_0 / V_F) \tag{1.13}$$

Since the free volume is dependent on temperature:

$$V_F = V_0 \alpha (T - T_0) \tag{1.14}$$

where α is the thermal expansion coefficient. Thus, we can write down the Vogel-Fulcher-Tammann equation (VFT) [38]:

$$\tau_r = \tau_{r0} \exp(B / (T - T_0)) \tag{1.15}$$

The viscosity η can be expressed as:

$$\eta = \eta_0 \exp(B / (T - T_0)) \tag{1.16}$$

where η_0 is the pre-exponential factor for viscosity, B and T_0 are constants, B controls how close the system follows the Arrhenius behavior. As T decreases from the T_{melt} to T_0, the probability of liquid atoms finding available spaces to move decreases and the viscosity of glass-forming liquid increases exponentially.

For strong glasses such as SiO_2, η follows the Arrhenius behavior from T_{melt} down to T_g [37]–[39]. Whereas fragile glasses such as chalcogenide PC materials, η follows the Arrhenius behavior at high T (T close to T_{melt}), with low E_x (< 0.5 eV) that is similar to the activation energy of atomic diffusion, while at low T (T close to T_g), E_x is high (> 2 eV) and [44], [45]. Note that in this model, only the behavior at high T is considered as Arrhenius, while at low T, it is usually referred as non-Arrhenius or super-Arrhenius.

This behavior for fragile glass-forming glass also occurs in the atomic diffusivity and the growth velocity, because the viscosity and the atomic diffusivity D has the following correlation based on Stokes–Einstein relation (SER) [37]:

$$D = \frac{k_B T}{6\pi\eta R} \tag{1.17}$$

where R is the radius of the spherical particle. Finally, D can be expressed as:

$$D = \frac{k_B T}{6\pi\eta_0 R}\exp(-\frac{B}{T - T_0}) \tag{1.18}$$

Thus, D is dependent on η, which in turn leads to the non-Arrhenius dependent growth of crystalline phase at high T.

The fragility index m [39], which describes the degree of fragility for the glass-forming liquid, is directly correlated to B and can be described by:

$$m = d\log_{10}(\eta)\Big/ d\frac{T_g}{T}|_{T=T_g} \tag{1.19}$$

Combining (1.16) and (1.19) we have:

$$m = \frac{BT_g}{2.3(T_g - T_0)^2} \tag{1.20}$$

The typical value of m for strong glass-forming liquid (such as SiO_2) is 16, while for fragile glass-forming liquid (such as chalcogenides) is 200 [39].

The fragility model described by VFT works well when T is above T_g. but not for lower T. Arrhenius behavior with activation energy of around 2 eV has been observed for GeTe to be valid down to 440 K [46], [47], which is on lower bound of T_g for GeTe-based chalcogenides (reported values range from 430 K to 530 K [35], [39], [48]). One possible explanation is that the VFT based fragility model tends to overestimate η (or the activation energy for η) at low T. One issue of the VFT is the asymptote at T_0 and modified version of VFT was proposed [49] to address that. Moreover, evidence of SER breakdown has been observed for

chalcogenides [50] when T is near or below T_g and D can be underestimated based on (1.18). Thus, the measured temperature dependency of crystallization rate may not be accurately described by VFT.

1.2.5 Multi-excitation Entropy

Since experimental data for chalcogenides at T near or below T_g shows Arrhenius behavior with a higher temperature independent E_x (> 2 eV) rather than a temperature dependent E_x as suggested by VFT, the fragility model is not universal. This suggests that a different modality of crystallization with a constant E_x is present and dominates the process at low T due to the lower E_x and faster crystallization rate comparing to the fragility model. However, if such modality is valid for the entire temperature range, the crystallization process should have been much faster (10 – 100 fs rather than 10 – 100 ns for GeTe) due to the extremely strong temperature dependency of the crystallization rate even at high T. This is not true because the pre-exponential factor for crystallization time τ_{x0} is unphysically small at low T (of the order of 10^{-24} s) will increase while increasing T. That the temperature dependent pre-exponential factor "compensates" the rate at low temperatures with high E_x is a widely observed phenomena and is often phenomenologically labelled as the Meyer–Neldel (MN) rule [51], [52].

In [50] and [51], an empirical correlation between ΔS and ΔH is described as:

$$\Delta S = \frac{\Delta H}{T_{MN}} \tag{1.21}$$

where T_{MN} is an empirical MN temperature. A unified mechanism of two different modalities with different activation energies, structural relaxation and crystallization, was proposed in that work. It attributes the change in ΔS and the pre-exponential factors to the change in ΔH due to different modalities in different temperature regimes.

To explore the physical insights of this behavior, the theory of multi-excitation entropy can be applied [53], [54]. The temperature dependent free energy activation energy ΔG can be decoupled into an entropy term ΔS and an enthalpy term ΔH. Since free energy is given by:

$$\Delta G = \Delta H - \mathrm{T}\,\Delta S \tag{1.22}$$

The relaxation time can be written as:

$$\tau_r = \tau_{r0} \exp(\frac{\Delta G}{k_B T}) = \tau_{r00} \exp(-\frac{\Delta S}{k_B}) \exp(\frac{\Delta H}{k_B T}) \tag{1.23}$$

where τ_{r00} is a temperature independent pre-exponential factor that is fairly unchangeable (atomic vibration frequency $\tau_{r00}^{-1} \sim 10^{13}\ s^{-1}$). The enthalpy of activation ΔH depends on the crystallization modality at different temperatures. For a given crystallization modality and ΔH, multiple excitations are required to provide large excitation energy. The entropy of activation ΔS can be expressed based on the Bolztmann statistic:

$$\Delta S = k_B \ln(W) \tag{1.24}$$

where W is the number of microscopically distinct states which give rise to the same macroscopic thermodynamic state. The W can be further expressed based on the number of combinations of choosing required phonon excitations to overcome the barrier from a bath of phonons:

$$W = \frac{N!}{n!(N-n)!} \tag{1.25}$$

where n is the number of phonon excitations necessary to pass the barrier ΔH and N is the total number of phonons within a interaction volume, which in this context, is the amorphous volume to be crystallized. We can also correlate n and ΔH as:

$$n = \frac{\Delta H}{E_E} \tag{1.26}$$

where E_E is the energy associated with each quantum. Finally, the pre-exponential factor τ_{r0} can be written as:

$$\tau_{r0} = \tau_{r00} \frac{n!(N-n)!}{N!} \tag{1.27}$$

In other words, at low temperature, the need for large number of excitations to achieve high excitation energy results in high entropy, and lowers the τ_{r0} to unphysically small value (and attempt frequency to unphysically high value); while at high temperature, the possible number of combinations is so small that the τ_{r0}^{-1} is fixed at the atomic vibration frequency τ_{r00}^{-1}. The specific values for n and N depend on the material and the interactive volume [54]. Only if $n << N$ and N is independent of ΔH, we can obtain the MN rule described by (1.21). However, temperature dependencies of n and N have not been explored. Thus, it is still not clear if the two distinct activation energies at different temperature regimes (e.g. 2 eV and 0.5 eV for GeTe), are due to modality switching, temperature dependency of the activation free energy (as proposed in the fragility model) or temperature dependency of the entropy term.

1.2.6 Threshold Switching

Threshold switching is a simultaneous and reversible transition from the OFF-state to the ON-state when the voltage applied to the amorphous PC material exceeds certain threshold V_{th} in the I-V characteristic. As a result, a highly conductive state of amorphous material is formed. Afterwards, significant increases in device current cause Joule heating and memory switching due to crystallization. Memory switching has a known mechanism that is the same as explained by the classic crystallization theory in section 1.2.3. Threshold switching is essential in reducing SET voltage for two-terminal PC devices, such as memory cells, where direct Joule heating inside the PC material is required to transform it between two states. Since the OFF-state resistivity is very high ($> 1\Omega\cdot$m), if threshold switching were not allowed, it would have required SET voltage that is orders of magnitude higher than the available voltage headroom in modern electronic devices to achieve reasonable power and generate enough heat for the memory switching. On the other hand, threshold switching and V_{th} determines how much voltage and power that the PC material in the OFF-state can withstand without being transformed to the ON-state.

The physical mechanism of the threshold switching is still not clear. Several hypotheses, such as Poole-Frenkel conduction and field-induced carrier generation, are invoked to explain subthreshold non-

linear I-V characteristic and threshold switching observed in GST memory devices. The Poole-Frenkel model suggests a trap-limited model and is field-induced and thermally activated. It can explain the subthreshold conduction well [55], but is not able to address the switching effect alone and other models such as nonequilibrium carrier distribution or non-uniform electric field are required [56]–[58]. The field-induced carrier generation model suggests that hot electrons are generated from traps through a field-induced process. The positive feedback event of electrons obtaining kinetic energy through the electric field and creating more electrons through collisions eventually allows the conductive path forming [59]–[62]. A simplified model of field-induced carrier generation is shown as following. The p-type amorphous material conductivity is given as:

$$\sigma = q\mu_p p_0 / (1 - g(E)\tau_0) \tag{1.28}$$

where μ_p is the hole mobility, p_0 is the intrinsic hole density, τ_0 is the recombination time constant, $g(E)$ is the field-induced generation rate, given by:

$$g(E) = A\exp(-\frac{E}{E_0}\frac{1}{k_B T}) \tag{1.29}$$

These models suggest that threshold switching is a result of negative differential resistance (NDR), i.e. that for the device under test, $dV/dI \leq 0$. Thus, by letting $g(E) = \tau_0^{-1}$, the threshold field E_{th} can be extracted as [59]:

$$E_{\text{th}} = k_B T E_0 \log(A\tau_0) \tag{1.30}$$

By experimentally idendifying the NDR event, we can extract material related parameters such as τ_0, A and E_0 to better estimate E_{th}.

One alternative hypothesis is field-induced nucleation switching initially suggested by Ovshinsky [28]. In this hypothesis, the crystallization nucleation barrier decreases with increased applied electric field. In a classical crystallization model, the system free energy G is given by:

$$G = -\Omega\mu + A\sigma + W_E \tag{1.31}$$

where Ω is the volume and A is the surface area of the nuclei, W_E is the electrostatic energy. It assumes spherical nuclei, so $\Omega = 4/3\pi r^3$, $A = 4\pi r^2$ and $W_E = -r^3 E_0^2 \varepsilon / 2$ where r is nuclei radius. At critical radius $r_0 = 2\sigma / \mu$, the nucleation barrier with the absence of electric field W_0 is given by Eq. (1.2). With the presence of electric field, the nucleation barrier W is given by:

$$W = W_0 (1 + E_0^2 r_0^3 \varepsilon / W / 4)^{-2} \tag{1.32}$$

E_0 is the applied electric field and nucleation barrier W decreases with increasing E_0.

V. G. Karpov *et al.* [63]–[66] proposed a modified model in which a needle shaped nucleus is suggested instead of a spherical shape. Two geometry factors, height (h) and radius (r) of the needle, are used. As a result of the strong depolarizing fields the of needle shape, W_E is smaller than for the spherical case and is dependent on the ratio, h/r. By mapping the free energy in two dimensions, they found that the nuclei tend to grow along the direction of electric field (increase h) while keeps the radius at the minimum radius (αr_0). Note that this radius is smaller than r_0 by the factor α (<1) and is the considered the minimum needle radius for the needle nuclei to be stable. Assuming $h >> r$, W can be rewritten as:

$$W = W_0 \frac{\tilde{E}}{E_0}, \tilde{E} = \sqrt{\frac{3\pi^3 \alpha^3 W_0}{32\varepsilon r_0^3}} \tag{1.33}$$

with $\tilde{E}$ defined above as a kind of characteristic field. They also introduced delay time τ_D, defined as the time it takes for PCS to switch to the ON-state at constant electric field E_0.

$$\tau_D = \tau_{D0} \exp\left(\frac{W}{k_B T}\right) \equiv \tau_{D0} \exp\left(\frac{W_0 \tilde{E}}{k_B T E_0}\right) \tag{1.34}$$

This time, τ_D, has an Arrhenius dependence on E_0^{-1}. For $E_0 >> \tilde{E}$, the theory is in consistent with their observation from measurements on GST based devices.

1.2.7 Section Summary

In this section, mechnisms have been introduced to explain phenomena in the phase change crystallization process and threshold switching event. These models provide physical insights and are in good agreement with reported data. In the next few chapters, we will apply these models to analyze crystallization rate and threshold voltage data in our expierments to identify the operating mechanisms. Specifically, we will examine the consistency between threshold voltage data and NDR/nucleation switching models in Chapter 4. We will also combine the classic nucleation theory and the fragility model with our crystallization rate data to quantitatively explain the crystallization process in Chapter 6 and Chapter 7.

1.3 Application in RF Switch Technologies

1.3.1 RF Switch Technologies

RF switches in Reconfigurable RF can be used to route RF signals from different inbound ports to outbound ports. Finer grain reconfigurability can be achieved by allowing the circuit to switch between components with different RF properties [14]. It has been demonstrated that the RF switches can be used for reconfiguring inductors [67], inductive-capacitive voltage controlled oscillators (LC-VCO) [68], [69], low noise amplifiers (LNA) [70], [71], power amplifiers (PA) [72], [73], antennas [74], [75], etc. using various technologies.

An RF switch needs to be appropriately designed to meet the circuit specifications. By setting the RF switch to its OFF-state, it should efficiently block the RF signals. On the other hand, an ON-state RF switch should allow signal to pass through without degrading the signal significantly. Thus, an ideal OFF-state RF switch is expected to behave as an open from the input and output ports (high isolation), while an ideal ON-state RF switch should not introduce any additional resistance along the signal path (low insertion

loss). It is desirable that RF switches have low ON-state resistance R_{ON} (smaller than 1 Ω) to achieve low insertion loss, high OFF-ON ratio R_{OFF}/R_{ON} (larger than 10^4) and low OFF-state capacitance C_{OFF} (smaller than 20 fF) to achieve high isolation. A commonly used figure of merit is the cutoff frequency f_{CO}, given by $1/(2\pi R_{ON}C_{OFF})$.

CMOS RF switch is a commonly used technology due to the CMOS compatibility and convenience to integrate with circuits. However, to achieve low R_{ON}, CMOS switches are large in size and have poor isolation due to large capacitance [76]–[78].

Alternatively, f_{CO} can be improved by using other non-silicon based technologies. It has been demonstrated that MEMS RF switches with high f_{CO} can be applied to reconfigurable RF circuits. However, a large bias voltage (typically > 20 V, but it has been demonstrated down to 15 V) [79] is required on the switch to maintain its ON-state, which makes it not practical in systems with limited supply voltage, such as RF systems in cell phones. Also, reliability and robustness of MEMS RF switches remain to be improved [74], [76]–[80].

High electron mobility transistors (HEMTs) technology using III-V materials is another option. HEMTs can be designed to have low R_{ON} due to the high carrier mobility in the channel, and also show great power handling capability for applications in PA. However, since a different substrate is required for this technology, it is difficult to monolithically integrate HEMTs with CMOS process [76], [77], [81].

Phase change switch (PCS) is the RF switch technology that this thesis will be focused on. The unique property of PC materials makes it possible to use resistivity in two phases to represent two states in a single pole single throw switch: high resistivity for OFF-state and low resistivity for ON-state. PC materials are very attractive due to their low ON-state sheet resistance and can be built into RF switches with high f_{CO}. The ON-OFF conductivity ratio is usually in the order of from 10^5 to 10^7 depending on the materials [29], [47], [82]. Moreover, due to its non-volatility, the static power consumption is zero since it is not required to maintain the states. Only programming power is needed to transform the switch between

two states. This property will significantly reduce the power consumption for the entire system. Also, although carefully engineer of heat sink is required, PCS can be monolithically integrated with CMOS process.

1.3.2 PCS Designs

The design considerations of PCS with high f_{CO} include the material selection, the device architecture and the geometry design. For material selection, GeTe is typically chosen instead of $Ge_2Sb_2Te_5$ (GST), which is commonly used in memory devices, since GeTe has much lower resistivity (10^{-6}-10^{-5} Ω·m) than GST (10^{-5}-10^{-4} Ω·m) [29], [82], [83].

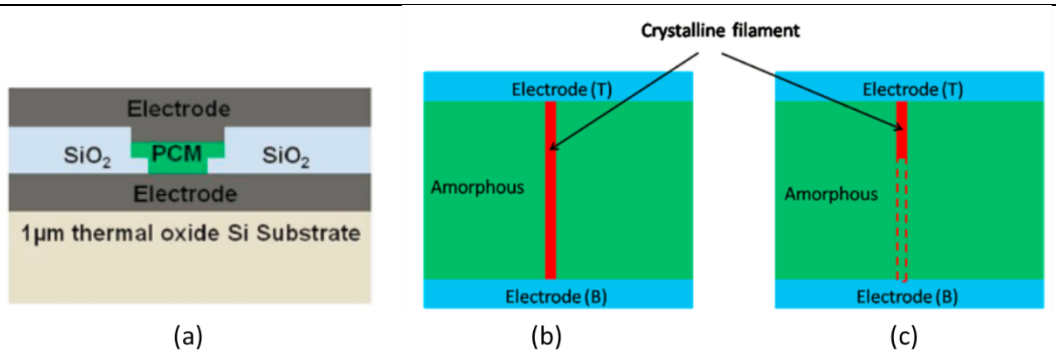

Figure 1.4 (a) cross-section schematic of the two-terminal PCS (b) the crystalline filament forms during the SET operation that shorts the electrodes (c) RESET operation amorphizes part of the crystalline filament. Adapted from [82].

Different device architectures have been proposed to achieve high f_{CO}. As shown in Figure 1.4 (a), a two-terminal GeTe PCS was demonstrated by E. K. Chua *et al.* [82]. GeTe is sandwiched by two metal layers on top of a thick thermal oxide layer on silicon substrate. Sourcing current from one metal contact to the other through GeTe will generate Joule heat inside it. A thermal oxide layer is used to electrically isolate the bottom electrode from silicon substrate and provide thermal isolation to reduce programming power. The magnitude and duration of current pulses can be controlled to SET, RESET or read the PCS.

However, with the intended low R_{ON}, it is impractical to deliver enough current and power to melt GeTe due to the power reflection caused by impedance mismatch between PCS and source. From a compatibility point of view, one would have to design huge transistors (10 times larger than the PCS itself in area) in order to source enough current to RESET the PCS, which will increase the total capacitance and decrease the bandwidth of the system. Another issue is the incomplete crystallization due to the filament formation when transforming GeTe from amorphous phase to crystalline phase. Since the memory switching is triggered by the threshold switching, a conductive filament with very small radius (100 nm – 300 nm, calculated based on resistance values and dimensions in [82]) will form once the field applied along the signal path exceeds the threshold field as shown in Figure 1.4 (b) and (c). Due to the low resistivity of the conductive filament, the surrounding amorphous materials are "shorted" and most of the current is drawn through the filament. The radius of the filament will grow due to the continuous crystallization of the surrounding amorphous region, but eventually reach a steady state condition in which the radius stops increasing. As a result, it is not possible to crystallize the entire volume of the PC material, leading to a high ON-state resistance after SET operation.

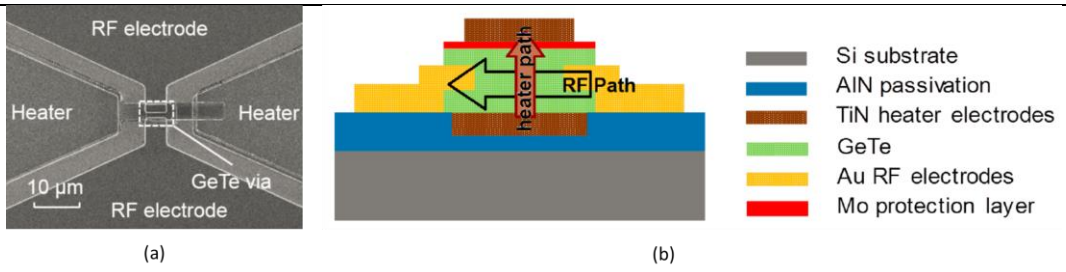

Figure 1.5. (a) top view SEM image and (b) cross-section schematic of the four-terminal directly heated PCS. Adapted from [84].

A four-terminal directly heated PCS was demonstrated by M. Wang *et al* [84]. In this architecture, as shown in Figure 1.5, two TiN heaters are vertically connected through a GeTe layer that needs to be transformed, forming the programming path. Two RF electrodes are laterally connected through the GeTe

layer, forming the signal path. Decoupling the programming path from the signal path allows separate engineering of the heaters so that the joule heating is not directly generated inside the PC material. In this case, one can avoid the incomplete crystallization during the SET operation. However, the signal path is still electrically connected with the programming path, results in a low impedance path when the PCS is in the OFF-state, making it impractical in real system since the heater cannot be left floating.

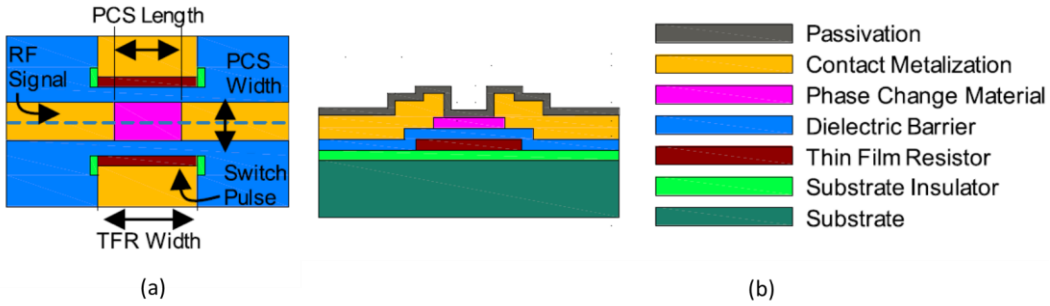

Figure 1.6. (a) top view and (b) cross-section view schematics of the four-terminal indirectly-heated PCS. Adapted from [41].

N. El-Hinnawy *et al.* firstly demonstrated a 4-terminal GeTe PCS that can be controlled by a heater electrically isolated from the switch signal path [76], [85]–[87]. As shown in Figure 1.6, a thin film heater is built on top of an insulating substrate. The PCS and the heater are thermally connected by a dielectric barrier layer. It is called an indirectly-heated PCS since the programming path is decoupled from the signal path and one can engineer the material and geometry of the heater in order to achieve maximum power transfer and meet both voltage and current constraints. By sending electrical pulses with different voltages and pulse widths to the heater, one can deliver enough heat into the PCS and SET/RESET it to the ON-state/OFF-state by controlling the duration and voltage of the pulses. In the case of integration with CMOS circuits, source transistors can be designed to be much smaller and the bandwidth does not need to be sacrificed to meet the power requirement. Decoupling the two paths provides design space not only for the programming power and R_{ON}, but also for C_{OFF}, which is determined by the dielectric barrier thickness and

the overlapping area between the heater and the PCS. This design also enables the scaling capability – the performance of the switch will be improved as the size becomes smaller and smaller.

Although compared to the directly heated PCS design, this design has a higher power because of the thermal gradient between the heater and the PC layer, various methods can be applied to lower the power consumption. One approach is to decrease the barrier layer thickness to minimize the temperature gradient. But this approach will increase the coupling capacitance between the PC layer and the heater, resulting in poor RF performance. Another approach is to use barrier material that has high thermal conductivity and is also insulator. G. Slovin *et al.* has shown that using AlN as the barrier material is beneficial for this power-capacitance trade-off. Due to its high thermal conductivity (130 W/m-K for sputtered films), it allows lower power without sacrificing the capacitance [88]. It has been shown that one can improve the f_{CO} by 50% with only 14% increase in the maximum power required to RESET the switch.

1.3.3 PCS in RF Circuits

Previous work have shown basic reconfigurable RF components using PCS and integration prototypes of the PCS with RF circuits through flip-chip bonding process. Figure 1.7 shows a reconfigurable inductor demonstrated by C.-Y. Wen *et al.* using the two terminal directly heated via style PCS [67]. They achieved a 110% inductance change using the PCS with a reasonable quality factor (12.4/5.8). Following this work, C.-Y. Wen *et al.* demonstrated a reconfigurable LC VCO using the two-terminal via style PCS. In this work, the PCS chip was flip-chip bonded to the VCO CMOS. Switches were applied to inductors in the LC tank for frequency tuning. The VCO can be reconfigured between 4 and 7 GHz or 4.5 and 5.5 GHz depending on the connection configurations of reconfigurable inductors. These initial trials of using the PCS to reconfigure RF component show the potential of using it in larger circuits and systems. However, due to the incomplete crystallization in the via-style PCS, multiple crystallization pulses were required to fully SET the PCS to the designed ON-state.

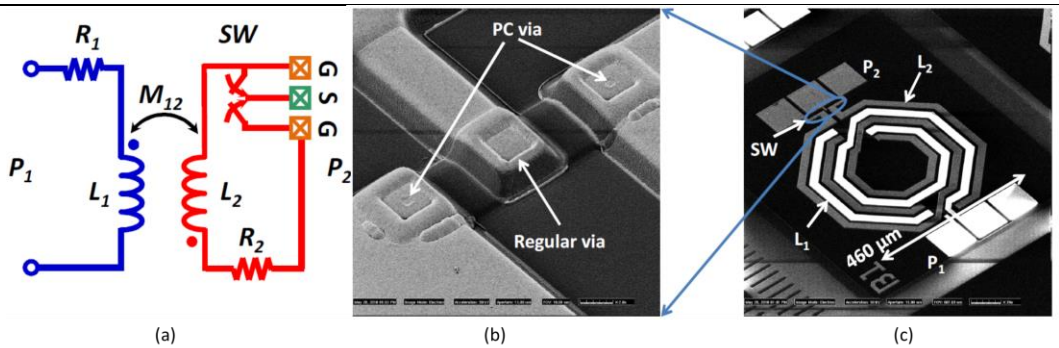

Figure 1.7. (a) circuit schematic of the reconfigurable inductor (b) SEM image of the PC via (c) SEM image of the reconfigurable inductor. Adpated from [67].

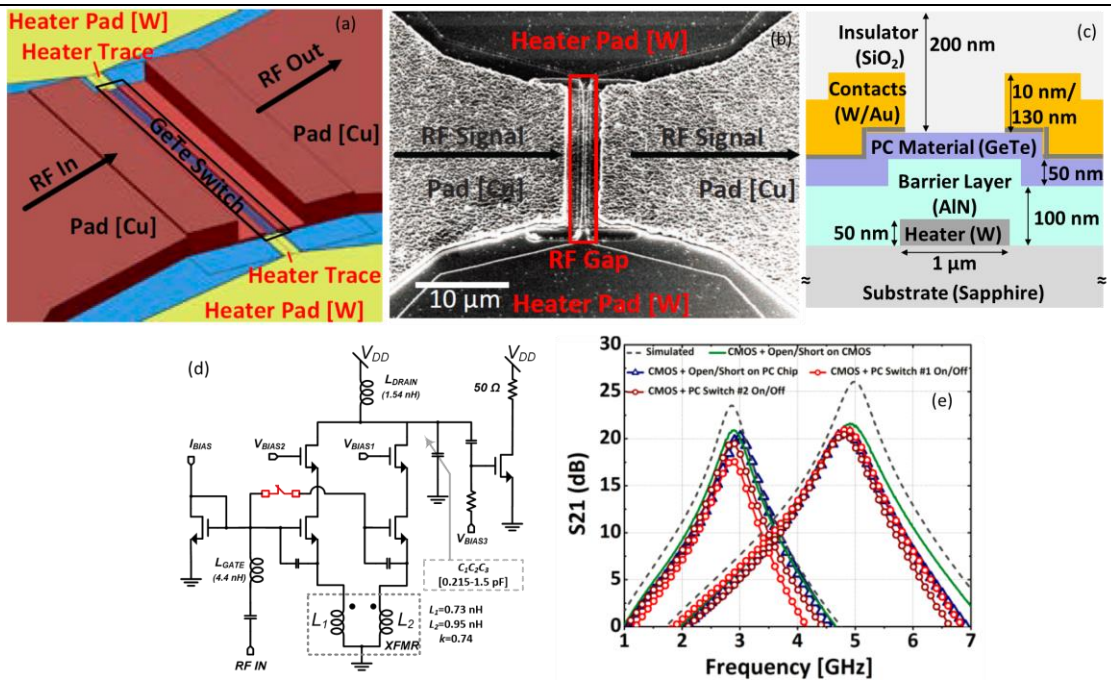

Figure 1.8. (a) 3-D perspective view (b) top view SEM image and (c) cross-section schematic of the four-terminal indirectly-heated PCS for use in the reconfigurable LNA. (d) circuit schematic of the reconfigurable LNA (e) S21 response at 3/5 GHz modes achieved by simulation, open/short on CMOS, open/short on PC chip and ON-state/OFF-state PCS. Adapted from [70] and [88].

R. Singh *et al.* demonstrated a working prototype of integrating the four-terminal indirectly-heated PCS with foundry taped-out CMOS LNA through flip-chip bonding process as shown in Figure 1.8 [70]. In the reported PCS, AlN was used as the barrier layer to achieve better f_{CO} with lower power. Sapphire is selected as the substrate material to minimize the RF loss through the substrate. The PC material Ge_xTe_{1-x}, was sputtered from two elemental targets and was optimized to have the lowest possible resistivity in the ON-state, which significantly reduced the PCS ON-state resistance and improved the f_{CO} of the PCS and the noise figure of the LNA. Figure 1.8(d) shows the measured versus simulated S21 with different switch configurations and comparison groups. The LNA can be reliably reconfigured between 3 and 5 GHz modes, and using the PCS presents almost the same performance as using an ideal short and open on the CMOS chip.

1.3.4 Objective for RF PCS

The results of the above work show that the four-terminal indirectly-heated PCS is an extremely promising technology and can be further applied in more complex RF systems such as transceivers and make them reconfigurable. However, there is a huge space for performance improvement such as power consumption and power handling.

In low power applications, the voltage and power are limited for switching the PCS. Although we can use high thermal conductivity materials as the barrier layer, the improvements in power consumption, especially the maximum required power during RESET operation, are still limited. Alternatively, we improve the power by engineering the heat sink below the heater. However, there is a trade-off between the speed and the power of the PCS. In order to lower the power, the thermal resistance between the heater and the thermal ground needs to be as high as possible, which in turn slows down the RESET speed. From a PC material amorphization point of view, a slow thermal response could lead to an unsuccessful RESET due to the slow quench. Thus, a major focus of this thesis will be on studying the PC material electro-thermal properties and crystallization dynamics and understanding the design trade-off between the speed (also the functionality) and the power of the PCS.

In reconfigurable RF power amplifier applications, large signal PCS that can handle watt-level (> 1 W) RF signals is desired, such that the PCS can maintain the states while high voltage RF signal is being continuously applied to it. Also, the PCS has to withstand high power (> 1 W) without significant distortion in the linearity, which may be caused by heating and non-linear conduction inside the materials. This is not a major concern when the PCS is in the ON-state, since the crystalline PC material shows metallic behavior and very good linearity. On the other hand, the thermal time constant of the device is 10 – 100 higher than that of the RF signals, as a result, the heating effect is not significant. This is because the frequency of temperature changes cannot follow the RF frequencies, and it is the RMS power instead of the peak power that contributes to the heating. But for the PCS in the OFF-state, as discussed in the previous section, a threshold switching can be triggered when the voltage applied directly to PCS reaches threshold voltage V_{th}. If the peak-to-peak voltage of RF signal applied to the PCS exceeds V_{th}, this reversible "break down" event will occur to the PCS and the PCS will fail to maintain the OFF-states. Thus, the threshold switching behavior is the limitation for high power handling capability of the PCS. This thesis will also discuss the understanding of the threshold switching behaviors.

1.4 Application in Memory Technologies

1.4.1 Emerging Non-volatile Memories

Unlike volatile memories such as SRAM or DRAM, non-volatile memories do not require voltage bias and power to maintain the states of information stored in the cells. Flash memory, which is based on floating gate MOSFETs that allows electrical pulses to inject or remove charges from the floating gate, has been a production level technology for more than a decade [16], [89], [90]. However, it has always been treated only as a competitive technology to magnetic hard drive or external storage devices [21] due to its slow read and write time as well as low reliability comparing to SRAM and DRAM.

Spin-transfer torque magnetic RAM (STT-MRAM) [15], [16], [90] is a promising technology that allows spin-polarized current to change the magnetic orientation in a magnetic junction layer, which will

result in different resistance states depending on the polarity difference between the free layer and pinned layer. This technology has fast read and write time (< 20 ns) and can be potential replacement for DRAM [90]. However, the trade-off between switching current/power and data thermal stability becomes the scaling limitation for this technology [90].

Resistive RAM (RRAM), another technology targeting to replace DRAM, has great compatibility with CMOS, fast write time (< 20 ns) and high density [90]. RRAM is typically a two-terminal metal-insulator-metal device where the insulator materials can be switched between different states with various resistivity by electrical pulses. A conductive filament is formed when the voltage applied to the device exceeds a certain threshold. However, the endurance of RRAM (around 10^6 cycles) remains to be addressed for it to become a production level technology [90].

The properties of phase change materials make it also good candidate for non-volatile memory. The performance and power of phase change memory (PCM) scales with the cell size (demonstrated down to 45 nm node) [15], [17], [27], [91], which enables ultra-high density production. On the other hand, like RRAM, PCM is also CMOS backend compatible [92]. The data retention time can be more than 10 years [91], [93], and the endurance has been demonstrated to be more than 10^9 [17], [91], making it a good replacement for Flash memory [15], [17], [24], [27]. Other work has been done to improve the bit per area by implementing multibit per cell storage for PCM [94][95]. Also, to improve the density, CMOS-less selectors using ovonic switching oxide materials have been studied to enable 3D integration of multilayer PCM [25]. The write time is limited by the crystallization process and is around 50 to 100 ns [15], [17], [27], [91], [96], making it not suitable for replacing DRAM at the current stage. However, due to the growth dominated crystallization for GeTe-based PCM, it has been shown that highly scaled PCM cell can achieve sub-10 ns switching in both SET and RESET operation [97], suggesting that this technology still has great potential for being used as the unified memory with extremely high density and low cost [23].

1.4.2 PCM Designs

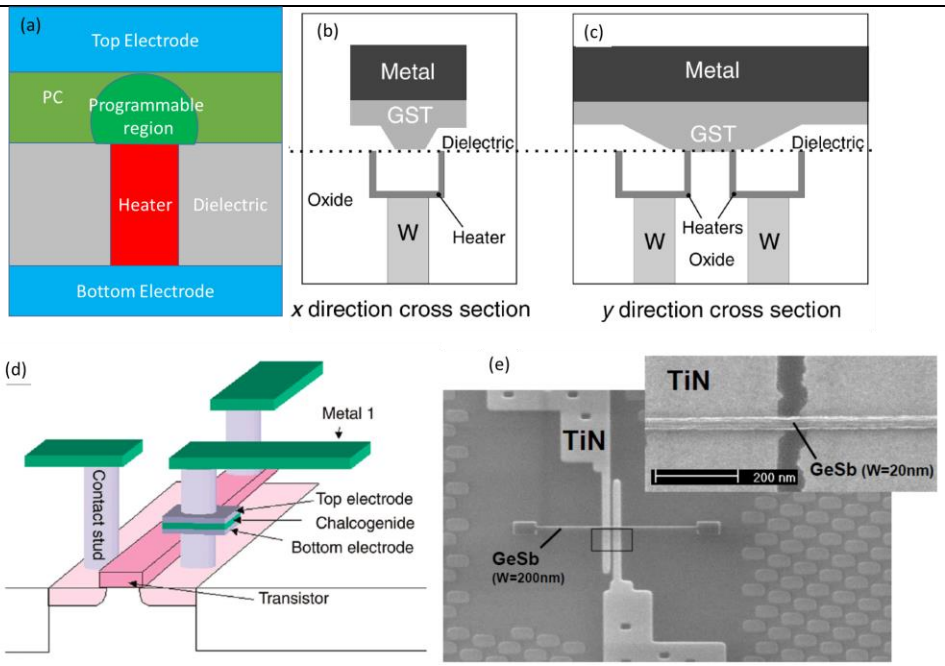

Figure 1.9. (a) cross-section view of the mushroom type PCM architecture, adapted from [91]. (b) x direction and y direction cross-section views of the micro-trench PCM architecture, adapted from [58]. (d) 3-D schematic of integration of PCM and MOSFET, adapted from [98]. (e) phase change bridge, adapted from [99].

A scalable design is needed to compact PCM cells and provide high speed and low power. As shown in Figure 1.9(a), a mushroom type architecture has been widely adapted. The PC layer sits on top of a heater cylinder and the top of the PC and the bottom of the heater are connected to metal interconnections [91]. By sending current through the electrodes, Joule heat can be generated at the interface of the heater and the PC layer, forming a mushroom like hot zone. In the hot zone, the PC material can be transformed between crystalline and amorphous phases, representing "0" and "1". Figure 1.9(b) and (c) show the micro-trench design proposed by F. Pellizzer *et.al* [92], [100], which allows better heat confinement and heating efficiency for low programming current. In this design, U-shape heaters are buried beneath the PC layer, mostly separated by dielectric with small contact regions. However, bad interface between the heater and

the PC layer causes reliability issues, leading to another design in which the heater cylinder in the mushroom structure is replaced with PC materials [93]. Confining the programmable region of PC materials in a smaller space farther away from the electrodes will benefit both power and endurance.

This two-terminal vertical device architecture is most commonly used due to its simple structure, ease of fabrication and compatibility with CMOS process. Figure 1.9(d) shows the 3-D schematic of how PCM can be integrated with MOSFET in the CMOS process [98]. Alternatively, signals can go through the PCM in the lateral direction rather than the vertical one, similar to the designs in RF PCS. Figure 1.9(e) shows a phase change bridge (PCB) design [99], where two TiN electrodes were located on top of the ultra-thin (< 10 nm) PC line, allowing small threshold voltage for RESET and fast switching. This design potentially allows less sensitivity due process variation comparing to the conventional vertical structures.

1.4.3 Objective for PCM

As one of the major limitations for PCM to become the next generation unified memory is the writing speed, specifically the crystallization speed, it is critical to understand the limitation and improve it. As discussed previously, at $T_{x,min}$, the shortest crystallization time $t_{x,min}$ can be observed. It is necessary to identify the temperature and time at which the fastest crystallization occurs and understand the limiting mechanism. However, the crystallization dynamics of chalcogenides have strong non-Arrhenius behavior, making them difficult to be predicted using simple models. Thus, this thesis will discuss the understanding of the crystallization dynamics at both low T and high T, as well as the methodologies and test vehicles developed for this study.

1.5 Thesis Outline

The thesis will discuss the study of crystallization dynamics and electro-thermal properties of PC materials for use in both RF switch and non-volatile memory applications, and how these properties can be applied to advance these technologies.

Chapter 2 will discuss the accurate thermometry of the high temperature high speed thin-film micro-heater, which can be used as the external heat source to transform the PC materials. It is critical for estimating the temperature transients for any given electrical inputs as well as measuring the electro-thermal properties of PC materials. Heater reliability measurements and evidence of electro-migration as the heater failure mode will also be presented.

Chapter 3 will discuss the design and fabrication of the 1st generation PCS test device (1st gen device) and the methodology used to achieve in-situ measurements of crystallization dynamics of PC materials. Measurements of critical quench time (CQT), the longest temperature cooling time constant allowed for successful PC material amorphization, will be presented, which is important for defining the design space of low power RF PCS. It will also discuss the crystallization time measurements of PC materials, which shows evidence of non-Arrhenius behavior at different temperature regimes.

Chapter 4 will discuss the threshold voltage (V_{th}) study of amorphous PC materials, as understanding the threshold switching mechanism is useful for building RF PCS with higher power handling capability. Several important observations will be presented for the amorphous GeTe: the non-NDR threshold switching, time dependent V_{th}, and the size dependent variation of V_{th}. The understanding remains incomplete, but the observed scaling relationships provide useful insights into the threshold switching mechanisms and can be used in estimating V_{th} for various devices.

Chapter 5 will discuss the design and fabrication process of the 2nd generation PC test device with nano-scale dimensions and ultra-high speed (2nd gen device). It will be used to study crystallization dynamics in the high T (T > 700 K) regime with crystallization time down to sub-10 nanosecond. This is important for studying and quantifying the non-Arrhenius behavior of PC materials, which is one possible mechanism that sets the limitation for building non-volatile PC memory devices with ultra-fast writing speed.

Chapter 6 will discuss the study of crystallization dynamics and quantification of non-Arrhenius behavior of PC materials using the 2nd gen device, with the crystallization time ranging from millisecond to sub-10 nanosecond and the temperature ranging from 480 K to 1000 K. The limitation of the crystallization speed will be presented. The comparison between two sets of crystallization measurement results using the 1st gen device and the 2nd gen device will be shown, which provides evidence of growth-dominated crystallization.

Chapter 7 will show the applications of different models to explain the non-Arrhenius behavior. Growth and nucleation dominated models and a fragility-based model will be examined. The fragility model shows good agreement with the experiments and other reported data. A unified framework is developed to estimate the performance of RF switches by simulating the crystallization process using the fragility model and can potentially be used to assist in designing better RF switches. Specifically, CQT (for low power consumption), V_{th} (for high power handling capability) and its variation can be estimated for any given electrical inputs and device architecture. Validation of this framework using the data from the CQT measurements will be presented. Finally, correlations between V_{th} and power will be simulated based on an appropriately designed RF PCS using this framework, providing insights on the design trade-offs.

Chapter 8 will summarize the study in this work and list the major contributions, and discuss the possible future work for improving the performance of RF switches and memory devices.

Chapter 2: Thin Film Micro-Heater Design and Thermometry

2.1 Abstract

An embedded thin film micro heater is a critical component in a PCS as it determines the functionality and power consumption of the PCS. It has been shown that an embedded micro heater or thermal stage can be used to study the thermal properties and crystallization dynamics of phase change materials [101], [102]. Thus, designing a heater that can enable in-situ measurement of eletro-thermal properties of phase change materials can be very useful to understand the crystallization dynamics. In this chapter, a thin film micro heater is designed to serve this purpose, and a thorough study and experiments of heater thermometry will be presented. The heater described in this chapter can reliably reach 1664 K at a rate of 1.67×10^{10} K/s and quench to room temperature with a thermal RC time constant (time for T to fall by a factor of e) of less than 40 ns. Time domain transmissometry was used to measure heater temperature transients for given electrical inputs. Finite element modeling results on heater temperature transients show a good consistency between experiments and simulations with 0.2% mismatch in the best case and 13.1% in the worst case.

This heater is used in the 1st generation phase change switch test device (1st gen device) presented in Chapter 3. The 1st gen device provides reasonably fast thermal response (thermal time constant around 40 ns) and can be fabricated using simple optical lithography processes. On the other hand, the 2nd gen device, defined by more complicated E-beam lithography processes, will be discussed in Chapter 5 and Chapter 6. The 2nd gen device consists of a nano-scale heater with much smaller dimensions and much faster thermal response than this heater (thermal time constant around 5 ns). But nevertheless, we choose this heater to start with due to the simplicity of fabrication and will present the development of heater thermometry using this heater. This methodology is universal and can be applied to accurately assess the temperatures of heaters with any geometry, specifically for the heaters of 2nd gen devices in Chapter 6.

2.2 Heater Design and Process

To switch phase change material, such as GeTe, into the OFF-state it must be heated above its melting temperature (1000 K) and then cooled quickly (typically with thermal RC time constant less than 100 ns) to below the crystallization temperature[97], [103], [104]. To put the same material into the ON-state is less demanding since heating to a temperature below the melting point along with a duration time longer than 30 ns can be sufficient to crystallize the material [103]. Thus to take the PC material into the OFF-state requires greater electrical power to achieve the higher temperatures as well as switch design that permits cooling in a time constant shorter than 100 ns to prevent crystallization. This process places the greater constraints on the electrical drive as well as the switch architecture. A heater physically separate from the switch can be used to turn the switch ON or OFF by producing a desired temperature and time profile. The heater must be capable of being driven, with sufficient power at high speed so that one can reach temperatures above 1000 K and cool sufficiently fast. If the heater is modeled as a first order system consisting of a parallel thermal resistance (R_{th}) and thermal capacitance (C_{th}), then cooling will follow an exponentially decaying temperature profile with a time constant, $\tau = R_{th}C_{th}$. The constraint of τ is device geometry dependent and can vary with the PC amorphous sizes. For the RF PCS in Figure 1.8 and the 1st gen device presented in Chapter 3, the value of τ must be on the order of 100 ns. But for the 2nd gen device with much smaller dimensions, this number must be less than 10 ns, as will be explained in Chapter 6 and Chapter 7. Some work have shown heater designs which are either capable of reaching temperatures above 1000 K [105]–[107], or to cool in less than 1 μs [101], [102], [108]. However, previously reported heaters are not able to meet both of these requirements.

The geometry of the heater is carefully chosen to meet the design specifications within the limitation of testing equipment and fabrication process. The maximum voltage that can be delivered to the heater is limited by the capability of the Agilent 81110A pulse generator (below 10 V). So for generating a given temperature, the voltage required should be minimized. A simple back-of-the-envelope analysis

shows that required voltage is given by $V = \sqrt{TR / R_{th}}$, where T is temperature, R is electrical resistance of the heater and R_{th} is thermal resistance between the heater and the ambient (bottom of substrate). Since R increases while R_{th} decreases with heater length, reducing heater length will reduce the required voltage for a given temperature. On the other hand, minimizing heater width will minimize the heated volume of substrate and thus reduce the thermal capacitance and speed up the device thermal response. Thus, the heater width is chosen to be 1 μm, which is the minimum feature size in our lithography process using contact mask aligner. Heater length is chosen to be 5 μm taking account of alignment tolerance in the future process of aligning 1μm wide PC device to the center of the heater.

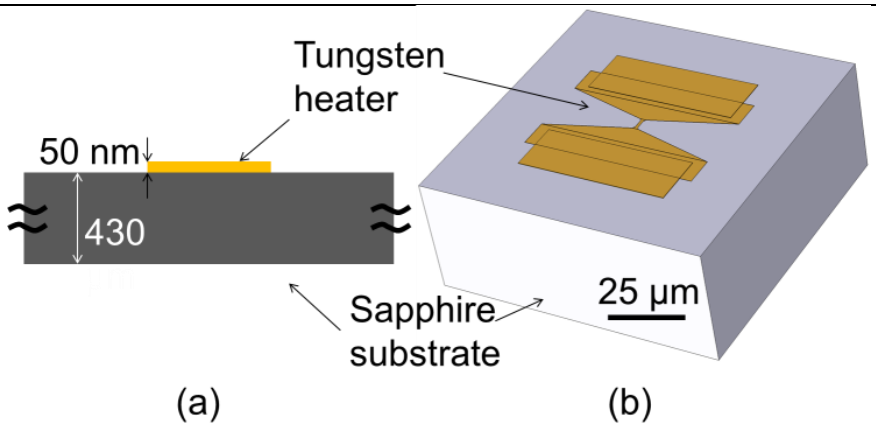

Figure 2.1 (a) cross-sectional view of the device (b) COMSOL perspective view of the device. The modeled dimensions of substrate (100 μm × 100 μm × 40 μm) is smaller than the actual dimensions (25400 μm × 25400 μm × 430 μm) but large enough to eliminate any substrate size effects.

In Figure 2.1(a), we present the structure of the heater which consists of a 55 nm thick layer of tungsten on top of a 430 μm thick sapphire substrate. The heater was produced by depositing a well-oriented 55 nm thick tungsten layer by DC sputter on the sapphire substrate. The sputtering was done using the CVC sputtering system in CMU Nanofab Facility. The DC power was set to be 50 W, the Ar gas flow rate was set to be 20 sccm to achieve a sputtering pressure of 5 mT. X-ray rocking curves about the (110) reflection

showed a full-width half-maximum of 0.5º. This layer was then patterned using photolithography with AZ 4110 photoresist, as an etch mask. A Florine-based reactive ion etching (RIE) step was then performed, with 100 W of power, with 22.5 sccm CHF_3 flow and 16 sccm O_2 flow at 100 mT. The final pattern for the heater is 1 μm wide and 5 μm long and includes leads and pads for landing probes. A second 100 nm thick tungsten layer for the contact pads was deposited in the same way and patterned using photolithography and a lift off process.

Figure 2.1(b) shows a perspective view of the heater. To model the heater operation, we constructed a finite element simulation (COMSOL) using the measured dimensions of a fabricated heater and a 100 μm × 100 μm × 40 μm bulk sapphire substrate. The modeled substrate is large enough to ensure simulation results independent of substrate size.

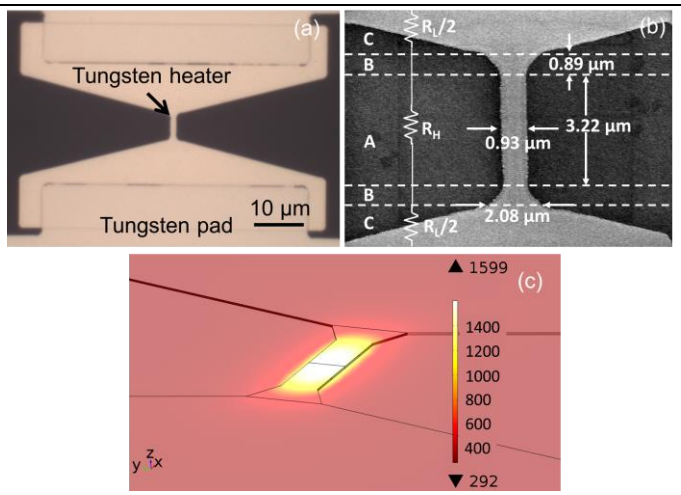

Figure 2.2 (a) optical microscopic image (left view) of the device (b) SEM image (right view) of the heater region with measured dimensions of each feature. (c) perspective view of the simulated temperature map of the heater

Figure 2.2 shows an optical microscope and SEM image of the heater. The central part of the heater, which is shown as part A in Figure 2.2(b), has a width of 0.93 μm. While the transition regions, which are

shown as part B in Figure 2.2(b), have width that increases from 0.93 μm to 2.08 μm gradually. The model calculation was based on the actual measured dimension of the heater rather than the design parameters as shown in Figure 2.2(b). Also incorporated into the model was the resistance of section A and B as heater strip resistance R_H, while the resistance of part C is considered as heater lead resistance R_L. Figure 2.2(c) shows the perspective view of the simulated temperature map of whole structure with input voltage pulse of 5 V 100 ns. The details about pulse measurement and corresponding simulation will be discussed in the following sections.

2.3 Heater Thermometry Measurement Setup

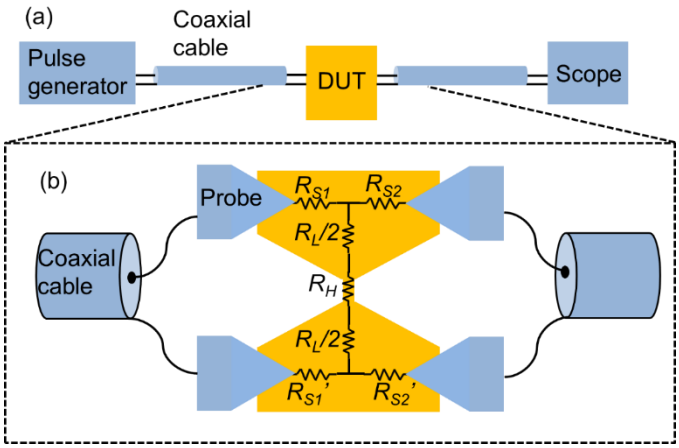

Figure 2.3 (a) Set up for TDT measurement circuit (b) Schematic for parasitic resistance of device in TDT measurement.

We employed time domain transmissometry (TDT) using the arrangement shown in Figure 2.3(a) to measure the temperature of the heater. A pulse generator (one of the output ports from Agilent 81110A pulse generator) with a 50 Ω output resistance and an oscilloscope (one of the channels in Agilent DSO1014A) with a 50 Ω input resistance were connected to RF probes (Cascade air coplanar GS/SG probes with 100 μm pitch size) through two 2.92 mm coaxial cables. The RF probes made contact on two sides of the pads as shown in Figure 2.3(b). After a voltage pulse is launched from the pulse generator to the heater,

the heater temperature rises via joule heating. The heater resistance also rises due to the linear dependence of the resistance on temperature. The temperature coefficient of resistance (TCR) of tungsten is known to be constant over the entire temperature range below the melting point [109], [110]. Thus, by knowing the resistance change of the heater, we can infer the temperature of the heater. We measured the transmitted voltage as a function of time resulting from the incident voltage pulse using the oscilloscope. From the transmitted voltage, we can calculate the heater resistance as a function of time. We then infer the temperature of the heater as a function of time using the TCR of the heater.

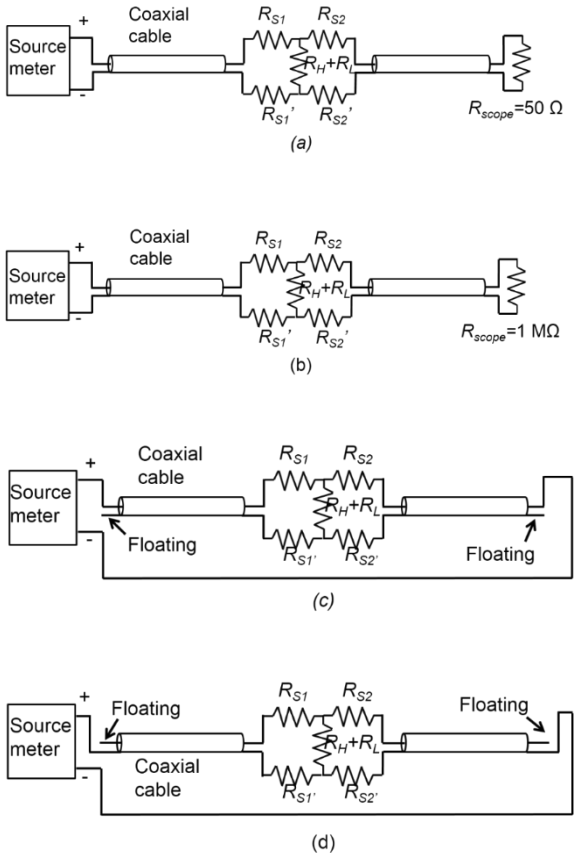

Figure 2.4 Testing circuits for parasitic resistance measurement

To accurately extract the temperature from the measured voltage pulse, we need to know the parasitic series resistances $R_{S1} + R_{S1}^{'}$ and $R_{S2} + R_{S2}^{'}$ and the heater strip resistance R_H as shown in Figure

2.3(b). These parasitic series resistances originate in the resistance of cables and probes as well as contact resistance between probes and pads. Figure 2.4 shows the circuit used for measuring parasitic resistances. A source meter (Keithley 2400) and an oscilloscope are connected to two sides of the device as shown in Figure 2.4(a) and Figure 2.4(b). The difference between Figure 2.4(a) and (b) is the value of the input impedance of the oscilloscope. By changing this load resistance from 50 Ω and 1 MΩ, we can write equations (2.1) and (2.2) below where R_{M1} to R_{M4} is the resistance measured from the source meter:

$$R_{M1} = R_{S1} + R_{S1}^{'} + \left(R_H + R_L\right) \| \left(R_{S2} + R_{S2}^{'} + 50\right) \tag{2.1}$$

$$R_{M2} = R_{S1} + R_{S1}^{'} + R_H + R_L \tag{2.2}$$

In equation (2.2), since R_H+R_L is around 20 Ω, we can assume it is much less than 1 MΩ. In Figure 2.4(c) and (d), the signal side and the ground side of the cables are floating, and we can write equations (2.3) and (2.4):

$$R_{M2} = R_{S1} + R_{S1}^{'} + R_H + R_L \tag{2.3}$$

$$R_{M4} = R_{S1}^{'} + R_{S2}^{'} \tag{2.4}$$

Combining the four equations, we can solve for $R_{S1} + R_{S1}^{'}$ and $R_{S2} + R_{S2}^{'}$.

To determine the exact heater strip resistance R_H, we performed four-point DC measurements on 5 devices with the same pad size and 1 μm heater width but different heater lengths ranging from 1 μm to 20 μm. By linearly fitting the resistance data as a function of heater length and finding the y-axis intercept we can determine the lead resistance R_L and calculate the heater resistance R_H. Since R_H is more than 60% of the total resistance of the device, more than 60 % of the power will be dissipated in the heater strip with a small volume of 0.25 μm^3. The power density in the heater strip is 80 times more than that in the other parts of the device. Thus it is reasonable to assume that the heater strip is the only part that is heated up and R_H is the resistance that changes with temperature as well as time.

A key parameter that must be determined and is required to determine the temperature of the heater is the TCR of the tungsten thin film. To determine this, a Van der Pauw structure of an identically deposited tungsten sheet film with the same thickness as the heater layer was heated from 25 ℃ to 105 ℃ with an interval of 10 ℃ using a heated chuck. Measurement was not performed in higher temperatures due to the limited range of the heated chuck. At each temperature, we performed four-point sheet resistance measurement on this sample. We determined the TCR of the tungsten by taking the slope of the plot of $\left(R_{\square} - R_{\square 0}\right) / R_{\square 0}$ versus ΔT, where $R_{\square}$ is the sheet resistance at temperature T, $R_{\square 0}$ is the sheet resistance at room temperature and ΔT is the temperature difference with respect to room temperature. Based on [109], it is reasonable to assume the TCR is constant over larger temperature range and can be used to infer temperature from room temperature to tungsten's melting temperature.

2.4 Simulation

We simulated the TDT measurement in COMSOL to model and verify our measurement. We modeled the 3-D heater device using measured values for thickness and heater dimensions as determined from fabricated devices. We used three coupled physics modules in COMSOL to simulate the system response: i) electrical circuit, ii) heat transfer and iii) electrical current.

For the electrical circuit simulation, the nodes and components are defined such that it matches the circuit in Figure 2.3. It should be noted that the applied voltage used in the pulse voltage source (V_{source}) should be twice of the input voltage (V_{in}) from the pulse generator to the heater in the experiment. This is because in order to deliver V_{in} to a 50 Ω load, the pulse generator has to source $2V_{in}$ so that half of it drops on the load while the other half drops on the pulse generator internal impedance (also 50 Ω). For the heat transfer simulation, we set the bottom of the substrate to be room temperature (293 K). The rest of the exposed boundaries are set to be thermal isolation. The initial condition for temperature is 293 K in all domains. We set the entire heater domain to be the joule heating heat source. Thus the simulations do not make the assumption that only the narrow section of the heater heats up. For the electrical current

simulation, we set the two ends of the heater pads to be nodes in electrical circuit simulation. The initial condition for voltage is 0 V in all domains.

We used the temperature dependent thermal conductivity (k_{th}) and heat capacity at constant pressure (C_p) of sapphire as provided by [111] and [112] respectively, shown in Figure 2.5. The resistivity of the heater layer tungsten thin film was measured to be 143±1 nΩ·m at room temperature by four-point measurements on Van der Pauw structures. This is much higher than the bulk value (55 nΩ·m) [109], but similar to the reported value (121 nΩ·m) for 60 nm thin film [113]. From the simulation, we obtained the expected voltage drop that would be observed across the oscilloscope, the spatial average temperature for the heater region, the lumped heater resistance and the temperature distribution along the length of the heater. By comparing simulated and measured oscilloscope voltage and the lumped heater resistance, we calculated that mismatches for both cases are smaller than 2 %. Thus, we determined that our model was sufficiently accurate to predict the heater behavior.

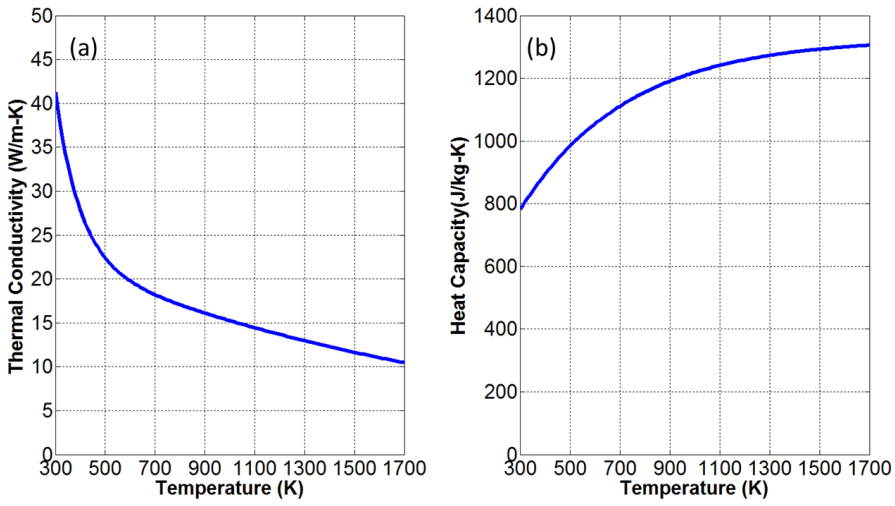

Figure 2.5 (a) temperature dependent thermal conductivity [111] and (b) temperature dependent heat capacity at constant pressure of sapphire [112]

2.5 Temperature Extraction

We established a temperature extraction method to extract lumped average temperatures of the heater as a function of time based on the parameters determined above and the transmitted pulse. The heater resistance $R_{H,\Delta T}$ at a temperature that is $\Delta\overline{T_{eff}}$ above room temperature is given by:

$$R_{H,\Delta T} = R_H\left(1+\alpha\Delta\overline{T_{eff}}\right) \tag{2.5}$$

where α is the tungsten TCR. For this method to be valid, a constant TCR is required over the entire temperature range of interest. Ref. [110] and [109] show that the TCR of tungsten is constant even over temperatures close to the melting point.

Since the device is in parallel with the oscilloscope, the parallel resistance R_P is:

$$R_P = \left(R_{H,\Delta T} + R_L\right)\left\|\left(R_{S2} + R_{S2}^{'} + 50\right)\right. \tag{2.6}$$

Thus, the total DC resistance seen from the input node R_T will be:

$$R_T = R_{S1} + R_{S1}^{'} + R_P \tag{2.7}$$

Knowing the total DC resistance, we can calculate the transmission coefficient, the ratio of incident voltage and reflected voltage:

$$\Gamma = 2R_T / \left(R_T + 50\right) \tag{2.8}$$

For pulse measurements where the transient part of the pulse is negligible (2 ns) comparing to the steady state part (60 ns to 100 ns), we do not take into account parasitic capacitance and inductance from the device and the testing circuits in the transmission coefficient calculation. Also we can write the expression for voltage seen on the oscilloscope V_O as:

$$V_O = V_I \Gamma \frac{R_P}{R_T} \frac{50}{R_{S2} + R_{S2}^{'} + 50} \tag{2.9}$$

where V_I is the input voltage. Combining Eq. (2.5) – (2.9), we can calculate $\Delta\overline{T_{eff}}$ from each data point associated with V_O and extract the temperature as a function of time.

The temperature $\overline{T_{eff}}$ extracted from the resistance $R_{H,\Delta T}$ is defined as the effective average temperature. The effective average temperature $\overline{T_{eff}}$ can be considered as the spatial average temperature $\overline{T_V}$ if we assume that temperature is uniformly distributed in the heater strip (section 2.1 shown in Figure 2.2) so that temperature of each part of the heater has the same contribution to the resistance change. The increased $\overline{T_V}$ is defined by (2.10) given the temperature as a function of position in the heater:

$$\Delta\overline{T_V} = \frac{\int_V \Delta T(x,y,z)dV}{V} \tag{2.10}$$

However, lateral heat flow along the length of the heater (vertically from top to bottom as oriented in Figure 2.2) causes non-uniform temperature distribution. $\overline{T_{eff}}$ can still be regarded as an approximation of $\overline{T_V}$ if the following two assumptions are valid. First, the temperature is uniform along the width of the heater (horizontal direction as oriented in Figure 2.2). Second, the resistance per unit length along the length of the heater strip is constant. Following is a detailed proof.

Using the first assumption in this section, (2.10) can be reduced to a 1-D integral as:

$$\Delta\overline{T_V} = \frac{\int_0^l \Delta T(x)dx}{l} \tag{2.11}$$

where x is coordinate along the length of the heater and l is the length of the heater. Thus x is 0 on one end of the heater and l on the other end. One can also write down the heater resistance $R_{H,\Delta T}$ in a distributed form:

$$R_{H,\Delta T} = \int_0^l \left(r_H(x)\left(1+\alpha\Delta T(x)\right)\right) dx \tag{2.12}$$

where $r_H(x)$ is the room temperature resistance per unit length of the heater. The heater resistance at room temperature is given by:

$$R_H = \int_0^l r_H(x)dx \tag{2.13}$$

Substituting (2.13) into (2.12), the heater resistance is:

$$R_{H,\Delta T} = R_H + \int_0^l \left(r_H(x)\alpha\Delta T(x)\right) dx \tag{2.14}$$

Combing (2.5) and (2.14), we can write the distributed form of $\Delta\overline{T_{eff}}$ as:

$$\Delta\overline{T_{eff}} = \frac{\int_0^l r_H(x)\Delta T(x)dx}{R_H} \tag{2.15}$$

Thus effective average temperature $\Delta\overline{T_{eff}}$ is the average temperature weighted by distributed resistance. Using the second assumption, $r_H(x)$ can be written as a constant r_H and $R_H = lr_H$. $\Delta\overline{T_{eff}}$ can be rewritten as:

$$\Delta\overline{T_{eff}} = \frac{r_H \int_0^l \Delta T(x)dx}{R_H} = \frac{\int_0^l \Delta T(x)dx}{l} \tag{2.16}$$

It is proved from (2.11) and (2.16) that $\Delta\overline{T_{eff}} = \Delta\overline{T_V}$ based on the assumptions described above. $\Delta\overline{T_{eff}}$ can be used to approximate $\overline{T_V}$ and the temperature extraction method can be a quick way of thermometry without simulations.

2.6 Preparatory DC measurements

The measured parameters determined prior to the TDT measurements as described above are shown in Table 2.1. Using the arrangement shown in Figure 2.4 and Eq.(2.1)-(2.4), we measured $R_{S1} + R_{S1}^{'}$ and $R_{S2} + R_{S2}^{'}$.

Table 2.1 Parameters for extracting temperature

Parameters	Values
$R_{S1} + R_{S1}^{'}$ (Ω)	2.86 ± 0.02
$R_{S2} + R_{S2}^{'}$ (Ω)	4.17 ± 0.02
R_H (Ω)	12.90 ± 0.1
R_D (Ω)	20.16 ± 0.2
R_H / R_D	0.64 ± 0.01
TCR (ppt/K)	2.2 ± 0.1

Figure 2.6 shows the measured device resistance R_D as a function of heater length. The linear fit has an intercept of 8.16 Ω which is the device lead resistance R_L. Since R_D=R_H+R_L, we can calculate the ratio of heater resistance R_H to R_D for a 5 μm long heater. We used the ratio instead of the actual measured R_H because R_D may be different from device to device, due to thickness variation. We then calculated R_H for the device under test (with a heater length of 5 μm) using this ratio and its value of R_D.

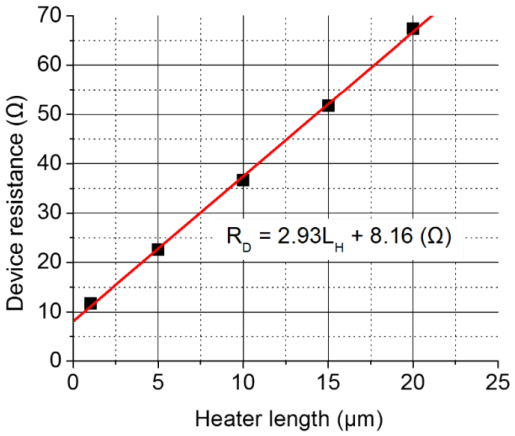

Figure 2.6 Device resistance measurements as a function of heater length, where device resistance $R_D=R_H+R_L$

Figure 2.7 shows the TCR measurement results. The uncertainty in the measurement is indicated by the size of data points which are ±2℃ in temperature and ±3 mΩ/□ uncertainty in sheet resistance. A linear fit to the data, gives a TCR of 2.2±0.1 ppt/K. From [110], the extracted bulk tungsten TCR data is 5.8 ppt/K and electrical resistivity at room temperature is 54.6 nΩ·m. This is consistent with Matthiessen's rule, which describes the resistivity as $\rho = \rho_L + \rho_i$, where ρ_L is the temperature dependent term caused by thermal phonons and ρ_i is the temperature independent term caused by electron scattering effects. For thin film metal resistivity we have:

$$\rho = \rho_i + \rho_{RT}(1+\alpha_b \Delta T) \tag{2.17}$$

where ρ_{RT} is the bulk resistivity at room temperature and α_b is the bulk TCR. It shows that the measured thin film resistivity ρ is sum of the temperature independent term ρ_i and temperature dependent term $\rho_L = \rho_{RT}(1+\alpha_b \Delta T)$. We also have:

$$\rho = (\rho_i + \rho_{RT})(1+\alpha \Delta T) \tag{2.18}$$

where α is the thin film TCR. It shows that shows that ρ is dependent on thin film room temperature resistivity $\rho_i + \rho_{RT}$. From (2.17) and (2.18) we can derive thin film TCR as:

$$\alpha_b / \alpha = (\rho_{RT} + \rho_i) / \rho_{RT} \tag{2.19}$$

For the 55 nm thick fabricated tungsten thin film, the room temperature electrical resistivity is higher than the bulk value by a factor of 2.64, which is the measured value of $(\rho_{RT} + \rho_i) / \rho_{RT}$ in (2.19). While the tungsten thin film TCR is lower than the bulk value by a factor of 2.62, which is the measured value of α_b / α in Eq. (2.19). Thus, the measurement values are consistent with the theoretical derivation, as expected. On the other hand, we can also conclude from (2.19) that thin film TCR is constant as long as bulk TCR remains constant over the entire temperature range of interest.

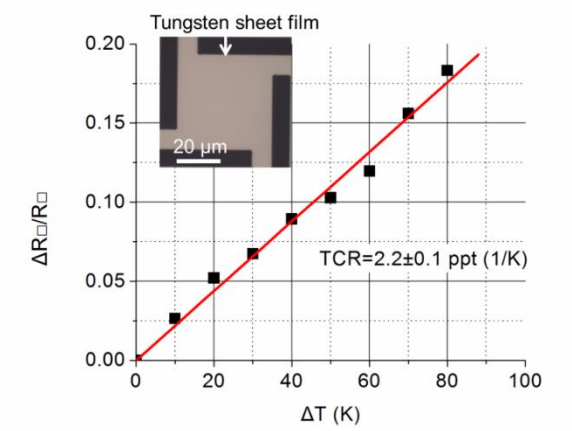

Figure 2.7 TCR measurement results. (Insert) Van der Pauw structure used to measure sheet resistance for TCR measurements.

2.7 Pulse measurements

Since contact resistance is strongly dependent on the contact condition between the probes and the pads, we performed pulse measurements immediately after the DC measurement to keep conditions

unchanged for both probes. Using the arrangement shown in Figure 2.3(a), the TDT measurement was performed on the device under test. Figure 2.8 shows the schematic of an input pulse from the pulse generator. The pulse has a maximum voltage of 5 V and a 1 V dc bias. The 1 V dc bias is used to read the resistance change after the pulse is "off" without causing significant heating in the heater. Simulation shows that 1 V bias will generate ΔT of 26 K from room temperature in the heater at steady state, which is less than 4% of the target temperature (1000 K) for the heater. The rise and fall time, defined as the time for the voltage to change between 90% and 10% of the total voltage difference, are both 2 ns. The pulse maximum voltage was fixed and the pulse width varied to bring the heater to different temperatures.

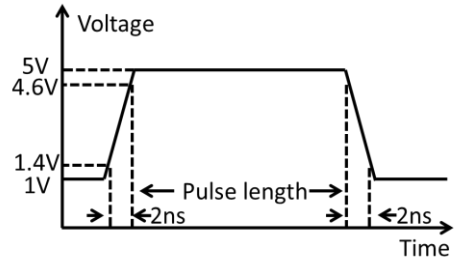

Figure 2.8 Input pulses with fixed voltage level and varied pulse length

Figure 2.9 (a) shows the transient voltage as observed on the oscilloscope for 60 ns, 80 ns and 100 ns wide pulses. The solid lines are simulated results while the noisy lines are measured. The calibrated measured voltage and simulated voltage are in good agreement with each other and the mismatch is smaller than 1.9 %. The narrow peaks and small bumps observed in the voltage curves after the pulse is off are possibly due to the reflection of inductive discontinuity in the measurement circuits, where the inductive discontinuity is caused by the parasitic inductance of the scope and the reflection is due to the impedance mismatch between cables and connectors. Figure 2.9(b) shows the simulated and measured lumped heater resistance as a function of time for different pulse widths. These also are in good agreement on the ramp up region and part of the ramping down region (with mismatch smaller than 1.2 %). The larger mismatch of 26.9 % that lasts 20 ns after the pulse is turned "off" is due to the reflection in the voltage.

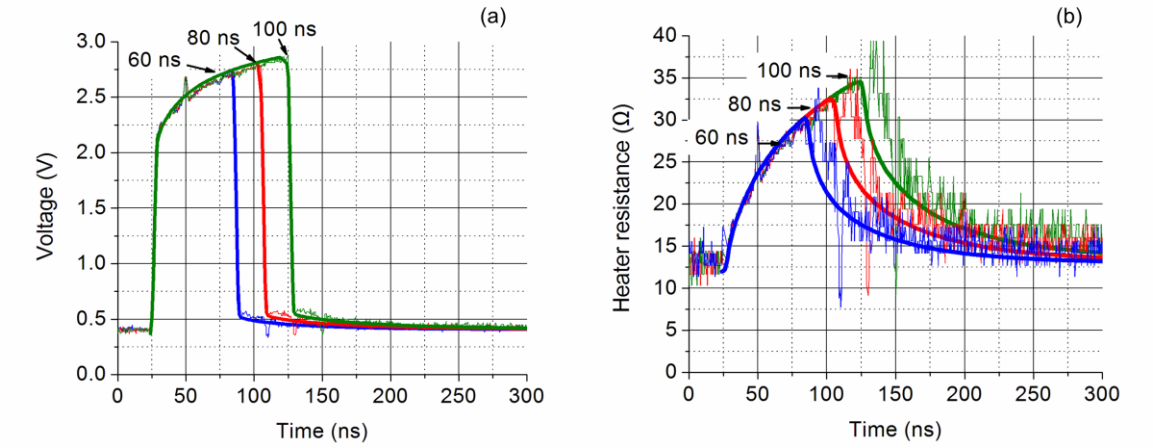

Figure 2.9 (a) simulated (dotted lines) and experimental (solid lines) voltage transmitted to the scope as a function of time for different pulse width (b) simulated (dotted lines) and experimental (solid lines) lumped heater resistance change as a function of temperature.

Figure 2.10(a) shows the modeled temperature as a function of position along the length of the heater (vertically from top to bottom as oriented in Figure 2.2) right before the pulses were turned off. Due to the lateral heat flow in the heater, the temperature distribution along the length of the heater is not uniform. Different parts of the heater contribute differently to the measured heater resistance change. However, in Figure 2.10(b), the temperature distribution is much more uniform along the width of the heater. This is due to limited heat flow in the width direction.

Simulated $\overline{T_V}$ and $\overline{T_{eff}}$ (extracted from simulated resistance transient shown in Figure 2.9(b)) are plotted versus $\overline{T_V}$ for a 5 V 100 ns pulse as shown in Figure 2.11. The good consistency (with mismatch smaller than 0.8 %) between simulated $\overline{T_V}$ and $\overline{T_{eff}}$ confirms that the distribution is uniform enough for the first assumption in section 2.5 to be valid. Since the cross-section area of the heater strip is designed to be

the same along the length of the heater, the second assumption is also valid that the resistance per unit length of heater is constant. Thus, $\overline{T_{eff}}$ should be a good approximation of $\overline{T_V}$.

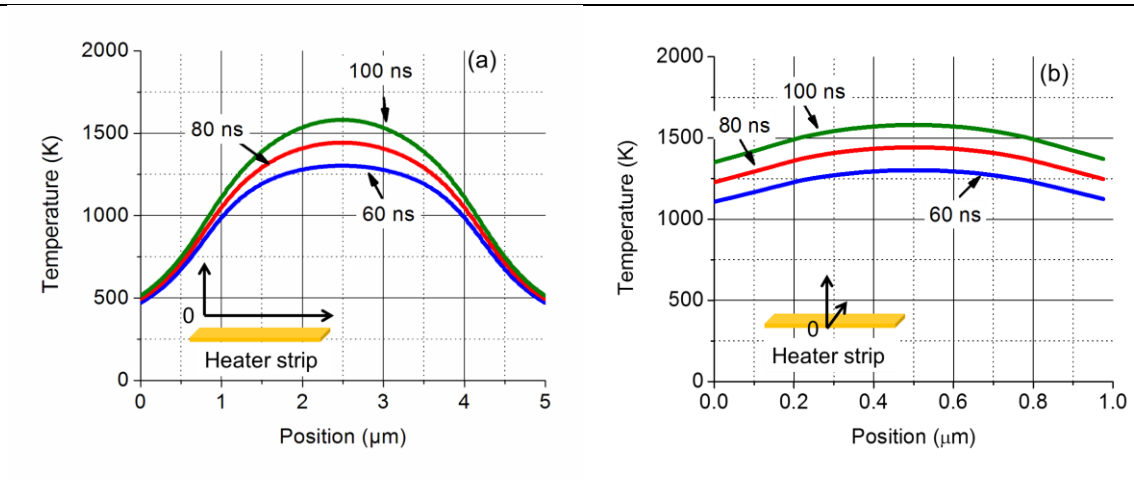

Figure 2.10 Simulated temperature profile (a) along the length of the heater and (b) along the width of the heater at 60 ns, 80 ns and 100 ns and (c) and

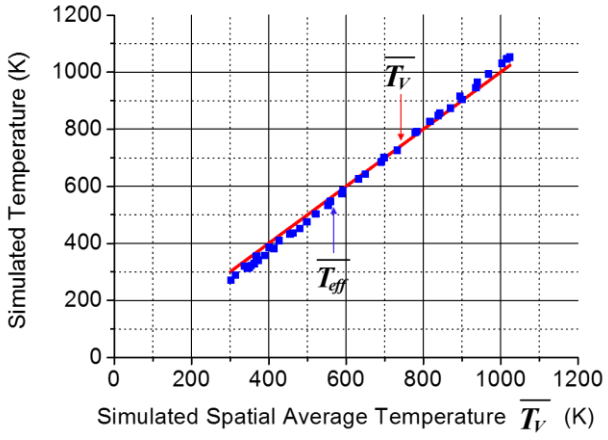

Figure 2.11 Simulated effective temperature and spatial average temperature plotted for a 5 V 100 ns pulse

Using Eq. (2.5) – (2.9) and parameters (series resistances, heater strip resistance and TCR of tungsten) determined in the DC measurement, $\overline{T_{eff}}$ was extracted from the measured heater resistance transients in Figure 2.9(c). In Figure 2.12, the dotted lines are simulated $\overline{T_V}$ and the solid lines are $\overline{T_{eff}}$ extracted from measurement and they are in good agreement.

Figure 2.12 shows that the maximum $\overline{T_V}$ of 60 ns, 80 ns and 100 ns wide pulses are 880 K, 960 K and 1050 K respectively. In the central 1 μm region, the maximum temperatures are 1309±9 K, 1457±14 K and 1664±20 K. In this region, the temperature distribution is relatively uniform and one is able to heat uniformly and predictably in this region. For the 100 ns wide pulse, the heating rate in the center of heater is 1.67×10^{10} K/s.

Despite the fact that there is 26.9 % mismatch during the 20 ns immediately after the pulse is turned "off", we were still able to measure an effective RC time constant, which is defined as the time needed for the heater temperature to cool from 100% to 37% of its maximum temperature. The values we found were 28 ns for the 60 ns wide pulse and 38 ns for the 100 ns wide pulse. Since this is a distributed thermal system that can be approximated as a system with multiple thermal time constants, the above temperature transient reflects the shortest time constant of the system. To reach true steady state, requires about 1 μs, the longest time constant of the system. By using short pulses we avoid activating these slower cooing thermal reservoirs and can operate at high speed. It should be noted that the increase of the observed time constant with increasing pulse length indicates increasing activation of the slower cooling reservoir, consistent with our understanding of the multi-time constant system response. At higher temperatures the sapphire thermal conductivity is lower and the heat capacity is higher, typically at 1500 K, k_{th} = 12 W/(m·K) and C_p = 1290 J/(kg·K), therefore the time constant is larger [111], [112]. Since the temperature distribution along the length of the heater is not uniform, the thermal RC time constants in the center of the heater will be higher than the lumped values.

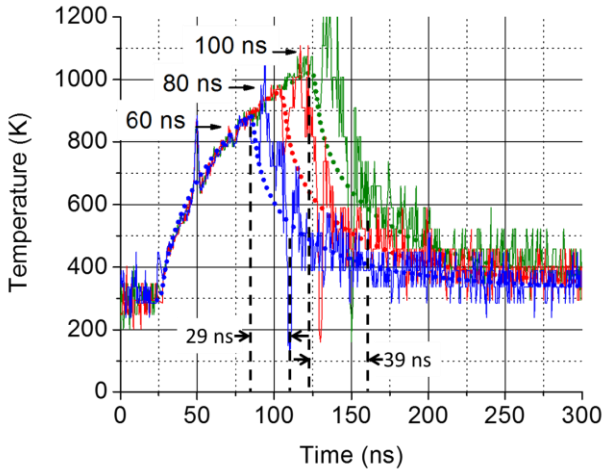

Figure 2.12 (dotted lines) simulated $\overline{T_V}$ and (solid lines) extracted $\overline{T_{eff}}$ according to lumped heater resistance change in Fig. 7(c) and TCR of tungsten

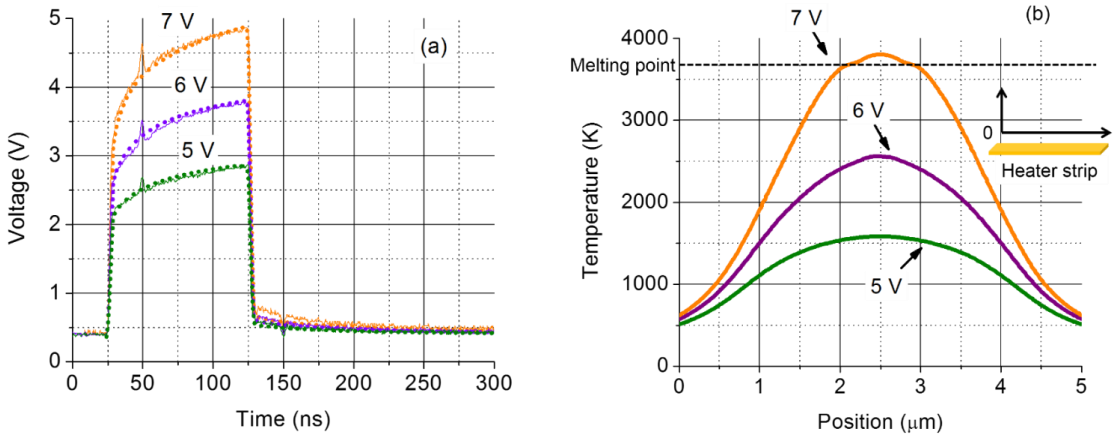

Figure 2.13 (a) Simulated (dotted lines) and experimental (solid lines) scope voltage as a function of time for different input voltages (b) Simulated temperature as a function of position at 100 ns for different input voltages

In another set of pulse measurements, the pulse width was fixed and the input voltage set to 5 V, 6 V and 7 V. Figure 2.13(a) shows the fit for simulated and measured oscilloscope voltage. Figure 2.13(b) shows the modeled temperature distributions along the length of the heater at 100 ns. As can be seen, the higher the temperature the less uniform the temperature distribution.

For the temperature simulation with a 7 V input voltage, the temperature profile along the length of the heater shows an abrupt change in the center and the central temperature is slightly higher than the melting temperature. We attribute this to the latent heat of fusion of tungsten. When heater temperature reaches the melting temperature of tungsten, the heat capacity of tungsten becomes enormous (higher than 5 kJ/(kg·K)) and this slows the heating rate in the material as it melts. Our simulations include the effects of the latent heat of fusion as the material melts. The melting temperature is set to be 3695 K, latent heat of fusion is set to be 260 kJ/kg [114], and the transition interval temperature range is 50 K.

Table 2.2 Comparison for simulation and extracted temperature					
Input voltage (V)	5	5	5	6	7
Pulse width (ns)	60	80	100	100	100
Max extracted $\overline{T_{eff}}$ (K)	884	981	1074	1535	2290
Max simulated $\overline{T_V}$ (K)	886	960	1024	1450	1990
Mismatch (%)	0.2	2.1	4.7	5.5	13.1

In Table 2.2 simulated and extracted temperatures for different pulse inputs in terms of voltage and time are compared. The consistency between maximum simulated $\overline{T_V}$ and maximum extracted $\overline{T_{eff}}$ decreases when the temperature is higher. We attribute this growing difference in extracted and simulated maximum temperatures to the simulated $\overline{T_V}$ being less accurate in predicting the extracted temperature

when the distribution is less uniform in the width direction. We have very good consistency between simulation and extracted temperatures with a mismatch smaller than 5.5% when maximum extracted $\overline{T_{eff}}$ are smaller than 1535 K. For the highest temperature, part of the tungsten was melted and due to the latent heat of fusion, the non-uniformity is even stronger. The mismatch is 13.1%, suggesting that the temperature prediction has limited accuracy at this operating point.

2.8 Heater Reliability

Figure 2.14 shows the device resistance as a function of pulse number. This measurement provides a sense of the durability of the heater. The heater was pulsed using a fixed pulse width of 100 ns with 2 ns rise and fall time and various input voltages. The maximum simulated $\overline{T_V}$ and extracted $\overline{T_{eff}}$ are shown in Table 2.2 and temperature distributions at 100 ns are shown in Figure 2.13(b). At 5 V, the resistance is 24.654±0.007 Ω through all 10,000 pulses and is very stable, presumably because of the low maximum temperature. At 6 V, the resistance slightly decreases from 24.65 Ω to 24.58 Ω with more pulses cycling the heater. We attribute this due to the annealing of the tungsten at higher temperature, possibly causing grain growth in the tungsten. At 7 V, the resistance decreases significantly and continuously from 24.58 Ω to 24.30 Ω because the $\overline{T_V}$ is higher and the temperature at the central region of heater is above the melting point of tungsten. The heater was destroyed after 5000 pulses at 7 V. When we attempted to increase the pulse maximum voltage to 8 V, the heater failed immediately. With this heater design a 5 V 100 ns pulse allows our device to maintain the heater resistance over time and at a maximum central temperature of 1664 K. The heater also shows some durability for a limited number of pulses at ultra-high center temperatures of 3800 K (7 V pulses).

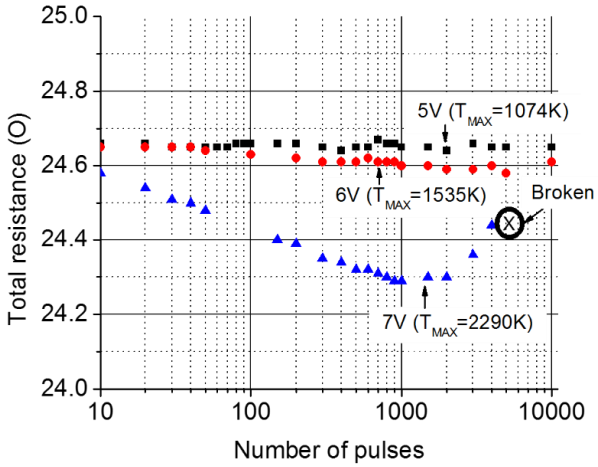

Figure 2.14 Cycling test results at different pulse height. Pulse width and pulse edge are fixed at 100 ns and 2 ns. The device was broken after 5000 pulses at 7V (maximum extracted $\overline{T_{eff}}$ is 2290K)

The heater reliability was also studied for different substrates and various heater length with the same heater width. Figure 2.15 shows the comparison of the minimum failure temperatures (MFT) between different substrates. The MFT is the lowest temperature that causes the heater to fail (broken) for a single pulse. The $\overline{T_{eff}}$ were used here, extracted using the previously described methodology. The red data points were taken from heaters with various length on top of the sapphire substrate while the blue ones were from heaters on a silicon substrate with 1 μm thick thermal SiO_2. For both substrates, the heater width is fixed at 1 μm but the length varies from 5 μm to 20 μm. Figure 2.15(a) shows that, for both substrates, the MFT decreases when the length increases. On the other hand, for the same heater length, the MFT is higher for the SiO_2 substrate than the sapphire. This can be explained by the current density required to generate given temperature in the heater being different. Shown in Figure 2.15(b), the heaters on sapphire substrate will need higher current density to generate the same temperatures than the heaters on SiO_2. This is because the thermal resistance from the heater to the thermal ground is much lower for the sapphire, causing the required

power and thus the current density to be much higher. The observations can be explained by the electro-migration in the heater. In the electro-migration, a higher current density results in a higher probability of materials transport, which leads to the heater broken. Since the heater can be modelled as a lumped element with small discretized elements connected in series, a single failure in the small element can cause the entire heater to fail. As a result, the probability for a longer heater to fail is higher, causing the MTF for longer heaters lower than the shorter heaters.

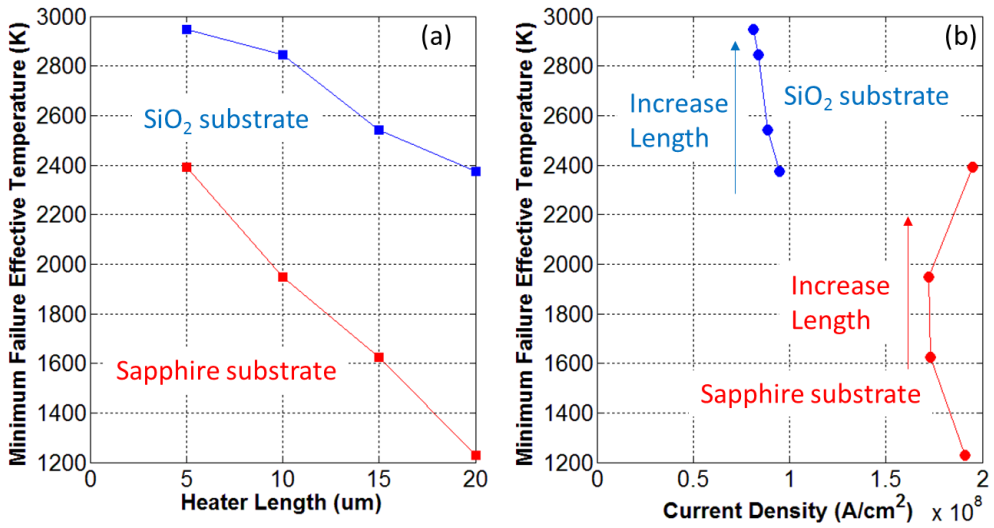

Figure 2.15 (a) minimum failure effective temperatures as a function of heater length and (b) minimum failure effective temperatures as a fucntion of current density on sapphire substrate (red data) and SiO_2 substrate (blue data).

2.9 Summary

In this chapter, tthegeometry and fabrication process of a micro-heater using thin film tungsten on a sapphire substrate for high temperature high speed heating is described. This heater design is able to reach a maximum central temperature of 1664 K at a rate of 1.67×10^{10} K/s. The heater is also able to quench quickly with a thermal RC time constant of less than 40 ns. The heater also shows very good stability at a

center temperature of 1664 K and can even be operated up to 2550 K. Meeting specifications is necessary for the heater to be used for transforming the PC materials to be built on top.

TDT was used to measure the heater temperature transients and the measurement results can be accurately predicted and verified by a 3-D COMSOL model. The maximum $\overline{T_V}$ mismatch between measurements and simulations is less than 0.2% in the best case with a lower temperature and 13.1% in the worst case with a higher temperature. This methodology can be used for extracting temperature transients for any given electrical inputs to the heater, which is extremely helpful for studying temperature dependent electrical properties and crystallization dynamics for PC materials. In addition, preliminary experiments showed that lower operating current density results in better reliability, suggesting that the heater failure mechanism is likely to be the electro-migration.

Chapter 3: Crystallization Dynamics Study for Phase Change RF Switch

3.1 Abstract

In this chapter, crystallization dynamics for PC material will be discussed, with the goal of lowering the programming power and thus the total power consumption of the RF PCS. Specifically, the 1st generation equiatomic GeTe PCS test device (1st gen device) with micro-scale dimensions driven by an electrically isolated tungsten heater (discussed in the previous chapter) will be presented for measuring the critical quench time (CQT) of PC materials. The CQT is defined as the longest thermal time constant (i.e. the slowest cooling) that still results in an amorphous PC material after the PC layer has been melted. This information is important in low power RF PCS design, since a longer CQT typically relaxes heater design constraints and, in turn, allows the lowering of the minimum power required to turn the switch to the OFF-state.

We will firstly discuss the power speed trade-off of RF PCS design and the rationale of how CQT affects the design. A step by step fabrication process for the 1st gen device will be shown. The detailed methodology of in-situ CQT measurement and crystallization time measurement for TTT diagram will then be discussed. The CQT measurement results are presented together with the bottom half of the TTT diagram as a self-consistent result. Finally, observation of the non-Arrhenius behavior of GeTe crystallization is reported and the activation energies of GeTe are extracted at different temperature regimes.

Both the CQT and crystallization time are device geometry dependent. The numbers reported in this Chapter are associated with the 1st gen device. We found that later that the crystallization time is dependent on the amorphous size by comparing the associated results using the 1st gen device and the 2nd gen device, and will discuss these implications in Chapter 6. Although these numbers cannot be directly used in estimating the performance of a more appropriately designed RF PCS as in Figure 1.8, the

methodology can be used to measure in-situ crystallization dynamics of PCS with any geometry. These numbers will also be used to reconcile with the crystallization models in Chapter 7, based on which a unified framework is developed to estimate the performance universally for different PCS device geometries.

3.2 Power Speed Trade-off

Since the RESET operation requires melting the PC materials, it sets the maximum power consumption. One approach to reduce the required switching power is by having a thermal isolation layer between the heater and the substrate. A first order thermal circuit model for the device is shown in Figure 3.1. Thermal resistance of passivation layer (thermal conductivity k_{th} of ~ 1 W/(m·K)) is neglected since it is in parallel with thermal resistance of metal contacts (k_{th} of ~60 W/(m·K) for thin film).

To generate a temperature increase of ΔT_{melt} on the top of PC layer, the required temperature increase of the heater ΔT_{Heater} is given by:

$$\Delta T_{Heater} = \frac{R_{th,contact} + R_{th,PC} + R_{th,dielectric}}{R_{th,PC} + R_{th,dielectric}} \Delta T_{melt} \tag{3.1}$$

$R_{th,contact}$ is determined by the gap size of the metal contacts, which is designed to be the minimum feature size in the fabrication process. $R_{th,PC}$ is determined by PC thickness while $R_{th,dielectric}$ depends on dielectric layer thickness, both can be decreased for lowering RESET power, P_{RESET}, at the cost of increasing R_{ON} and C_{OFF} respectively. The f_{CO} - P_{RESET} tradeoff makes the design space small for the layers on top of the heater. However, for a given ΔT_{Heater} at steady state:

$$P_{RESET} = \frac{\Delta T_{Heater}}{R_{th,isolation} + R_{th,sub}} \tag{3.2}$$

The larger $R_{th,isolation}$ is, the lower P_{RESET} is required to generate ΔT_{Heater} and ΔT_{melt}. From (3.1) and (3.2), P_{RESET} can be engineered by changing the thickness of thermal isolation layer.

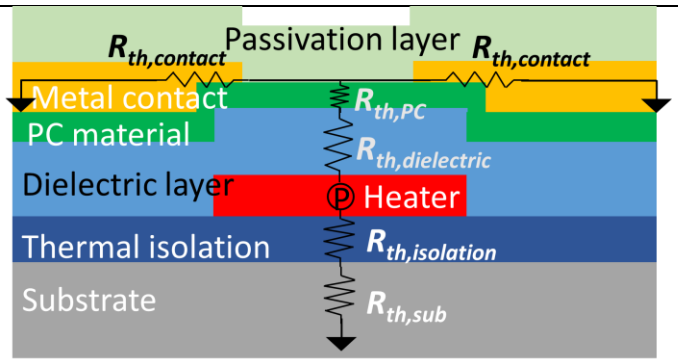

Figure 3.1. Thermal model for PCS driven by isolated heater. Thermal resistances of each layer are labeled as $R_{th,layerName}$.

Thus the isolation layer needs to be as thick as possible to reduce power, but adding thermal resistance to the isolation layer decreases the speed of thermal response of the PCS. One can trade speed for power in reconfigurable circuit applications since the devices are not required to have as small a switching time as in memory applications (memory typically requires times < 50 ns). However, too slow of a thermal response is unacceptable for PCS functionality. As shown in Figure 1.1, the PC material will be recrystallized in the cooling process if the quench time is longer than CQT. This power-speed tradeoff need to be well understood and careful design has to be made in order to keep the quench time within CQT and prevent RESET operation from failing. So estimating CQT for a given PCS configuration is extremely important as it defines design space for PCS's thermal response speed and P_{RESET}.

3.3 1st Gen Device Design and Fabrication Process

The 1st gen device used for crystallization dynamics study is shown in Figure 3.2. Figure 3.2(a) shows the microscopic image of the top view of the device. In this device, sapphire substrate is used to be consistent with the standard RF PCS described in [88] and [115], which provides reasonably high thermal conductivity while minimizing the RF loss through the substrate. The tungsten micro-heater has a length of 1 μm and a width of 5 μm and is vertically oriented in Figure 3.2(a) and (b), providing the capability of

heating the PC layer up to above 1600 K reliably with a rate of 1.67×10^{10} K/s and cooling down with a thermal time constant of less than 40 ns. This fast heater provides enough margin for measuring the CQT of the PC material. An AlN barrier is used in this device to electrically separate and thermally connect the heater and the PC material. Previous work has shown that using it can efficiently reduce the capacitance with minimal increases in the switching power due to its high thermal conductivity (bulk value of 285 W/(m·K)) [88]. The PC layer, with GeTe as the PC material, was sputter deposited and patterned into a 10 μm long, 1 μm wide micro-strip horizontally oriented in Figure 3.2(a) and (b). The 1 μm by 1 μm PC region on top of the heater is the region to be transformed, as shown in Figure 3.2(b).

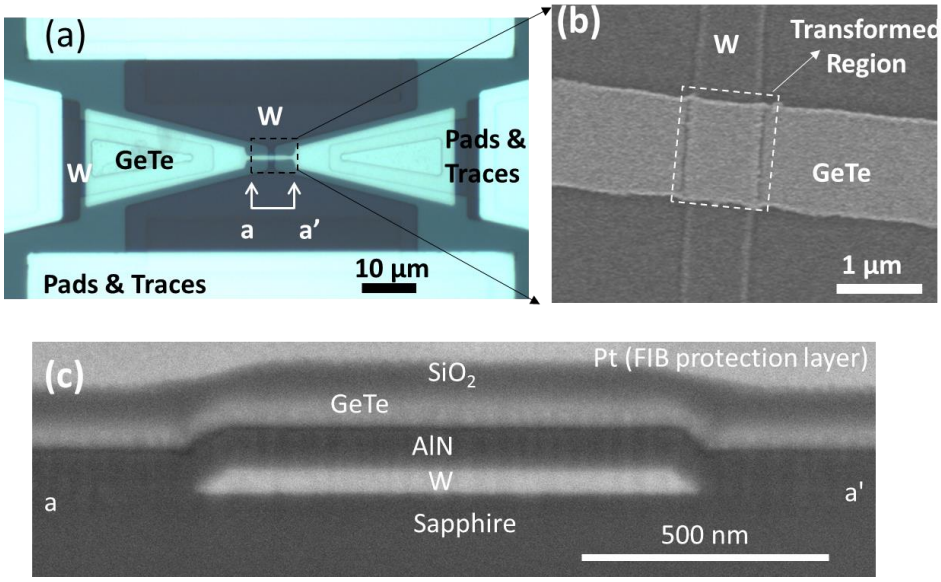

Figure 3.2 (a) Microscopic image (b) zoomed in SEM image of device top view (c) FIB cross-section image of the 1st gen device

Figure 3.2(c) shows the focused ion beam (FIB) cross-section image of this device. The tungsten thickness was determined to be 50 nm. The side wall angle of the tungsten heater is approximately 45º, provides good side wall coverage for the layers on top of the heater. The AlN thickness was determined to be 100 nm, considering the trade-off between the efficiency to program the PC layer and the side wall

coverage. PC layer thickness was designed to be 50 nm, also with the consideration of both power efficiency and side wall coverage. The SiO_2 passivation layer was also designed to be 50 nm for protecting the PC layer from oxidation.

The entire fabrication process flow for this device is shown in Figure 3.3, Figure 3.4 and Figure 3.5. Each figure shows two steps of in the flow, with the top view layout schematic, and two cross-section schematics from different orientations.

The first mask layer is for patterning tungsten micro-heater as well as the bottom tungsten contacts for the PC layer. As shown in Figure 3.3(a), the heater is vertically oriented, while the two tapers on the left and right sides are the bottom contacts. Using the AJA sputtering system, tungsten films was sputter deposited onto a 1-inch C-axis sapphire substrate, with 50 W DC power, 3 mTorr Ar pressure and 60 sccm Ar flow rate. For a 50 nm film, the sputtering time is 1300 seconds. The sputtering was performed at elevated temperature (850 ºC) to enable tungsten film to have lowest resistivity. This recipe resulted in a tungsten film resistivity of 83 nΩ·m, which is much lower than that of the room temperature deposited film (230 nΩ·m using AJA and 144 nΩ·m using CVC). This resistivity reduction at high temperature is likely due to the increased W atom mobility on the surface which results in larger grain boundaries and purer tungsten film.

Following the deposition of tungsten film, a standard photolithography step was performed. HMDS was firstly uniformly spinned (or optionally evaporated in HMDS oven with 10 minute vapor prime at 150° C) onto the wafer. HMDS is used for improving the adhesion between photoresist and the substrate. Absence of HMDS could cause small patterns to detach from the wafer surface after development. AZ4110 photoresist was then spun onto the wafer, at 4000 rpm for 1 minute, followed by 2 minutes of soft baking on a 95 ºC hot plate. This results in a photoresist thickness of around 1.1 μm. The resist was then exposed for 20 seconds at an exposure density of 5 mW/cm^2 using the MA6 mask aligner photolithography tool in CMU Nanofab, with the mask layer shown in Figure 3.3(a). The resist was then developed in a solution made of 1 part of AZ 400 K developer and 3 part of DI water for 1.2 minutes.

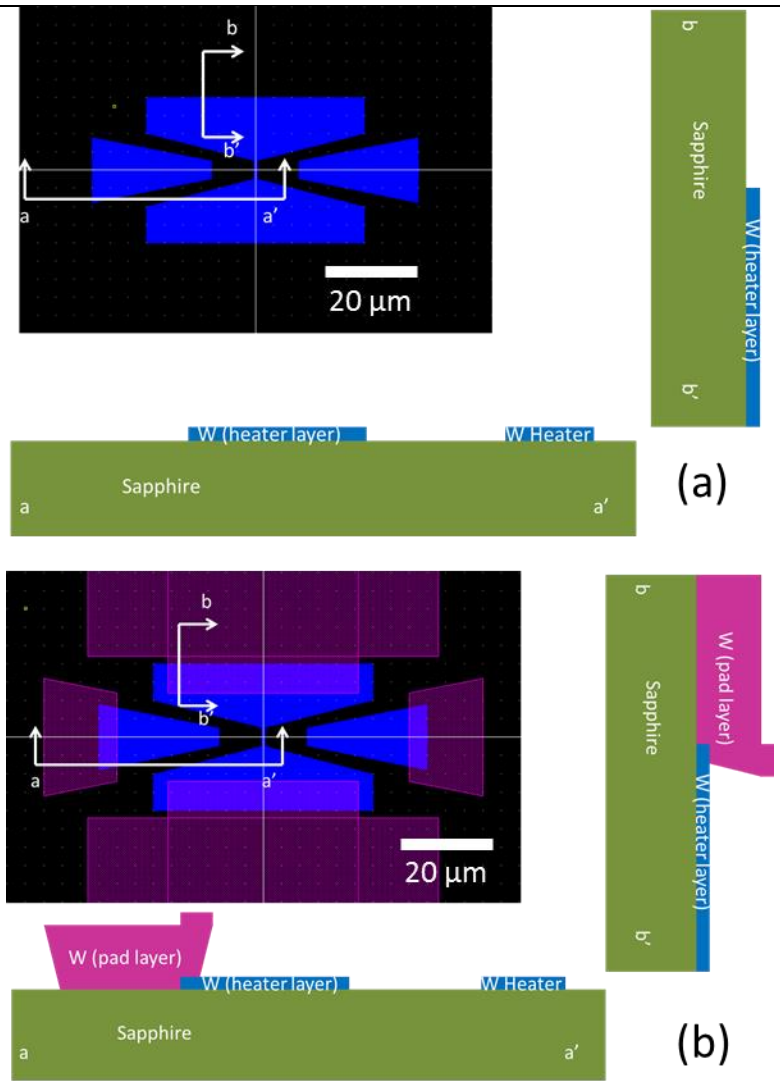

Figure 3.3 top view and cross-section schematics from two directions of (a) the first mask layer for the heater and (b) the second mask layer for the pad

An etch step was then performed to etch away the tungsten that is not protected by the photoresist. PlasmaTherm, an F-based RIE system was used in this step. The etch RF power was set to be 100 W, at 100 mTorr, with 22.5 sccm CHF_3 flow rate and 16 sccm O_2 flow rate. The etch rate for tungsten using this recipe is approximately 25 nm per minute. Taking over-etch into account, the total etch time for this step was 2.5 minute. The etch rate for sapphire is extremely small using this recipe (< 5 nm per minute), so the

over-etch will not affect the heater geometry and the side wall. After the RIE, an O_2 plasma etch step using IPC barrel etcher system was performed to soften the photoresist, with 100 W RF power and 1 Torr O_2 pressure for 2 minutes. Finally, the wafer was put in acetone and ultra-sonicated for 10 minutes to completely remove the photoresist.

The second mask layer is for patterning thick tungsten pads, shown in Figure 3.3(b). This thick layer is necessary because in order to open contacts for top layer metal traces and heater. It has to withstand the over-etch in two different etch steps: etch for contact window through AlN layer, and etch for PC layer. The thick pads were patterned by lift-off. A standard photolithogrphy step was performed using AZ4110 resist, using the exact same recipe as the previous layer. After the resist development, a resist descum step was performed using O_2 plasma, at 100 W DC power and 1 Torr O_2 pressure.

Following this, 100 nm thick tungsten was sputtered using the AJA sputtering system at room temperature, with the same power, gas flow and pressure conditions as the previous tungsten sputtering recipe. The high temperature condition is unneccessary because the film quality and resistivity is not critical for this layer. On the other hand, sputtering temperatures higher than 200 ºC may harden and even carbonize the photoresist, making it impossible to remove. Finally, the lift-off was completed by ultra-sonicating the wafer in acetone for 10 minutes.

The third mask layer is for patterning the contact windows through AlN, shown in Figure 3.4. First of all, 100 nm AlN was sputtered uniformly on the wafer using Tegal sputtering system. This step was achieved by reactively sputtering Al target in a gas condition with a mixture of Ar (23 sccm) and N_2 (32 sccm), at 7 kW AC power and 300 W DC power. During the sputtering, Al will react with N_2 and form AlN film on the wafer surface. The sputtering rate is approximately 1.3 nm per minute. Following this step, a standard photolithography step was performed to clear the photoresist on top of the thick heater pads. These regions will not be protected by the resist during the etch step for AlN. In this step, AZ400K developer should not be used since it will etch the AlN. Instead, a solution of 2 parts of AZ developer and 1 part of DI water should be used. The development time is approximately 1.4 minutes.

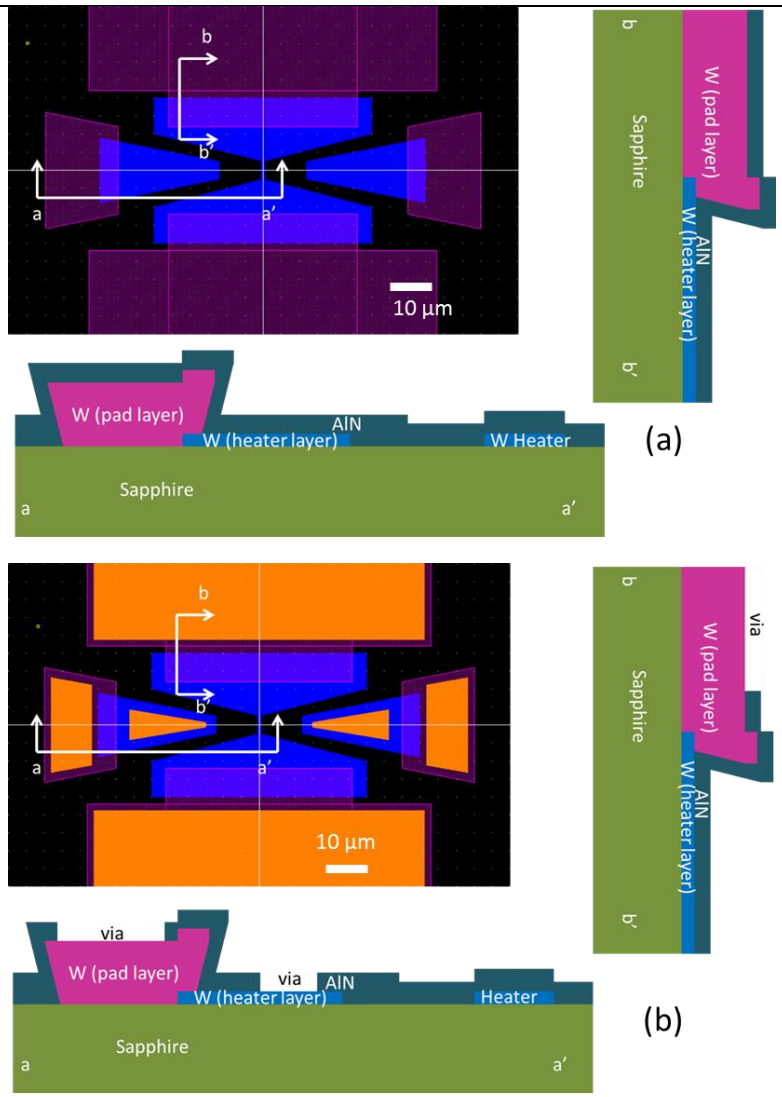

Figure 3.4 top view and cross-section schematics from two directions of (a) the AlN deposition step and (b) the third mask layer for etching via through AlN

Then, using the inductively coupled plasma (ICP) Versaline RIE system, the AlN can be etched at 100 W ICP power, 30 W DC bias power, 5 mTorr pressure, 25 sccm Cl_2, 5 sccm BCl_3 and 70 sccm Ar. The etch rate is approximately 60 nm per minute. But the total etch time was determined to be 120 seconds, taking over-etch into account. A standard O_2 plasma resist soften step was then performed, followed by 10

minutes ultra-sonication in acetone to remove the photoresist. This step not only opens the contacts for heater pads, but also for the PC layer to contact with the bottom tungsten pads.

The fourth mask layer is for patterning the PC layer, shown in Figure 3.5(a). The PC layer, 50 nm crystalline GeTe was uniformly sputtered using AJA system. Specifically, in this device, the GeTe was sputtered from an alloy target with 50% of Ge and 50% of Te. But alternatively, GeTe, or Ge_xTe_{1-x} can be sputtered from two elemental targets. It is required that the film is in the crystalline state since the lead trace of PC strip cannot be transformed by the heater. We will lose the sensitivity to see the resistance change in this case. The sputtering was done at 50 W DC power, 5 mTorr pressure, 60 sccm Ar flow rate, and 250 ºC elevated temperature. The sputtering rate for GeTe is 12 nm per minute. As comparing to sputter PC material at room temperature and anneal it to obtain crystallized film, sputtering it at elevated temperature is desirable in terms of side wall coverage. Due to the 10% volume change from amorphous GeTe to crystalline GeTe during the annealing, cracks could appear on the side wall, making the device very unreliable. Elevated temperature deposition of GeTe film eliminates this problem and provides good side wall coverage and reliability. Without taking the wafer out of the chamber and breaking the vacuum, another sputtering step of 50 nm SiO_2 was performed. The RF power was set to be 250 W, at 3 mTorr and 60 sccm Ar flow rate. The sputtering rate is approximately 1.9 nm per minute. The standard photolithography step was performed with AZ developer in resist development.

An ion-mill etch step was used to etch the SiO_2 and GeTe layer using the Commonwealth Scientific Ion Mill. On the one hand, GeTe is considered as hazardous material and etching it in RIE systems would introduce contamination. On the other hand, ion-mill etch rate for AlN is extremely low (< 2 nm per minute), so there is no concern of etching through the layers beneath the PC layer. The etching was done at 0.12 mTorr, 4 sccm of Ar flow rate, 10 mA Ar^+ ion beam current and 500 V voltage. The neutralized current should be around -1 mA. The etch rate for GeTe is around 25 nm per minute, while the etch rate for SiO_2 is around 10 nm per minute. The total etch time was determined to be 12 minutes, carefully taking into account the over-etch time that the exposed tungsten layer can withstand. Finally, the resist can be removed

using another O_2 plasma soften step followed by ultra-sonication in acetone. The PC layer formed the cross-bar like structure with the tungsten heater strip and made contacts with the bottom tungsten layer (defined by the first mask). The final metal traces will make contacts with the thick tungsten pads (defined by the second mask), providing electrical access to the PC layer.

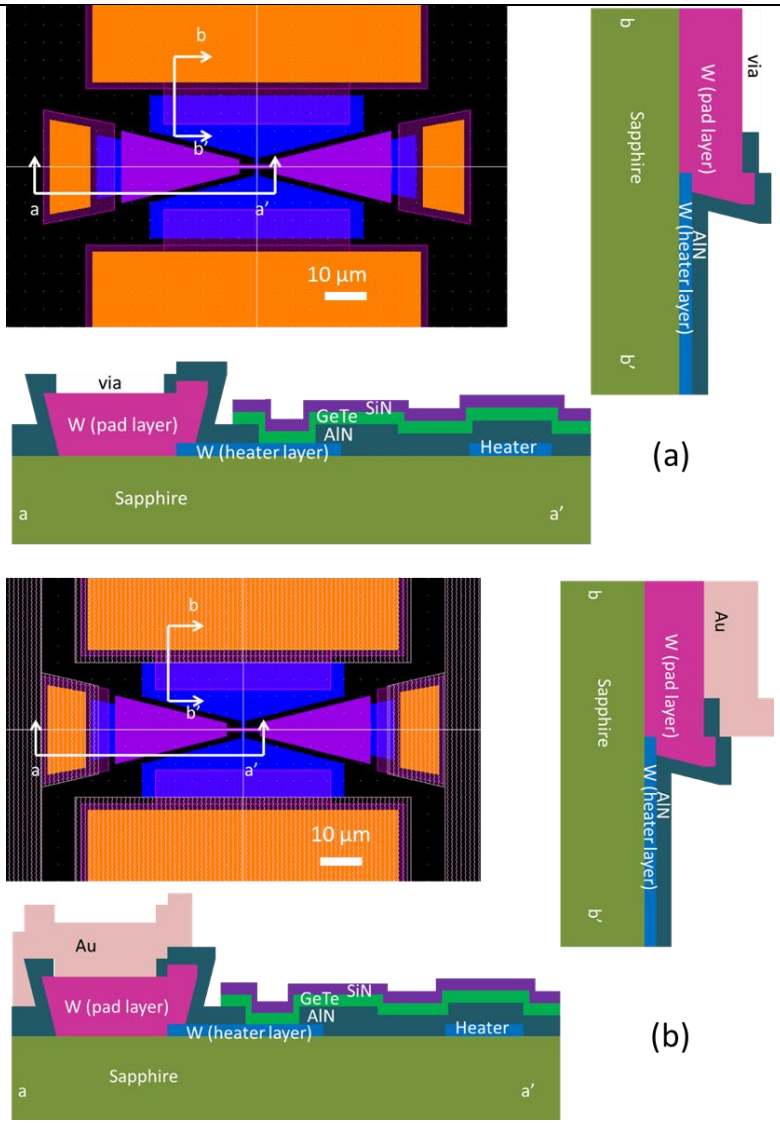

Figure 3.5 top view and cross-section schematics from two directions of (a) the fourth mask layer for PCS and (b) the fifth mask layer for metal traces

The fifth mask layer is for patterning metal traces for probe accesses through a lift-off process, shown in Figure 3.5(b). AZ4220 resist was used in this lithography process, providing around 2.2 μm thickness with the same spin recipe as in the previous steps. The exposure time in MA6 was set to be 30 seconds, and it took 1.7 minutes for resist development in the solution made of 2 parts of AZ developer and 1 part of DI water. A standard descum step was performed before the sputtering. Finally, metal traces were sputtered. Specifically, in this device, Au was used as the trace metal, but Pt or Cu can also be used. Using the AJA system, a thin layer (10 nm) of Ta was sputtered first as the adhesion layer, followed by 150 nm deposition of Au. By ultra-sonicating in acetone for 10 minutes, the lift-off was completed.

3.4 Preliminary Thin Films Characterizations

The ON-state resistivity of GeTe was measured to be 3.4±0.1 μΩ·m using the Van der Pauw method, which is higher than the reported bulk value of 1.5 μΩ·m [29], but is consistent with the reported thin film value of 3.1 μΩ·m [116]. The resistivity and temperature coefficient of resistivity (TCR) of the tungsten film were measured to be 83.4±1 nΩ·m and 3.1±0.1 ppt/K respectively using methods described in the previous chapter. The TCR of the crystalline GeTe was measured to be 1.4±0.1 ppt/K. The total heater resistance was measured to be 15 Ω and heater strip was measured to be 70.4% of it. The actual thickness of GeTe was determined to be 63 nm while that of the tungsten was determined to be 58 nm.

3.5 COMSOL Simulation

PC temperature transients generated by different heater pulses were determined by time domain transmissometry (TDT) combined with COMSOL simulation described in the previous chapter, based on input pulses from PG1 and transmitted voltage transients measured by Scope1. Figure 3.6(a) and (b) show the 3-D perspective view of the COMSOL model for this device. The precise structure of the device as shown in Figure 3.2 is used. The top passivation layer and part of the AlN layer has been hidden in Figure 3.6(b) to show more details beneath them. Similar to the simulation setup in the previous chapter, electric current, electric circuit and heat transfer modules were used. The electric current and electric circuit settings

remain the same as those used in the heater simulation, since the extra layers on top do not contribute to the electrical behaviors and power generating of the device switching process. For the heat transfer module, the bottom of the substrate was set to be 293 K, while the rest of the exposed surfaces were set to be thermally isolated.

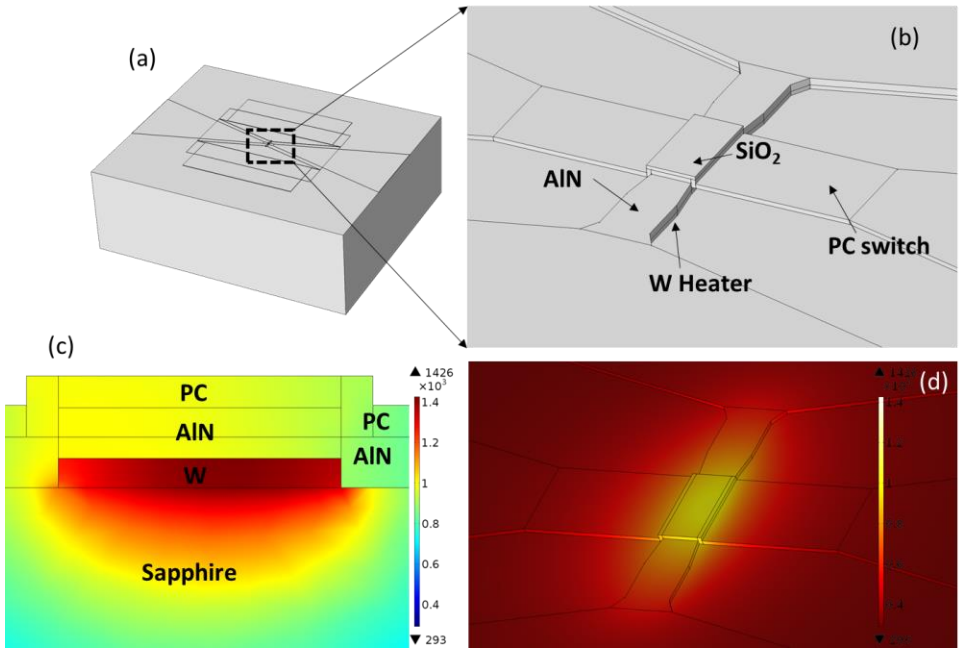

Figure 3.6 (a) 3-D perspectic schematic and (b) zoomed in schematic of the device structure modeled in COMSOL. (c) cross-section view and (d) perspective view (AlN layer is hidden) temperature profile generated by applying a 4 V 100 ns pulse to the heater, taken at t = 100 ns.

The TCR and resistivity of tungsten are set to be 83.4 nΩ·m and 3.03 ppt/K in the simulation, respectively, as measured from the thin films characterizations. The thermal properties of tungsten and sapphire are the same as those used in the previous chapter. The thermal conductivity, k_{th}, of GeTe is assumed to be 1.6 W/(m·K).[117] Like [88], the AlN is assumed to have a k_{th} of 50 W/(m·K). However, unlike [88], a thermally resistive interface layer, having an interface resistance-area product, RA_{th}, of 76 m^2-K/GW was included between the tungsten and AlN in order to match the experimental minimum

power to amorphize (MPA) measurements (simulated top PC surface exactly reaching melting temperature for MPA pulse). While this is a high value of interface thermal resistance, it is consistent with that reported in [118] for a W/AlN interface, and may reflect significant disorder at this interface. The uncertainty in the CQT value associated with the uncertainty in the assumed PC temperature as controlled by RA_{th}, is addressed below. The GeTe heat of fusion was not included in the simulation, since it was determined to have very small effect on the temperatures (maximum deviation in temperature is less than 1.5%) at the power level (MPA) in our experiments.

3.6 Device Cycleablility Measurement

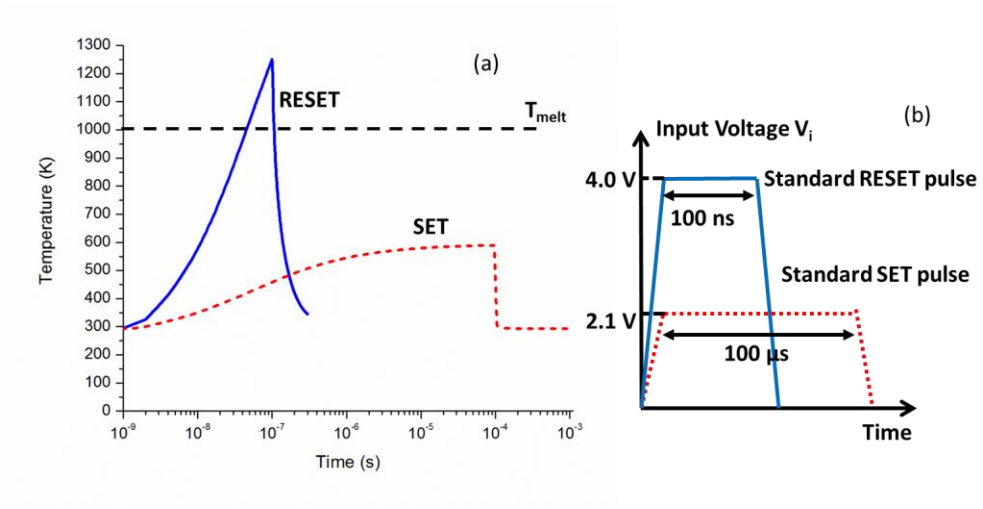

Figure 3.7 (a) simulated temperature transients of the top surface of the PC layer for standard RESET (solid blue curve) and SET (dashed red curve) operations, note that the time is in log scale for clearer comparison (b) standard RESET (solid blue curve , 4 V 100 ns) and SET (dashed red curve, 2 V 100 µs) pulses sent to the heater.

Figure 3.7 shows the simulated temperature transients based on two different electrical pulses as the heater input. The simulated transients were plotted in log scale of time for comparison between short and long transients in the same figure frame. The simulation was done using the model described in the

previous section, well-calibrated for accurate thermometry by enforcing the consistency between measurements and simulation. A standard RESET pulse, with 4.0 V magnitude, 100 ns pulse width and 2 ns rise and fall time can generate temperature above melting point of GeTe in the PC layer (> 1250 K) and provide enough quenching speed to amorphize the PC. A standard SET pulse, with 2.1 V magnitude, 100 μs pulse width and 2 ns rise and fall time, is sufficient to crystallize the PC layer from OFF-state to ON-state. Figure 3.8 shows the cyclability measurement of the resulting device. OFF-state and ON-state DC resistances were measured after each pulse. The PCS can be cycled between a 2.6±0.2 MΩ (OFF-state) and 620±3 Ω (ON state) more than 100 times without failing, demonstrating that that this is a reliable geometry for testing devices to determine the CQT. Note that the ON-state is too high to be useful as an RF switch due to the absence of high conductivity leads and dimensions chosen for speed rather than the lowest possible resistance.

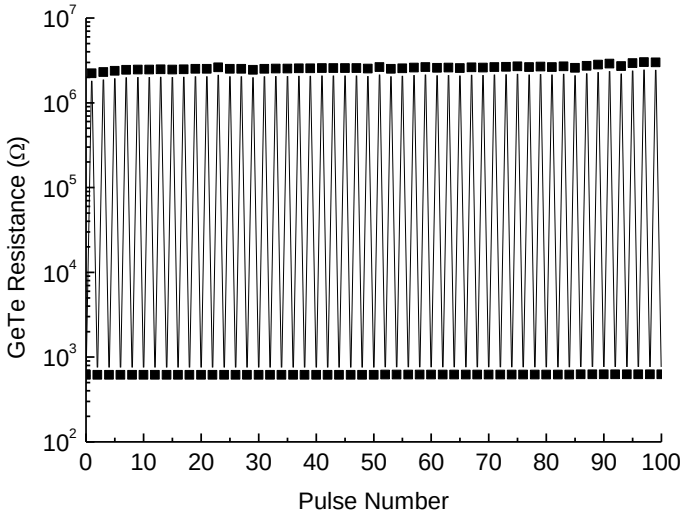

Figure 3.8 GeTe DC resistance measured over RESET/SET pulse cycles

3.7 Test Setup

Figure 3.9 shows the experimental set-up for in-situ measurement of crystallization dynamics. The heater is connected in parallel to a pulse generator input (PG1, output port 1 from the Agilent 81110A pulse generator) and a 50 Ω oscilloscope channel (Scope1, channel 1 of the DSO1014A oscilloscope) by 1 meter long 2.92 mm coaxial cables. The PC is connected in series with a pulse generator input (PG2, output port 2 from the Agilent 81110A pulse generator) and a 50 Ω oscilloscope channel (Scope2, Scope1, channel 2 of the DSO1014A oscilloscope) by 1 meter long 2.92 mm coaxial cables. A BNC coaxial cable was used to connect the trigger output of the pulse generator and the trigger channel (channel 3) of the oscilloscope.

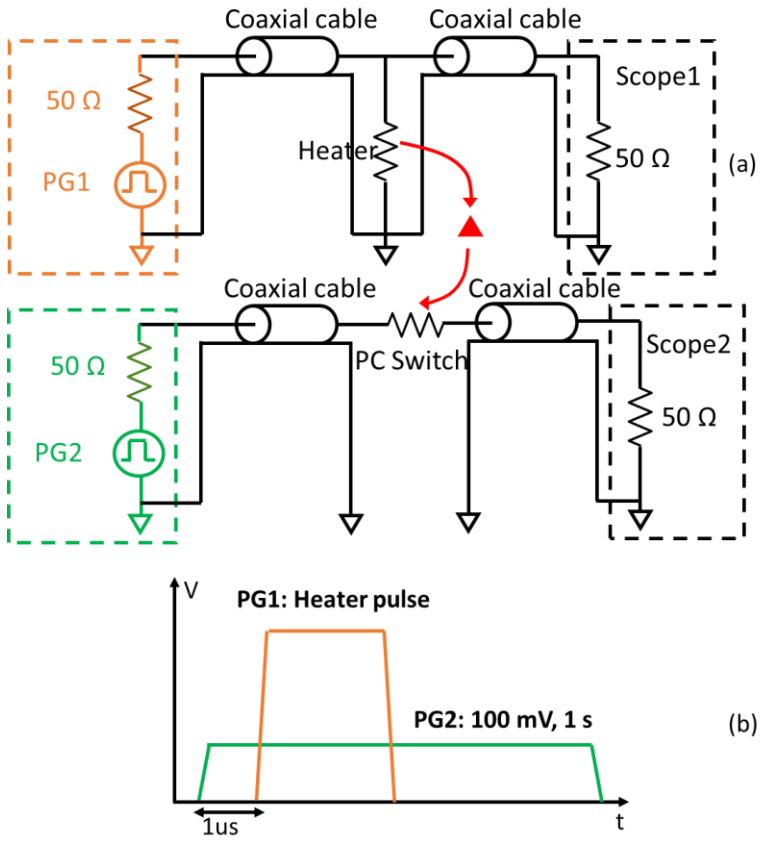

Figure 3.9 (a) testing circuit for CQT measurement and (b) configurations of the heater programming pulse (sent from PG1) and PC reading pulse (sent from PG2), the reading pulse is sent 1 μs ahead of the programming pulse

By applying pulses from PG1 to the heater, it is possible to heat the PC and produce SET/RESET operations. The voltage on Scope1 is the transmitted voltage transient from the heater which is used to determine the temperature transients. A standard read pulse with low reading voltage (100 mV) and long pulse width (1 s) was used with PG2 to sense the resistance change in the PC during heating. The voltage on Scope2, V_{Scope2} is related to the PC resistance R_{PC} by:

$$V_{Scope2} = 2V_{Read}\left(\frac{R_{Scope2}}{R_{PC}+R_{Scope2}}\right) \tag{3.3}$$

where V_{Read} is 100 mV and R_{Scope2} is 50 Ω. Thus the PC resistance can be extracted from V_{Scope2} based on (3.3). The standard read pulse was sent one micro-second ahead in time of the programming pulses, allowing enough time for the reading voltage transient to be stabilized for accurate sensing. The low voltage level should not cause any heating in the PC layer (simulation shows less than 1 K temperature rise) and is much lower than the threshold switching voltage of the PC layer (typically higher than 2 V for this type of device).

3.8 CQT Measurement

To estimate the CQT of this geometry, we iteratively pulsed the heater and measured the transmitted response from the scopes. At each iteration, the PC was firstly transformed to an ON-state by a standard SET pulse. A standard read pulse was then applied by PG2 to the PC. One micro-second later, we applied RESET pulses using PG1 to the heater with the same rise time (100 ns), pulse width (1 μs) and voltage (3.0 V), but various pulse fall-time for each iteration. The RESET pulse fall time was increased from 100 ns to 1 μs. This allows the heater to heat up the PC to the same peak temperatures but cool at different rates. For the Agilent 81110A pulse generator, it is required that the difference between pulse rise and fall time is smaller than 10x. To get the maximum range of pulse fall time (10 ns for fastest quenching to 1000 ns for slowest quenching), we used a RESET pulse configuration that is different than the standard RESET pulse, while still allowing the amorphization of the PC layer.

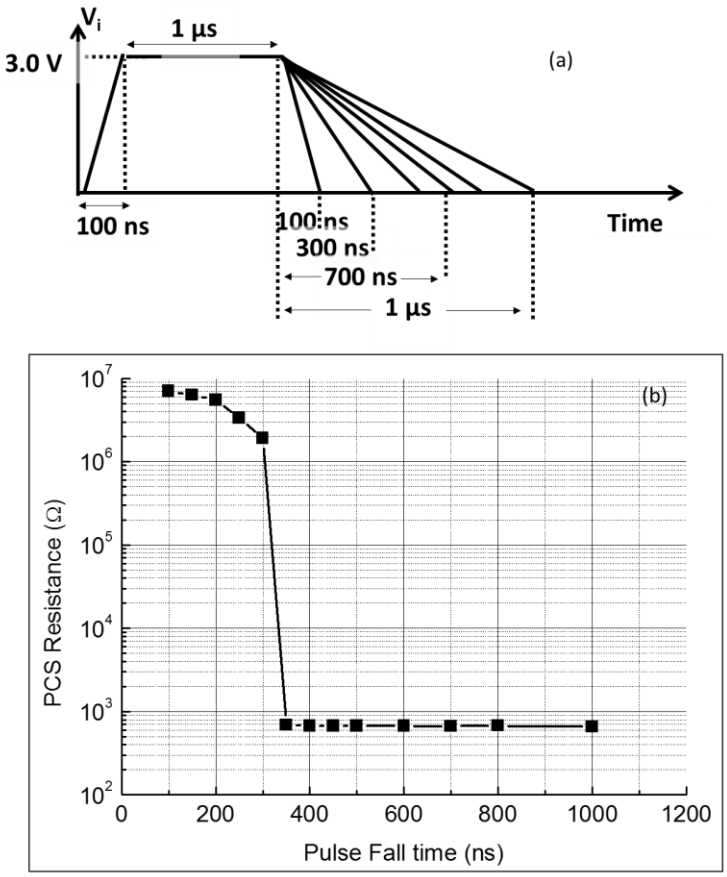

Figure 3.10 (a) RESET pulse configurations with different fall time (b) GeTe DC resistance measured after RESET pulses with different fall time

Figure 3.10 shows PC DC resistance measured after each RESET pulse. For fall times longer than 300 ns, the RESET pulse failed to transform the PC from the ON-state to OFF-state, suggesting that a pulse with a fall time of 300 ns will quench temperature in PC in time close to the CQT. As we further increased the pulse fall time, the resistance remains at 620 Ω, which is consistent with the ON-state resistance achieved by standard SET pulses. For fall times shorter than 300 ns, the PC resistance decreased while the pulse fall time was increased. This suggests that larger portion of the PC was re-crystallized with slower quenching.

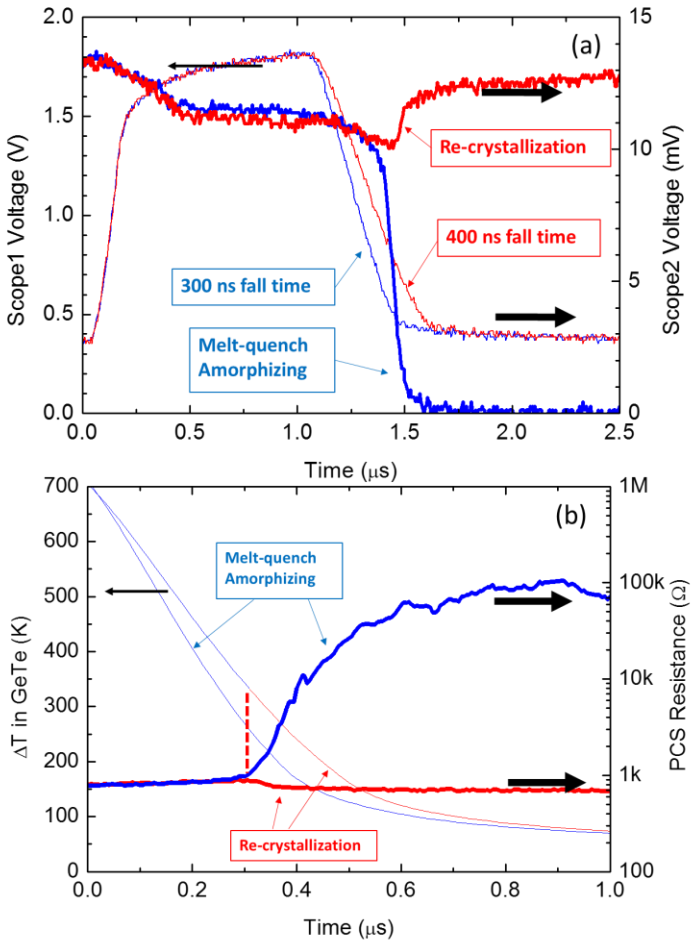

Figure 3.11 (a) Read voltage transients (Scope2) generated by RESET pulses with 300 ns (blue) and 400 ns (red) fall time and transmitted RESET pulse transients (Scope1) (b) Simulated temperature transients and extracted PC resistance transients at 300 ns (blue) and 400 ns (red) fall time. Starting time is adjusted to when temperature fell below ΔT_{melt}. Blue represents OFF-state and red represents ON-state.

Figure 3.11 shows how the read voltage transients (Scope2) and the resistance of the PC dynamically change when the RESET pulses with different fall times (300 ns and 400 ns) are applied. In

Figure 3.11(a), the thin curves represents voltage transients as measured by Scope1 while the thick curves represents those as measured by Scope2. In Figure 3.11(b), the thin curves represents the simulated PC temperature transients while the thin curves represents the extracted PC resistance transients corresponding to the thick curves in Figure 3.11(a). As shown in Figure 3.11(a), read voltage transients in both cases did not diverge until the time associated with the fall of the RESET pulses. For pulses with a 300 ns fall time (blue curve), the voltage continued decreasing, showing that the PC was transformed from the ON-state to the OFF-state. For the pulse with the 400 ns fall time, on the other hand (red curve), the voltage first decreased and then increased, showing that the PC was re-crystallized during the cooling process. Figure 3.11(b) shows how the PC resistance changed with respect to the PC temperature transients. The starting time of the plot is adjusted to the time when the temperature fell just below ΔT_{melt} (705 K, with absolute T_{melt} of 997 K) [119]. The temperature transient that cools more slowly corresponds to the re-crystallization behavior. We identify the time when the PC resistance reached the maxima as the point at which the re-crystallization occurred. Thus, we marked the curve before re-crystallization occurred in blue (OFF-state) and the curve after in red (ON-state). We simulated all temperature transients based on the input RESET pulses and transmitted voltage transients measured by Scope1, producing the red and blue curves shown in Figure 3.12.

From Figure 3.12, by locating the red curve with the fastest cooling time, we can find out the temperature that results in the minimum crystallization time, $\Delta T_{x,tmin}$, to be 303 K (absolute $T_{x,tmin}$ of 596 K). This value is consistent with [33]. But since this is a non-isothermal process during the temperature cooling, a material-related $T_{x,tmin}$ is yet to be determined by more reliable method. This will be discussed in details in Chapter 6 and Chapter 7. We can also find the temperature transient corresponding to the successful RESET pulse with the longest fall time (in this case 300 ns). By assessing the time for the temperature to cool from ΔT_{melt} to $\Delta T_{melt}/e$, we can determine the CQT to be 317 ns for these GeTe switches, under the assumption that an MPA pulse brings the top surface of the phase change layer exactly to its melting point (RA_{th} = 76 m^2-K/GW). With the conservative assumption of a maximum temperature overshoot at MPA of

35 ºC or 5% of the temperature rise (RA_{th} = 38 m^2-K/GW), the CQT was reduced to 294 ns. This yields a CQT of 305 ns ± 11 ns in this device, subject to this uncertainty of PC temperature (35 ºC) at MPA. It should be noted that this dependence of cooling time on assumed peak temperature is a feature of a distributed model. A simple lumped thermal model would not show such behavior as it would be described by a single thermal time constant, independent of peak temperature. It should also be noted that the exact values of RA_{th} and other thermal parameters are not critical in this uncertainty analysis. It is the uncertainty about the peak PC temperature (which we assume to be bounded at 5% overshoot) that determines the uncertainty in CQT. On the other hand, it should be noted that the measured CQT is geometry specific. A larger volume of amorphized PC layer could lead to a longer CQT. Although the measured CQT is specifically associated with this PCS design, the same methodology can be applied to various designs for RF PCS. In Chapter 6, more universal material-related crystallization dynamics properties will be investigated and reconciled with the CQT measurement results.

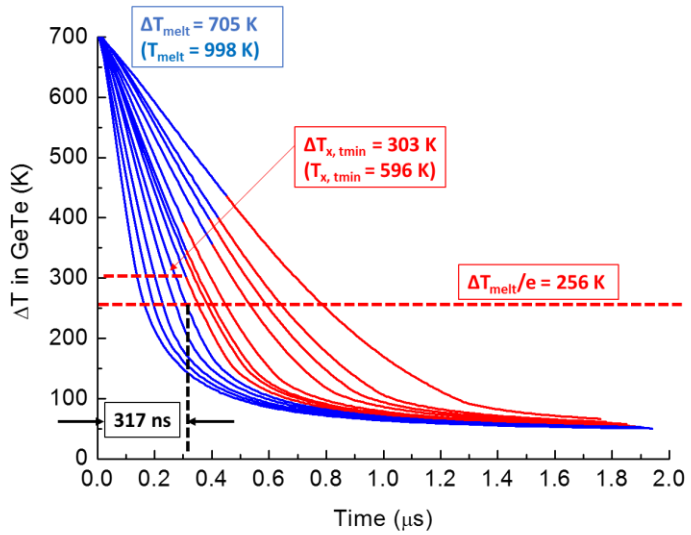

Figure 3.12 Temperature transients generated by pulses with different fall time. Blue represents OFF-state and red represents ON-state.

3.9 Crystallization Time Measurement

Using the same methodology and test vehicle, we can also measure the PC SET switching time (i.e. the crystallization time) as a function of temperature. The switching time, τ_x, is dependent on PC temperature, according to the Arrhenius equation for PC material crystallization as follows:

$$\tau_x = \tau_{x0} \exp\left(-\frac{E_x}{k_B T}\right) \tag{3.4}$$

Where τ_{x0} is a pre-exponential factor, E_x is the activation energy for crystallization and T is the absolute temperature. The PC was initially transformed to an OFF-state by a standard RESET pulse. A standard read pulse was then applied by PG2 to the PC. One micro-second after the read pulse, a SET pulse was applied by PG1 to the heater. Figure 3.13 shows the transmitted SET voltage transients measured by Scope1 (red in color) and transmitted PCS read voltage transients measured by Scope2 (black in color). The voltage on Scope2, V_{Scope2} is related to the PC resistance R_{PC} by (3.3). Thus V_{Scope2} is less than 1 mV when the PCS is in OFF-state with resistance around 2.5 MΩ. When the PC was heated, V_{Scope2} increased because the OFF-state PCS resistance decreases with increasing temperature. A sudden transition in V_{Scope2} was observed from a low voltage (1 mV) to a high voltage (14 mV) due to the transformation of the PCS to the ON-state with resistance around 620 Ω. We measured τ_x as the time from the beginning of the SET pulse to when the read voltage reached 50% of its final value. As shown in Figure 3.13, the GeTe SET switching time was 105 μs at 537 K (1.8 V SET voltage), and 1.02 μs at 615 K (2.1 V SET voltage), illustrating the exponential dependence noted in (3.4).

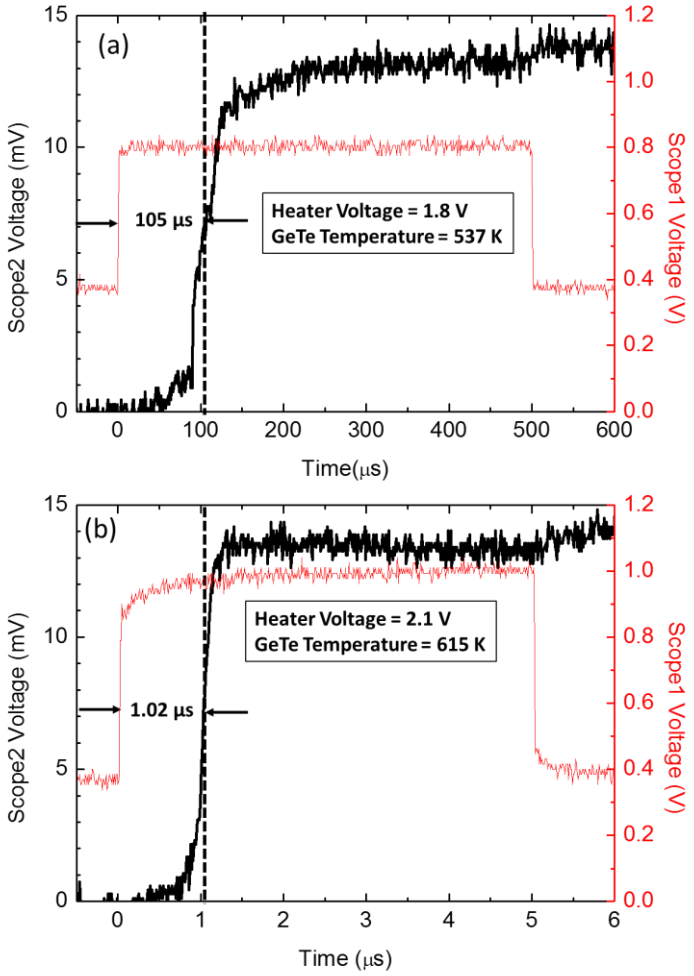

Figure 3.13 Transmitted heater SET pulses on Scope1 (red data) and PC read pulses on Scope2 (black data) for (a) 1.8 V SET voltage and (b) 2.1 V SET voltages

SET voltages varying from 1.6 V to 2.3 V were chosen to generate temperatures below the GeTe melting temperature for crystallization. The switching times and corresponding temperatures were measured to produce the bottom half of the crystallization boundary for the GeTe TTT diagram shown in Figure 3.14(a). Combining the bottom half of the TTT diagram with the temperature transients labelled as

blue and red colors in Figure 3.12, it can be seen in Figure 3.14(b) that the red curves are initiated at the point where the temperature transient crosses the crystallization boundary, as expected.

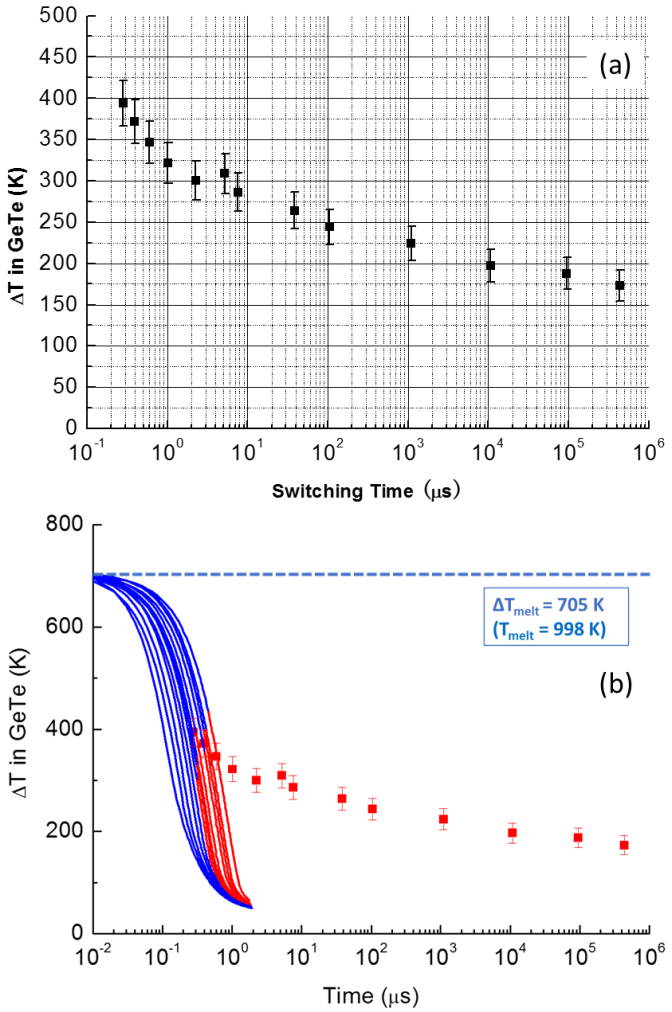

Figure 3.14 (a) the bottom half of the crystallization boundary for a GeTe TTT diagram determined from the described measurements (b) Temperature transients generated by pulses with different fall time combined with bottom half of TTT diagram (scattered data). Blue represents OFF-state and red represents ON-state.

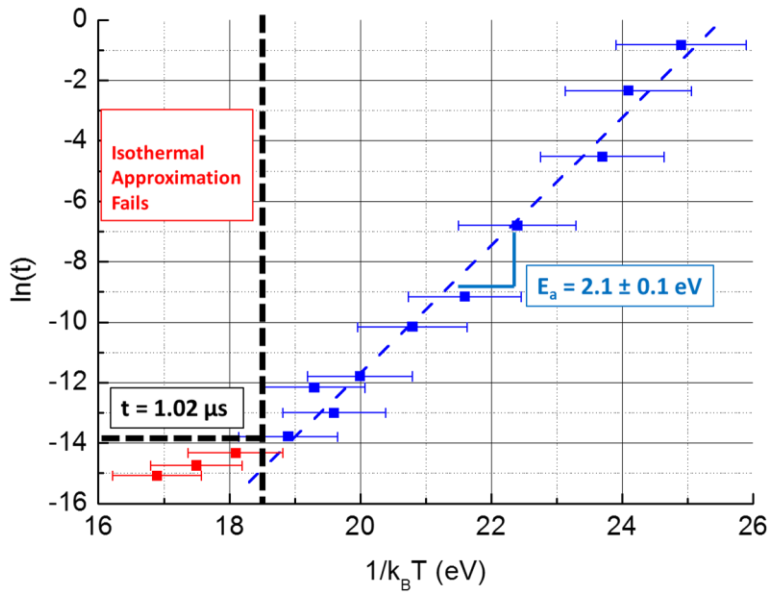

Figure 3.15 Arrhenius plot for GeTe crystallization. Blue data are used for crystallization activation energy extraction while red data are inaccurate due to the failure of the isothermal approximation. The method for correcting the non-isothermal data will be detailedly described in Chapter 7.

The activation energy for crystallization can be estimated by plotting the natural logarithm of the SET switching time as a function of $1/k_BT$ as shown in Figure 3.15. A sudden change of activation energy can be found at 630 K. At temperatures lower than 630 K and switching time longer than 1.02 µs (blue in color), the activation energy for crystallization E_x was be extracted to be 2.1±0.1 eV. This value is in good agreement with values reported for GeTe E_x: 1.96 eV [120], 2.19 eV [121] and 2.03 eV [46]. For time shorter than 1.02 µs (red in color), the isothermal approximation fails in this region. In support of this, Figure 3.13(b) shows that the temperature reached steady state approximately 1 µs after the pulse had been applied. Thus for switching times smaller than 1 µs, we cannot assume the PC is under isothermal condition and the temperatures of the red data are over-estimated, which is one possible source of this non-Arrhenius

behavior. Another material-related mechanism may be responsible for this non-Arrhenius behavior. Similar E_x (0.5 eV) has been observed by [102] and [36] at high temperatures ($T >$ 500 K and $T >$ 620 K respectively) , suggesting that the change of E_x is also due to the material crystallization dynamics properties other than the artifact of the experiments. The change of activation energy is attributed to the fragility of PC materials by [102] and [36].

As both of the sources may be responsible, to eliminate the artifact of the non-isothermal heating, devices with much faster thermal response were built. The study of the high temperature crystallization dynamics using the 2nd gen device will be further discussed in Chapter 6 and Chapter 7. Additionally in Chapter 7, we will re-visit the non-isothermal heating and develop an iterative method to address this issue and correct the data at high temperatures.

3.10 Summary

In this chapter, we have demonstrated the 1st generation PC test device driven by an electrically isolated heater thermally connected by AlN dielectric layer with good cycleability (> 100 cycles) that is suitable for measuring PC material properties, specifically the crystallization dynamics such as the CQT and the temperature dependent crystallization times. A detailed process flow and mask layouts was presented to thoroughly illustrate how to design and fabricate such a device. By using TDT measurements on this switch combined with dynamic sensing of the switch resistance and COMSOL simulation we were able to determine the bottom half of GeTe's the crystallization boundary on a TTT diagram. Moreover, by measuring RESET events using pulses with varying fall-times, we determined the CQT for these GeTe devices to be 305 ns ± 11 ns. This number is valuable for designing low-power PCS. It should be noted that the measured CQT is a design specific parameter, but the same methodology can be applied to different PCS designs. Chapter 6 and Chapter 7 will present a more universal mechanism that we can also reconcile with the CQT measurement results. The crystallization activation energy for crystallization is extracted be 2.1±0.1 eV at temperatures lower than 630 K. At high temperatures, the extracted activation energy is much

lower (0.5 eV). The high temperature data needs to be corrected as the PC is no longer under isothermal heating. But other than this artifact, the material related mechanism, fragility, may be also responsible for this non-Arrhenius behavior. This methodology can still be applied to study crystallization dynamics at low temperatures, and can be further applied to study indirectly-heated PCS using off-stoichiometric PC materials in the future.

Chapter 4: Threshold Voltage Study for Phase Change RF Switch

4.1 Abstract

For power amplifier applications, watt-level power handling is desired for RF switches. This requires the RF switch to withstand over 10 V in its OFF-state. However, the unwanted threshold switching may occur when the voltage applied to the PC switch exceed certain threshold, causing it to transform from OFF-state to ON-state. Thus, threshold voltage is a critical parameter for PC RF switch, as it determines the maximum power handling for the switch.

In this chapter, the techniques for threshold voltage measurement will first be presented. Several experimental observations of the threshold voltage properties will then be reported and discussed. The absence of negative differential resistance (NDR) suggests that GeTe has a different threshold switching mechanism as discovered for GST or oxide. The evidence of time dependent threshold voltage shows the possibility to raise threshold voltage by increasing frequency. Additionally, the correlation of resistance drifting and threshold voltage will be discussed.

A majority of this chapter will focus on the threshold voltage variation. The observation that the voltage variation origins from the threshold field variation will be presented. These variations will be then studied for different device structures. Their dependency on geometry of the device will be presented, which will provide insight to the switching mechanism. On the other hand, the quantification of threshold field and its variation is also useful for predicting the threshold voltage of PC RF switches.

4.2 Threshold Voltage Measurement

Three different methods to measure the threshold voltage V_{th} will be discussed in this section. The most frequently used method is the DC I-V sweep using the Keithley 2400 source meter. As shown in Figure 4.1(a), the source meter is directly connected to the PC device through needle probes and BNC cables. The needle probes should land on the two electrodes to access the OFF-state PC material, so that

the voltage can be applied to it. A series resistor with resistance of R_s is usually used as a ballast resistor to prevent from overdriving the current through the PC device, which could blow up the device, when the threshold switching occurs. Typically, R_s needs to be higher than the ON-state resistance of the device to allow most of the voltage drops on itself when the device is ON. Figure 4.1(b) shows the output voltage of the source meter as a function of time during a typical I-V sweep for the device. The voltage is raised step by step and in each step the voltage is held for 100 ms. Meanwhile, the source meter can read the current go through the device, generating an I-V characteristic of the device. Note that the PC voltage V_{PC} needs to be extracted from the measured voltage V_{meas} and measured current I_{meas}:

$$V_{PC} = V_{meas} - I_{meas} \times R_s \tag{4.1}$$

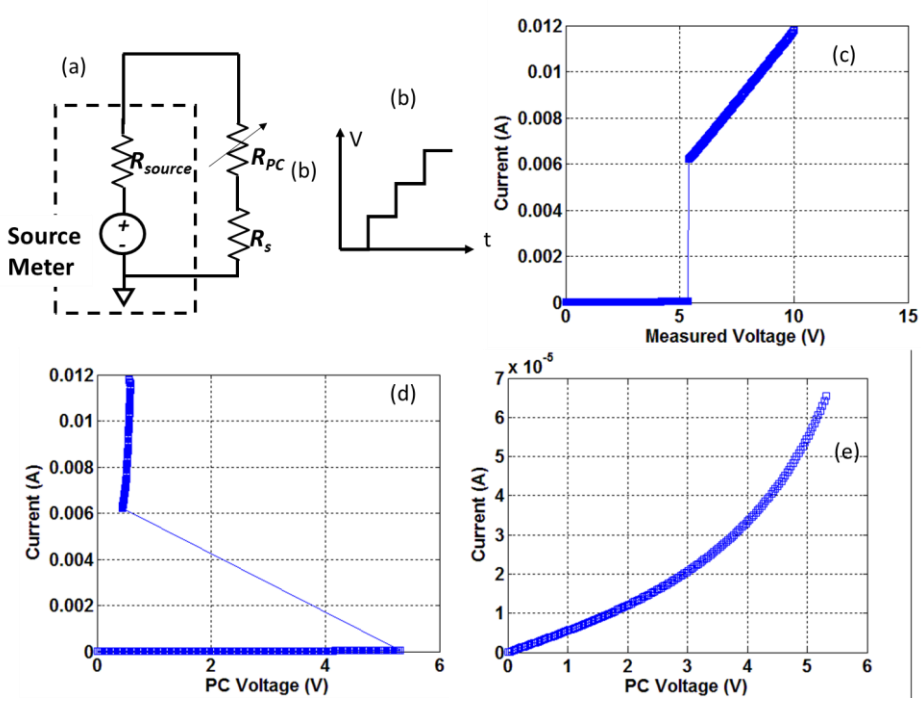

Figure 4.1 (a) DC I-V sweep circuit setup using Keithley source meter (b) schematic of source meter output voltage (c) I-V characteristic for the measured voltage and current (d) I-V characteristic for the PC device (d) zoomed in view of the PC device I-V characteristic

Figure 4.1(c) shows a typical I-V sweep of device current (same as measured current) versus measured voltage, with a R_s of 890 Ω. Based on (4.1), the PC I-V characteristic can be extracted, shown in Figure 4.1(d). A zoomed in view of the PC I-V characteristic is shown in Figure 4.1(e). It can be seen that for this device the V_{th} is around 5.3 V. When the device is in OFF-state, the total resistance is high and thus the measured current is below 70 μA. After the device voltage exceeded the V_{th}, the total resistance drops and the total current is raised to higher than 6 mA. In Figure 4.1(d) it can be seen that, the device voltage also suddenly drops from 5.3 V to around 0.6 V, since most of the voltage now drops on the series resistor to protect the device.

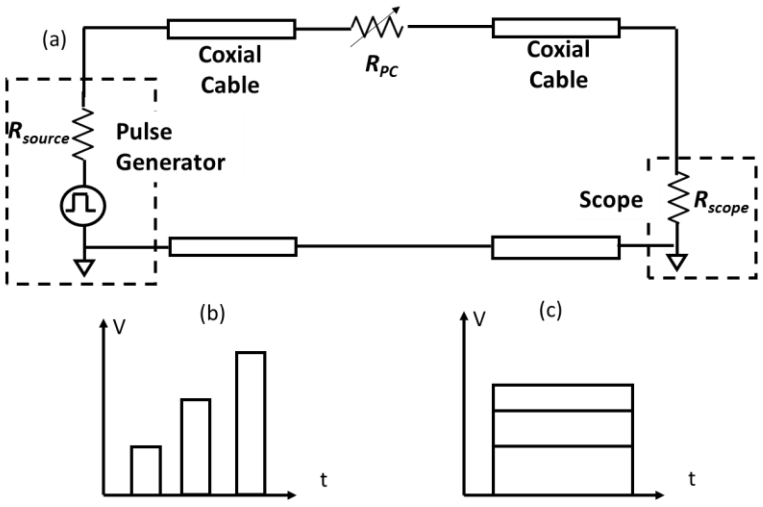

Figure 4.2 (a) circuit setup for pulsed I-V and time dependent V_{th} measurement (b) output voltage schematic for pulsed I-V measurement (c) output voltage schematic for time dependent V_{th} measurement

Alternatively, pulse generator can be used to generate pulsed I-V characteristic. Figure 4.2(a) shows the circuit schematic for pulse measurements on the PC devices. The pulse generator is connected with the PC device and the oscilloscope through coaxial cables and RF probes. A through setup is used so that the PC device is in series with the scope. In this way, the impedance of the scope (50 Ω) serves as a ballast

resistor. For each pulse, the output voltage from the pulse generator is V_{source} and the voltage on the scope is V_{scope}. Thus, the voltage on the device V_{PC} can be calculated as:

$$V_{PC} = 2V_{source} - V_{scope} \tag{4.2}$$

And the current I_{PC} can be calculated as:

$$I_{PC} = V_{scope} / R_{scope} \tag{4.3}$$

The pulsed I-V characteristic is useful when the temperature inside the PC device is a concern. Similar to the DC I-V sweep, pulses with the same pulse width but elevated voltages will be sent to the device in sequence, as shown in Figure 4.2(b). For the same V_{th}, the shorter the pulse width is, the lower the temperature is generated in the PC. In this way, threshold voltage can be studied by eliminating the artifact of possible temperature effect. However, due to the high PC OFF-state resistance, V_{scope} is very small (< 50 mV), which leads to a low signal to noise ratio for the pulsed I-V characteristic before the threshold switching occurs.

Another measurement can be achieved using this setup is the time dependent threshold switching measurement, which will be discussed in detail in section 4.4. The output voltage schematic is shown in Figure 4.2(c). In this measurement, long pulses (pulse width of 100 ms) will be sent to the PC device with elevated voltages. The sudden change of PC resistance can be captured by the scope voltage during the pulsing. This change of resistance corresponds to the threshold switching at the input pulse voltage. For different voltages, the time when the change takes place varies. In this way, a correlation between time and V_{th} can be obtained.

4.3 Absence of Negative Differential Resistance Switching

Negative differential resistance (NDR) is observed to take place when the threshold switching occurs for chalcogenides (e.g. GST) and can be explained by various electronic based models such as

thermally assisted hopping or impact ionization [58], [59]. After the NDR event, the conductive filament is formed and allows more current to pass through to eventually be crystallized through joule heating and the classic crystallization process, referred as memory switching. However, in the NDR regime, despite that the conductive filament exists, the PC material is still considered as amorphous. This is because the OFF-state can be spontaneously recovered when the voltage is not maintained on the device [62]. In other words, no phase transformation takes place.

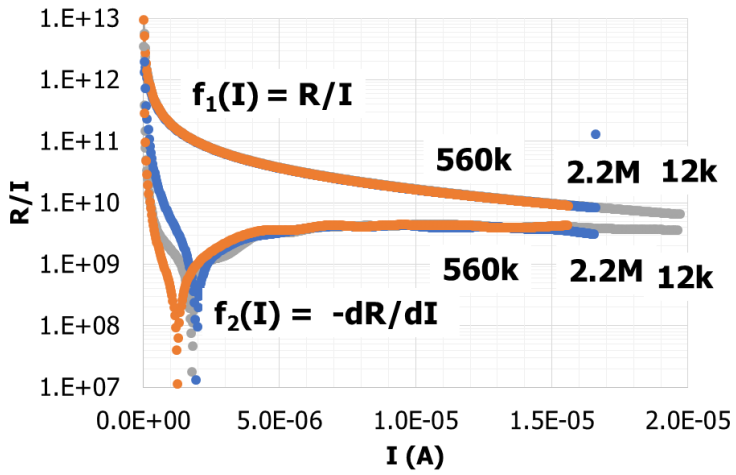

Figure 4.3 Combined plot of $f_1(I)$ and $f_2(I)$ for different ballast resistors

However, such NDR events are not observed in the I-V characteristic for GeTe based devices. To examine the NDR event, we can perform the following transformations on the I-V characteristic measured from the OFF-state RF PCS shown in Figure 1.8. From Ohms' Law, and assuming a current dependent resistance of the PC $R(I)$, we have:

$$dV = R(I)dI + IdR(I) \tag{4.4}$$

By dividing both halves by IdI, we have:

$$\frac{dV}{IdI} = \frac{R(I)}{I} + \frac{dR(I)}{dI} \tag{4.5}$$

Since by definition, NDR occurs when *dV/dI* is zero, we can define two functions:

$$f_1(I) = \frac{R(I)}{I} \tag{4.6}$$

$$f_2(I) = -\frac{dR(I)}{dI} \tag{4.7}$$

Based on (4.5), the intersection of $f_1(I)$ and $f_2(I)$ will be the start of NDR.

As shown in Figure 4.3, transformed I-V characteristic for different ballast resistors are plotted as $f_1(I)$ and $f_2(I)$. A clear discrepancy can be seen when the threshold switching occurs between two functions for all ballast resistors. The threshold switching directly leads to the memory switching after the I-V sweep. This suggests that NDR is not associated with the threshold switching for GeTe, and the mechanism of threshold switching for GeTe could be different from that for GST.

4.4 Evidence of Time Dependent Threshold Voltage

Threshold voltage V_{th} is observed to be time dependent. Its time dependency is especially of interest for the RF switch applications, because for different frequencies, V_{th} could vary. Using the experimental setup described in section 4.2 and Figure 4.2, we can quantify the time dependency of the V_{th}. The four-terminal directly-heated RF PCS shown in Figure 1.8 are used in this study. For each experiment, the PC is firstly transformed to the OFF-state using the heater. Then a pulse is directly sent to the PC, connected in the way shown in Figure 4.2(a). As shown in Figure 4.4(a), at the beginning of the pulse arrival, the scope voltage is negligible. This is due to the high OFF-state PC resistance comparing to the scope. However, after a certain switching delay time t_D, the scope voltage suddenly increases, in the orders of 1 V. For an applied voltage of 5 V, this corresponds to an ON-state PC resistance of 200 Ω, much smaller than the OFF-state value (50 kΩ). After the removal of the pulse, the PC resistance remains at 200 Ω, suggesting that this threshold switching directly leads to a permanent memory switching. Based on the COMSOL simulation,

the temperature rise caused by the pulse sent to the PC is negligible (< 1 K), not enough for directly causing the crystallization.

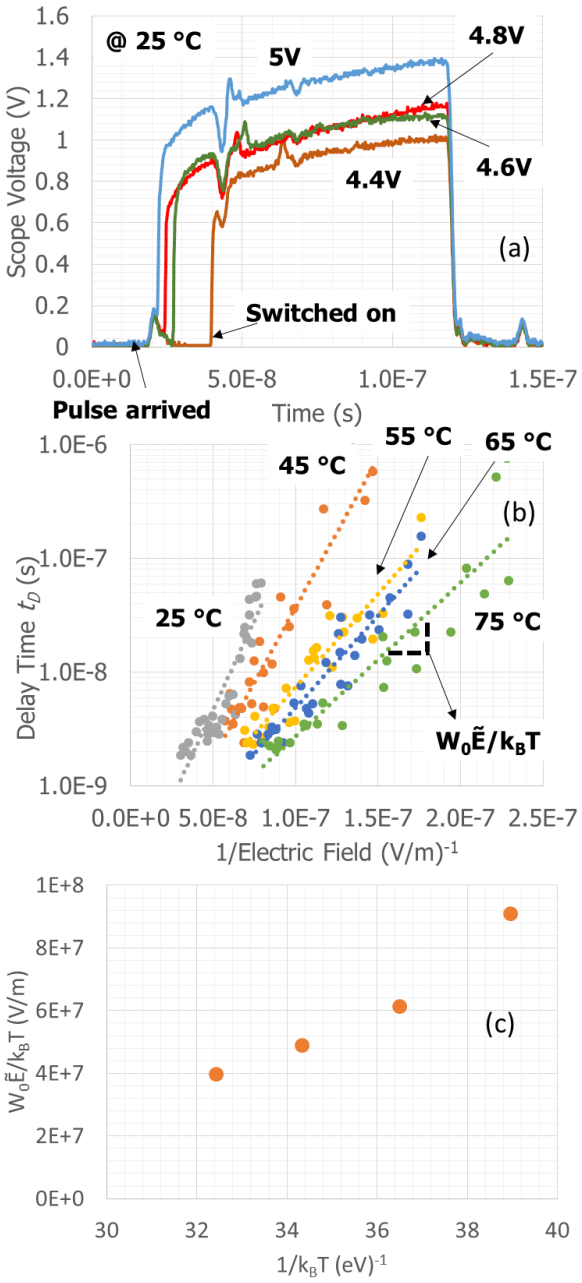

Figure 4.4 (a) Scope voltage transients for different input pulses at 25 ºC (b) the switching delay time t_D plotted versus 1/E at different stage temperatures (c) extracted E_0 plotted against $1/k_BT$

On the other hand, by sending pulses with different voltages to the OFF-state PC, the values for the switching delay time t_D are also different. Figure 4.4(b) shows the measured t_D as a function of $1/E$, where the electrical field E is calculated based on the amorphous region size (estimated from the OFF-state resistance) and the voltage applied to the PC. It can be seen that $log(t_D)$ is proportional to $1/E$, suggesting that an exponential dependency exists:

$$t_D = t_{D0} \exp(\frac{E_0}{E}) \tag{4.8}$$

where t_{D0} is a pre-exponential factor, E_0 is a parameter controls the field dependency for the delay time. This observation is consistent with the observations in [63]–[66].

The E_0 can be further studied for its temperature dependency. As shown in Figure 4.4(b), the same set of experiments were repeated for different temperatures and the slope (E_0) varies when the temperature changes. In the nucleation switching model proposed in [63]–[66], E_0 can be expressed as:

$$E_0 = \frac{W_0 \tilde{E}}{k_B T} \tag{4.9}$$

where W_0 is the classic nucleation barrier, $\tilde{E}$ is a characteristic electric field. Thus the V_{th}-time correlation can be expressed as:

$$V_{th} = \frac{W_0 \tilde{V}}{k_B T \log(\frac{t_D}{t_{D0}})} \tag{4.10}$$

where $\tilde{V}$ is a characteristic voltage.

This model is attractive since it allows non-NDR event for threshold switching, but is not consistent with the data observed. As shown in Figure 4.4(c), E_0 is plotted against $1/k_BT$ as in an Arrhenius plot, and the slope can be extracted as $W_0 \tilde{E}$, a material dependent parameter. However, by fitting the data, the

intercept ends up with a large value of -2×10^8 V/m, not the expected value of zero. Although W_0 is also temperature dependent, but the temperature dependency is too weak at low T to give rise to the negative intercept. Thus, the origins of this disagreement and the effectiveness of the nucleation switching model remain to be investigated. But nevertheless, (4.8) is still useful for us to estimate the room temperature time dependent V_{th}.

4.5 Threshold Voltage and PCS Resistance

Linear correlation can be found between the V_{th} and OFF-state resistance R_{OFF} in the four-terminal directly-heated RF PCS. This correlation could be attributed to the amorphous size being different for different R_{OFF}. Since it is commonly recognized that for the same PC material there exists a constant threshold field E_{th}, the V_{th} should be proportional to the amorphous size. However, R_{OFF} is known to drift to higher values over time, the mechanism of which is considered as the structural relaxation in the amorphous material [51]. The drifting effect will not change the amorphous size, but only the amorphous resistivity ρ_a. Thus in this section, experiments will be performed to confirm that the linear $V_{th} - R_{OFF}$ correlation is caused by different amorphous size and not the drifting effect.

For each RF PCS, the device was first RESET to OFF-state by pulsing the heater and the R_{OFF} was measured right after the RESET. I-V sweep method described in section 4.2 and Figure 4.1 was used to measure the V_{th} right after the R_{OFF} measurement. As shown in Figure 4.5(a), the red scattered data represents the $V_{th} - R_{OFF}$ correlation measured right after the RESET for each RF PCS. Although there is a big variation in V_{th}, a linear correlation between the V_{th} and R_{OFF} can still be identified. In another set of experiments, RF PCS devices were first RESET to OFF-state. Twenty-four hours later, R_{OFF} was measured for each device, following by the V_{th} I-V sweep measurements. The $V_{th} - R_{OFF}$ correlation measured 24 hours after the RESET is presented as blue scattered data shown in Figure 4.5(a). The slope of the correlation can be written as:

$$\frac{dV_{th}}{dR_{OFF}} = \frac{A_a E_{th}}{\rho_a} \tag{4.11}$$

where A_a is the cross-section area. By comparing the red data and blue data, it can be seen that the dV_{th}/dR_{OFF} right after RESET is 5 times higher than 24 hours after the RESET. On the other hand, shown in Figure 4.5(b), R_{OFF} measured 24 hours after RESET is plotted versus the R_{OFF} measured right after the RESET. The slope of 5 suggests that the resistivity ρ_a drifted up by 5 times over 24 hours. This consistency with the dV_{th}/dR_{OFF} ratio is an evidence that the threshold field E_{th} does not change significantly with the drifting effect. Thus, the V_{th} – R_{OFF} correlation can be mostly attributed to the amorphous size change. This observation ensures that the power handling performance will not drift with time significantly and introduce design complexity from a repeatability point of view.

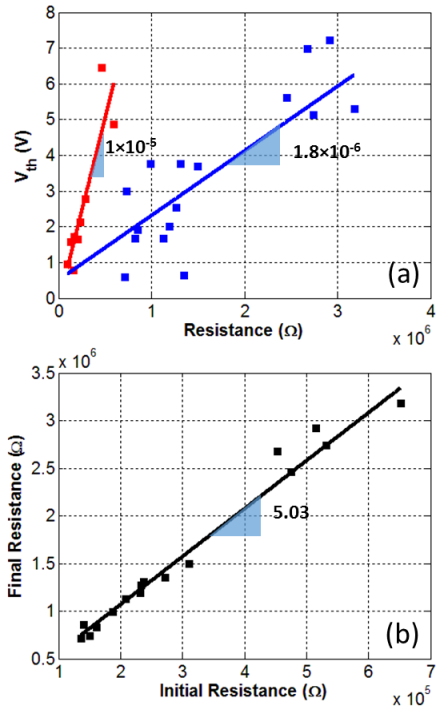

Figure 4.5 (a) V_{th} plotted versus R_{OFF} measured right after the RESET (red) and 24 hours after the RESET (blue) (b) correlation between R_{OFF} measured right after the RESET and 24 hours after the RESET

4.6 Variation of Threshold Voltage

The variation of V_{th} in PC material is a potential concern for high power handling PCS applications. Huge variations of V_{th} (e.g. 1.5 ± 1.3 V) for the same device has been observed for the four-terminal directly-heated RF PCS. This would not be acceptable in real applications since in the worst case of V_{th}, even small RF signals could accidentally break down the RF PCS. Understanding the variation is not only critical for improving the yield for high power handling RF PCS, but also can provide insights to the threshold switching mechanisms for the PC material. To start with, experiments will be presented to investigate the possible variation sources from the switching delay time and the amorphous size.

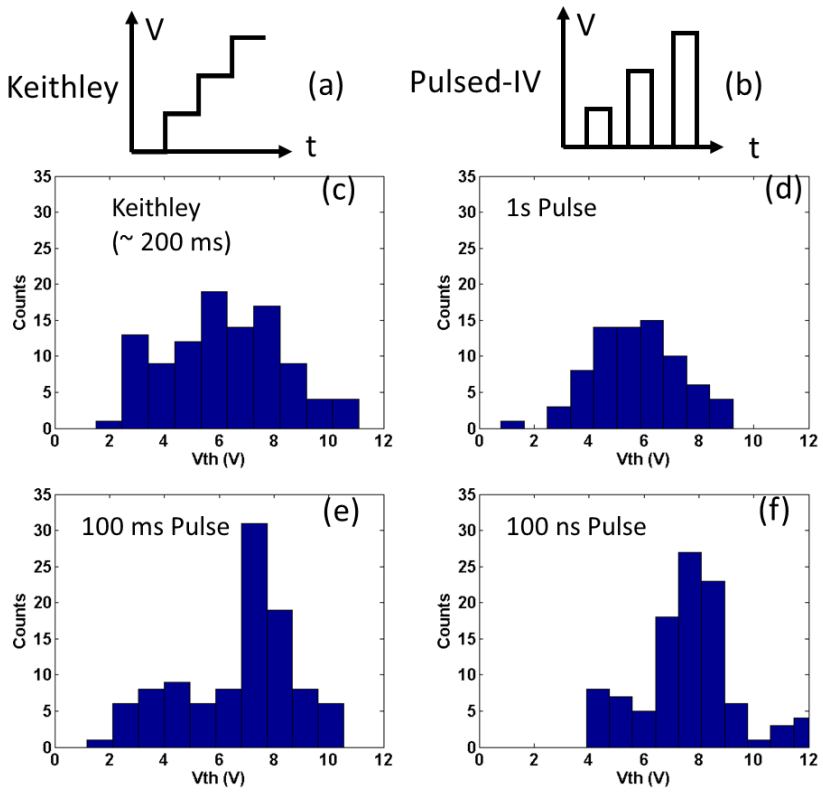

Figure 4.6 Applied voltage from (a) Keithley DC I-V sweeps and (b) pulsed I-V sweeps. Histograms of V_{th} measured by (c) DC I-V sweeps, (d) pulsed I-V sweeps with 1 s pulse width, (e) pulsed I-V sweeps with 100 ms pulse width and (f) pulsed I-V sweeps with 100 ns pulse width

Table 4.1 Measured V_{th} mean, standard deviation and coefficient of variation using different methods				
Methods	Keithley	1s pulse	100ms Pulse	100ns Pulse
Mean	6.24	5.69	6.73	7.59
Standard Deviation	2.21	1.63	2.08	1.76
Coefficient of Variation	0.35	0.28	0.31	0.23

As reported by [63]–[66], the variation increases with the threshold switching delay time. Since the Keithley source meter is used in our measurements, the delay time is in the order of 200 ms. Thus, pulsed I-V measurements described in section 4.2 can be applied to study the time dependency of the variation.

Figure 4.6 shows the comparison among histograms generated using both DC I-V measurements and pulsed I-V measurements with different pulse widths. Table 4.1 summarizes the mean, standard deviation and coefficient of variance for the V_{th} measured using different methods. It can be seen that the mean slightly increases when decreasing the pulse width, qualitatively consistent with (4.10). However, the coefficient of variance does not decrease with the pulse width, suggesting that the time dependency is not involved in the large variation.

The variation of V_{th} could also be caused by the variation of the amorphous size. However, the amorphous size is difficult to determine without having sophisticated TEM characterization of the FIB cross-section of the device. On the other hand, R_{OFF} is also proportional to the amorphous size. Since V_{th} is not dependent on ρ_a as discussed in the previous section, the correlation between variations of R_{OFF} and V_{th} can be investigated rather than the size.

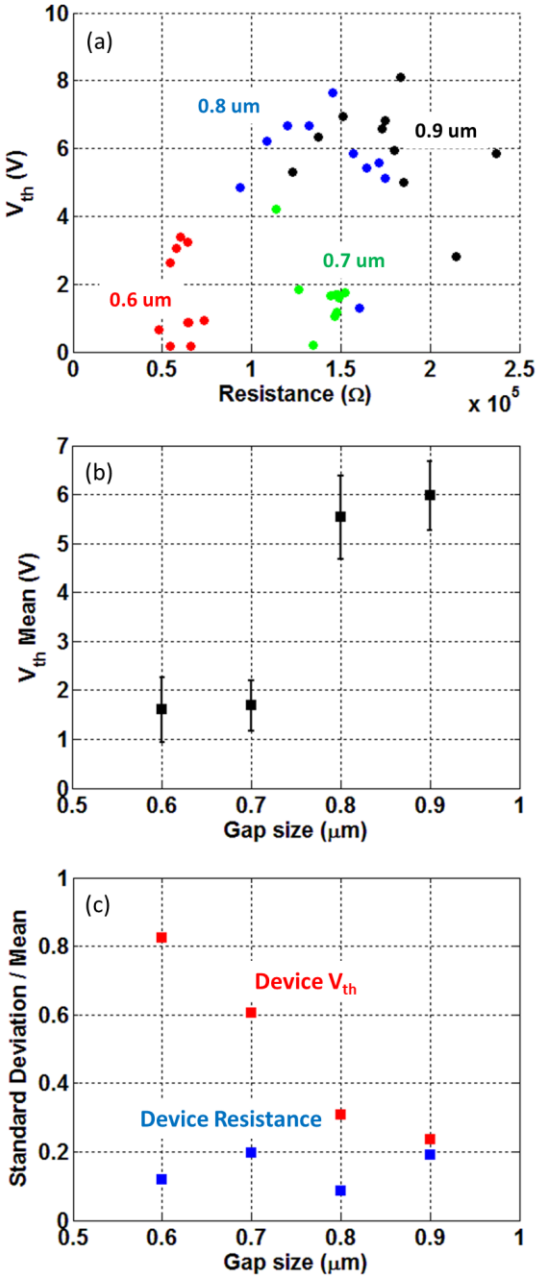

Figure 4.7 (a) V_{th} measured for RF PCS with different RF gap sizes plotted versus the OFF-state resistance of the devices (b) Mean V_{th} for the same device plotted versus the device RF gap size (c) standard deviation over mean for V_{th} (red) and OFF-state resistance (blue) versus the RF gap size

RF PCS with different RF gap sizes ranging from 600 nm to 900 nm were used in the V_{th} measurements. The V_{th} measurement was performed on the same device for multiple times to get the statistical behaviors. As shown in Figure 4.7(a), for each device, both the OFF-state resistance R_{OFF} and V_{th} have significant variation. In Figure 4.7(b), the mean V_{th} data are shown for each RF gap size and the larger RF gap size results in higher V_{th}. This can be explained by the thermal environment being different. In the PCS with larger RF gap, the gold electrodes which serve as another heat sink are farther away from the heater. As a result, a larger melted zone and larger PC amorphous size can be achieved in the PCS with larger RF gap.

Figure 4.7(c) shows coefficient of variation c_v (the ratio of standard deviation over mean) for both V_{th} (red color) and R_{OFF} (blue color). The c_v is used here since we are interested in the correlation between variations of R_{OFF} and V_{th} rather than the absolute standard deviations. For all four devices, the c_v are below 0.2 for the R_{OFF}, but can be as high as 0.8 for the V_{th}. The fact that c_v for V_{th} and R_{OFF} are not the same suggests the variation in V_{th} is not simply caused by varying amorphous size, but also the E_{th}. On the other hand, c_v for V_{th} decreases when increasing gap sizes (increasing amorphous size), which is the opposite of one would expect for constant E_{th}. Thus, variation of the material related property E_{th} must be investigated. However, due to the uncertainty of the amorphous resistivity, we cannot extract the amorphous size, and thus E_{th}, from R_{OFF} accurately. PC devices with known amorphous size are needed in this study.

4.7 Geometry Dependent Variation of Threshold Voltage and Field

To quantitatively investigate the E_{th} variation, a vertical structure with known amorphous size is designed and fabricated. As shown in Figure 4.8(a), as-deposited amorphous GeTe is sandwiched by bottom and top gold/tungsten electrodes (tungsten in contact with GeTe), sitting on top of silicon substrate. The heat sink of the device is good enough to eliminate any significant Joule heating and temperature rise inside the amorphous GeTe during the I-V sweep before the threshold switching occurs. The thickness of GeTe and area of top electrodes can be varied to study the geometry dependency. Note that these are single event

devices and cannot be RESET back after the switching because they lack a heater. For each geometry configuration, over 50 devices were used to perform V_{th} measurements. Figure 4.8(b) shows the correlation between V_{th} and R_{OFF} for devices with 300 nm thick GeTe. A higher relative variation for V_{th} is observed than for R_{OFF}. This is another strong evidence that the variation in V_{th} is from the E_{th} determined by the material property, rather than the geometry.

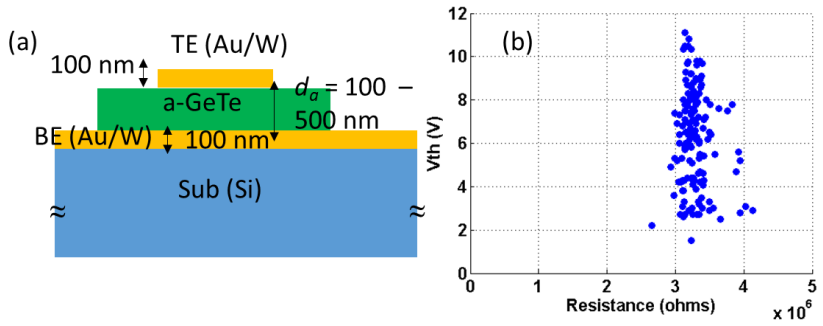

Figure 4.8 (a) cross-section schematic for the vertical structures (b) V_{th} versus R_{OFF} measured using 50 devices with the same geometry

Figure 4.9 shows the amorphous length dependent means and standard deviations for both V_{th} and E_{th}. As can be seen from Figure 4.9(a) and (b), the V_{th} mean increases with the amorphous length, d_a, while the E_{th} mean remains approximately the same for all d_a. This is consistent with the fact that E_{th} is a material dependent property. In Figure 4.9(c) no correlation between V_{th} standard deviation and d_a can be observed, while in Figure 4.9(d), E_{th} standard deviation shows a clear trend of decreasing with increasing d_a. This is also consistent with the RF PCS data shown in Figure 4.7(c).

On the other hand, neither V_{th} nor E_{th} is a strong function of area. Figure 4.10 shows the area dependency for V_{th} and E_{th} standard deviations. Strong area dependency for both V_{th} and E_{th} cannot be observed from this figure. This suggests that the threshold switching is not triggered by random defect in the amorphous material, where a positive feedback of the field enhancement on the defect eventually causes a runaway in the current. Since if that were the case, the E_{th} standard deviation should be strongly dependent

on the area and will decrease significantly with increasing area, and the E_{th} mean should also show the same trend.

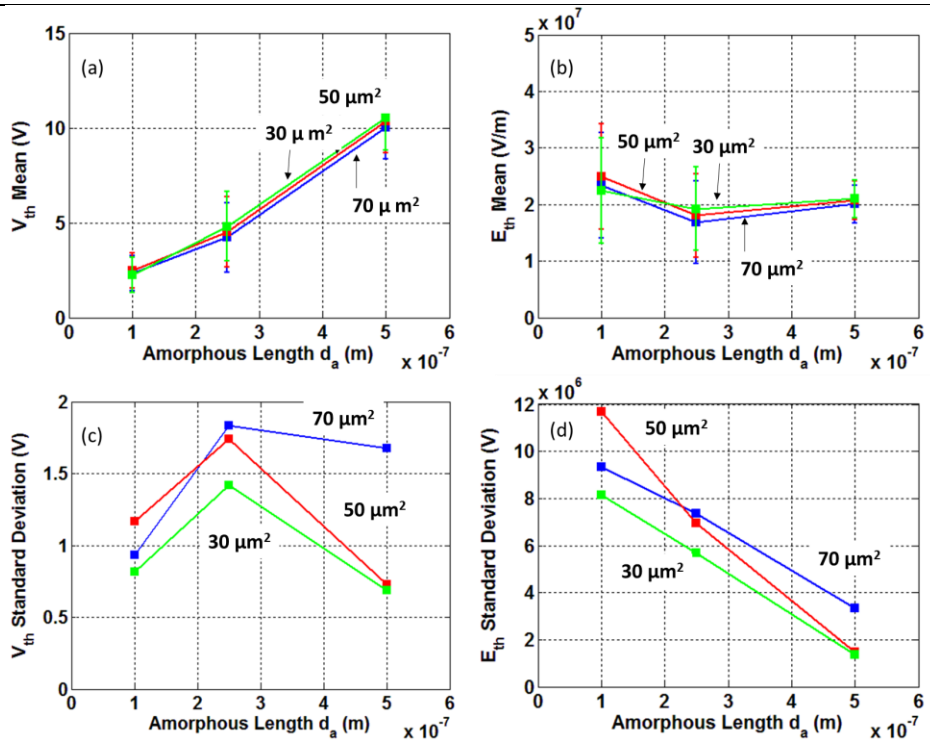

Figure 4.9 Means of (a) V_{th} and (b) E_{th} as a function of amorphous length d_a. Standard deviations of (c) V_{th} and (d) E_{th} as a function of d_a

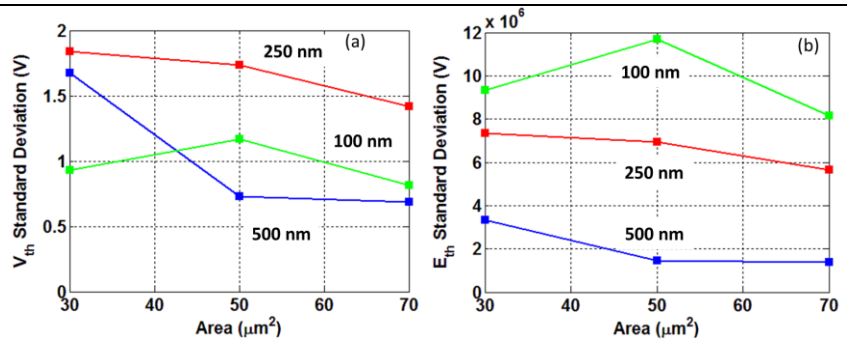

Figure 4.10 Standard deviations of (a) V_{th} and (b) E_{th} as a function of electrode area

The above experiments were performed on limited dimensions (d_a < 500 nm) and more data with a larger range of d_a and area are needed to support the above findings. Figure 4.11 shows two different lateral structures defined by optical and E-beam lithography processes. The amorphous length d_a ranges from 2 μm to 5 μm in the optical defined structure and from 500 nm to 2 μm in the E-beam defined structure. The cross-section areas are both estimated to be 100 nm^2, around 6 orders of magnitude smaller than the areas in the vertical structures.

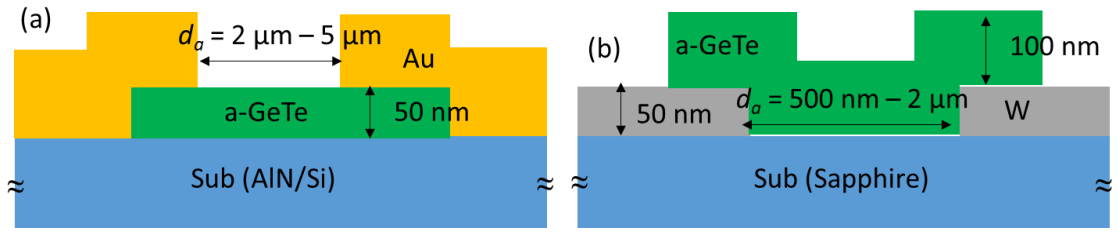

Figure 4.11 cross-section schematics for lateral amorphous structures defined by (a) optical lithography and (b) E-beam lithography

Figure 4.12 shows the combined plots for data collected from all three different structures. Blue represents the vertical structures with d_a ranging from 100 nm to 500 nm, black represents the lateral structures defined by E-beam with d_a ranging from 500 nm to 2 μm and red represents the lateral structures defined by optical lithography with d_a ranging 2 μm to 5 μm. As can be seen from Figure 4.12(a) and (b), the V_{th} mean linearly increases with d_a while E_{th} mean remains constant over the entire amorphous length range from 100 nm to 5 μm. The E_{th} is determined to be around 2.3 × 10^7 V/m, of the same order as values reported by [122] (5 × 10^7 V/m for GeTe), [123] (5.6 × 10^7 V/m for GST and 1.9 × 10^7 V/m for AIST). That E_{th} is constant in the entire range is also suggests that when the threshold switching occurs, the non-uniform electrical field distribution $E(x)$ (x is the direction across the length) is not significant for d_a > 100 nm. Although $E(x)$ may still be non-uniform locally, it must satisfy the following constraint:

$$\int_0^{d_a} E(x)dx\Big|_{th} = \overline{E_{th}}d_a \tag{4.12}$$

Thus, the more non-uniform the electric field is distributed, the more it deviates from the experimental constraint defined by (4.12). This argues against the theory that the sub-threshold non-linear conduction is caused by space charge limited conduction [124], which requires strong electrical field non-uniformity. The threshold switching model described in [56] also requires a region with strong non-uniform electrical field. But since in this work, the model is only investigated for d_a < 40 nm (with local field enhanced region size < 10 nm), it may still satisfy (4.12) due to the small dimensions.

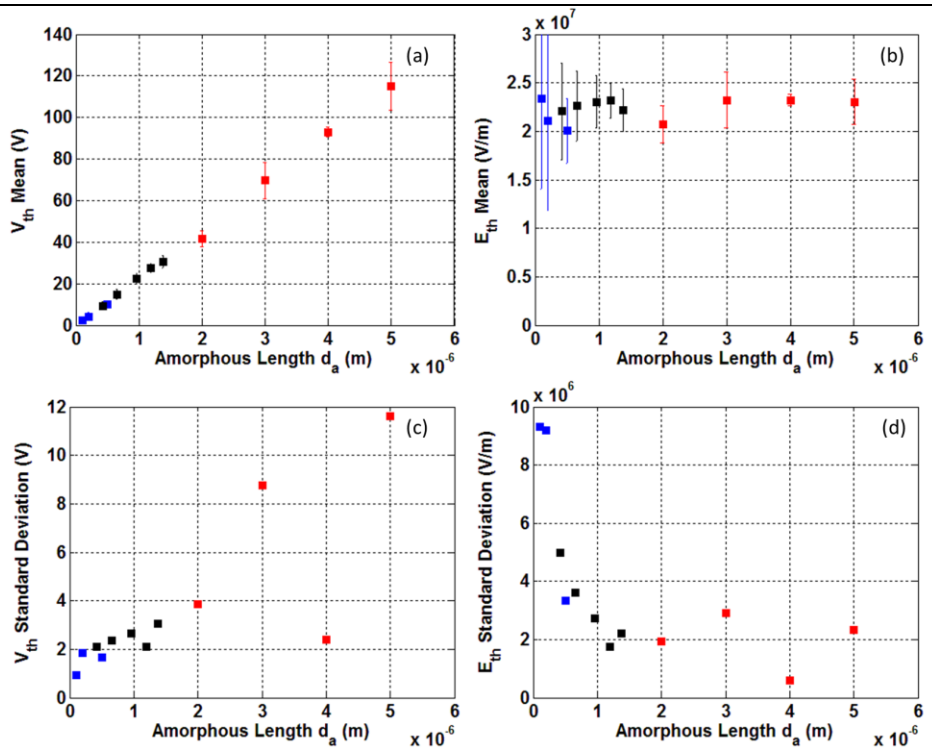

Figure 4.12 Means of (a) V_{th} and (b) E_{th} as a function of d_a. Standard deviations of (c) V_{th} and (d) E_{th} as a function of d_a. The data were measured using devices with all three different structures. Blue represents the vertical structures, black represents the lateral structures defined by E-beam and red represents the lateral structures defined by optical lithography.

Figure 4.12(c) and (d) shows the d_a dependency of standard deviations of V_{th} and E_{th}. Unlike Figure 4.9(c) where the correlation between V_{th} standard deviations and d_a is not obvious, Figure 4.12(c) shows that it still increases with d_a. On the other hand, Figure 4.12(d) shows that E_{th} drops when increasing d_a in a strong non-linear fashion. The reason why V_{th} and E_{th} standard deviation have opposite correlations with d_a can be attributed to the fact that the E_{th} standard deviation is "amplified" by d_a, according to:

$$\sigma_{V_{th}} = d_a \sigma_{E_{th}} \tag{4.13}$$

The fact that V_{th} and E_{th} standard deviation data for structures with very different cross-section areas (6 orders of magnitude difference) fall in the same trend is another strong evidence in support to Figure 4.10 that the variation is not area dependent and threshold switching is not triggered by random defect.

By plotting the standard deviations of V_{th} and E_{th} versus d_a in log-log scale, we can generate Figure 4.13. By inspecting the slopes we can see that:

$$\sigma_{V_{th}} \propto d_a^{\,0.48} \approx \sqrt{d_a} \tag{4.14}$$

$$\sigma_{E_{th}} \propto d_a^{\,-0.52} \approx \frac{1}{\sqrt{d_a}} \tag{4.15}$$

This behavior can be modelled by a Poisson process, where the total amorphous length can be divided up into characteristic lengths associated with fluctuations, the physical origins of which remain unclear.

Although the mechanism is yet to be explained and reconciled with existing theories, this simple model can be used to estimate the threshold voltage variations for given amorphous size.

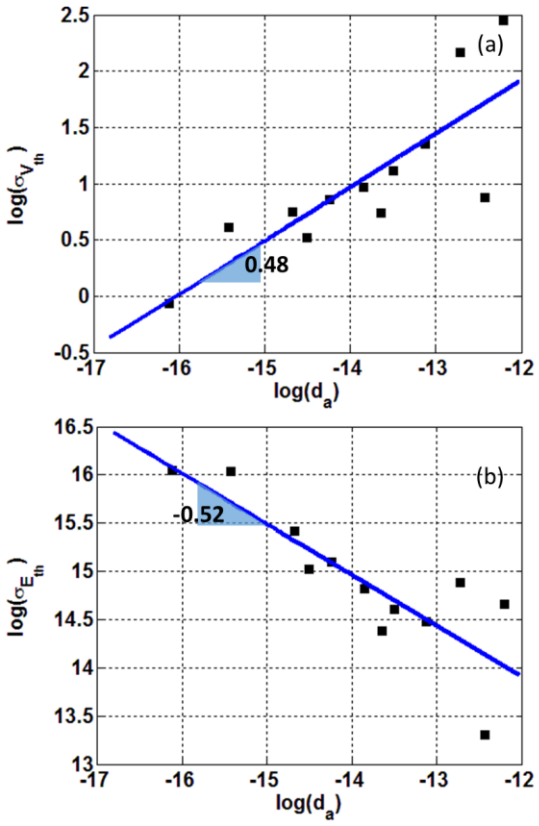

Figure 4.13 log-log plots of (a) V_{th} standard deviation versus d_a and E_{th} standard deviation versus d_a

4.8 RF Switch Matrix

Figure 4.14 shows three different architectures of the PC switch for improving the power handling capability. The single PC switch has reference performance metrics V_{th}, C_{OFF} and R_{ON}. By making two switches in series, one can sacrifice R_{ON} to improve C_{OFF} and V_{th}, while the overall cutoff frequency is unchanged. However, it is generally required that the R_{ON} to be as small as possible to reduce the noise figure. By making a 2x2 switch matrix, one can double the V_{th} without affecting C_{OFF}, R_{ON} and thus the cutoff frequency. This will result in larger area, but can still be a good trade-off to improve the power handling.

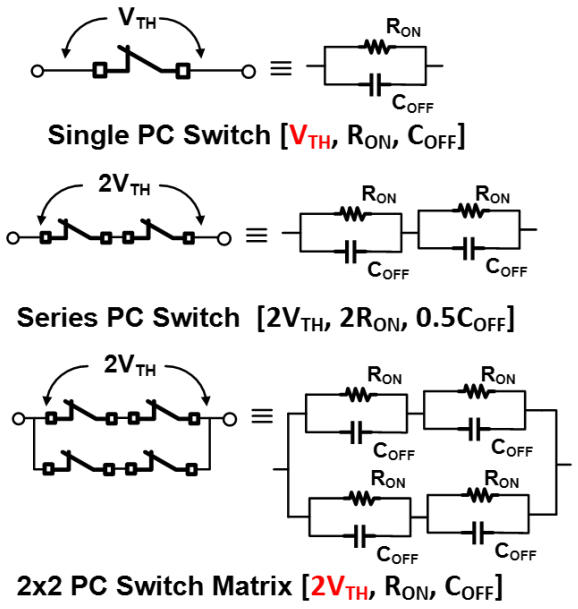

Figure 4.14 Architectures of single PC switch, series PC switch and 2x2 PC switch matrix

However, the distributions of V_{th} scale differently for the single switch and the switch matrix. For the single switch with amorphous length l_a, the standard deviation of E_{th} can be expressed as σ_s. For the single switch with doubled amorphous length 2 l_a, the E_{th} standard deviation is thus 0.707 σ_s based on its scaling property, which results in a V_{th} standard deviation of 1.414 σ_s. For a 2x2 switch matrix, the E_{th} standard deviation is a convoluation of the standard deviations of two switches, result in a lumped standard deviation of 1.414 σ_s. Thus, for a 2x2 switch matrix, the V_{th} standard deviation of 2 σ_s.

Based on the above example, the design considerations can be summarized as follow. For the same amorphous length per single PC switch, a 2x2 switch matrix (or larger matrices) can be used to improve the power handling by increasing the V_{th} while sacrificing the area, allowing the C_{OFF}, R_{ON} and thus the cutoff frequency to remain the same. However, a single PC switch with the same C_{OFF}, R_{ON} and doubled amorphous length (or E_{th}) is more desirable due to the smaller V_{th} variation comparing to the switch matrix.

4.9 Summary

In this chapter, we firstly introduced measurement techniques for V_{th}, the general DC I-V sweep measurement and the pulsed I-V measurement for time dependent V_{th}. Next, based on analysis on the I-V characteristics of GeTe-based device, NDR was identified as not the triggering event for the threshold switching. Time dependent V_{th} was also investigated and the nucleation switching model was applied to explain the time dependency and as an alternative to the NDR model. Although the attempt to extract the material related characteristic electric field failed due to the inconsistency between the model and the data extrapolation, the experimental results are still valuable for estimating V_{th} time dependency at the room temperature. We also identified that the R_{OFF} drifting event did not significantly affect the V_{th}.

The second half of this chapter focused on the observations on the V_{th} variations. Sanity checks were performed to eliminate possible sources of the variations, such as resistance drifting, amorphous length variations and time dependent variations. The variation of E_{th}, which is determined by the material property, was assessed to be the source. Geometry dependency of V_{th} and E_{th} were then investigated by measuring V_{th} on PC devices with different structures. The independency of E_{th} variation on area suggests that the threshold switching is not triggered by positive feedback of field enhancement in random defect spots in the amorphous PC material. The fact that E_{th} mean remains the same from 100 nm to 5 μm argues against the theories (e.g. space charge limited conduction) require the field to be distributed non-uniformly across the entire amorphous length region. Finally, the V_{th} is observed to be proportional while the E_{th} is inversely proportional to the square root of d_a. This behavior follows a Poisson process, suggesting that the E_{th} variation origins from the fluctuations per unit amorphous length. The physical origins remain to be understood in the future work.

Note that we still lack a unfied model to quantitatively explain all the observations in the V_{th}. Table 4.2 summarizes the comparisons between existing models and the expiermental observations discussed in this chapter. The table shows both the consistency and discrepancy between the possible models responsible for certain mechanism and the empirical observations.

The scaling properties of V_{th} and E_{th} distributions are not summarized in this table, due to the lack of possible models to explain the phenomena. Altough we need further investigation of the correlation between the Poisson process and possible mechanisms, we can still utilize the scaling properties to predict RF switch performance and guide the switch geometry design (e.g. making design considerations for switch archiectures and switch matrix).

Table 4.2 Comparison between existing models and empirical observations			
Model	Observation	Consistency	Reference
High field energy gain in electron hopping	E_{th} is constant over the range from 100 nm to 5 μm, V_{th} is almost linear with amorphous length	Consistent with the fact that E_{th} is material related while V_{th} is not. Although this model requires non-uniform field distribution over less than 40 nm amorphous length, we lack data with amorphous length in that range to identify the consistency with this model	[56], [58]
	Standard deviations of E_{th} do not show strong area dependency	The model suggests local structural distortion and defects leads to the initiation of hopping process, which implies strong area dependency of E_{th} distribution	
Impact ionization	E_{th} is constant over the range from 100 nm to 5 μm, V_{th} is almost linear with amorphous length	Consistent with the fact that E_{th} is material related while V_{th} is not. Simple impact ionization model does not require non-uniform field distribution	[59], [61]
	NDR event is not present in GeTe	NDR is required in the simple impact ionization model, but not observed for GeTe	
Nucleation switching model	The log of switching time is proportional to E_{th}^{-1}	Qualitatively the same as described by the model, but the temperature dependency of the extracted slope is much stronger in the observation	[63], [65], [66]
	E_{th} is constant over the range from 100 nm to 5 μm, V_{th} is almost linear with amorphous length	Consistent with the fact that E_{th} is material related while V_{th} is not. Electric field can be linear before the nuclei is initiated	
Space Charge Limited Conduction (SCLC)	E_{th} is constant over the range from 100 nm to 5 μm, V_{th} is almost linear with amorphous length	SCLC requires strong non-uniform distribution of the electric field, which is not consistent with the observation	[125]

Chapter 5: Design and Process of the 2nd Generation High Speed Phase Change Test Device for High Temperature Crystallization Study

5.1 Abstract

In this chapter, a new design of a nano-scale high speed PC test device (referred as the 2nd gen device in the following context) is proposed to be used in studying crystallization dynamics at high temperature high speed regime, as it is critical for improving write speed for non-voltaile memory applications. Due to the micro-scale dimensions, the 1st gen device is too slow in thermal response to be used for identifying high speed crystallization process. The 2nd gen device has fast thermal response and can be used to perform crystallization time measurement in high T (> 700 K) and high speed (< 10 ns) regime. A brief introduction on the rationale of making this device will be presented. Then, the detailed design and fabrication process of the 2nd gen device will be discussed.

5.2 Introduction

As one of the candidates for unified memory technologies, PC materials are desired to have fast write and read speed. For the RESET write operation, since it is a melt-quench process that does not set a lower bound for the quench time, the speed limitation comes from the device thermal time constant and the driving circuits instead of the material itself. On the other hand, the crystallization is a thermally activated process which is limited by the material crystallization dynamic properties. Thus, the crystallization rate of chalcogenides determines the write speed in the SET operation (typically slower than the RESET operation). As can be seen from the TTT diagram in Figure 1.1, minimum crystallization time $t_{x,min}$ can be defined as the minimum time it takes to transform the PC material from amorphous state to crystalline state at the temperature $T_{x,min}$. Unlike in RF switch applications where we want to maximize the maximum

allowed quench time (CQT) in order to minimize power consumption (equivalent to maximizing $t_{x,min}$), we target for minimizing $t_{x,min}$ for memory applications, as it determines the slowest write speed in the system. According to measurements in Chapter 3, the crystallization time shows Arrhenius behavior at low temperatures (< 600 K), where the time is described by the equation:

$$\tau_x = \tau_{x0} \exp(-\frac{E_x}{k_B T}) \tag{5.1}$$

If the PC material could follow (5.1) with E_x of 2 eV and τ_{x0} of 2.4×10^{-24} s (although a more universal number of 1.2×10^{27} s^{-1} for the attempt frequency per atom can be calculated based on the amorphous length and atomic distance assuming a growth-dominated process, more will be discussed in Chapter 7), τ_x should have been much shorter (10 – 100 fs) than what has been observed (10 - 100 ns). However, τ_x is known to show non-Arrhenius behavior (E_x being different at different temperature regimes), that the pre-exponential factor τ_{x0} becomes orders of magnitude higher while E_x decreases from higher than 2 eV to below 0.5 eV with increasing T.

As discussed in Chapter 1, it is likely that the different mechanisms are likely to be controlling the crystallization in different temperature regimes, and this accounts for the change in effective activation energy for crystallization, shown in Figure 5.1(a). At high temperature (and high speed), crystallization appears to be controlled by the concentration of free volume in the amorphous state, as described by the fragility model and showing a lower activation energy, shown as the blue curve in Figure 5.1(a). At low temperature, the controlling mechanism appears to be independent of free volume and shows a much higher activation energy, shown as the red curve in Figure 5.1(a). Notably, this cross-over in mechanisms requires also that the pre-exponential factor in each of the relevant Arrhenius relationships be strongly temperature dependent. The pre-exponential factor of the red curve is required to increase dramatically such that this modality is not dominating at high T. This can be explained by the temperature dependent entropic multiplication factor as mentioned in Chapter 1.

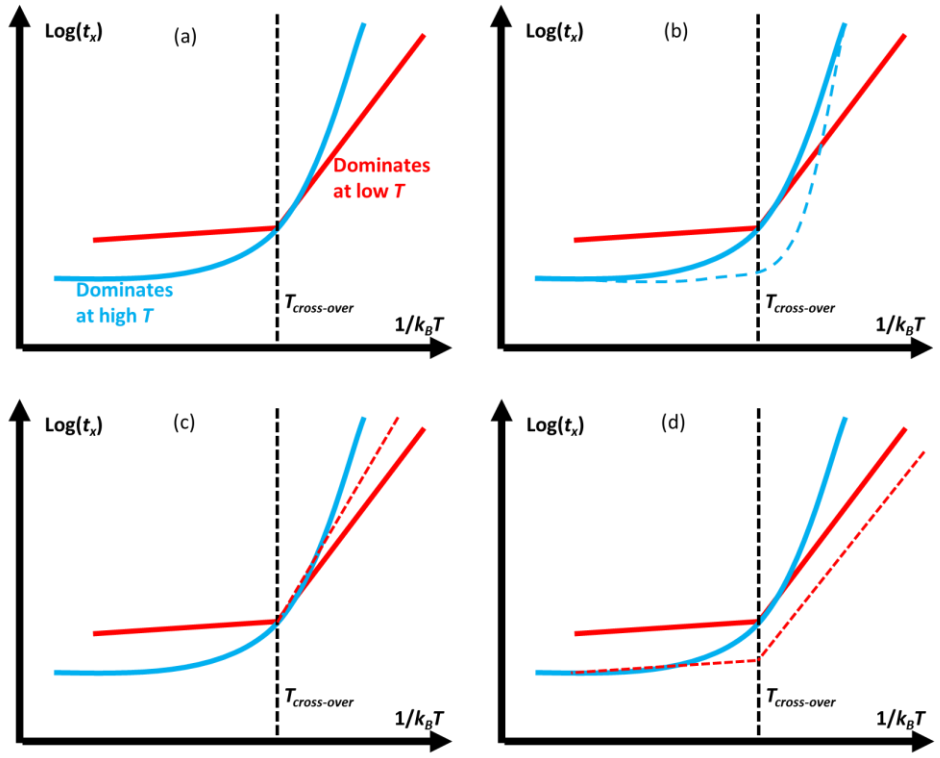

Figure 5.1 Arrhenius plot schematics for two different mechanisms controlling the crystallization at different regimes. The blue curve represents the one controlled by the free volume described by the fragility model, while the red curve represents the one independent of the free volume. Dashed curves represent the manipulations of the crystallization process to achieve either higher speed or better data retention

Given the applicability of the fragility model at high T, improving crystallization speed at high T, requires that E_x needs to be lower as the τ_{x0} is fixed at the attempt frequency of atomic vibration, which is failry unchangeable. As shown in Figure 5.1(b), the blue dashed curve shows the crystallization dynamics after this manipulation to achieve higher speed. On the other hand, if a separate crystallization modality consistent with the experimentally observed Arrhenius behavior in the low T regime exists, the retention can be improved by increasing the E_x of this modality, shown as the red dashed curve in Figure 5.1(c).

Additionally, it may also be possible to manipulate the pre-exponential factor, since its unphysically small value indicates that the entropic multiplication factor is in play and might be adjusted through doping, shown as the red dashed curve in Figure 5.1(d). Note that this will however sacrifice the data retention at low *T*. More will be said about those possible directions later in Chapter 7 and Chapter 8.

Although these models provide useful insights, it is necessary to firstly quantify the crystallization dynamics of chalcogenides in the high *T* sub-10 ns regime. It has been shown in Chapter 3 that crystallization time can be evaluated using the same test vehicle and methodology for CQT study, but due to the slow thermal response of the 1st gen device (thermal time constant ~ 40 ns), it is not possible to use it to identify sub-10 ns crystallization dynamics. Also, the isothermal assumption does not hold in the high *T* regime. The non-Arrhenius behavior reported in Chapter 3 can be caused by both the artifact of slow device thermal response and the PC material crystallization dynamic properties at high *T*. Additional analysis is needed to covert the transient temperature to the effective isothermal temperature and produce the isothermal Arrhenius plot. More on this analysis will be detailedly discussed in Chapter 7. As a result, the 2nd gen device with ultra-fast thermal response is needed. This chapter will focus on how to design and fabricate the 2nd gen device to be used for measurements in high *T* (> 700 K) and high speed (< 10 ns) regime.

5.3 The 2nd Generation Device Design

To design the device with much faster thermal response than the previously studied 1st gen device in Chapter 3, two structural changes were made. The first one is re-designing the heater dimensions into the nano-scale, so that the heat capacitance is reduced and as well as the thermal time constant. The second one is changing the PC layer from the in-directly heated lateral structure to the directly heated vertical structure. By removing the AlN layer, the PC layer is directly in contact with the heater, making the thermal resistance and thermal capacitance between the heater and the PC layer much smaller.

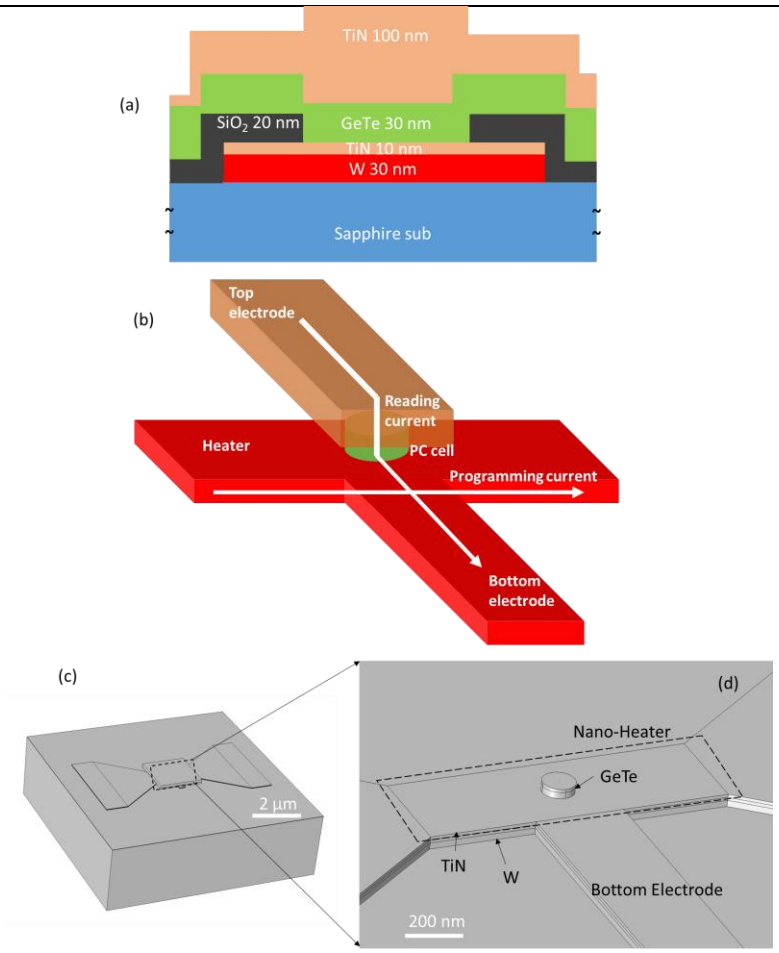

Figure 5.2 (a) cross-section and (b) 3-D perspective schematic of the 2nd gen device. (c) 3-D perspective schematic of the device structure modeled in COMSOL and (d) zoomed-in device perspective schematic with the top electrode (TiN layer) being hidden.

Figure 5.2(a) and (b) shows the cross-section and 3-D perspective of the the 2nd gen device, respectively. As can be seen, the W heater is designed to be 30 nm thick, 1 µm in length and 300 nm in width. The 10 nm TiN layer on top of the heater serves as an etch stop layer, which will be explained in the next section. A 20 nm SiO_2 layer is used to provide electrical isolation on top of the heater. A 100 nm diameter via is opened through the SiO_2 layer, so that the PC layer can be in direct contact with the heater. The third terminal in the center of the heater is designed as the bottom electrode of the PC layer. The 100 nm

thick TiN serves as the top electrode, which is in contact with the PC layer, but electrically separated from the bottom electrode and the heater.

By applying pulse between the two terminals of the heater, Joule heat can be generated to transform the PC layer sitting on top of the heater. By sending current through the top electrode to the bottom electrode, one can sense the resistance change of the PC layer after transformations. Figure 5.2(c) and (d) shows the 3-D model built in COMSOL for simulating the thermal response of the device for given electrical inputs.

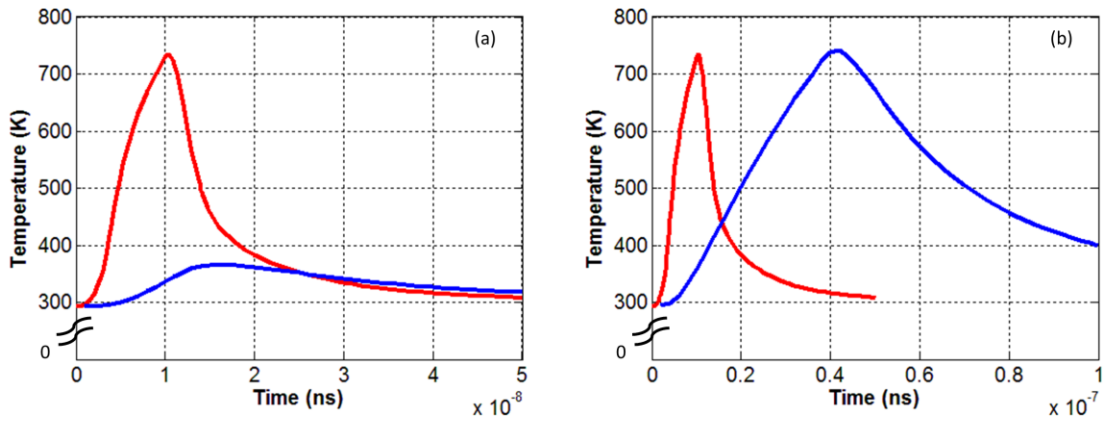

Figure 5.3 Comparison of the spatial average temperature transients in the PC layer generated by the heaters of the the 1st gen device (described in Chapter 3, blue curve) and the the 2nd gen device (red curve), (a) for the same heater pulse (3.4 V 10 ns) and (b) for the same heater voltage (3.4 V) to reach the same peak temperature

As can be seen in Figure 5.3(a), by sending 3.4 V 10 ns to the heater, the 1st gen device described in Chapter 3 can only heat the PC up to 370 K, while the 2nd gen device can heat the PC up to 730 K. Another simulation shows that the 2nd gen device can heat the PC above melting temperature with a thermal time constant of 5 ns, while the 1st gen device has a thermal time constant of 40 ns. Another comparsion in Figure 5.3(b) shows that for the same voltage of 3.4 V, it requires a pulse that is 4 times longer for the 1st

gen device to reach the same peak temperature. Using 3.6 V 5 ns pulse with rise and fall time of 2 ns, the 2nd gen device can heat the PC to the temperature of interest (700 K) within 10 ns with a heating rate of 4×10^{10} K/s, which is 8 times faster than the 1st gen device. While the 1st gen device can also achieve the same heating rate by sending the same narrow pulse (5 ns with 2 ns rise and fall time) with higher voltage, the cooling time constant is too long (40 ns) for the temperature transients to be used in identifying crystallization events in sub-10 nanosecond regime. The heating rate can potentially be higher than 10^{11} K/s at higher pulse voltage. Thus, the proposed design enables the 2nd gen device to measure crystallization dynamics of the PC within 10 ns.

5.4 Standard E-beam process

The fabrication process of the 2nd gen device consists of two optical lithography steps and three E-beam lithography steps. The optical lithography process using MA6 enables a minimum pattern size of 1 μm. However, for sub-micron lithography, the E-beam lithography process is required. FEI 600 SEM E-beam writing system in CMU Nanofab allows feature size to be as small as 50 nm, sufficient for the current design with a minimum feature size of 100 nm. In this section, standard E-beam lithography process will be discussed.

Before each E-beam step, PMMA A4 E-beam resist was spun onto the surface of the sample. The spin rate is 1000 rpm and the spin time is 60 seconds. Following this step, the sample was put on the 180 ºC hot plate for 2 minutes to soft bake the PMMA resist. This process will result in a 400 nm thick PMMA resist layer on top of the wafer. After this step, 20 nm aluminum was sputtered onto the wafer, on top of the PMMA, using the AJA system or the CVC system. This thin conduction layer of aluminum allows the sample topography, especially the alignment marks, to be recognized by the E-beam system. Excluding this step will result in significant charging effect during the E-beam imaging process. Aluminum is chosen because it is easy to be removed using AZ400K developer after the E-beam writing process, and the AZ400K developer will not attack the PMMA resist or affect the patterns at any circumstances.

During the E-beam writing, the exposure area dose is designed to be 400 $\mu C/cm^2$, with a writing resolution (beam center-to-center distance) of 1.72 nm. This recipe is calibrated corresponding to the 400 nm thick PMMA resist, and is used for all three E-beam steps in this process.

After the E-beam writing, the sample was firstly soaked in AZ400K developer for 1 minute to remove the aluminum. Then it was soaked in the PMMA developer solution with 1 part of MIBK and 3 part of IPA for 1 minute. The sample was then soaked in IPA for another 30 seconds for cleaning.

5.5 Nanoscale Heater Process

Shown in Figure 5.4, a 30 nm layer of high temperature deposited tungsten (HT W) was sputtered onto a C-plane sapphire substrate at elevated temperature (850 ºC) at base pressure smaller than 5×10^{-8} Torr. Tungsten sputtered at low base pressure and elevated temperature shows better resistivity and reliability.

Shown in Figure 5.4(a), this mask layer is used for patterning the bottom electrode for the PC, heater pads and E-beam alignment marks. It is required that the alignment marks show enough contrast during the E-beam imaging and can be recognized by the E-beam system, with the presence of the aluminum conduction layer on top of the PMMA. The contrast is determined by the amount of secondary electrons scattered from the alignment marks surface. As a result, the contrast is affected by the thickness and the materials of the alignment marks.

One approach is to sputter a stack of two metal layers, with TiN followed by aluminum. Aluminum and TiN were chosen because they could serve as etch stop materials for etching tungsten in the fluorine based RIE system. However, as shown in Figure 5.4(b), the alignment marks did not provide enough contrast for good alignment even with 100 nm thick TiN layer. This could be due to the limited secondary electrons scattered from TiN as comparing to the aluminum conduction layer.

Alternatively, tungsten can be used as the alignment mark materials. As shown in Figure 5.4(c), with 30 nm tungsten deposited at room temperature (RT W) as the bottom material for the alignment marks,

the contrast was improved by a lot and it is easy for the E-beam system to recognize the marks during the alignment process. However, this approach will not work on top of the HT W as the alignment mark metal stack is required to sit directly on top of the sapphire substrate. As a result, this step is decomposed into two optical lithography steps.

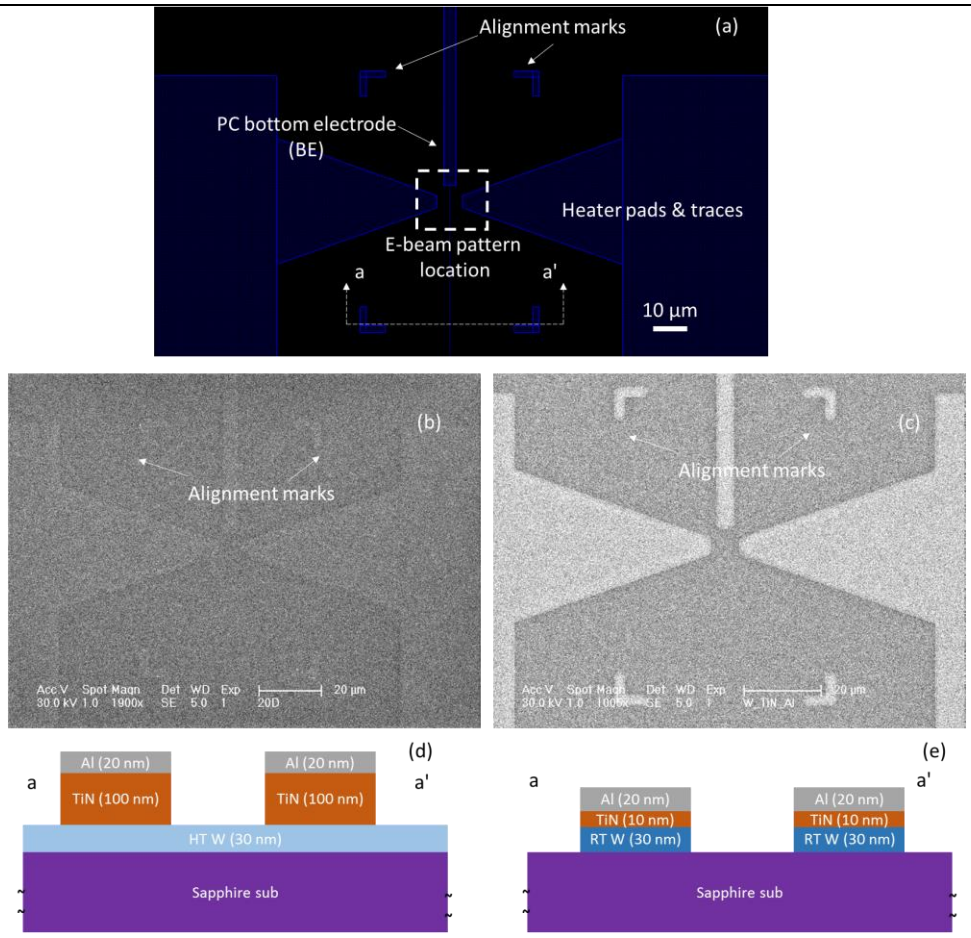

Figure 5.4 (a) layout of the optical mask layer for heater pads and traces and E-beam alignment marks. (b) SEM image of lifted-off alignment marks (20 nm Al and 100 nm TiN) on top of HT W thin film. (c) SEM image of lifted-off alignment marks (20 nm Al and 10 nm TiN and 30 nm RT W) on top of sapphire substrate. (d) cross-section schematic of (b). (e) cross-section schematic of (c).

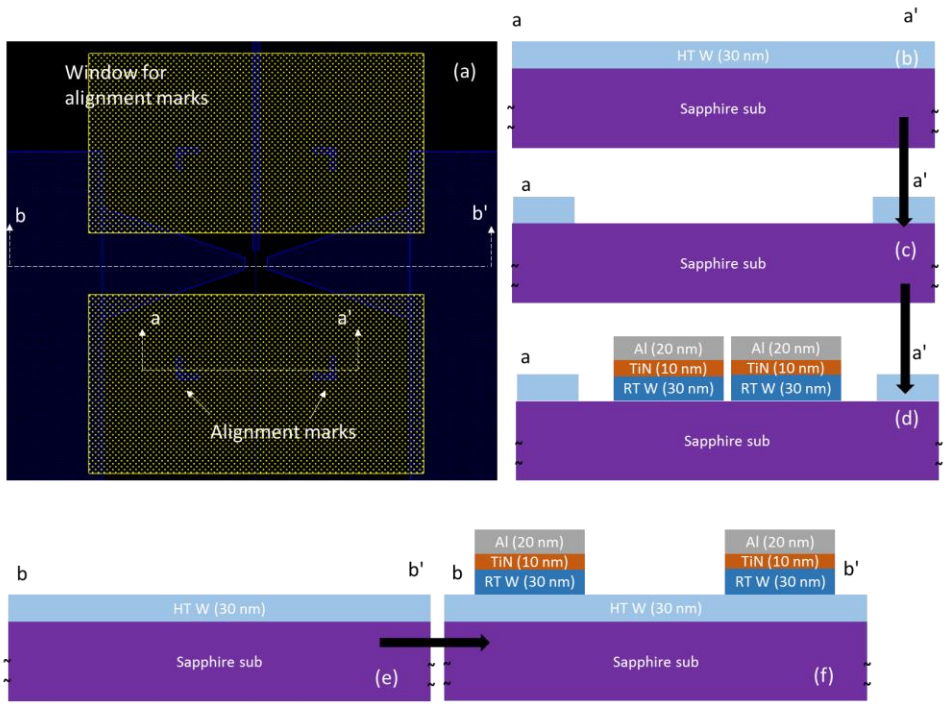

Figure 5.5 (a) the layout of the first optical mask layer for openning window through high quality tungsten (yellow dotted area) and the second optical mask layer for heater pads, traces and alignment marks. (b)-(d) and (e)-(f) show the process flow from two cross-section views of openning window through high quality tungsten, depositing and patterning alignment marks by lift-off

As shown in Figure 5.5(a), the first mask layer (boxes with yellow dots) is used for opening windows through the HT W layer to allow the alignment mark metal stack to sit directly on top of sapphire substrate. The sample was etched for 2.5 minutes in the PlasmaTherm system using the standard RIE recipe for etching tungsten. The second mask layer (solid pattern in dark blue) is used for alignment marks, heater traces and PC bottom electrode patterning. Both mask layers were processed using standard optical lithography with AZ4110 resist. All three metal layers were sputtered using AJA system, at 60 sccm Ar flow rate and 3 mTorr at room temperature. The RT W (30 nm) was sputtered at 50 W DC power for 780 seconds. TiN (10 nm) was sputtered at 200 W DC power for 350 seconds. Aluminum (20 nm) was sputtered at 100 W RF power for 530 seconds. Figure 5.5(b)-(d) show the process cross-section schematics of

alignment marks sitting on top of sapphire inside the window through the HT W. Figure 5.5(e)-(f) show the cross-section schematics of heater traces on top of high quality tungsten.

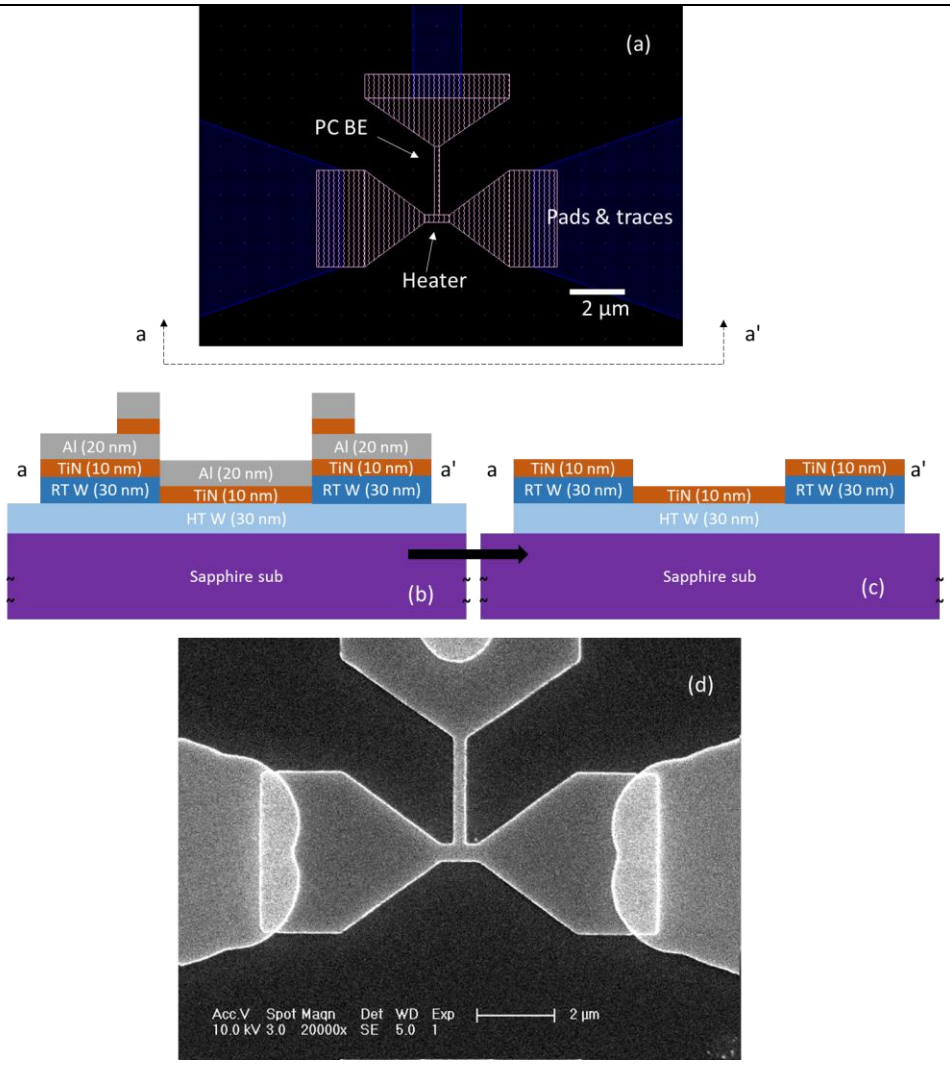

Figure 5.6 (a) layout of the first E-beam layer for patterning nano-scale heater (pink pattern) on top of the second optical layer (blue pattern). (b)-(c) process flow of patterning the HT W into the heater from cross-section view a-a'. (d) SEM image of the patterned nano-scale heater

After the first two optical lithography steps, a standard E-beam lithography step was used for patterning nano-scale heater structure (shown as the pink pattern in the center of Figure 5.6(a)). In this

structure, the heater is located horizontally. The third terminal metal line in the center of the heater is used as bottom electrode access to the PC layer. After the PMMA resist development, another 10 nm TiN and 20 nm aluminum was sputtered using the previously described recipes. It should be noted that no low quality tungsten was sputtered so there is only high quality tungsten in the region where most of the power is generated during the device operation to provide the best reliability.

After the lift-off step using acetone and ultra-sonication, the high quality tungsten was then etched in the PlasmaTherm fluorine based RIE system for 2.5 minutes using the standard RIE recipe. The aluminum was etched off using AZ400K developer. The final cross-section cartoon of this step is shown in Figure 5.6(c), where the entire pattern is covered by 10 nm TiN, which will be used as the second etch stop in the next process. Figure 5.6(d) shows the final SEM image of the heater structure.

5.6 E-beam Via and PC Layer Process

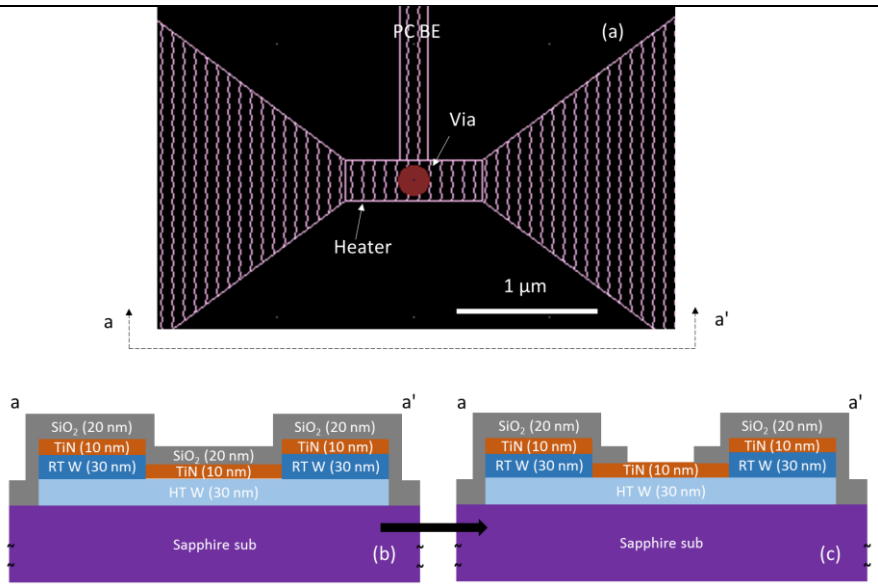

Figure 5.7 (a) layout of the second E-beam layer for via through oxide (red circle pattern in the center) on top of the first E-beam layer (pink pattern). (b)-(c) process flow of depositing SiO_2 and etch the via through SiO_2 from the cross-section view of a-a'.

After the heater had been fabricated, SiO_2 was sputtered using the AJA system for electrically isolating the heater and the top electrode. As shown in Figure 5.7, a second standard E-beam process is used for patterning the via through the SiO_2, allowing the PC layer to contact with the heater (bottom electrode).

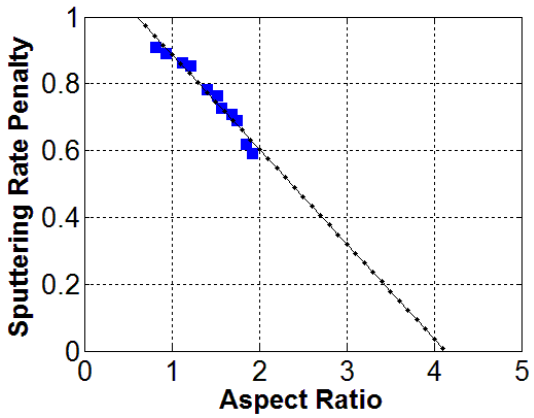

Figure 5.8 Sputtering rate penalty for the AJA sputtering system as a function of pattern aspect ratio. Blue scattered data were measured from calibration patterns, black dotted line is the fitting curve.

The thickness of SiO_2 is carefully designed based on the via size (100 nm diameter in this case) and the side-wall coverage. A SiO_2 layer that is too thin could provide poor side-wall coverage and fail to provide electrical isolation between the heater and the top electrode, while a layer that is too thick could lead to high sputtering rate penalty inside the via. The sputtering rate penalty (the reduction of sputtering rate comparing to the rate in large pattern with feature size > 1 μm using optical lithography) is a function of the aspect ratio of the via (the ratio of the via diameter and the via thickness). Figure 5.8 shows the sputtering rate penalty as a function of the pattern aspect ratio. The blue data were measured through a calibration process where small PMMA patterns with different aspect ratios were defined by E-beam, followed by sputtering PC materials using the AJA system and lift-off. The aspect ratios were calculated from the PMMA thicknesses and pattern diameters, the sputtering penlty were calculated based on the PC thicknesses measured after the lift-off. The black dotted line is the fitting curve. If the aspect ratio is larger

than 4.1, there is no penalty in sputtering rate. Note that this calibration study is specific to the target gun configurations (angle and distance to the sample) for the AJA sputtering system. Based on this calibration study, the thickness of SiO_2 is chosen to be 20 nm, which provides minimum sputtering rate penalty and good side-wall coverage.

After the PMMA resist development for the second E-beam step, the SiO_2 was etched using the PlasmaTherm system. The power was set to be 30 W, at 15 mT pressure with 15 sccm of CHF_3 and 5 sccm of CF_4. The etch rate for SiO_2 using this recipe was measured to be 5.3 nm per minute, while the etch rate for TiN was 1.5 nm per minute, showing good selectivity between the etched and etch stop materials. The sample was etched for 7 minutes and 33 seconds using this recipe, taking into account a 100% over-etch to ensure the SiO_2 layer was completely etched through. Figure 5.9 shows an AFM scan image of the device structure after the SiO_2 etch step.

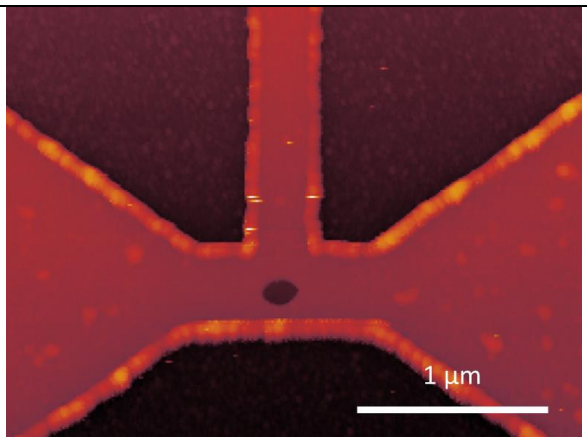

Figure 5.9 AFM scan image of the device after patterning the via through the SiO_2

The next step is the third E-beam lithography step for patterning the PC layer together with the top electrode. As shown in Figure 5.10, this layer is 2 µm wide (vertically located in Figure 5.10(a)), with 30 nm of PC material (GeTe) and 120 nm of TiN. TiN was chosen as the top electrode material due to its low thermal conductivity, which provides better thermal isolation and less temperature gradient inside the

PC layer. The PC layer is directly in contact with the heater (the bottom electrode) inside the via through the SiO_2.

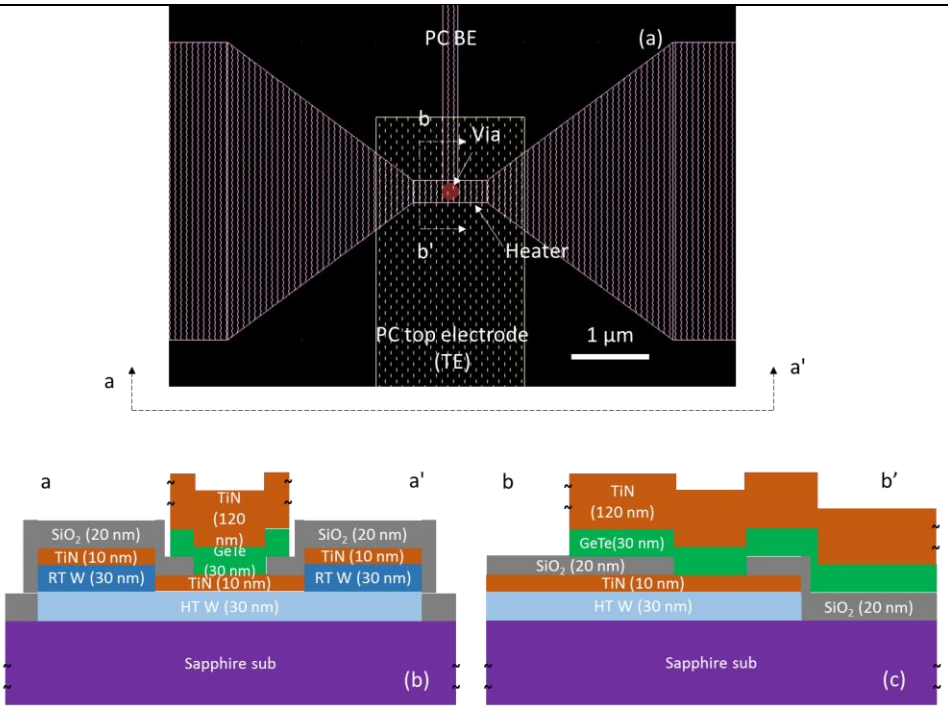

Figure 5.10 (a) the layout of the third E-beam layer for patterning PC and top electrode (yellow dashed pattern) on top of the first (pink pattern) and the second (red circle pattern) E-beam layers. (b)-(c) two cross-section views of the device after the lift-off

Two additional optical lithography steps were then required to allow electrical accesses to the device. As shown in Figure 5.11(b), a standard optical lithography using AZ4110 was firstly applied to etch through the SiO_2 and expose the heater traces defined by the first optical mask layer (shown in Figure 5.11(a)). Following that, another optical lithography step using AZ4210 was applied to lift-off thick metal traces for probe landing. As can be seen in Figure 5.11(c) and (d), the thick metal layer will be in electrical contact with the bottom heater trace layer as well as the top electrode layer. The metal layer is required to be as thick as 150 nm to avoid any step coverage issues. The materials can be Cu or Au which can provide

low resistivity and minimize the trace resistance. Figure 5.12 shows the final microscopic images of the top view of the device.

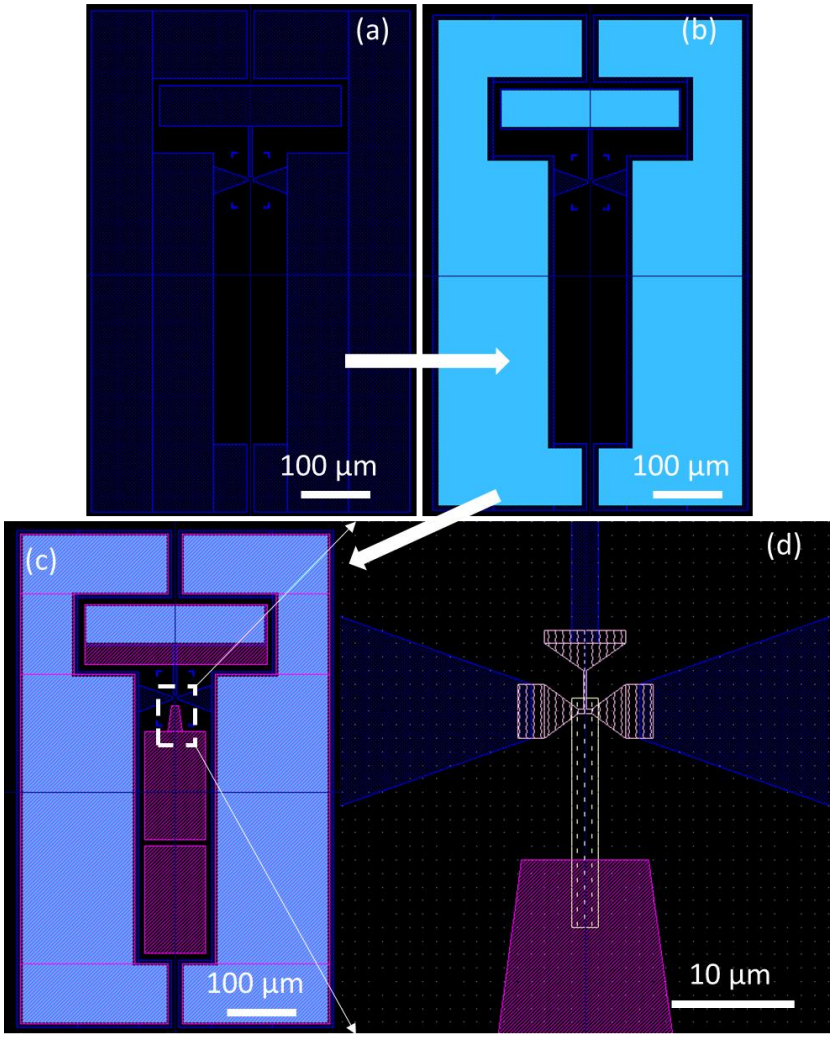

Figure 5.11 (a) layout of the second optical mask layer (blue pattern), the first optical mask layer for openning window through HT W is omitted here to focus on the process flow of patterning top metal traces for probe landing. (b) layout of the third optical mask layer for etching through the SiO_2 (light blue pattern). (c) layout of the fourth mask layer for depositing and lift-off the top metal traces (pink pattern with 45º oriented lines) (d) zoomed-in view for how the top metal trace layer is in contact with the top electrode layer defined by the third E-beam layer

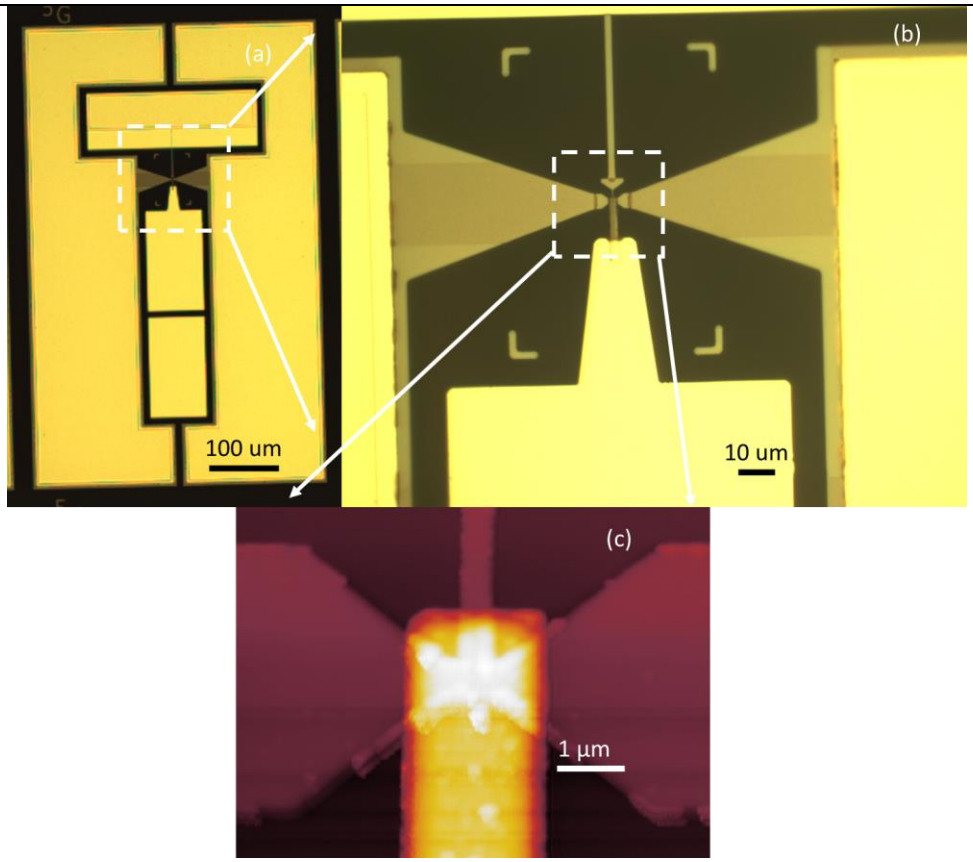

Figure 5.12 top view microscopic images of the final device (a) 1x zoomed-in view (b) 10x zoomed-in view. (c) AFM scan image of the critical section where the heater is oriented horizontally and the PC top and bottom electrodes are oriented vertically

5.7 Summary

In this chapter, a new device architecture and design is proposed to build the 2nd generation nano-scale high speed PC test device which can achieve ultra-fast heating and cooling rate with a thermal time constant of 5 ns. It is shown that by sending a 3.3 V 10 ns pulse or 4 V 5 ns pulse to the heater, the PC layer can be heated up above 700 K. The comparison shows that the 2nd gen device is 8 times faster than the the 1st gen device, with a heating rate of at least 4×10^{10} K/s. This device enables crystallization dynamics

measurements of PC materials in the sub-10 nanosecond regime. It not only will be used to evaluate the non-Arrhenius behavior in a much higher temperature and shorter crystallization time, but also can eliminate the possibility that the non-Arrhenius behavior is caused by the experimental artifact of slow device thermal response, as measured by the 1st gen device. Following that, the detailed fabrication process flow is presented. Four optical steps and three E-beam steps are used to fabricate this device. Detailed characterizations of this device will be presented in the next chapter.

Chapter 6: Crystallization Dynamics Study for Phase Change Memory Using the 2nd Generation Device

6.1 Abstract

In this chapter, the 2nd gen device is used to measure the crystallization dynamics and quantify non-Arrhenius behavior at high temperatures. Modelling and characterization of the 2nd gen device will be discussed firstly, as understanding the device behavior and accurate characterization of the device temperature transients are critical for measuring crystallization dynamics. Crystallization pulse measurement is then presented and crystallization behavior of the PC material has been investigated using pulses with duration ranging from 5 ns to 1 ms. A smaller crystallization activation energy is still observed in the short crystallization time high *T* regime, suggesting that the non-Arrhenius behavior for crystallization rate observed in Chapter 3 is not due to the experiment artifact of slow device thermal response. Finally, evidence of growth-dominated crystallization for GeTe is shown by comparing the Arrhenius plots measured using the 1st gen device and the 2nd gen device.

6.2 Device Model

The 3-D COMSOL model of the 2nd gen device is shown in Figure 5.2. To reduce the complexity of the model and improve the simulation time, only the critical section of the layout is modelled in COMSOL as shown in Figure 5.2(c). Similar to the simulation in Chapter 3, electric current module and heat transfer in solid module are combined to simulate Joule heating and temperature transients for given electrical pulse input. For boundary conditions, the two sides of the heater are set to be electrical terminals. The bottom of the substrate is set to be constant temperature (thermal ground) of 293.15 K. The initial potential is set to be 0 V and the initial temperature is set to be 293.15 K. The entire domains are set to be the heat source, where the power density is simulated based on the current density. The electric circuit module is used to simulate the exact circuit setup in the measurements, which is exactly the same as the

TDT setup in Figure 2.3 for the heater. The heater trace resistance is measured as 29.3 Ω, which is modelled as a series resistor in the electric circuit module. Table 6.1 summarizes the circuit connections. Similar to a SPICE model, each component is assigned to a positive node and a negative node in the circuit in COMSOL. This setup can be used to mimic the transmission line response in the TDT setup.

Table 6.1 Circuit connections in COMSOL electric circuit module

Component	Pulse Source	Source impedance resistor (50 Ω)	Heater	Heater trace resistor (29.3 Ω)	Scope resistor (50 Ω)
Positive node	1	1	2	3	2
Negative node	0	2	3	0	0

Table 6.2 Material properties in COMSOL model

Materials	k_{th} (W/(m·K))	C_p (J/(kg·K))	Density (kg/m^3)	ρ (Ω·m)	TCR	ε_r
Sapphire	Figure 2.5(a)	Figure 2.5(b)	3965	10^9	0	11.5
Tungsten	50	132	19350	10^{-7}	0.002	1
TiN	10	533	4506	5×10^{-6}	4×10^{-5}	1
SiO_2	1	730	2200	10^9	0	3.9
GeTe	1	303	6140	1	0	18

For material properties, tungsten resistivity is set to be 10^{-7} Ω·m, and the TCR of tungsten is set to be 0.002. Note that these are the properties for high temperature deposited tungsten, since the room temperature deposited tungsten is not modelled. Resistivity (ρ) of TiN is set to be 5×10^{-6} Ω·m, while the TCR is set to be 4×10^{-5}, which has negligible impact on the simulation results. For thermal conductivities (k_{th}), tungsten is set to be 50 W/(m·K), TiN is set to be 10 W/(m·K), SiO_2 is set to be 1 W/(m·K) and GeTe is set to be 1 W/(m·K). The sapphire thermal conductivity and heat capacity at constant pressure (C_p) remains the same as shown in Figure 2.5. However, unlike Chapter 3, an additional thermally resistive interface with thermal conductance of 10 MW/(m^2·K) is added between the tungsten and the sapphire substrate. This is necessary in the model for the heater to reach the desired temperature (melt the PC layer) when sending a MPA pulse to the heater, and to make the heater characterizations consistent with simulation. This discrepancy between two models could be due to the different tungsten grain sizes as they were deposited at different temperature and pressure conditions. Other properties will not significantly affect the simulation results. The detailed material properties are summarized in Table 6.2.

With the above model setup, two simulations results have been shown in Figure 6.1 and Figure 6.2, with input pulses of 3.3 V 100 ns and 1.8 V 100 ns respectively. It can be seen in Figure 6.1 that the 3.3 V 100 ns pulse is sufficient to heat the top PC layer up to above 1000 K so that it can amorphize the entire PC volume. However, due to the low thermal conductivity of GeTe (1 W/(m·K)) and high thermal conductivity of TiN (10 W/(m·K)), the top electrode serves as another heat sink and causes a significant temperature gradient between the top and the bottom of the PC. At the end of the pulse, the temperature gradient can be as large as 400 K. On the other hand, for the 1.8 V 1000 ns pulse, the peak temperature on top of the PC layer is 450 K while on the bottom it is 510 K, resulting in a 60 K gradient. Thus, the lower the peak temperature is and the longer the pulse is, the less temperature gradient there is along the thickness of the PC layer.

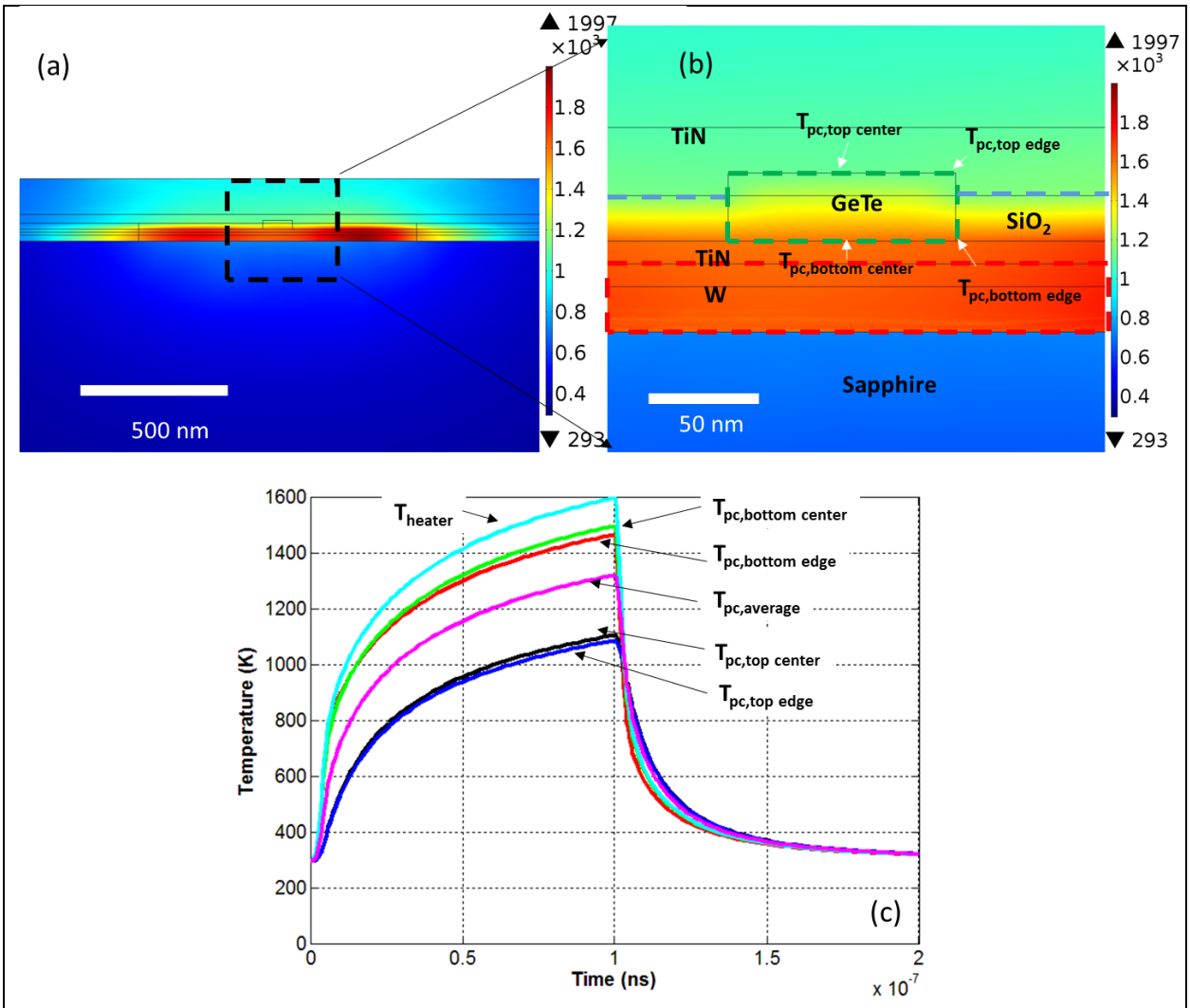

Figure 6.1 For input pulse of 3.3 V 100 ns, temperature profiles from (a) device cross-section view and (b) zoomed-in view of device cross-section and (c) temperature transients of different region in the PC layer

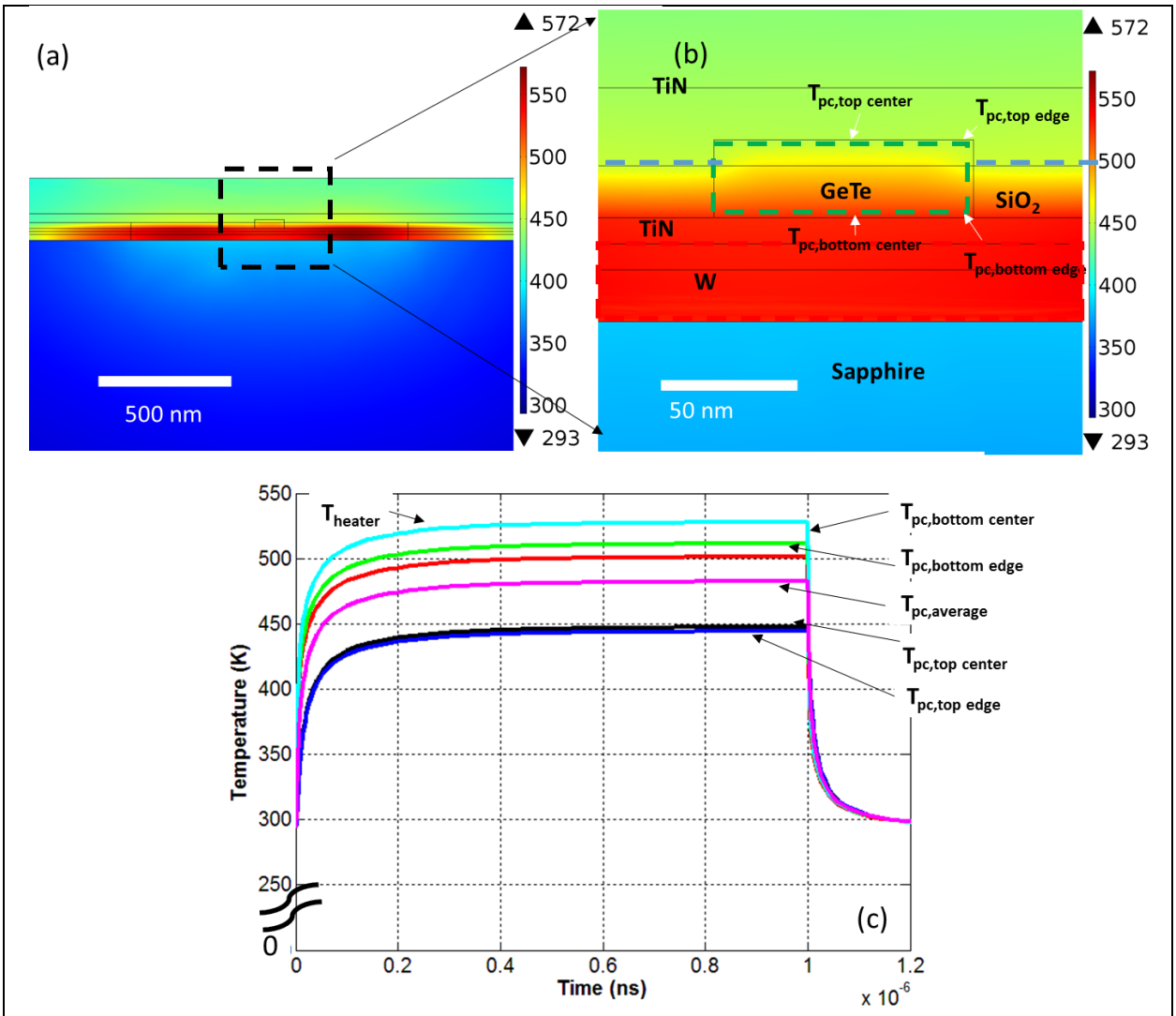

Figure 6.2 For input pulse of 1.8V 1000 ns, temperature profiles from (a) device cross-section view and (b) zoomed-in view of device cross-section and (c) temperature transients of different region in the PC layer

6.3 Test Setup

Figure 6.3 shows the circuit setup for crystallization dynamics measurements. The heater is connected in the same way as shown in Figure 2.3, where the GS and SG RF probes land on two side of the trace pads, putting the heater in parallel with the Agilent 81110A pulse generator (PG) and the Agilent

DSO1014A oscilloscope. They are connected through 2.92 mm coaxial cables. At the same time, two needle probes land on the pads for top and bottom electrodes of the PC, and are connected to the Keithley 2400 source meter to measure the PC DC resistance after each pulse.

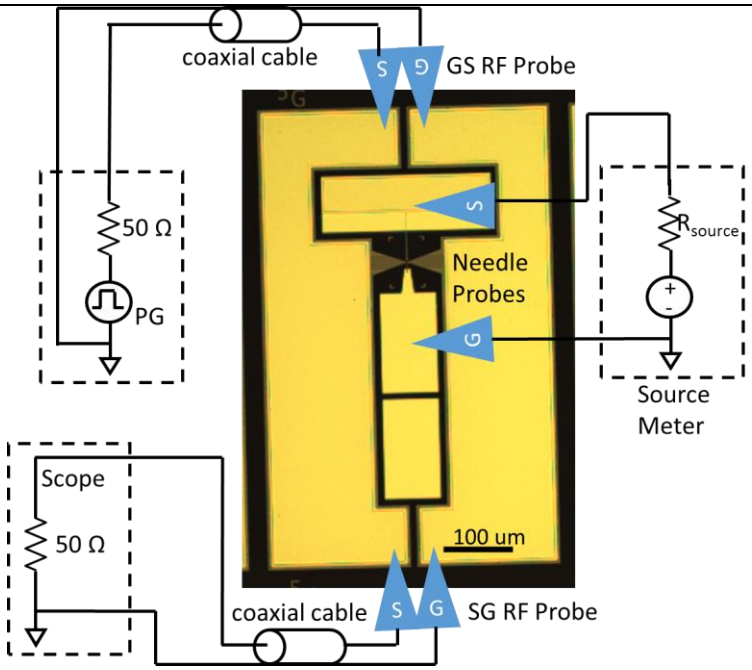

Figure 6.3 Circuit setup for crystallization dynamics measurements using the 2nd gen device.

6.4 Heater Characterization

Preliminary DC measurement for the heaters shows that the heater resistance is 60±2 Ω, with a trace resistance of 29 Ω that is not the meshed part of the COMSOL FEM but rather a series resistor in the electric circuit module. Applying the same methodology described in Chapter 2, accurate thermometry can be achieved on the nano-scale heater by combining TDT and COMSOL simulation. The experimental data and simulated data for the heater response at different pulse configurations are shown in Table 6.3. All pulses have the same rise and fall time of 2 ns. For pulse configurations which satisfy the entire range of interest for temperatures and times, the simulated and measured scope voltage V_s show good consistency. On the other hand, the mismatch between extracted and simulated heater resistance reflects the mismatch

between extracted temperature and simulated spatial average temperatures (since they are linearly correlated). The biggest mismatch is only 2.5 %, suggesting that the simulation model is accurate for predicting temperatures in the heater.

Table 6.3 Comparison of experiment and simulation data on heater thermometry

Voltage (V)	Pulse Width (ns)	Measured Peak V_s (V)	Simulated Peak V_s (V)	Extracted Peak R_h (Ω)	Simulated Peak R_h (Ω)	Mismatch (%)
2.2	20	1.53	1.52	67.4	66.1	1.9
3	20	2.16	2.14	78.4	77.8	0.8
1.7	500	1.16	1.18	63.2	64.7	2.3
2	500	1.40	1.41	68.3	70.0	2.5
1.5	100000	1.05	1.06	62.1	63.4	2.1
1.8	100000	1.28	1.29	65.9	66.3	0.6

6.5 Device Characterization

The preliminary DC characterization shows that the PC resistance is so high (> 1 GΩ) that the Keithley 2400 source meter is not able to accurately measure. While with an assumed amorphous resistivity of 1 Ω·m, the PC resistance is estimated to be 3 MΩ. This discrepancy comes from the huge contact resistance between the TiN and the amorphous GeTe. However, TiN has similar work function to tungsten that should have Ohmic contact with both amorphous and crystalline GeTe. As shown in Figure 6.4, a test structure is built with the absence of the PC layer to identify this issue. The calibration results show that even with the absence of the PC layer, the device still have non-linear I-V characteristic, suggesting there is a Schottky barrier between two TiN layers. This barrier could come from a thin layer of oxidized TiN, due to the bottom TiN layer having been exposed to the air during the fabrication. The barrier can be

removed by sweeping voltage across the device to trigger the break down event with a threshold voltage of around 2.6 V. As shown in Figure 6.4(b), the device has a linear I-V characteristic after the break down, with a DC resistance of 400 Ω.

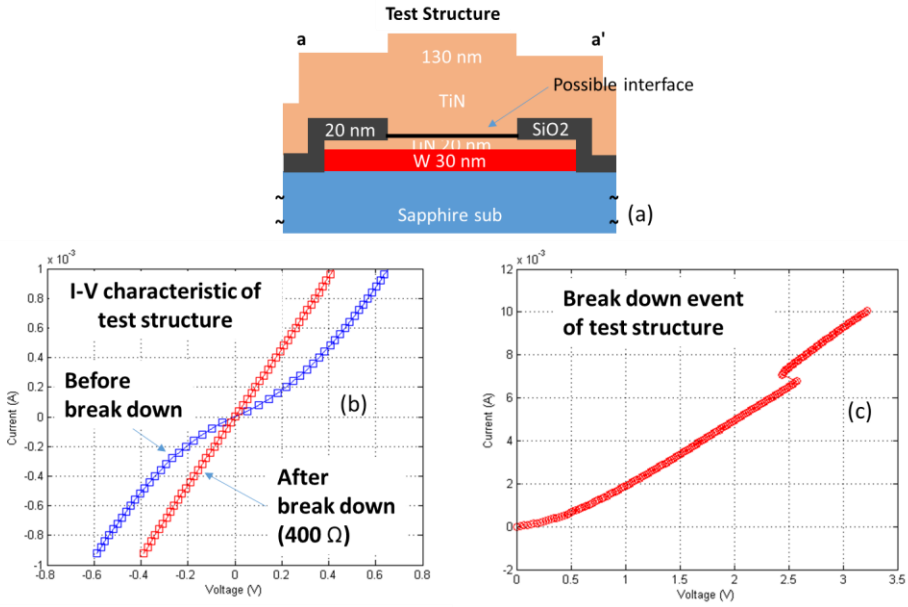

Figure 6.4 (a) cross-section schematic of the test structure for interface issue (b) I-V characteristic of the test structure before and after the break down sweep, in blue and red color respectively (c) I-V characteristic of the test structure during break down sweep

To obtain device with desired functionality, an initial conditioning MPC process is required. As shown in Figure 6.5, the PC resistance is measured after each pulse. Each pulse has a pulse width of 100 μs, with a rise and fall time of 2 ns. The pulse voltage is increased step by step. Using the 2.6 V 100 μs MPC conditioning pulse, the device can be crystallized to a reasonable ON-state resistance of 1400 Ω. Note that the PC resistance data for voltages smaller than 2.4 V is not accurate since the Keithley 2400 source meter is not able to accurately measure resistances higher than 1 GΩ.

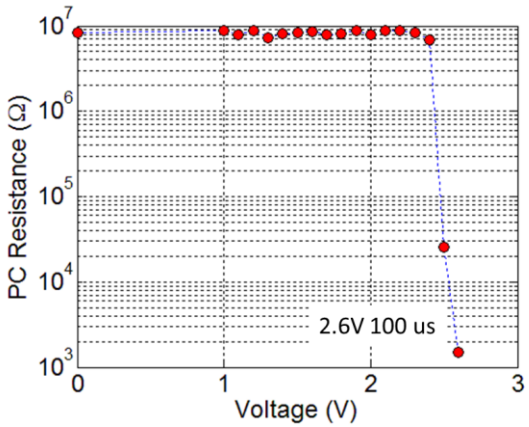

Figure 6.5 Change of PC resistance with voltage during the initial conditioning MPC process

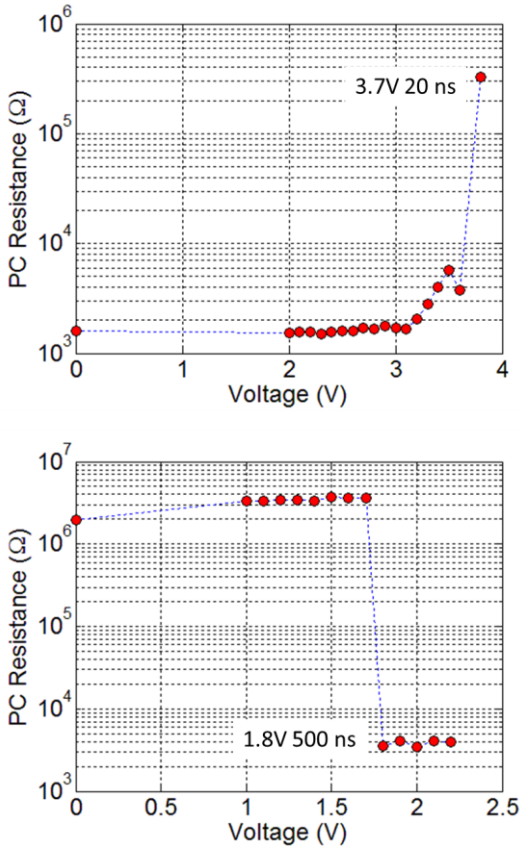

Figure 6.6 Change of PC resistance with voltage during the (a) MPA process and (b) MPC process

After the initial conditioning, the standard MPC and MPA measurements are performed on the device. As shown in Figure 6.6, the MPA pulse is characterized to be 3.7 V 20 ns and the MPC pulse is characterized to be 1.8 V 500 ns, which corresponds to 1100 K and 450 K at the bottom of the PC layer, respectively. These two pulses can be used to reliably cycle the device for more than 100 cycles, between the OFF-state resistance of 2.1 ± 0.3 MΩ and ON-state resistance of 1.7 ± 0.5 kΩ, as shown in Figure 6.7. These measurements suggest that the device has the desired functionality to be SET, RESET and cycled, so that can be further applied to measure the crystallization properties of PC material.

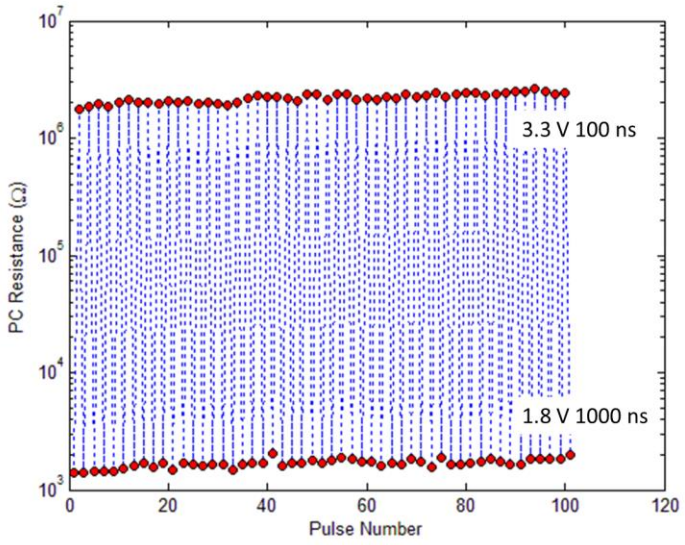

Figure 6.7 Cycleability measurement of the 2nd gen device

6.6 Pulse Measurements for Crystallization Dynamics

The crystallization dynamics measurements are done by sending heater pulses with different configurations and measuring the DC resistance of the PC after each pulse. After measuring the DC resistance, another standard RESET pulse (3.3 V 100 ns) is sent to the heater to re-amorphize the PC layer. By doing this, we can ensure that there is no accumulation effect of crystallization, and the pulse width of

each crystallization pulse reflects the crystallization time. As shown in Figure 6.8, pulse widths from 1 ms down to 5 ns are selected to span the entire time range of interest. For every pulse width configuration, it can be seen that the PC resistance starts with high OFF-state value, but eventually can be SET to the ON-state resistance using a single pulse. For pulse width longer than 20 ns, the ON-state resistance is around 1.5 kΩ; while for 20 ns and 10 ns pulses, the resistances are higher, but still are three orders of magnitude lower than the OFF-state values. This can be attributed to the more in-complete crystallization for shorter pulses.

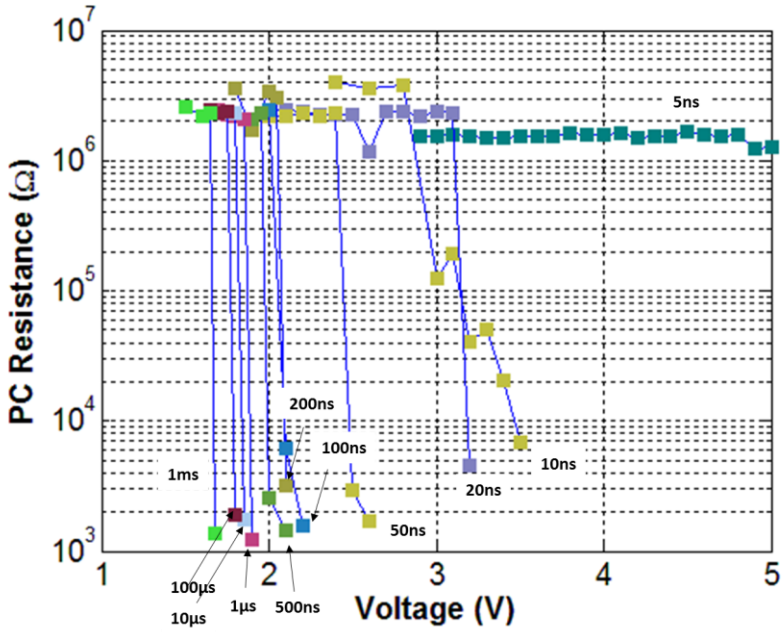

Figure 6.8 PC DC resistance measured after each crystallization pulse as a function of voltage, with different pulse widths. Note that a RESET operation is performed between each step to re-amorphize the PC layer

For 5 ns pulse, the voltage is increased all the way to 5 V, which can generate a peak temperature of 1050 K at the top of the PC layer. This suggests that within the temperature range from 305 K (generated by the first pulse with voltage of 2.9 V) to the GeTe melting point 1000 K, 5 ns is not enough for

crystallizing the entire PC layer. This observation is consistent with the C-curve in the TTT-diagram and suggests that there exists $t_{x,min}$, which in this case is around 10 ns for this device. It is also consistent with the pulse measurement discussed in [97], where the $t_{x,min}$ is around 3 ns for devices with slightly smaller PC volume (60 nm × 60 nm × 20 nm).

6.7 Analysis of Crystallization Dynamics

To generate the Arrhenius plot, each step is simulated using the well-calibrated COMSOL model with each crystallization pulse as the input. The simulated temperature transient at the bottom of the PC layer is obtained. Due to the big temperature gradient in the PC layer and that the thickness of the amorphous region is uncertain, the bottom temperature is taken as a reference. The peak temperature for each transient is used to generate the Arrhenius plot, shown as the blue data in Figure 6.9(a). In the low T regime ($T \leq 600$ K), the activation energy E_x is extracted to be around 2.17 eV, which is consistent with the E_x measured using the 1st gen device. The pre-exponential factor τ_{x0} is around 5.2×10^{-26} s, which is smaller that of the 1st gen device (2.4×10^{-24} s), this can be attributed to the amorphous size being different between two device structures. In the high temperature regime ($T > 600$ K), however, the similar non-Arrhenius behavior of change in E_x (to 0.3 eV) and τ_{x0} (to 5.1×10^{-10} s) is observed. This is also consistent with the measurements using the 1st gen device.

However, the same issue of non-isothermal process in the high temperature regime still exists. For pulse width longer than 1 μs, there is negligible temperature transient effect and can be considered as isothermal crystallization process. For pulse width shorter than 1 μs, the non-isothermal heating caused by the temperature transient effect cannot be ignored. To address this problem, the effective crystallization temperature is calculated for each crystallization pulse that is shorter than 1 μs. The effective crystallization temperature $T_{x,eff}$ for a given temperature transient is the steady-state temperature which should have generated the same crystallization portion in the same time as the transient temperature would have achieved.

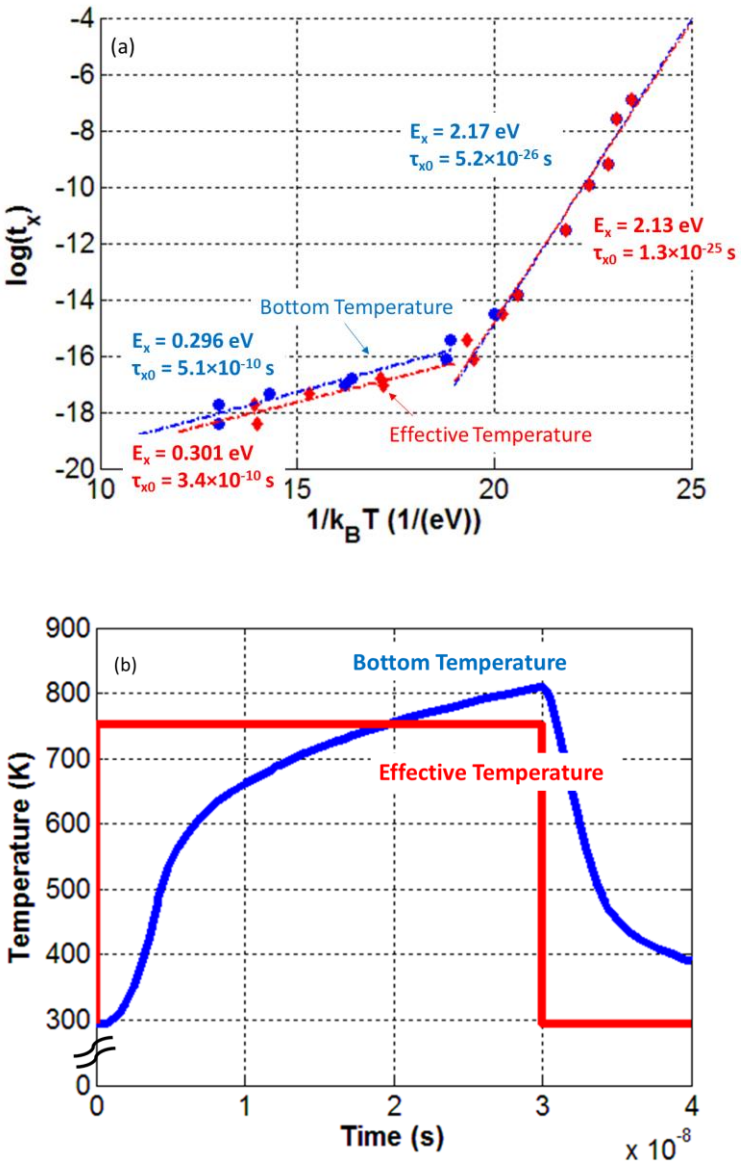

Figure 6.9 (a) Arrhenius plot generated using peak temperature at the bottom of the PC (blue) and effective temperature of the PC (red) (b) simulated temperature transient (blue) for crystallization pulse of 2.8 V 30 ns and the corresponding effective temperature transient (red)

To calculate $T_{x,eff}$, the crystallization process achieved by the simulated temperature transient is discretized into a series of small crystallization processes with time step Δt of 100 ps and steady-state

temperatures *T(t)* at each step. For each small crystallization process, the crystallization rate is calculated based on the τ_{x0} and E_x extracted from blue data in Figure 6.9(a):

$$r(t) = r_0 \exp(-E_x / k_B T(t)) \tag{6.1}$$

This assumes the Arrhenius model extrapolated from the low *T* regime is valid over the entire temperature range. By summing up the crystallization rate over time, the crystallization volume Vol_x can be obtained:

$$Vol_x = \sum_{t=0}^{t_{END}} r_0 \exp(-E_x / k_B T(t)) \Delta t \tag{6.2}$$

The effective crystallization temperature $T_{x,eff}$ can then be calculated by solving:

$$r_0 \exp(-E_x / k_B T_{x,eff}) t_{PW} = Vol_x \tag{6.3}$$

where t_{PW} is the pulse width time. The $T_{x,eff}$ is then:

$$T_{x,eff} = \frac{E_x}{k_B \log(\frac{r_0 t_{PW}}{Vol_x})} \tag{6.4}$$

Figure 6.9(b) shows the comparison between the temperature transient from the simulation (in blue color) and the $T_{x,eff}$ (in red color) calculated using the above method, at the crystallization pulse of 2.8 V 30 ns. For a temperature transient with peak temperature of 810 K, $T_{x,eff}$ is 756 K to achieve the same level of crystallization in 30 ns. This method can be applied to all steps with pulse width shorter than 1 μs, generating the red data in Figure 6.9(a).

In the low *T* regime, the E_x and τ_{x0} are extracted to be 2.13 eV and 1.3×10^{-25} s respectively. In the high *T* regime, these two parameters are extracted to be 0.3 eV and 3.4×10^{-10} s. In both regimes, the parameters are very similar to those extracted from the blue data, suggesting that the transient effect in the temperatures does not significantly affect the measurement of E_x.

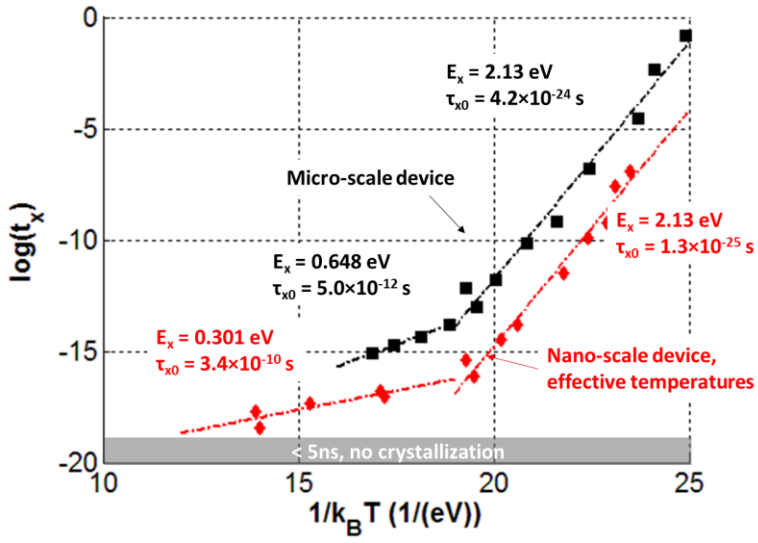

Figure 6.10 Arrhenius plot measured using the 1st gen device (black squares) and the 2nd gen device (red diamonds)

Figure 6.10 shows the comparison of Arrhenius plots obtained using the 1st gen device and the 2nd gen device, in black and red data respectively. It can be seen that E_x for both case are both 2.13 eV at low T ($T \leq 600$ K), while τ_{x0} of the 2nd gen device data is 32 times smaller than that of the 1st gen device data. This is also consistent with the fact that 2nd gen device has smaller amorphous PC size to crystallize, as mentioned previously. It also suggests that the crystallization process is a growth-dominated process, where the crystallization time is dependent on how fast the crystalline front grows towards the amorphous region, quantified by the growth velocity. For both devices, a simple 1-D growth process can be assumed. Because for both devices there exists crystalline phase and amorphous-crystalline boundaries even after the RESET operation. Figure 6.11 shows the direction of crystalline front growth for both devices.

The pre-exponential factor is then given by:

$$\tau_{x0} = \frac{l_a}{v_{g0}} \tag{6.5}$$

where v_{g0} is the pre-exponential factor for growth velocity and l_a is the amorphous region size. We can get the ratio of the pre-exponential factors for two devices:

$$\frac{\tau_{x0,micro}}{\tau_{x0,nano}} = \frac{l_{a,micro}}{l_{a,nano}} \tag{6.6}$$

Since the amorphous region size is unknown, we can estimate the ratio of the amorphous region size for the two devices by their OFF-state DC resistances and cross-section areas:

$$\frac{l_{a,micro}}{l_{a,nano}} = \frac{R_{micro}A_{micro}}{R_{nano}A_{nano}} \tag{6.7}$$

From the DC measurements for both devices, R_{micro} is around 2.2 MΩ, R_{nano} is around 1 MΩ, A_{micro} is estimated to be 7.8×10^{-14} m^2 and A_{nano} to be 6.1×10^{-15} m^2. The ratio is then estimated to be 28, close to the ratio of 32 as shown in Figure 6.10.

In the high T regime (T > 600 K), E_x of the high-speed device is smaller. This may be due to the lack of data with higher temperature for 1st gen device, so that E_x at high T is underestimated. Note that for $t \leq 5$ ns, no crystallization can be achieved, based on the crystallization pulse measurement shown in Figure 6.8. This can be a strong evidence that the crystallization process is slowed down at high temperatures, due to either the turnover in the TTT diagram caused by the loss of driving force, or the decrease in E_x based on the fragility model. The quantification of this will be further discussed in the next chapter.

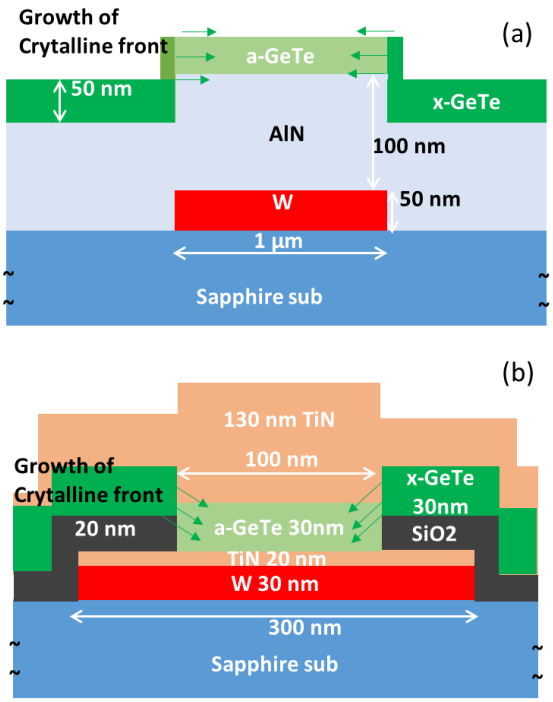

Figure 6.11 Cross-section schematics of (a) the 1st gen device and (b) the 2nd gen device. The green arrows in both figures show the direction of growth of the crystalline front during the crystallization process

6.8 Summary

In this chapter, the characterization of the 2nd gen device is discussed. The detailed modelling for the 2nd gen device, as well as the comparison between the TDT measurements and the simulation is presented to confirm that the heater thermometry is still accurate for this device in high *T* regime. The study of the interface issue and the required conditioning process has been discussed to ensure that the devices have the correct behavior. It is shown that we are able to reliably SET, RESET and cycle the devices.

Next, the crystallization pulse measurements data are presented to show the device resistance after crystallization attempts as in the time range from 1 ms done to 5 ns, within the temperature range of interest. Evidence that crystallization fails at 5 ns or shorter time is presented, showing the limitation of

crystallization time for this device. Using the crystallization time and temperature data, a new Arrhenius plot is generated, with the correction of the temperature transient effect. The comparison of Arrhenius plot between the 1st gen device and the 2nd gen device has been shown, suggesting that the crystallization is a growth-dominated process.

Chapter 7: Non-Arrhenius Models and Unified Framework for PC RF Switch Performance Estimation

7.1 Abstract

In this Chapter, different models including growth dominated model, the nucleation dominated model, the combined model of growth and nucleation and the fragility model will be investigated to explain the data from last Chapter on the non-Arrhenius behavior for crystallization. A growth-dominated crystallization model combing the fragility model is proposed to quantify the growth rate crystallization process over the entire temperature range, from room temperature to the melting point of GeTe. An iterative approach is developed to extract model parameters based on measurement data. The maximum growth rate is found to be 1.4 m/s at 860 K. Next, a unified framework based on this model is developed to simulate the crystallization process for RF PC switches with given geometry and electrical inputs. The CQT measurement is re-visited and simulated using this framework. The results are in good agreement with the measurement data. Finally, the unified framework is applied to study the power-threshold voltage trade-off for an appropriately designed RF PCS, showing that this framework has great potential to be used in estimating performance for RF PCS with different designs.

7.2 Introduction

In the previous Chapter, $T_{x,eff}$ is calculated based on finding the isothermal temperature for given pulse width which results in the same crystallization volume achieved by integrating the crystallization rate over time using simulated temperature transients and the simple model of Arrhenius equation extrapolated from the low T regime. But this model is likely to over-estimate the crystallization rate at high T, thus over-estimating $T_{x,eff}$. In this Chapter, we will apply the growth dominated model, the nucleation dominated model, the combined model of growth and nucleation and the fragility model respectively to correct the over-estimation at high T and quantify the non-Arrhenius behavior. Growth velocity and diffusion

coefficient at given T can be estimated using the fragility model. The quantification of this model helps us better understand the limitation of crystallization dynamics and thus the writing speed for PCM.

On the other hand, the understanding of crystallization dynamics can be applied to estimate the performance for RF switches. As discussed in Chapter 3, CQT is an important property for designing low power RF switches. While the CQT is extracted to be 310 ns using the 1st gen device and the methodology described in Chapter 3, it is a specific property for that device geometry. However, a more generalized CQT is needed for applying to RF switches with different structures and geometries. In this chapter, a unified framework is presented which combines the device modelling and the crystallization dynamics to estimate RF switch performance, including CQT (for lower power consumption), threshold voltage V_{th} (for higher power handling) and its variation of a given PC RF switch device architecture. The CQT measurement results will be revisited and reconciled to validate this framework. Finally, the framework is applied to study the power-V_{th} trade-off for an appropriately designed RF PCS.

7.3 Growth and Nucleation Models

The method described by (6.1) - (6.3) can be generalized as a unified method to calculate $T_{x,eff}$ using advanced non-Arrhenius models. For any model, the crystallization rate can be expressed as a temperature dependent term $r(t)$. To estimate the total crystallization volume, we can modify (6.2) as:

$$Vol_x = \sum_{t=0}^{t_{END}} r(T(t))\Delta t \tag{7.1}$$

$T_{x,eff}$ can then be calculated by solving:

$$r(T_{x,eff})t_{PW} = Vol_x \tag{7.2}$$

In classic crystallization theory for chalcogenide, growth and nucleation models have been studied thoroughly, as described in Chapter 1. The loss of driving force at high T causes the turnback of the crystallization rate curve in the TTT diagram, and is the possible source of non-Arrhenius behavior. For

nucleation dominated crystallization, $r(T)$ is described by (1.5). The enthalpy of fusion ΔH is assumed to be 1.45 GJ/m^3 [33], the average volume of particle attaching to crystalline phase is assumed to be 3.2×10^{-23} cm^3 [31]. To achieve the best fit at low T (T < 600 K), the pre-exponential factor for nucleation I_0 is set to be 5×10^{25} s^{-1}, and the surface energy difference σ is set to be 0.065 J/m^2, which is similar to the value used for GST [126], [127].

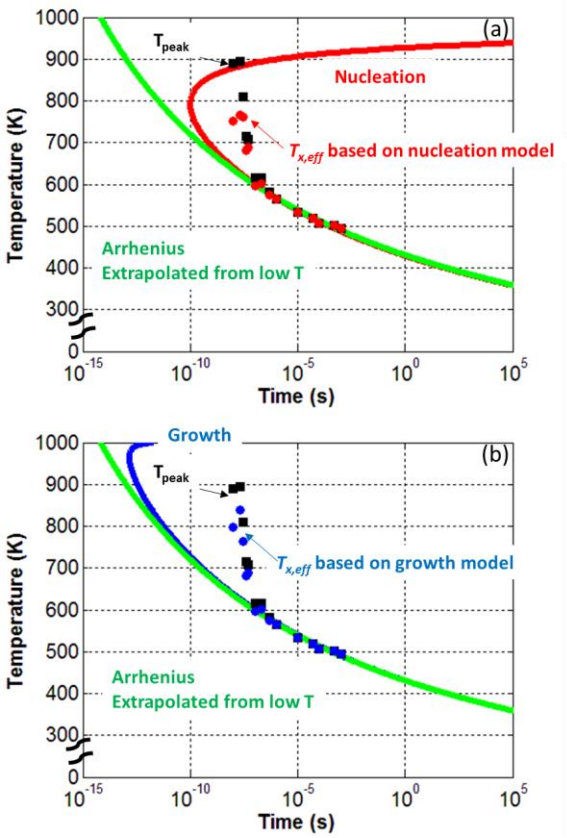

Figure 7.1 (a) TTT diagram of Arrhenius model extrapolated from the low T regime (greed solid line), nucleation dominated model (red solid line) together with the original T_{peak} (black squares) and $T_{x,eff}$ calculated based on nucleation model (red circles) (b) TTT diagram of Arrhenius model extrapolated from the low T regime (greed solid line), growth dominated model (blue solid line) together with the original T_{peak} (black squares) and $T_{x,eff}$ calculated based on growth model (blue circles)

As shown in Figure 7.1(a), the TTT diagram of nucleation dominated model (in red color) is plotted together with the Arrhenius model extrapolated from the low T regime (in green color). Meanwhile, the black squares are shown as the original un-corrected peak temperature T_{peak} from the transient, and the red circles are $T_{x,eff}$ based on the nucleation dominated model. It can be seen that with these parameter setting, the two models and the data for $T_{x,eff}$ are consistent at low T. But at high T, the nucleation rate peaks at around 800 K, with a minimum crystallization time of 100 ps. This deviates from the Arrhenius behavior at a much shorter crystallization time, comparing to the measurement data. Thus, even though this model corrects the overestimation of T for high T data, it fails to explain the experimental observation that crystallization cannot happen in time less than 5 ns.

For growth dominated crystallization, the crystallization rate is considered the same as the growth rate, which is described by (1.7). Using the same value for ΔH, v_p and σ, and by setting the pre-exponential factor u_0 to 7.7×10^{24} s^{-1} (consistent with the pre-exponential τ_0 of 1.3×10^{25} s in Figure 6.10), the growth dominated model can fit the low temperature data well, as shown in Figure 7.1(b). It can be seen that the growth dominated model deviates from the Arrhenius model at temperatures much closer to the melting point (1000 K), with a minimum crystallization time shorter than 1 ps. Thus, neither the nucleation dominated model nor the growth dominated model alone can be applied to explain the high temperature crystallization dynamics.

7.4 Fragility Model

As discussed in the previous chapter, the ratio of pre-exponential factors in Figure 6.10 is consistent with the growth dominated crystallization process. The fragility model relates the crystallization rate r, dominated by the crystalline phase growth rate u, to the viscosity η described by the VFT from (1.18), and yields the temperature dependent growth rate:

$$r(T) \approx u(T) = u_0 T \exp(-\frac{B}{T - T_0})(1 - \exp(-\frac{\mu v_p}{k_B T})) \tag{7.3}$$

The non-Arrhenius behavior mainly depends on driving force term $1-\exp(-\frac{\mu v_p}{k_B T})$ that dominates the growth rate at T close to the melting point ($T > 900$ K), and the fragility fitting constants B and T_0. The driving force term has the same parameters as those in the previous section. By fitting this equation with the original T_{peak} data, B is extracted to be 923.4 K, T_0 to be 426.6 K and u_0 to be 1.37×10^6 1/(K·s). The first iteration fitted model is shown as the black dashed line in the Arrhenius plot in Figure 7.2(a). Using these fitting parameters as initial values, we can apply (7.3) to (7.1)-(7.2) to calculate the $T_{x,eff}$ for each point, followed another iteration of fitting based on $T_{x,eff}$. After 10 iterations, we can extract the converged parameters from the final fitting, B to be 1094.0 K, T_0 to be 421.3 K and u_0 to be 4.84×10^6 1/(K·s). The final model after the 10th iteration is shown as the magenta dashed line in Figure 7.2(a), together with the final $T_{x,eff}$ for each point.

Figure 7.2(b) shows the TTT diagram for the extrapolated low T Arrhenius model and the fragility models. The fragility model (magenta dashed line) diverges from the low T Arrhenius model (green solid line) at $T < 480$ K or $T > 600$ K. In the temperature range from 480 K to 600 K, the two models can almost represent the same behavior observed from the measurements. At $T > 850$ K, the loss of driving force starts to dominate the process. The minimum crystallization time $t_{x,min}$ of 6.9 ns can be found at $T_{x,min}$ of 850 K, consistent with the observation that no crystallization can be achieved using 5 ns pulse during the pulse measurements. Also, it is known that the Stokes–Einstein Relation (SER) will break down at temperatures close or below glass transition temperature T_g [50], that the diffusion coefficient D is no longer reciprocally dependent on viscosity η, and remains high in spite of large η. Thus, for $T < T_g$, the model will underestimate the crystallization rate. However, since our experiments are conducted in ultra-high speed regime, we are interested in T ranges from 600 K to 1000 K at which crystallization process can be well explained by the fragility model and the VFT. To avoid infinite and negative crystallization time caused by $T <= T_0$ in the VFT, an extrapolation of the low T Arrhenius model is used for $T <= T_g$, results in the modified fragility model (magenta solid line) in Figure 7.2(b).

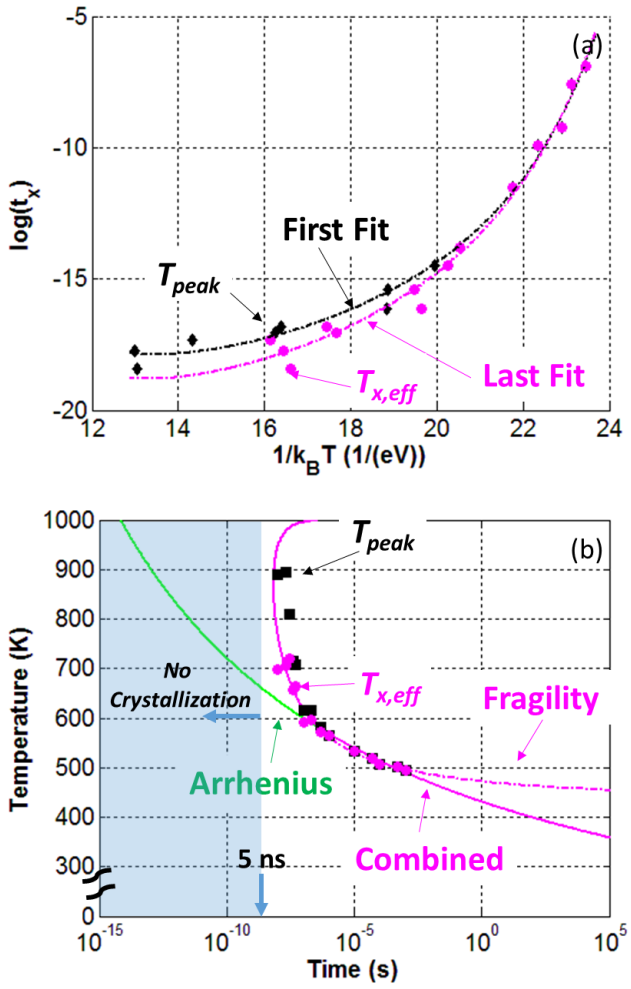

Figure 7.2 (a) Arrhenius plot of the original T_{peak} data (black squares) and the $T_{x,eff}$ calculated based on the fragility model (magenta circles), together with the fragility model after the first iteration fitting (black dashed line) and the final iteration fitting (magenta dashed line) (b) TTT diagram of the Arrhenius model extrapolated from the low T regime (green solid line), the converged fragility model (magenta dashed line), the modified fragility model (magenta solid line) together with the original T_{peak} data (black squares) and the $T_{x,eff}$ data (magenta circles)

7.5 Growth Rate Estimation Based on Fragility Model

Since the crystallization growth rate u given by (7.3) is geometry specific, the growth velocity v_g can be calculated based on the device geometry and the growth rate, given by:

$$v_g = v_{g0,T} \exp(-\frac{B}{T - T_0})(1 - \exp(-\frac{\mu v_p}{k_B T})) \tag{7.4}$$

Where $v_{g0,T}$ is a temperature dependent pre-exponential factor that is not geometry specific, and can be calculated as:

$$v_{g0,T} = l_a u_0 T \tag{7.5}$$

Where l_a is the thickness of amorphous material being crystallized during the process. For a film with thickness l_a in the order of 30 nm, $v_{g0,T}$ for growth velocity can be estimated to be 14.5 m/s at 300 K and 43.5 m/s at 900 K. Note that they are not the actual growth velocity at these temperatures, but the pre-exponential factors. A temperature independent pre-exponential factor v_{g0} can be defined as $v_{g0,T}/T$, which is 0.0484 m/(K·s). The diffusion coefficient pre-factor D_0 be estimated as [44]:

$$D_0 = v_{g0,T} \lambda \tag{7.6}$$

Where λ is the average atomic distance, estimated to be 0.3 nm [33]. The diffusion coefficient pre-factor D_0 can thus be estimated as 4.3×10^{-9} m^2/s at T = 300 K and 1.3×10^{-8} m^2/s at T = 900 K. These values are close to the extracted D_0 for GeTe, 5.2×10^{-9} m^2/s [33]. The attempt frequency can then be calculated as approximately [128]:

$$f_0 = \frac{D_0}{\lambda^2} \tag{7.7}$$

Which is 4.8×10^{10} s^{-1} at 300 K and 1.4×10^{11} s^{-1} at 900 K. These are more reasonable values comparing to the pre-exponential factor extracted from the low T Arrhenius model (e.g. 1.2×10^{27} s^{-1} as mentioned in the introduction of Chapter 5) and closer to the commonly assumed value (10^{12} s^{-1}) for surface phonon frequency [128].

Figure 7.3 shows the diffusion coefficient D and growth velocity v_g as a function of T/T_{melt}, plotted from glass transition temperature T_g to T_{melt}, where T_{melt} is 1000 K for GeTe. The growth velocity peaks at about 860 K, almost the same as reported in [129], which is also the $T_{x,min}$ for the growth dominated crystallization process. From the inset of Figure 7.3, the maximum growth velocity is found to be 1.4 m/s, slightly lower than the reported value 3.3 m/s in [129].

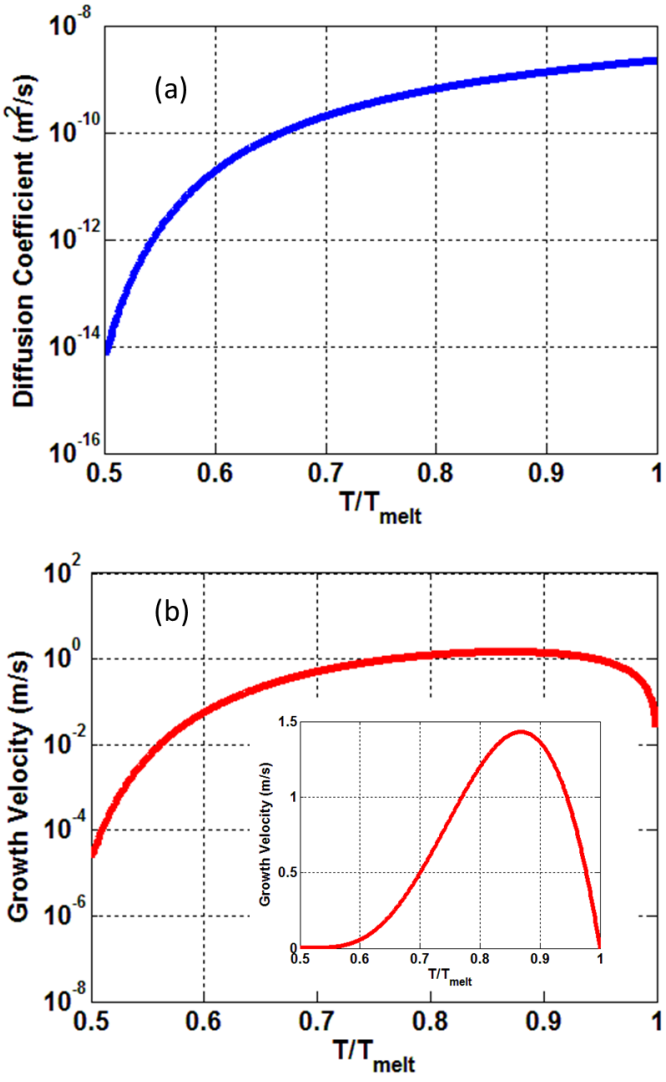

Figure 7.3 (a) diffusion coefficient D and (b) growth velocity v_g as a function of T/T_{melt}, the inset is plotted in linear scale to show maximum growth velocity

7.6 Unified Framework for RF Switch Performance Estimation

To predict the RF switch, the growth velocity can be used as a generalized property to predict the crystallization process and the final fraction of crystallized material for given device structure. For any device structure and heater pulses, the temperature transients can be generated using the COMSOL model. Again, the model can be validated by the thermometry method described in Chapter 2. Using the simulated temperature transients, the fraction of crystallized material at the end of the crystallization process can be estimated based on (7.1), where the temperature dependent crystallization rate *r(T)* is model specific. As discussed in the previous section, the fragility model can generate *r(T)* that is most consistent with the observation from the crystallization pulse measurements and the reported data from various literatures [33], [128], [129]. Thus, in this section, we will also apply that model to simulate the growth process.

Table 7.1 Parameters for the growth velocity

Parameter	Value
B (K)	1090
T_0 (K)	421
ΔH (J/m^3)	1.45×10^{9}
v_p (cm^3)	3.20×10^{-23}
v_{g0} (m/(Ks))	4.84×10^{-2}

The growth velocity can be described by the following:

$$v_g = v_{g0} T \exp\left(-\frac{B}{T - T_0}\right)\left(1 - \exp\left(-\frac{\mu v_p}{k_B T}\right)\right) \tag{7.8}$$

The parameters is summarized in Table 7.1. Note that the driving force μ is given by (1.3). The 1st gen device geometry is used here as an example to describe the framework, as well as validate the correctness of the framework, by checking the consistency between the predicted crystallization fraction and the CQT measurements.

Three measurements with different input heater pulses and PC temperature transients are used to calculate the crystallization fraction π_x. PC temperature transients shown in Figure 7.4(a) are the same as those shown in Figure 3.12 with the corresponding input pulses. The pulse voltage is 3 V, pulse width is 1 μs, pulse rise time is 100 ns and pulse fall times t_{fall} are 100 ns, 300 ns and 400 ns respectively. The pulses are all able to melt the PC layer at first, and quench the temperature at different speeds, as discussed in Chapter 3. The three pulses will respectively result in PC DC resistances of 7.0 MΩ, 1.9 MΩ and 670 Ω, as shown in Figure 3.10(b).

By inputting the transients to the growth velocity model and assuming an initial amorphous length of 700 nm (initial melted zone size), the growth velocity and the fraction of crystallized material as a function of time can be generated, as shown in Figure 7.4(b) and (c). The fraction of crystallized material is 0.40, 0.82 and 1.02 respectively. This is consistent with the CQT measurements since for the cases with t_{fall} of 100 ns and 300 ns, the PC layer is successfully amorphized, corresponding to a π_x less than 1; while for the t_{fall} of 400 ns, the entire volume is crystallized, corresponding to a π_x larger than 1. We can also plot the transients in a similar fashion as shown in Figure 3.11 and Figure 3.12 where blue curves represent that the PC is still in OFF-state while the red curves represent that it has been crystallized into ON-state. At t_{fall} of 400 ns, the fraction of crystallized PC reaches 1 at around 300 ns, at the PC temperature of 630 K, as shown in Figure 7.4(a). These values are also consistent with the in-situ experiments shown in Figure 3.11(b), that at t_{fall} of 400 ns the recrystallization happened at T = 630 K.

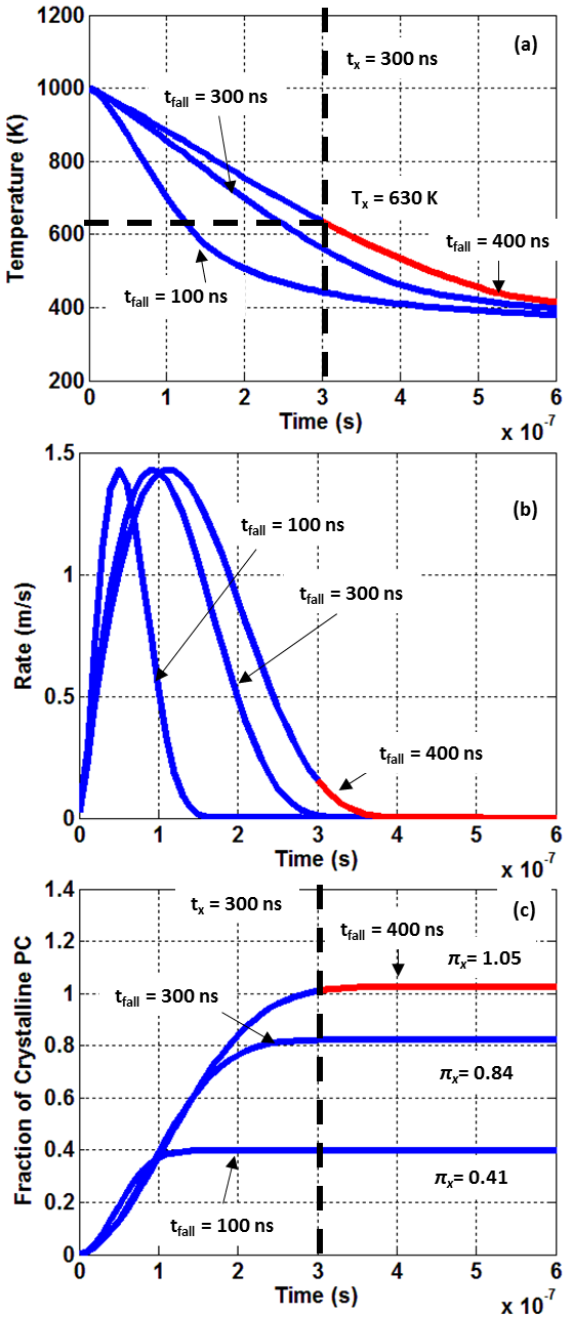

Figure 7.4 (a) temperature transients of the PC corresponding to pulse fall times t_{fall} of 100 ns, 300 ns and 400 ns, respectively. The time is adjusted to start at when the temperature just decreases below the melting point. (b) rate transients at different t_{fall} (c) transients of crystalline fraction at different t_{fall}. Blue and red color represents the PC OFF-state and ON-state respectively

Moreover, by substituting $\pi_{x,100ns}$ = 0.40 and $\pi_{x,300ns}$ = 0.82 into:

$$\frac{R_{OFF,100ns}}{R_{OFF,300ns}} = \frac{1-\pi_{x,100ns}}{1-\pi_{x,300ns}} \tag{7.9}$$

The OFF-state resistance ratio of these two cases can be calculated as 3.35. This value is close to the measured resistance ratio of 3.68.

The above consistencies with the in-situ CQT experiments discussed in Chapter 3 suggest that the fragility model based temperature dependent growth velocity can be applied to predict the crystallization behavior for the devices. Finally, the remained amorphous size can also be calculated as 126 nm and 420 nm, at t_{fall} of 100 ns and 300 ns respectively.

This framework can be further applied to the more appropriately designed RF switch devices described in the previous work [70][88], which have cutoff frequency of 5.3 THz and R_{ON} of 2 Ω and are ready to be integrated with the CMOS chips. In this way we can demonstrate the framework in a real word case, to estimate the performance of the RF switch in terms of power consumption and power handling.

The RF switch architecture and geometry is shown in Figure 1.8. This device is expected to have the same crystallization behavior (crystalline front grows from the two sides of the PC layer) due to the same PC material (GeTe) being used and the similar architecture. The heater width is 1 μm and the length is 25 μm, much larger than the one in the 1st gen device, to ensure a PC width of 20 μm for low resistance. The heater and PC thickness are both 50 nm, and the AlN 100 nm. The RF gap (distance between two gold electrodes) is 600 nm. The exact same material settings shown in Table 6.2 is used for modelling this device in COMSOL. In the model, the device is directly connected to the pulse source with a 50 Ω output impedance. The temperature transients on top of the PC layer can be thus simulated based on different pulse inputs, which can be further used for simulating the crystallization process based on the growth velocity model. An extra layer of SiO_2 can be added between the heater and the substrate with different thicknesses, serves as a thermal isolation layer. By increasing the thickness of the thermal isolation layer, the device can

achieve lower power consumption, but on the other hand less amorphous PC volume due to slower quenching and thus lower threshold voltage.

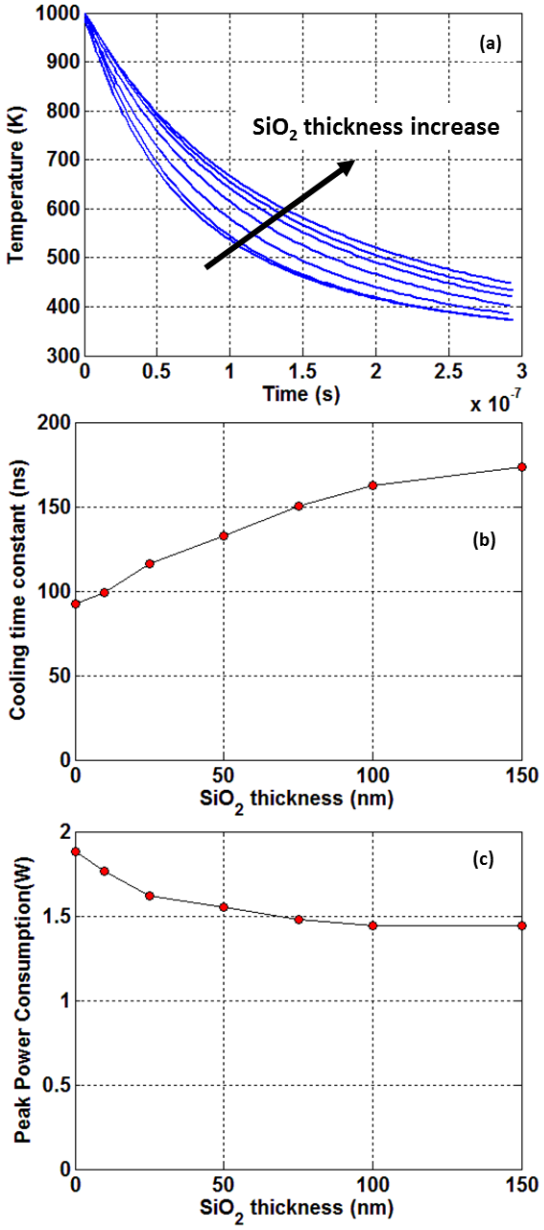

Figure 7.5 (a) temperature transients for different SiO_2 thicknesses, time is adjusted to start at when the temperatures just fall below the melting point (b) cooling time constant as a function of SiO_2 thickness (c) peak power consumption as a function of SiO_2 thickness

For different SiO_2 thicknesses, the input pulses are adjusted to achieve the RESET operation and produce the same peak temperature (10 K higher than the melting point) at the top of the PC. Thus, each pulse carries the minimum power to amorphize the PC. As shown in Figure 7.5(a) and (b), although the same portion of PC is melted for each pulse, the cooling temperature transients as well as the cooling time constant are different due to different thermal isolation. Figure 7.5(c) shows that the peak power consumption decreases by increasing SiO_2 thickness, as expected. However, when the SiO_2 thickness reaches 100 nm and beyond, the power cannot be reduced further. This is because the thermal resistance to the substrate is too high that the vertical heat flow to the substrate is very small comparing to the lateral heat flow. As a result, increasing the thermal resistance to the substrate further will not increase the overall thermal resistance to the thermal ground. For 100 nm thick thermal isolation layer, the power is reduced by 23% comparing to the case where no thermal isolation layer is presented.

Figure 7.6(a) shows the simulated temperature contour at the end of the pulse. It can be seen that the melted zone of the PC layer has a minimum width of 115 nm on the top, which can be considered as the initial amorphous length. Outside the melted zone, the PC material is still crystalline. Based on this, the crystallized portion can be estimated using the temperature dependent growth velocity and the temperature transients in Figure 7.5(a). Figure 7.6(b) shows the remaining amorphous region lengths after the RESET operations as a function of SiO_2 thickness. As expected, the amorphous region length is smaller for thicker SiO_2 and longer quench time. Without thermal isolation layer, we can produce a 61 nm amorphous region; while for 100 nm thermal isolation layer, the amorphous region size is only 16 nm.

Correspondingly, we can apply the threshold field extracted in Chapter 4 to estimate the threshold voltage V_{th} as well as the standard deviation for each device. For the device without thermal isolation, V_{th} is estimated to be 1.4 ± 0.5 V, which is consistent with the measured data shown in Figure 4.7 for the same device. The 100 nm thermal isolation layer will result in a V_{th} of 0.5 ± 0.3 V so small that even small signal can potentially break down the switch. A V_{th} of 10 V and above is desired for high power handling applications. Thus, even for the case without thermal isolation, the V_{th} is not high enough.

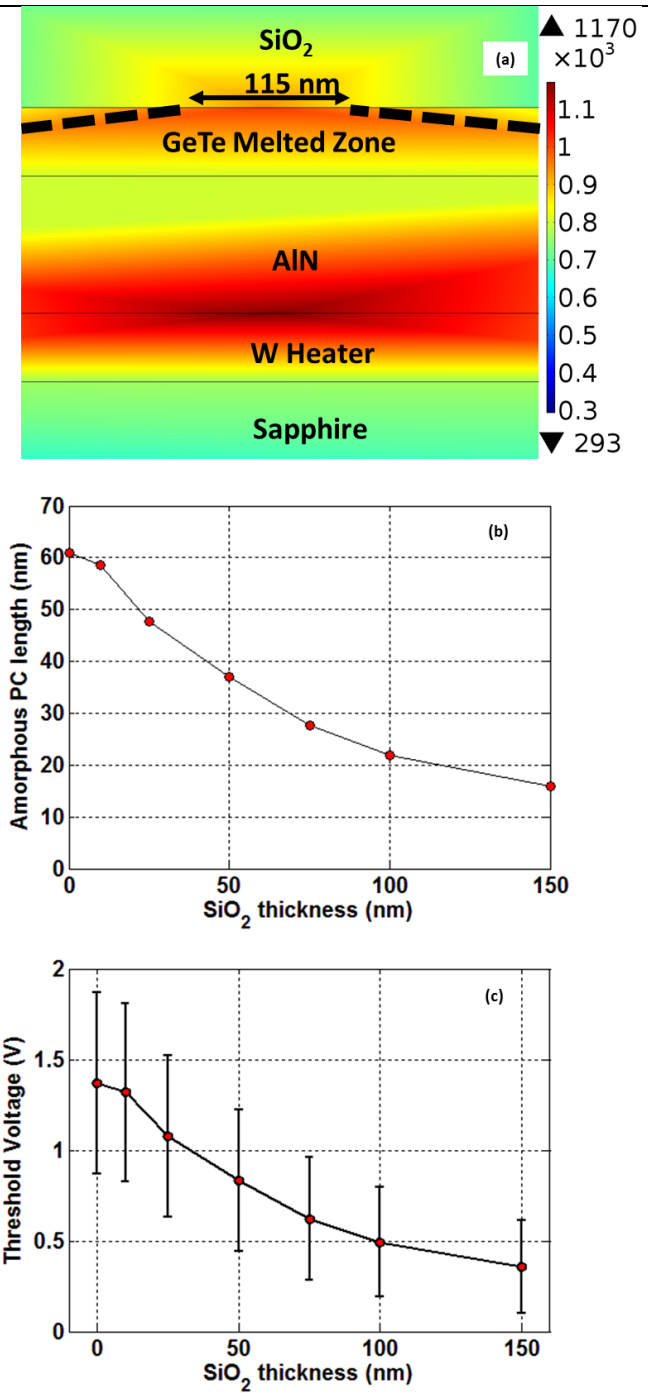

Figure 7.6 (a) simulated cross-section schematic of the temperature contour at the end of the amorphization pulse (b) estimated amorphous region sizes after each RESET and (c) estimated threshold voltage and variance as a function of SiO_2 thickness

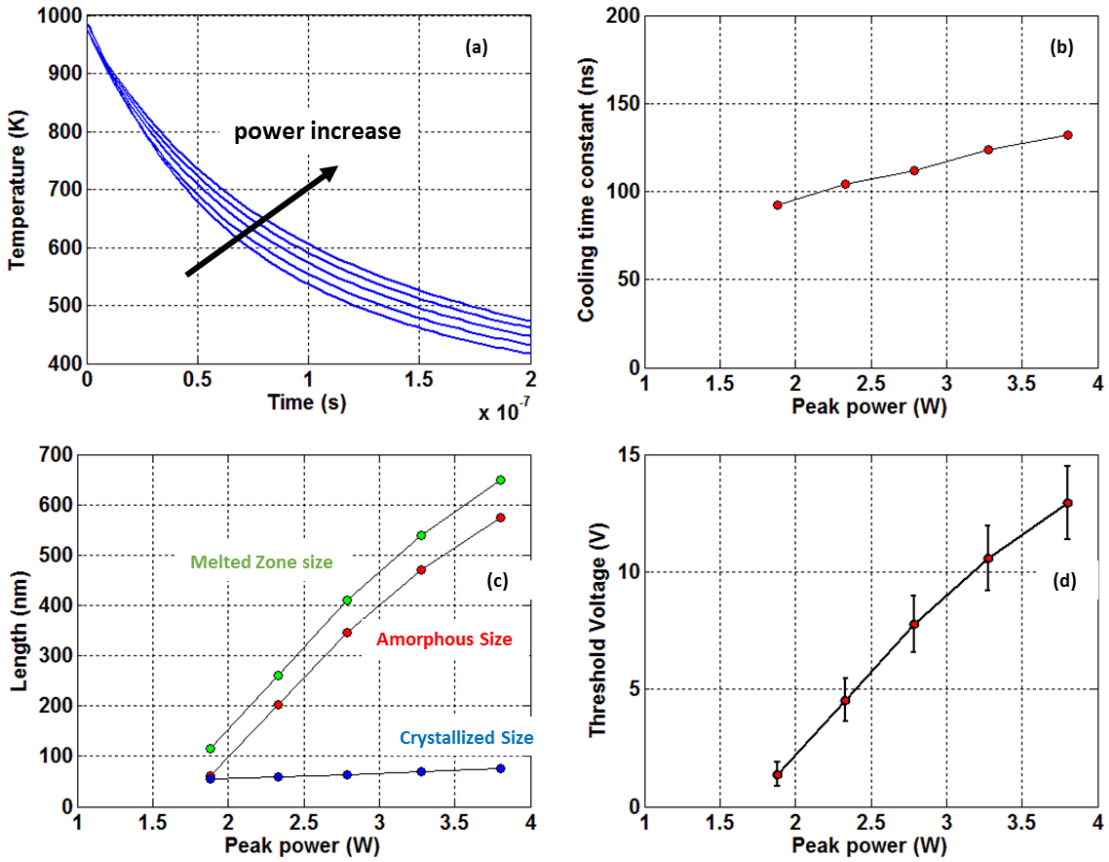

Figure 7.7 (a) temperature transients for different peak powers, using device without thermal isolation layer, time is adjusted to start at when the temperatures just fall below the melting point (b) cooling time constant as a function of power (c) simulated melted zone size (green), amorphous PC size (red) and crystallized PC size (blue) as a function of peak power (d) estimated threshold voltage as a function of peak power

The V_{th} can be improved by increasing the heater power. By delivering more power to the heater, a larger melted zone can be achieved in the PC layer, potentially results in larger amorphous volume. The RF switch with no thermal isolation layer is used in the simulation. Although the temperature cools more slowly for higher power as shown in Figure 7.7(a)(b), the increment of crystallized PC volume is still smaller than that of the melted zone volume. Figure 7.7(c) shows the comparison of melted-zone size (green color),

crystallized PC size (blue color) and amorphous PC size (red color) as a function of powers. The resulted amorphous PC sizes can be further used to estimate the V_{th}, as shown in Figure 7.7(d). It can be seen that by applying power of 3.25 W, a V_{th} slightly above 10 V. This suggests that there is a trade-off between the V_{th} and the RESET power, and thus between the power handling and the programming power consumption.

Note that this framework assumes a 1-D crystalline growth problem as the crystallization process and the temperature dependent growth velocity is the key parameter in the simulation. Although it can be generalized to predict RF switches with any geometries, there are still constraints for the device architectures and material types. First, the crystallization process of PC devices with spherical heating profiles and amorphous regions as in mushroom memory cells must be simulated in three dimensions. Thus, modifications to this framework are needed (e.g. apply the temperature dependent growth velocity in a 2-D/3-D FEM simulation model to predict the spatial distribution of growth velocity at any given time). Second, for nucleation-dominated PC materials, growth velocity may not be the key parameter to estimate crystallization rate. Instead, accurate measurement of nucleation rate is required and percolation models based on both growth and nucleation rates need to be developed.

Nevertheless, for the desired 1-Ω RF switch with the same architecture as discussed in this work, this framework has not generalization issue. Since the amorphous length is independent of the RF switch width to the first order, an 1-Ω RF switch will have the same crystallization process as the that of the RF switch discussed above. For the switch matrix architecture, the framework can also be applied to predict the crystallization process. Each switch can be simulated individually based on their electro-thermal models. To first order, the crystallization process of a 2x2 matrix will not be different than that of a PC switch with doubled amorphous length, as in both cases, the crystalline front has to travel double the original amorphous length to crystallie the entire structure. As a result, the trade-off between the RESET power and the threshold voltage is also unchanged. The standard deviations of V_{th} and E_{th} for the matrix can be calculated based on the convolution of standard deviations of single switches and the material dependent peroperteis summarized in this framework.

7.7 Summary

In this chapter, we first discussed the different models used for explaining the non-Arrhenius behavior of crystallization dynamics, especially at high temperatures. Growth and nucleation models in the classic nucleation theory have been examined but fail to agree with the measurement that no crystallization event was observed for time shorter than 5 ns. Alternatively, the fragility model was applied to explain the change of activation energies at different temperature regimes. Combining with the evidence that the crystallization of GeTe is growth dominated, a temperature dependent growth velocity model was derived.

Based on this model, a unified framework to estimate the performance of PC RF switch is developed. To validate the accuracy and effectiveness of this framework, the measurement results of the CQT measurements in Chapter 3 were examined. By inputting the temperature transients generated for given device structure and electrical input, the growth dominated crystallization process can be simulated. The estimated fraction of crystallized volume after a RESET operation agrees with the measured DC OFF-state resistance data. On the other hand, the crystallization time and temperature also agrees with the in-situ crystallization measurements in Chapter 3.

Finally, the framework is applied to a more appropriately designed RF switch. The trade-off between power consumption and threshold voltage is discussed by varying the thermal isolation thickness between the heater and the substrate.

Chapter 8: Conclusions and Outlook

8.1 Conclusions

This thesis presented the study of the crystallization dynamics and threshold voltage of phase change materials for their applications in reconfigurable RF switches and non-volatile memories. It discussed in detail the related device design and fabrication, methodology development, experimental observations, modelling and analysis for each piece of the study. Specifically, the detailed summary of methodology contributions can be found in Table 8.1.

The first contribution is the design, fabrication and thermometry of a micro-scale thin-film heater as the external heat source for the PC materials that can reach 1664 K at a rate of 1.67×10^{10} K/s and have a thermal time constant less than 40 ns. Combining TDT experiments and COMSOL FEM modelling, the methodology for heater thermometry was developed to achieve uncertainty less than 0.2% in the best case with a lower temperature and 13.1% in the worst case with a higher temperature. This methodology can be further applied in designing and measuring heaters with nano-scale geometry. This work is the foundation for all the other studies on the crystallization dynamics without which the PC electro-thermal properties cannot be characterized reliably. This work has been published in Review of Scientific Instruments titled with “Thermometry of a High Temperature High Speed Micro Heater” [130].

The second contribution is the methodology development for measurement of CQT and crystallization time. The 1st generation PC test device with relatively fast thermal response, and good cycleability was designed and fabricated. In-situ measurement techniques for CQT and crystallization time was developed to characterize the crystallization dynamics. Although the CQT result is device structure specific, this methodology can be applied to measure the CQT for appropriately designed RF PCS to determine its heat sink design space for low power applications. The in-situ crystallization time

measurement also provided evidence of non-Arrhenius crystallization behavior. This work has been submitted to the IEEE Transactions on Electron Devices.

The third contribution is the experimental observations on the V_{th} for GeTe that provides several insights into the threshold switching mechanisms. The threshold switching for GeTe was found to be unrelated to NDR, time dependent and independent of resistance drifting. Another important finding was that the large V_{th} variations originate in E_{th} variation, which is independent of amorphous cross-section area but proportional to $d_a^{-1/2}$. This interesting behavior suggest a Poisson process, where the total amorphous length can be divided up into characteristic lengths associated with fluctuations. The physical origins of this fluctuation length scale remain unclear. On the other hand, the area independency suggests threshold switching is not caused by field enhancement with positive feedback on random defects. The finding that E_{th} mean remains constant implies that the field is relatively uniformly distributed across the amorphous length, arguing against theories based on non-uniformly distributed field such as space charge limited conduction. This work will be submitted to the Applied Physics Letter.

The fourth contribution is design and fabrication of the 2nd generation nano-scale high speed PC test device. E-beam lithography based fabrication process was presented. This device allows measurements of crystallization dynamics to span the entire range of interest for both temperature (300 K to 1000 K) and time (5 ns to 1 ms). This device enables us to study the crystallization dynamics and quantify the non-Arrhenius behavior in different temperature regimes, which is critical for understanding the limitation of write speed improvement for memory applications.

The fifth contribution is the quantification of the non-Arrhenius behavior for GeTe at different temperature regimes. Crystallization pulse measurements using the 2nd gen device were used to produce Arrhenius plot for time ranging from 5 ns to 1 ms. The minimum crystallization time was assessed to be 10 ns. By comparing the data with measurements using the 1st gen device, GeTe crystallization process was identified to be growth-dominated. A methodology was developed to correct non-isothermal crystallization based on an iteratively converging model constraint by any non-Arrhenius crystallization rate model and

input temperature transients, which is useful when the device cannot be heated sufficiently fast to produce isothermal crystallization. Different crystallization dynamics models were applied to address the non-Arrhenius behavior. Fragility model combing with growth dominated crystallization was identified to be most consistent with crystallization measurements and reported data.

The sixth contribution is the unified framework for estimating RF PCS switching dynamics. In this framework, the fragility model was used to calculate the growth rate and simulate the crystallization process. For any growth-dominated PC material (e.g. GeTe) and device geometry, this framework is capable of estimating the crystallized fraction of PC materials at any time. This framework was reconciled with the CQT in-situ measurements. Finally, it was applied to an appropriately designed RF PCS to estimate the power consumption, threshold voltage and its variation for different thermal isolation design, following by the discussion of the trade-off between the power and threshold voltage. Combining this with the second, fourth and fifth contributions, this work will be submitted to IEEE Transactions on Electron Devices.

Table 8.1 Summary of Methodology Contributions		
Methodologies	Novelty	Relavant Literatures
TDT for heater thermemorty	This method has been applied to estimate heater temperature and study electro-thermal properties of PC materials reported by different literatures, but we are the first to demonstrate high speed TDT (< 50 ns) for thermometry	[101], [102], [131]
Measurement of crystallization activation energies	Kissinger Analysis is typically used. We are the first to use embedded external heater and in-situ crystallization measurement to identify activation energies	[102], [120]
In-situ measurement of crystallization dynamics	We are the first to use embedded external heater and in-situ pulse measurement to obtain the bottom part of the TTT diagram. Other relevant work applied laser to obtain data in the high temperature high speed regime or used direct-heated structures with FEM simulation	[36], [132]
Critical quench time measurement	We are the first to develop the technique to measure critical quench time	
Crystallization dynamics measurement in the sub-10 ns regime	We are the first to combine pulse measurement techniques, TDT thermometry and E-beam defined high speed device to identify crystallization time in less than 10 ns. Other work has demonstrated high speed device nanosecond switching without thermometry.	[97]
Measurement of non-Arrhenius behavior, fragility and temperature dependent growth velocity	Most relevant work applied differential scanning calorimetry (DSC) or laser measurements. We are the first to use pulse measurement to identify these behaviors	[45], [129]

8.2 Future Work

To build RF PCS with lower programming power, the unified framework can be used to assist the design by estimating the power and threshold voltage for different heat sinks. The unified framework can also be used in simulating crystallization process for RF PCS to be monolithically integrated with CMOS. As there is thick SiO_2 passivation layer on top of the CMOS chip (~ 10 μm), the melt-quench RESET operation is unlikely to succeed. An additional AlN layer can be added between the device and the PC as a heat spreading layer, making the effective thermal resistance small and the quench process faster. Using this framework, AlN thickness can be carefully designed to make functional low power RF PCS on top of the CMOS. Devices with optimal heat sink design that leverages both the power consumption and power handling can then be fabricated and integrated with CMOS RF circuits monolithically or through flip-chip bonding. However, to break the trade-off and achieve lower power hand higher threshold voltage simultaneously requires different materials. Off-stoichiometric GeTe is a potential candidate. The E_x is known to vary with compositions and using Ge_xTe_{1-x} with higher E_x allows a slower crystallization process. But the trade-off between the ON-state resistivity and power consumption needs to be carefully assessed to maintain the high f_{CO}.

To build RF PCS with higher power handling, the future work can focus on three different aspects. The first aspect is to study the V_{th} on melt-quenched film rather than as-deposited film. In this thesis, single-use PC devices with as-deposited amorphous material and known dimension were used. However, V_{th} can be different from the measured values in for the melt-quenched films in cyclable PC devices. The 2nd gen device can be used in this study, as it has known amorphous thickness and melt-quenched amorphous materials. The second aspect is to develop techniques for measuring V_{th} for RF PCS with RF large signals applied to it. Since V_{th} is time dependent, the RF V_{th} will deviate from the values measured using DC or pulse I-V sweeps. RF V_{th} determines the read-world power handling capability for a RF PCS. The third aspect is to develop a comprehensive understanding of the threshold switching mechanisms based on the observations in this thesis. Once a reliable model is established, not only we can use it to predict V_{th}, but it

also can imply how to optimize materials to achieve higher V_{th}. Finally, as discussed in Chapter 7, building the switch matrix allows higher V_{th} with the same cut-off frequency while sacrificing the area. Due to the scaling properties of the V_{th} and E_{th} distribution, the switch matrix may result in a much higher variation in the V_{th}. We need further experiments to validate this assumption to better understand the trade-off between single RF switch and switch matrix.

To build memories with faster write speed, alternative materials need to be explored. Although fragility model provides good quantitative description for the non-Arrhenius crystallization process at $T > T_g$, a more universal theory is desired. Combing the fragility model with the multi-excitation entropy model is a possible direction. Although the model remains to be validated, but finding materials that can extend valid regime for the crystallization modality with high E_x Arrhenius behavior (currently only observed in the low T regime) can potentially increase the crystallization speed. Through doping, it may be possible to change the entropic multiplication factor and thus the temperature dependency of the pre-exponential factor such that the unphysically small pre-exponential factor in that modality can be extended.

However, the goal of achieving high crystallization speed inevitably conflicts with the goal of improving data retention. The trade-off between the speed and the data retention time needs to be carefully investigated in the future. We can engineer the material so that the fragility is higher, by making the T_0 higher and the B lower in the fragility model. Doing so allows the crystallization speed to not slow down at lower temperatures (e.g. 600 K to 800 K) while have a more sudden decrease (higher activation energies) at temperatures lower than 600 K to improve the data retention. To achieve so, atomic configurations in the PC materials need to be changed in a way that more free volume (or entropic configurations) is available at high temperatures and less is available at low temperatures. This can possibly be achieved by engineering the PC materials to enforce less covalent bonds in the amorphous materials at high temperatures.

On the other hand, this thesis has shown the scaling of crystallization time with amorphous size. This scaling behavior is yet to be studied, possibly through making the 2nd generation nano-scale high speed

device design with various PC thickness and via sizes. It is necessary to measure the valid regime for the scaling and what is the intrinsic crystallization speed limit regardless of the geometry.

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